SUN MICROELECTRONICS

STP5110A

July 1997

UltraSPARC™-I CPU Module

DATA SHEET — 167 MHz UltraSPARC-I + 0.5 MB E-Cache + UDBs

DESCRIPTION

The UltraSPARC-I module is a high performance, SPARC V9 compliant, small form factor processor module, which interfaces to the UltraSPARC Port Architecture (UPA) interconnect bus.

The main components on the module are: one UltraSPARC-I CPU, two UltraSPARC-I UDB data buffer chips, one 32kx36 tag SRAM, four 32kx36 (for 1/2 Mbyte E-Cache) data SRAMs, and a MC100LVE111 clock buffer.

All components on the module operate at 3.3 V. All signal levels to and from the module are at 3.3 V LVTTL, except for the differential clock inputs, which are at 3.3 V PECL levels. The module runs synchronously with the system interface at a 2:1 frequency ratio. The module will be available with the UltraSPARC-I running at 167 MHz. The interface to the module is through a high-speed edge connector.

Features	*Benefits*
• High performance UltraSPARC-I CPU module	• Delivers approximately 7.7 SPECint95, 11.4 SPECfp95 at 167MHz
• Programmable bus speed	• Easy upgrade to faster processors
• SPARC V9 compliant	• Provides the performance of the V9 architecture
• Implements VIS instruction set	• Comprehensive hardware support for 3D Graphics, H-261 compression/decompression, and MPEG2 decompression
• 128-bit wide data bus	• High bandwidth (Peak bandwidth of 1.3 GB)
• Cache coherency support for multi-processing	• Allows a wide range of scalable systems to be built
• 1/2MB of E-Cache	• UltraSPARC's pipelined E-Cache interface delivers high performance
• 3.3V LVTTL	• Allows very high bus speeds and power savings
• 158.75mm x 107.95mm form factor	• Small footprint
• UPA is implemented on a 110-pin dual high-speed card edge connector to connect the module with the UPA interconnect bus	• High performance impedance controlled connector provides reliable signal integrity.

BLOCK DIAGRAM

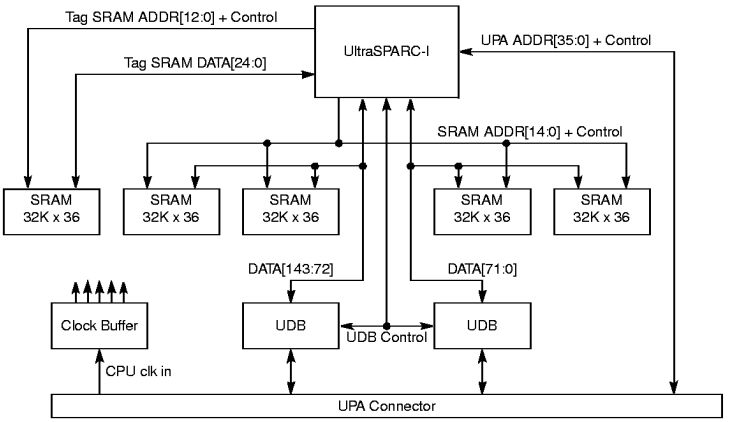


Figure 1. Module Block Diagram

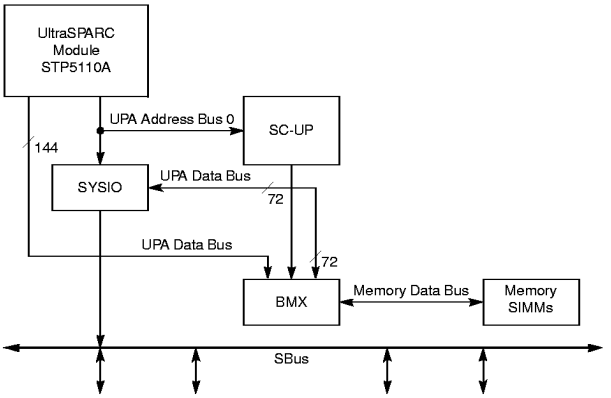


Figure 2. STP5110AUPA Uniprocessor System Configuration

SUMMARY OF CHANGES FROM PREVIOUS RELEASE

Specification	Previous Release	Current Release
UltraSPARC Revision	Rev_2x or Rev_4x	Rev_4x only
PCB Impedance	55Ω ±10%	52.5Ω ±10%
PCB Stackup	–	Swapped V_{DD}/V_{DD_CORE}/GND layers for better EMI
Thermister	Underneath the board	Next to CPU package on top
Power/Ground plane metal	0.5 oz copper	1.0 oz copper
SRAM/CPU clock skew	850 ps	670 ps
UPA bus loading	WC 60Ω BC 50Ω	WC 58Ω BC 47Ω
UPA/SYS_DATA setup	3.8 ns	3.9 ns
UPA/SYS_DATA tcq	6.0 ns	6.1 ns

ULTRASPARC-I CPU

The UltraSPARC-I CPU is a high-performance, highly integrated superscalar processor implementing the SPARC V9 64-bit RISC architecture. UltraSPARC-I is capable of *sustaining* the execution of up to *four* instructions per cycle even in the presence of conditional branches and cache misses. UltraSPARC-I is an implementation of the 64-bit SPARC V9 architecture. It supports a 44 bit virtual address space and a 41 bit physical address space. The instruction set also includes the VIS instruction set that accommodates the most common operations related to two-dimensional image processing, three-dimensional graphics and video compression/decompression algorithms, and other pixel based algorithms. Support for high bandwidth bcopy is also provided through block load and block store instructions.

The system interface signals run at a 2:1 ratio of the internal CPU frequency. All signals that interface with the system are compatible with LVTTL levels. All signals that interface with the SRAMs and the UDBs are LVCMOS levels. The clock is a differential low-voltage PECL input.

The UltraSPARC-I CPU is packaged in a plastic 521 pin (323 signals, 197 power/gnd pins, and 1 index pin) 1.27 mm (50 mil) pitch BGA (ball grid array) package. The package dimension is 43 mm by 43 mm.

UltraSPARC-I Data Buffer (UDB)

The UltraSPARC-I module has two UltraSPARC-I Data Buffer (UDB) chips. The two UDBs connect UltraSPARC-I and its external cache to the 144-bit UPA interconnect data bus. All data that moves between the UltraSPARC-I module and the system pass through the UDBs, including cache fill requests, writeback data of dirty displaced cache lines, copyback data of cache entries being requested by the system, non-cacheable loads and stores, and interrupt vectors going to and from the CPU.

The UDBs have a 128-bit interface plus 16 parity bits on the CPU side, and a 128-bit interface plus 16 ECC bits on the system side.

The UDBs run at the same frequency as the system. Therefore, it runs at a 2:1 ratio of the CPU frequency. All signals that interface with the system are compatible with LVTTL levels. All signals that interface with the SRAMs and the CPU are LVCMOS levels. The clocks are differential low-voltage PECL input.

The UltraSPARC-I UDB is packaged in a plastic 256 pin (177 signals and 79 power/gnd pins), 1.27mm (50 mil) pitch BGA (ball grid array) package. The package dimension is 30 mm by 30 mm.

External Cache

The External Cache is connected to the E-Cache data bus. Five SRAM chips are used to implement the 512KByte cache. One SRAM is used as the tag SRAM and four are used as data SRAMs. Each SRAM is a 32kx36 synchronous memory chip.

The SRAMs cycle at the same frequency as the CPU. The SRAM interface to the CPU also runs at the same frequency as the CPU. The SRAM signals operate at LVCMOS levels. The SRAM clocks are differential low-voltage PECL input.

The SRAMs are packaged in a plastic 119 pin, 1.27mm (50 mil) pitch BGA (ball grid array) package. The package is 22 mm by 14 mm.

PCB CONSTRUCTION

The PCB construction is optimized for low propagation delay with minimum noise coupling. The impedance specification is 52.5Ω ±10% for inner signal layers (striplines) and outer layers (microstrips), with a signal propagation speed of 170 - 190 ps/inch on all layers. The overall board thickness is 63 ±9 mil. To minimize crosstalk, adjacent internal layers do not have signals routed on top of each other.

TABLE 1: PCB Layer Stacking

layer 1	signal 1/BGA Pads	1.0 oz. copper/ 6mil trace
layer 2	V_{SS}	1.0 oz. copper
layer 3	signal 2	1.0 oz. copper/ 4mil trace
layer 4	signal 3	1.0 oz. copper/ 4mil trace
layer 5	V_{DD}	1.0 oz. copper
layer 6	signal 4	1.0 oz. copper/ 4mil trace
layer 7	signal 5	1.0 oz. copper/ 4mil trace
layer 8	V_{DD_CORE}	1.0 oz. copper
layer 9	signal 6	1.0 oz. copper/ 4mil trace
layer 10	signal 7	1.0 oz. copper/ 4mil trace
layer 11	V_{SS}	1.0 oz. copper
layer 12	signal 8	1.0 oz. copper/ 6mil trace

UPA INTERCONNECT PINOUT

The UltraSPARC-I module complies with the UPA128M (see UltraSPARC user's manual) interface and supports full master/slave functionality with the 128-bit Databus.

The UPA_PORT_ID[4:2] are hardwired on the module to "0" in this profile. UPA_PORT_ID[1:0] are brought out to the connector pins, and have to be hardwired in the system. This optimizes this profile for systems with 4 or fewer processors. Systems that need to support greater than 4 modules need to map the limited set of UPA_PORT_IDs from this module to the range of required UPA_PORT_IDs by implementation-specific means in the system.

Two types of power are supported on this module: V_{DD} at 3.3V, and V_{DD_CORE} that is set by a DC-DC regulator on the system. V_{DD_CORE} is intended to supply the core of the processor chip on the module, and is currently set to 3.3V by the external DC-DC regulator.

Figure 1 and *Figure 1* show the pinout of the module interconnect.

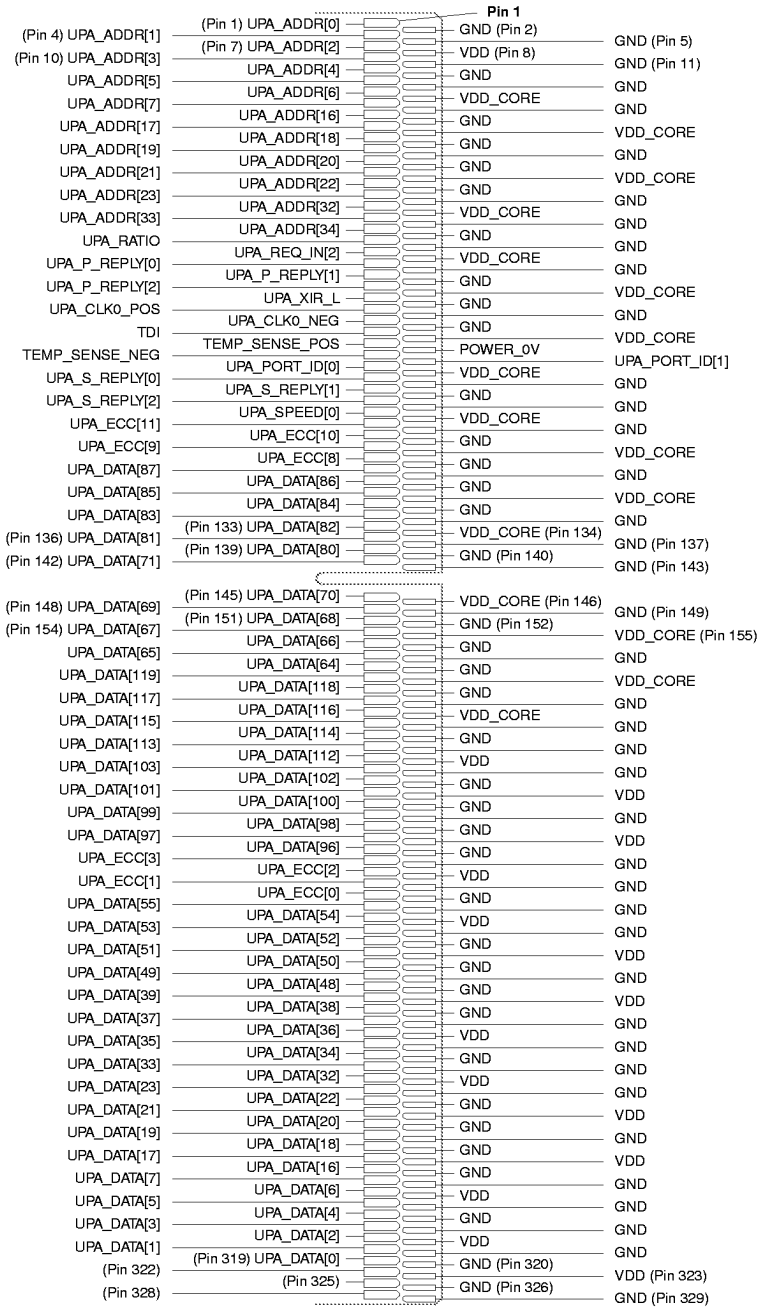


Figure 1. UPA Connector Pin-Out Assignment (Top)

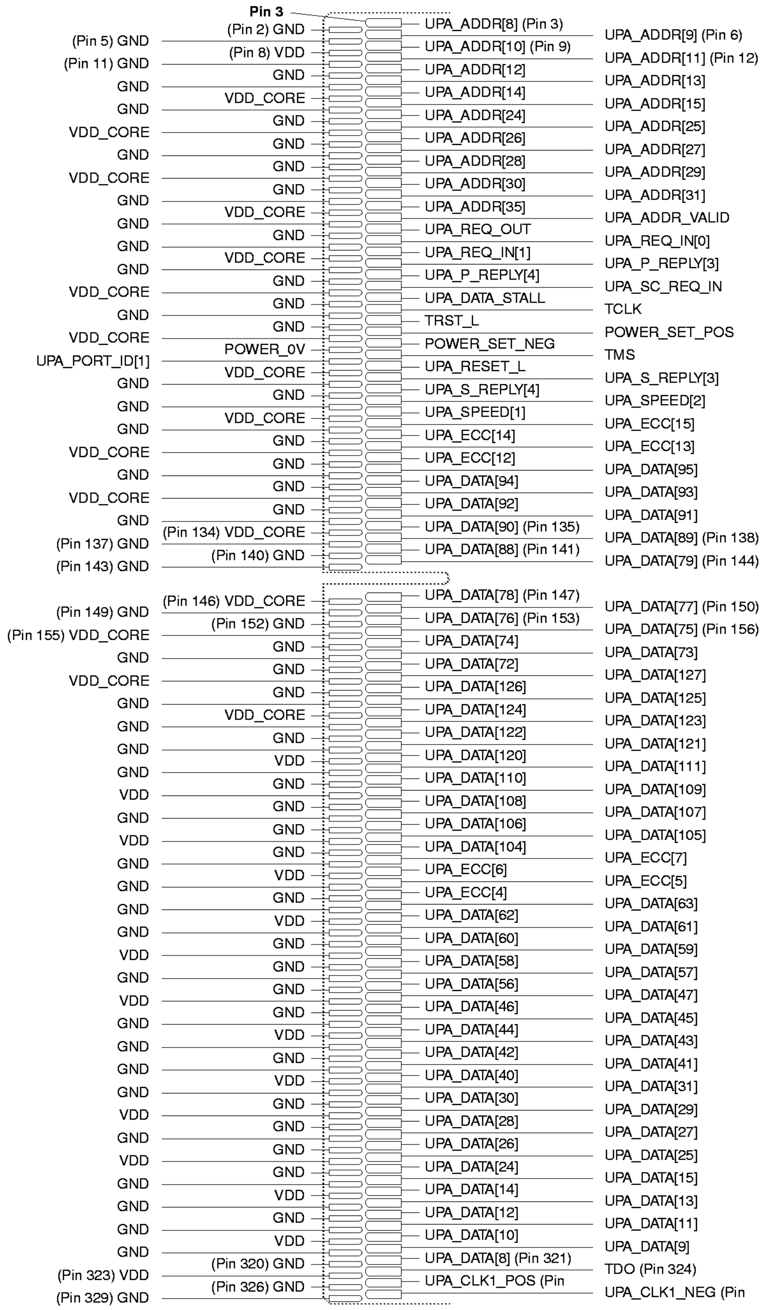


Figure 1. UPA Connector Pin-Out Assignment (Bottom)

UPA SIGNALS DESCRIPTION

System Interface

Signal	Type	Name and Function
UPA_ADDR[35:0]	I/O	Packet switched transaction request bus. Maximum of 3 other masters and 1 system controller can be connected to this bus. Includes 1-bit odd-parity protection.
UPA_ADDR_VALID	I/O	Bidirectional radial UltraSPARC-I Bus signal between UltraSPARC-I and the System. Driven by UltraSPARC-I to initiate UPA_ADDR transactions to the System. Driven by System to initiate Coherency, Interrupt or Slave transactions to UltraSPARC-I. Synchronous to system clock. Active high.
UPA_REQ_IN[2:0]	I	UltraSPARC-I system address bus arbitration request from up to 3 other UltraSPARC-I Bus ports that might be sharing the UPA_ADDR. Used by UltraSPARC-I for the distributed UPA_ADDR arbitration protocol. Connection to other UltraSPARC-I Bus ports is strictly dependent on the Master ID allocation. Synchronous to system clock. Active high.
UPA_SC_REQ_IN	I	UltraSPARC-I system address bus arbitration request from the system. Used by UltraSPARC-I for the distributed UPA_ADDR arbitration protocol. Synchronous to system clock. Active high.
UPA_S_REPLY[4:0]	I	UltraSPARC-I system Reply packet, driven by SC_UP to the UPA port. Synchronous to system clock.
UPA_DATA_STALL	I	Driven by SC_UP to indicate whether there is a data stall.
UPA_P_REPLY[4:0]	O	UltraSPARC-I system reply packet, driven by UltraSPARC-I to the system. Synchronous to system clock.
UPA_DATA[127:0]	I/O	UPA Interconnect Data bus.
UPA_ECC[15:0]	I/O	ECC bits for the data bus. 8-bit ECC per 64-bits of data.
UPA_ECC_VALID	I	Driven by SC_UP to indicate ECC is valid for the data on the UPA interconnect data bus.
UPA_REQ_OUT	O	Arbitration request from this module. Active high.
UPA_PORT_ID[1:0]	I	Module's identification signals.

Clock Interface

Signal	Type	Name and Function
UPA_CLK[1:0]_POS UPA_CLK[1:0]_NEG	I	UPA Interconnect Clock. Two copies are provided, one for each UDB.
CPU_CLK_POS CPU_CLK_NEG	I	Differential Clock inputs to the clock buffer on the module.
UPA_RATIO	I	Sets the clock divider mode. Set to "0" for 2:1 UPA ratio, and "1" for 3:1 UPA ratio. [1]
UPA_SPEED[2:0]	O	Encodes the maximum operating speed of the module, set to "001".

1. Contact Sun Field Engineering for information on operating the STP5110 with a 3:1 UPA ratio.

JTAG/Debug Interface

Signal	Type	Name and Function
TDO	O	IEEE 1149 test data output. A three-state signal driven only when that TAP controller is in the shift-DR state.
TDI	I	IEEE 1149 test data input. This pin is internally pulled to logic one when not driven.
TCLK	I	IEEE 1149 test clock input. This pin if not hooked to a clock source must always be driven to a logic 1 or a logic 0.
TMS	I	IEEE 1149 test mode select input. This pin is internally pulled to logic one when not driven.
TRST_L	I	IEEE 1149 test reset input (active low). This pin is internally pulled to logic one when not driven.

Initialization Interface

Signal	Type	Name and Function
UPA_RESET_L	I	Driven by SC_UP for POR (power-on) resets and on fatal system reset. Asserted asynchronously. Deasserted synchronous to system clock. Active low.
UPA_XIR_L	I	Driven to signal externally initiated reset (XIR). Actually acts like a non-maskable interrupt. Synchronous to system clock. Active low, asserted for one clock cycle.

Misc. Signals

Signal	Type	Name and Function
TEMP_SENSE_NEG TEMP_SENSE_POS	O	Connected to a thermistor next to the CPU package.
POWER_SET_POS POWER_SET_NEG	O	POWER_SET_NEG is tied to GND on the module. POWER_SET_POS is connected to GND via a 3.83K ohm resistor. Useful for V_{DD_CORE} reference.
POWER_0V	O	Connected to GND via an 866 ohm resistor. Useful for GND reference.

CLOCK DISTRIBUTION

This section describes how the various clocks are distributed on the module. Both routing topology and clock termination are discussed.

The JTAG TCK signal is distributed to UDB, SRAMs and UltraSPARC-I. Each UDB will receive a separate UPA clock from the system. The UPA_CLK[0]_POS and UPA_CLK[0]_NEG are also connected to the UltraSPARC-I to generate a phase signal for determining the phase relationship between the CPU clock and UPA clock. The phase signal at UltraSPARC-I pin will be 650 ps earlier than the system clock signals at UDB pins. Trace lengths for UDB clocks are adjusted for equal delay from the connector.

The CPU clock is delivered to a MC100LVE111 clock buffer chip and redistributed to the UltraSPARC-I and five SRAMs. CPU and SRAM trace lengths from the MC100LVE111 are adjusted so that SRAMs are clocked 670 ps earlier than UltraSPARC-I. The rising edge of the UPA clock will always line up with the CPU clock with minimal skew. The CPU clock trace length on this module is 16.2". The UPA clocks trace length on this module are 7.6".

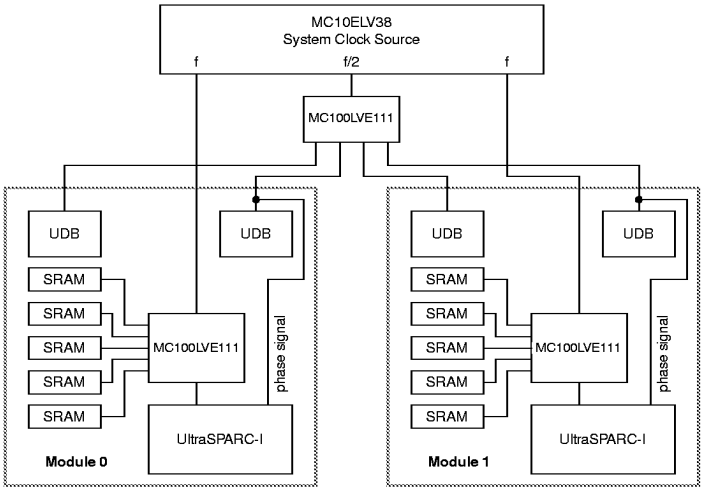


Figure 3. Module Clock Distribution

TABLE 2: Clock Skew Between Different Chips

Clock Skew	Worst Case Skew
CPU clk to UDB clk	500 ps
CPU clk to system ASIC clk	500 ps
UDB clk to system ASIC clk	500 ps

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Units
V_{DD}	Supply voltage range for I/O	-0.5 to 4.6	V
V_{DD_CORE}	Supply voltage range for CPU core	-0.5 to 4.6	V
V_I	Input voltage range[2]	-0.5 to V_{DD} + 0.5	V
V_O	Output voltage range	-0.5 to V_{DD} + 0.5	V
I_{IK}	Input clamp current (V_I < 0 or V_I > V_{DD})	±20	mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{DD})	±50	mA
	Current into any output in the low state	50	mA
T_{STG}	Storage temperature	-20 to 90	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions "is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Unless otherwise noted, all voltages are with respect at V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage for I/O	3.2	3.3	3.4	V
V_{DD_CORE}	Supply voltage for the CPU core	3.2	3.3	3.4	V
V_{SS}	Ground	–	0	–	V
V_{IH}	High-level input voltage	2.0	–	V_{DD} + 0.2	V
V_{IL}	Low-level input voltage	-0.3	–	0.8	V
I_{OH}	High-level output current	–	–	10	mA
I_{OL}	Low-level output current	–	–	10	mA
T_A	Operating ambient temperature	0	–	40 [1]	°C

1. The preliminary maximum case temperature (measured on the case, in the middle of the package) is limited to 90 °C when the UltraSPARC-I is consuming 30 Watts @ 167 MHz and at 10K feet.

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High-level output voltage	V_{DD} = Min, I_{OH} = Max	2.4	–	–	V
V_{OL}	Low-level output voltage	V_{DD} = Min, I_{OL} = Max	–	–	0.4	V
I_{CC}	Supply current for V_{DD}	V_{DD} = Max	–	5	8	A
I_{CC_CORE}	Supply current for V_{DD_CORE}	V_{DD_CORE} = MAX	–	5	7	A
I_{OZ}	High-impedance output current (Outputs without pull-ups)	V_{DD} = Max, V_O = 2.4 V	–	–	20	µA
		V_{DD} = Max, V_O = 0.4 V	–	–	-20	µA
	High-impedance output current (Outputs with pull-ups)	V_{DD} = Max, V_O = V_{SS} to V_{DD}	–	–	250	µA
I_I	Input current (inputs without pull-ups)	V_{DD} = Max, V_I = V_{SS} to V_{DD}	-20	–	20	µA
	Input current (inputs with pull-ups)	V_{DD} = Max, V_I = V_{SS} to V_{DD}	–	–	-250	µA

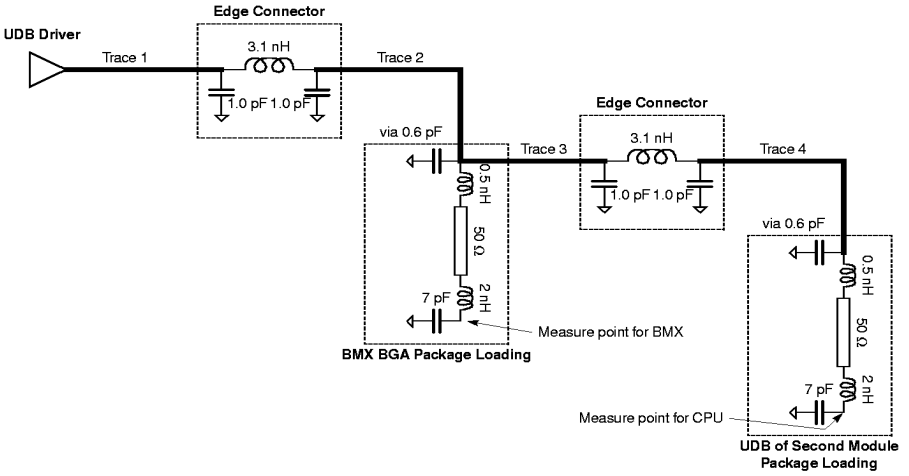
Power consumption

The UltraSPARC-I requires two V_{DD} supply voltages. V_{DD} and V_{DD_CORE} are currently required to be 3.3V ± 100 mV. The V_{DD_CORE} supply should be programmable to allow for upgrades to higher speed modules. The estimated maximum power consumption of the STP1030A is 30 Watts @ 167 MHz.

TIMING SPECIFICATIONS

UPA Timing Specification

Preliminary timing specifications for the Module are specified at the edge connector pins in a typical system shown in *Figure 4*.



Worst Case: $Z_0 = 58\Omega$, $T_P = 190$ ps/inch, Trace 1 Length = 4.2", Trace 2 Length = 0.6", Trace 3 Length = 1.2", Trace 4 Length = 4.2"
Best Case: $Z_0 = 47\Omega$, $T_P = 170$ ps/inch, Trace 1 Length = 1.4", Trace 2 Length = 0.2", Trace 3 Length = 0.2", Trace 4 Length = 1.4"

Figure 4. Module System Loading for SYS_DATA, SYS_ECC

TABLE 3: Setup and Hold Time Specifications

Symbol	Description	Waveform	167 MHz [1]		Unit
			Min	Max	
tsu	SYS_DATA[127:0] setup time	1	3.9	–	ns
tsu	SYS_ADDR[35:0] setup time	1	2.9	–	ns
tsu	SYS_ECC[15:0] setup time	1	3.9	–	ns
tsu	S_REPLY[3:0] setup time	1	4.4	–	ns
th	SYS_DATA[127:0] hold time	1	0.7	–	ns
th	SYS_ADDR[35:0] hold time	1	0.6	–	ns
th	SYS_ECC[15:0] hold time	1	0.3	–	ns
th	S_REPLY[3:0] hold time	1	0.6	–	ns

1. These timing parameters are referenced to the receiver clock input pin on this module.

TABLE 4: Propagation Delay, Output Hold Time Specifications

Symbol	Description	Waveform	167 MHz [1]		Unit
			Min	Max	
tp	SYS_DATA[127:0] clk to out	2	–	6.1	ns
tp	SYS_ADDR[35:0] clk to out	2	–	3.1	ns
tp	SYS_ECC[15:0] clk to out	2	–	6.1	ns
toh	SYS_DATA[127:0] clk out	2	1.1	–	ns
toh	SYS_ADDR[35:0] clk out	2	0.0	–	ns
toh	SYS_ECC[15:0] clk out	2	1.4	–	ns

1. These timing parameters are referenced to the driver clock input pin on this module.

Timing Measurement Waveforms

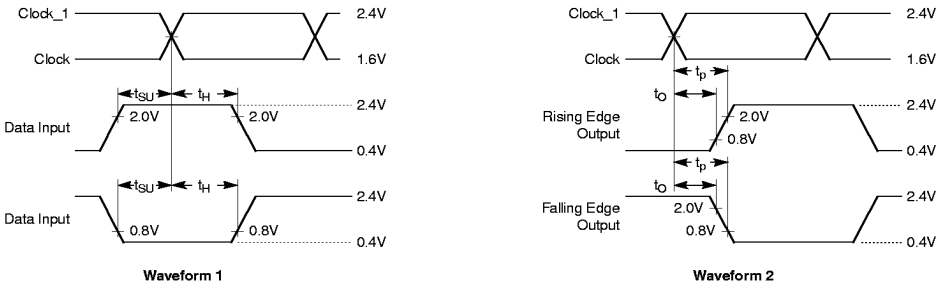


Figure 5. LVTTL Voltage Waveforms

MECHANICAL SPECIFICATIONS

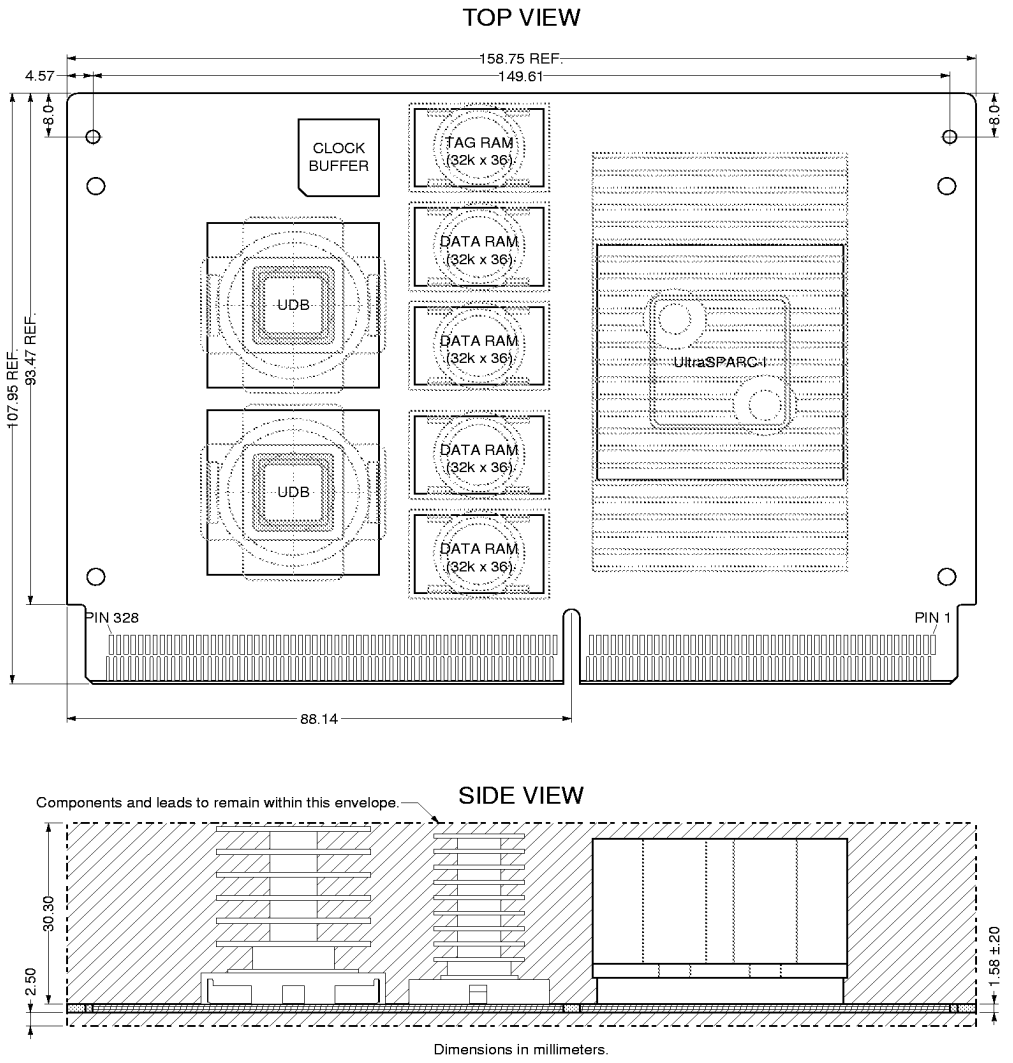


Figure 6. CPU Module Dimensions

THERMAL SPECIFICATIONS

The maximum junction temperature (T_j) specification is 105 °C, which is equivalent to the maximum case temperature (T_C) of 90 °C for the UltraSPARC-I CPU. T_C can be obtained from the following relationship:

$$T_C = T_a + P_d \times \theta_{ca}$$

where T_a is the ambient air temperature, P_d is the power dissipation, and the case-to-air thermal resistance (θ_{ca}) for the CPU with a heat sink are listed in the table below.

Thermal Resistances

	Air Flow (ft./min)			
	200	300	400	500
θ_{ca} (°C/W) [1]	1.41	1.09	0.95	0.88
θ_{ca} (°C/W) [2]	1.15	0.98	0.88	0.81

1. Free-stream airflow.
2. Ducted airflow.

TESTABILITY

The STP5110A UltraSPARC-I module implements the IEEE 1149.1 standard to aid in board level testing. Boundary Scan Description Language (BSDL) is available for the device.

JTAG (IEEE 1149.1) TIMING

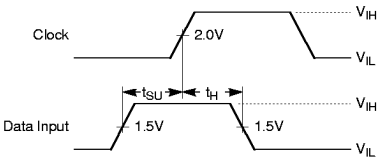


Figure 7. Voltage Waveforms - Setup and Hold Times

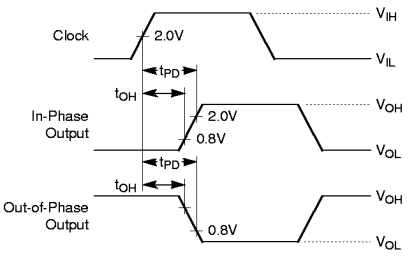


Figure 8. Voltage Waveforms - Propagation Delay Times

ORDERING INFORMATION

Part Number	Speed	Description
STP5110AUPA-167	167 MHz CPU, 83 MHz UPA	167 MHz CPU Bus, 83 MHz UPA module with UltraSPARC-I (STP1030A), 0.5 MB SRAMs, and UDBs.

Document Part Number: STP5110A