DATA SHEET

UAA3536HN

Low power GSM/DCS/PCS multi-band transceiver

Objective specification

File under Integrated Circuits, ICXX

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Philips
Semiconductors

PHILIPS

Low power GSM/DCS/PCS multi-band transceiver

UAA3536

FEATURES

- Multiple band application for GSM, DCS and PCS cellular phone systems

- Compliant to GPRS class 12 operation

- Compliant to EDGE RX operation

- Low noise and wide dynamic range low IF receiver

- More than 35 dB on chip image rejection in receive

- More than 84 dB gain control range in receive

- Integrated channel filter

- Integrated TX filters

- High precision IQ modulator

- Multi-Band Tx modulation loop architecture including offset mixer and phase-frequency detector

- Fully integrated fractional N RF synthesiser with AFC control possibility

- Fully integrated RF VCO with integrated supply regulator

- Semi integrated reference oscillator with integrated coarse AFC possibility and with integrated supply regulator

- Two outputs to control RF frontend switches (pin diodes)

- Fully differential design minimizing cross-talk and spurs

- Functional down to 2.4 V and up to 3.3 V

- 3-wire serial bus interface

- HVQFN40 package

APPLICATIONS

- GSM 900 MHz, DCS 1800 MHz and PCS 1900 MHz hand-held transceivers.

GENERAL DESCRIPTION

The UAA3536 integrates the receiver and most of the transmitter section of GSM, DCS and PCS hand-held transceiver.

The receiver consists of two distinct parts. First, the RF receiver front-end which amplifies the GSM, DCS or PCS aerial signal, converts the chosen channel down to a low IF of 100 kHz, and provides in addition more than 35 dB image suppression. The frontend gain is switchable by one 20dB gain step. Some selectivity is provided at this stage by an on-chip low-pass filter, and channel selectivity is provided by means of a high performance integrated band-pass filter. Then, the IF section further amplifies the wanted channel, performs gain control to tune the output level to the desired value and rejects DC. The IF gain can be varied over a range of 68 dB.

The transmitter consists of a closed loop modulation architecture. The down converted feedback RF transmit signal is mixed with the IQ modulation signals. In a phase frequency detector it is compared with the LO signal divided down to about 60 or 114 MHz and drives the charge pump for the external TX VCO.

The local oscillators (LO) signals required are provided by an on chip VCO for operation of the RF section. The frequencies of the RF VCO are set by an internal fractional N synthesiser PLL circuit, which are programmable via a 3-wire serial bus. Comparison frequency is 26 MHz (12 Hz step programmability) derived from the 26 MHz reference signal which is generated with the semi integrated reference oscillator. The quadrature phase RF LO signals required for IQ mixers in reception are generated internally. The reference oscillator can be without frequency control. In this case the precise receive and transmit frequencies have to be programmed via the fractional N synthesiser. A coarse AFC control is possible via programmable switched capacitors.

Two outputs are available to control external RF frontend switches, e.g. used for band selection.

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The circuit can be powered-up into four different modes, RX, TX, SYN or REF mode, depending on supply voltages applied, the logical level at pins RXON/TXON/SYNON and the 3-wire bus serial programming. In RX (TX) mode, all sections required for receive (transmit) are turned on. The SYN mode is used to power-up the synthesiser and the RF VCO prior to the RX or TX mode. In the SYN mode, some internal LO buffers are also powered-up such that VCO pulling is minimized when switching on the receiver or the transmitter. The reference oscillator (REF mode) is turned on by applying the supply voltage. Additionally band selection is done using the 3-wire bus serial programming allowing the proper enabling of the LNAs and TX charge-pump current programming.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3536HN	HVQFN40	plastic, heatsink very thin quad flat package; 40 terminals; $6 \times 6 \times 0.85$ mm	SOT618-1

BLOCK DIAGRAM
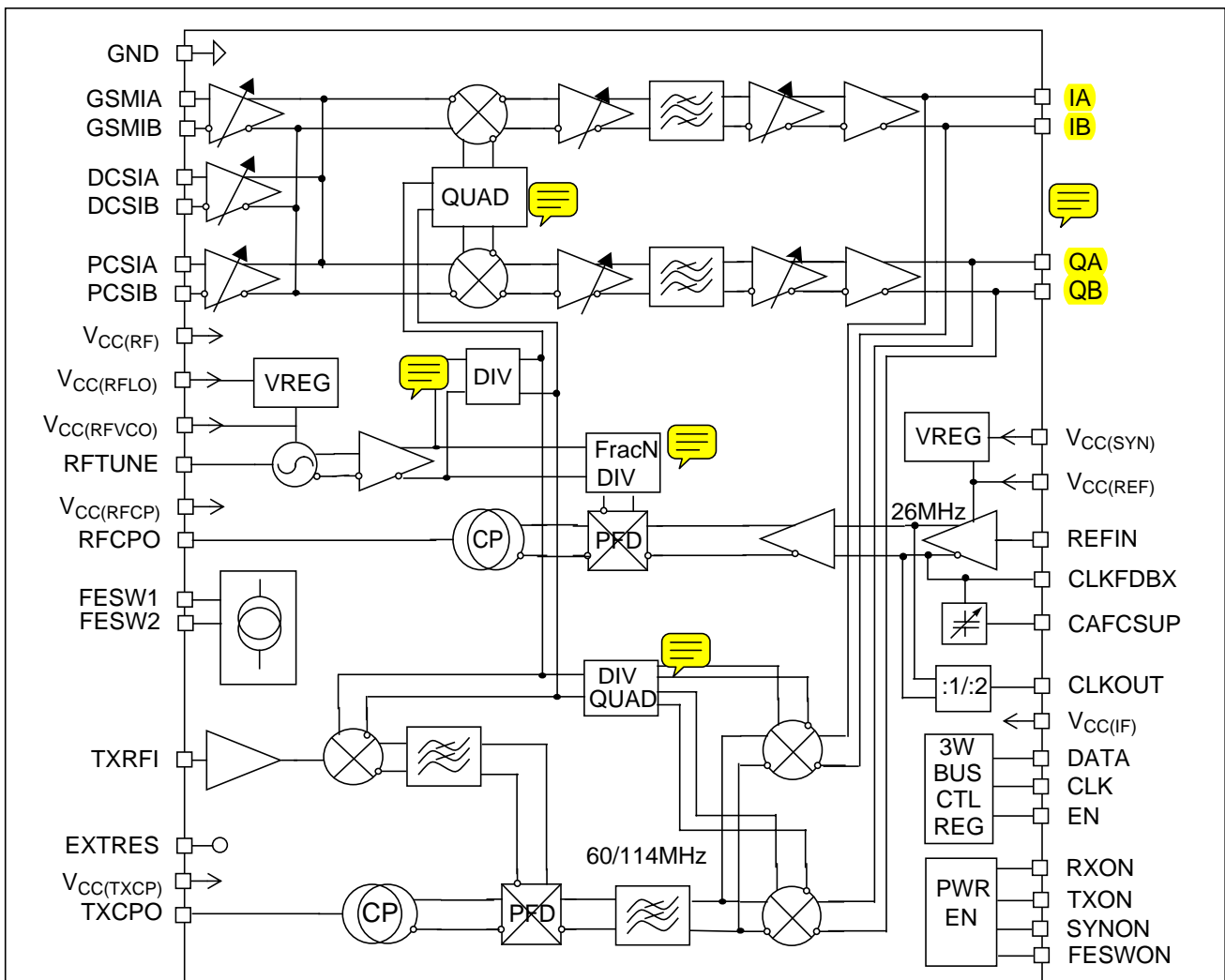
Fig.1 Block diagram.
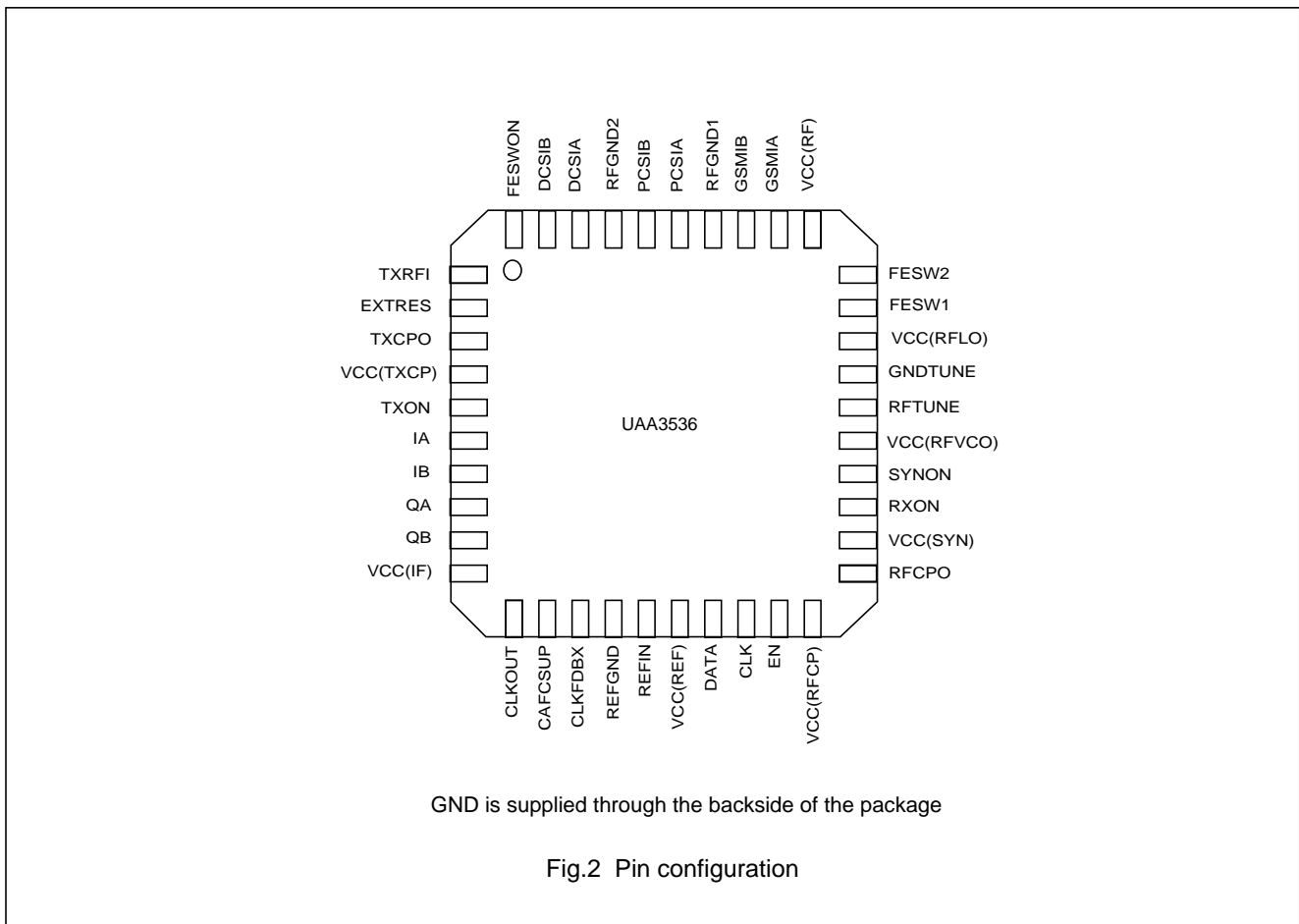
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PINNING

SYMBOL	PIN	DESCRIPTION
TXRFI	1	Input from RF transmit VCOs
EXTRES	2	reference resistor for transmit modulation loop
TXCPO	3	transmit modulation loop charge-pump output
$V_{CC(TXCP)}$	4	transmit modulation loop charge-pump supply
TXON	5	TX mode control pin
IA	6	baseband input-output; I path
IB	7	baseband input-output; I path
QA	8	baseband input-output; Q path
QB	9	baseband input-output; Q path
$V_{CC(IF)}$	10	IF supply
CLKOUT	11	reference oscillator output
CAFCSUP	12	coarse AFC memory supply
CLKFDBX	13	reference oscillator feedback
REFGND	14	Ground for reference oscillator
REFIN	15	reference oscillator input
$V_{CC(REF)}$	16	reference oscillator supply
DATA	17	3-wire bus; DATA input
CLK	18	3-wire bus; CLOCK input
EN	19	3-wire bus; ENABLE control pin
$V_{CC(RFCP)}$	20	RF charge-pump supply
RFCPO	21	RF charge-pump output
$V_{CC(SYN)}$	22	synthesizer supply
RXON	23	RX mode control pin
SYNON	24	SYN mode control pin
$V_{CC(RFVCO)}$	25	RF VCO supply
RFTUNE	26	tuning input of RF VCO
GNDTUNE	27	Ground for RF VCO tuning
$V_{CC(RFLO)}$	28	RF LO supply
FESW1	29	frontend switch control output
FESW2	30	frontend switch control output
$V_{CC(RF)}$	31	RF front-end and transmit modulation loop supply
GSMIA	32	receiver GSM RF input
GSMIB	33	receiver GSM RF input
RFGND1	34	Ground for RF frontend
PCSIA	35	receiver PCS RF input
PCSIB	36	receiver PCS RF input

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SYMBOL	PIN	DESCRIPTION
RFGND2	37	Ground for RF frontend
DCSIA	38	receiver DCS RF input
DCSIB	39	receiver DCS RF input
FESWON	40	frontend switch control input

GND is supplied through the backside of the package

Fig.2 Pin configuration

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FUNCTIONAL DESCRIPTION

RF Receiver

The receiver front-end converts the aerial RF signal from EGSM (925 - 960 MHz), DCS (1805 - 1880 MHz) or PCS (1930 - 1990 MHz) bands down to a low intermediate frequency (IF) of 100 kHz. The first stages are symmetrical low noise amplifiers (LNAs) with one 20dB gain step. They are matched to 50 W using external baluns. The LNAs are followed by an I, Q down-mixer. It consists of two mixers in parallel but driven by quadrature out of phase LO signals. The In phase (I) and Quadrature phase (Q) IF signals are low pass filtered to provide protection from high frequency offset interferers. The low IF I and Q signals are then fed into the channel filter.

Channel filter and AGC

The front-end low IF I and Q outputs enter the integrated bandpass channel filter with provision for five 8 dB gain steps in front of the filter. The filter is a self-calibrated fifth order band-pass filter centred around 100 kHz and has a bandwidth of 240 kHz for GSM mode, 300kHz for EDGE mode. Being filtered the low IF I and Q are further amplified with provision for ten 4 dB gain steps and fully integrated DC offset compensation. Realised with an active high pass circuit this compensation either operates continuously or keeps the acquired offset correction during the bursts depending on the programming. The low IF output buffer provides close to rail-to-rail output signals.

IQ modulator

I and Q baseband signals are applied to the IQ modulator that shifts the modulation spectrum up to the transmit IF. It is designed for low harmonic distortion, low carrier leakage and high image rejection to keep the phase error as small as possible. The modulator is loaded at its IF output by an integrated low pass filter that supress unwanted spurs prior to get into the phase detector. The clock drive is generated by division of the RFLO signal provided for the transmit offset mixer.

Transmit modulation loop

The analog transmit modulation loop is composed by an on-chip offset mixer with spur filter and by a phase/frequency detector with charge pump. The loop is closed off-chip by a loop filter and transmit VCO. The analog PLL copies the modulation to the off-chip transmit VCO and acts as a tracking filter. A PLL of at least third order is required to meet noise requirements at 20 MHz offset from carrier. The PLL bandwidth must be greater than 700 kHz in order to keep a low dynamic phase error and to minimize the acquisition time. The IF frequencies used are about 60 MHz for GSM/PCS and about 114 MHz for DCS.

RF VCO

The RF VCO is fully integrated and self calibrating on manufacturing tolerances. It consists of 20 different frequency ranges that are selected internally depending on the frequency programming. It covers the necessary bandwidth of 1804 to 1991MHz and is tuned via the RF charge pump and the external loop filter. An internal supply voltage regulator using $V_{CC(RFLO)}$ as input supplies the RF VCO and minimises parasitic couplings and pushing. This regulator and the RF VCO are turned on by the SYNON signal. The 20 different frequency ranges are realised by switching of varactors' cathodes between GND and an internal supply that is generated dynamically. Due to slow discharge of this supply burst mode operation is possible only. For test purpose a fixed supply can be chosen.

RF LO section

The RF LO section covering the 1804 to 1991 MHz bandwidth is driven by the internal RF VCO module. It includes the LO buffering for the RF PLL, a divider by two or one for GSM and DCS/PCS respectively which drives a quadrature generation network to supply the RX IQ down-mixer or it drives the transmit modulation loop offset mixer and the clock divider driving the IQ modulator.

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RF FracN Synthesiser PLL

A high performance RF fractional N synthesiser PLL is included on chip which allows to synthesise the frequencies of the RF VCO. Very low close-in phase noise is achieved which allows to widen the PLL loop bandwidth for shorter settling time. The programmable 'main' dividers are controlled by a second order SD modulus controller. They divide the RF VCO signal down to frequencies of 26 MHz (12 Hz step programmability). Their phase is then compared in a digital phase/frequency detector (PFD) to that of the 26 MHz reference clock signal. The phase error information is fed back to the VCO via the charge pump circuit that 'sources' into or 'sinks' current from the loop filter capacitor, changing the VCO frequency such that the loop gets finally 'phase locked'. The charge pump output current is adapted internally to compensate for changes of RF VCO gain so that the tolerance of the PLL bandwidth is minimised.

Reference Oscillator

An amplifier is integrated to build a crystal oscillator. Externally only a quartz and few passive components are needed. 26 MHz is the reference frequency. It is turned on when the supply voltage $V_{CC(SYN)}$ is applied. After division by two a reference clock of 13MHz is supplied to the other parts of the system through the pin CLKOUT. On request 26MHz can be made available on this pin. An internal supply voltage regulator using $V_{CC(SYN)}$ as input supplies the reference oscillator and minimises parasitic couplings and pushing. AFC can be done by the FracN synthesiser programming or via an external varactor. Additionally a coarse AFC control with a resolution of 8 bit is integrated via switchable capacitors. The programming of the coarse AFC capacitors is maintained during sleep mode through supplying the register via pin CAFCSUP. An off chip capacitor is connected to CAFCSUP and is charged via an internal diode from pin $V_{CC(REF)}$. Furthermore instead of realising this semi-integrated oscillator a reference clock coming from an external module can be applied to pin REFIN. This module can be supplied through $V_{CC(REF)}$ pin.

Control of frontend switches

Two outputs are provided to drive RF switches of the phone, e.g. for switching between bands.

Power-up reset

A power-up reset generates a reset pulse at power supply ramp-up to initialise digital functions.

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LIMITING VALUES

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T_{amb}	operating ambient temperature	-30	+70	°C
T_{stg}	storage temperature	-40	+150	°C
V_{CC}	supply voltages	-0.3	3.6	V
V_{CCCP}	supply voltages for RX and TX charge pumps	-0.3	4.25	V
P_{MAX}	maximum power dissipation	-	1	W

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\,j-c}$	thermal resistance from junction to case	25	K/W

DC CHARACTERISTICS

V_{CC} = 2.6V; V_{CC}CP = 4.0 V; T_{amb} = 25 °C; unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins VCC(RF), VCC(IF), VCC(RFLO) and VCC(SYN)						
V_{CC}	supply voltage	note 1	2.4	-	3.3	V
Pin VCC(RFVCO)						
$V_{CC(RFVCO)}$	internal supply voltage of RF VCO	output only	1.75	1.87	2	V
Pin VCC(REF)						
$V_{CC(REF)}$	internal supply voltage of reference oscillator	output only; VCC(SYN)>=2.6V; -30°C<=T_{amb}<=70°C	2.3	-	2.5	V
I_{OUTREF}	source current to external	VCC(SYN) turned on	2	-	-	mA
Pin VCC(RFCP)						
$V_{CC(RFCP)}$	supply voltage of phase detector and charge pump		3.8	-	4.25	V
Pin VCC(TXCP)						
$V_{CC(TXCP)}$	supply voltage of phase detector and charge pump		2.6	-	4.25	V
Pins VCC(RF), VCC(IF), VCC(RFLO), VCC(SYN), VCC(TXCP) and VCC(RFCP)						
I_{CCPD}	supply current (V_{CC} = 2.6 V; V_{CC}CP = 4.0 V); normal mode	power-down (total); VCC(SYN)=0V; RXON, TXON, SYNON and FESWON = Hi Z; pins EN, DATA, and CLK = Hi Z	-	10	30	µA
I_{CCPD}Pres	supply current (V_{CC} = 2.6V, V_{CC}CP = 4.0V); preset mode	power-down (total); VCC(SYN)=0V; RXON, TXON, SYNON and FESWON = 0; pins EN, DATA and CLK = 1	-	100	200	µA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CCREF}	supply current REF mode	reference oscillator active (SYNVCC=2.6V)	-	4.6	5.3	mA
I_{CCRX}	supply current RX mode	RX and SYN mode active; FESW off	-	69	82	mA
I_{CCTX}	supply current TX mode	TX and SYN mode active; FESW off	-	69	87	mA
$I_{CCTXFESW}$	supply current TX mode, FESW active	TX and SYN mode active; I_{FESW1} = 2mA; I_{FESW2} = 2mA	-	73	91	mA
I_{CCSYN}	supply current SYN mode	SYN mode active	-	40	46	mA
Pin VCC(RF)						
I_{CCRX}	supply current of RF receiver and RFQUAD (one LNA only)	RX mode active	-	18	-	mA
I_{CCLNA}	supply current of one LNA only	RX mode active	-	7.5	-	mA
I_{CCTX}	supply current of transmit modulation loop (without charge pump)	TX mode active	-	14	-	mA
Pin VCC(IF)						
I_{CCRX}	supply current for IQ low IF bandpass filter	RX mode active	-	4	-	mA
I_{CCRX}	supply current IQ AGC and buffer	RX mode active	-	3	-	mA
I_{CCTX}	supply current IQ Modulator path	TX mode active	-	10.5	-	mA
Pin VCC(RFLO)						
I_{CCRX}	supply current of RF VCO, RF LO buffer and divider section	SYN mode active; RX mode active	-	24	-	mA
I_{CCTX}	supply current of RF VCO, RF LO buffer and divider section	SYN mode active; TX mode active	-	28	-	mA
I_{CCSYN}	supply current of RF VCO and RF LO buffer	SYN mode active	-	19	-	mA
Pin VCC(SYN)						
I_{CCREF}	supply current of reference oscillator		-	4.6	-	mA
I_{CCSYN}	supply current of reference oscillator and RF synthesizer	SYN mode active	-	17	-	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin VCC(RFCP)						
I_{CPRF}	supply current RFLO charge pump	SYN mode active; ext. resistor = 22.6 kΩ (1%); programmed to 0.52mA; in lock: during freq. acquisition: during precharge (for 32.5μs after synth. turnon); note 2	-	-	0.32 0.87 6	mA
Pin VCC(TXCP)						
I_{CPTX}	supply current TX charge pump	TX mode active; ext. resistor = 22.6 kΩ (1%); TXI1=1; TXI2=1; in lock; during freq. acquisition; note 2	-	-	0.9 2.45	mA
Pins IA, IB, QA and QB						
V_{IQ}	common mode input-output IQ voltage range	(Via + Vib) / 2 or (Vqa + Vqb) / 2; note 3	1.15	1.25	1.35	V
Pin EXTRES						
V_{EXTRES}	reference voltage for I_{CP}	R_{ext}=22.6kΩ (1%)	0.95	1.0	1.05	V
Pin CAFCSUP						
$V_{CAFCSUP}$	internal supply voltage	SYNON=1	-	VCC(REF)	-	
Pins FESW1, FESW2 (4)						
V_{FESW}	output voltage	I_{source}=10mA	2.3	-	2.5	V
V_{FESW}	output voltage	outputs in tri-state	0	-	VCC(RF)	
Logical input levels: pins EN, DATA, CLK, RXON, TXON, SYNON, FESWON						
V_{IH}	logical HIGH level		0.9	-	VCC(SYN) + 0.3	V
V_{IL}	logical LOW level		-0.3	-	0.3	V

Notes:

1. For VCC < 2.6V only functionality is guaranteed, AC characteristics are not guaranteed

2. These performances are measured and guaranteed on evaluation board.

3. RX mode: DC supplied from the IC
   TX mode: DC supplied from external

4. Currents are supplied from open drain PMOS transistors.

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AC CHARACTERISTICS

V_{CC} = 2.6V; $V_{CC}CP$ = 4.0 V; T_{amb} = -30 to +70 C; unless otherwise stated

RF receiver section

Measured in a 50 Ω impedance system, including external input baluns and matching networks to 50 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins GSMIA and GSMIB						
f_{RF}	RF input frequency range		925	-	960	MHz
R_{IN}	differential input resistance	parallel RC input model	-	110	-	Ω
C_{IN}	differential input capacitance	parallel RC input model	-	1.0	-	pF
NF	noise figure; max AGC gain	notes 1, 1	-	3.7	4.2	dB
NF_{LG}	noise figure; max AGC gain; low LNA gain	HGLG = 0; notes 1, 2	-	23	-	dB
ΔG_{LNA}	LNA gain step	HGLG = 0 <-> 1	16	20	24	dB
G_{OFF}	LNA off-state gain difference	LNA = 1 <-> 0; note 1	45	-	-	dB
P_{OFF}	LNA off-state power handling	LNA = 0; note 1, 3	3	-	-	dBm
Pins DCSIA and DCSIB						
f_{RF}	RF input frequency range		1805	-	1880	MHz
R_{IN}	differential input resistance	parallel RC input model	-	170	-	Ω
C_{IN}	differential input capacitance	parallel RC input model	-	0.8	-	pF
NF	Noise figure, max AGC gain	notes 1, 2	-	4.2	4.7	dB
NF_{LG}	noise figure; max AGC gain; low LNA gain	HGLG = 0; notes 1, 2	-	23	-	dB
ΔG_{LNA}	LNA gain step	HGLG = 0 <-> 1	16	20	24	dB
G_{OFF}	LNA off-state gain difference	LNA = 1 <-> 0; note 1	45	-	-	dB
P_{OFF}	LNA off-state power handling	LNA = 0; notes 1, 3	6	-	-	dBm
Pins PCSIA and PCSIB						
f_{RF}	RF input frequency range		1930	-	1990	MHz
R_{IN}	differential input resistance	parallel RC input model	-	170	-	Ω
C_{IN}	differential input capacitance	parallel RC input model	-	0.7	-	pF
NF	Noise figure, max AGC gain	notes 1, 2	-	4.4	4.9	dB
NF_{LG}	noise figure; max AGC gain; low LNA gain	HGLG = 0; notes 1, 2	-	23	-	dB
ΔG_{LNA}	LNA gain step	HGLG = 0 <-> 1	16	20	24	dB
G_{OFF}	LNA off-state gain difference	LNA = 1 <-> 0; note 1	45	-	-	dB
P_{OFF}	LNA off-state power handling	LNA = 0; note 1, 3	6	-	-	dBm

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins GSMIA, GSMIB, DCSIA, DCSIB, PCSIA and PCSIB						
S11	input power matching	note 1	-	-15	-10	dB
$SPUR_{IN}$	spurious power level at RF input	in 900 to 1000 MHz band, note1	-	-	-57	dBm
		in 1800 to 2000 MHz band, note 1	-	-	-47	dBm
		out of preceding bands, note 1	-	-	-45	dBm
CP1	1 dB input compression point; minimum AGC gain	T_{amb} = 25 °C; HGLG=1; note 1	-25	-	-	dBm
$CP1_{LG}$	1 dB input compression point; minimum AGC gain	T_{amb} = 25 °C; HGLG=0; note 1	-7	-	-	dBm
IP3	input referred 3rd order intercept; maximum AGC gain	T_{amb} = 25 °C; HGLG=1; notes 1, 4	-18	-	-	dBm
$IP3_{LG}$	input referred 3rd order intercept; maximum AGC gain	T_{amb} = 25 °C; HGLG=0; notes 1, 4	0	-	-	dBm
IP2	input referred 2nd order intercept; maximum AGC gain	T_{amb} = 25 °C; HGLG=1; notes 1,5	27	-	-	dBm
$IP2_{LG}$	input referred 2nd order intercept; maximum AGC gain	T_{amb} = 25 °C; HGLG=0; notes1, 5	40	-	-	dBm
Blocking	C/N ratio at blocking	T_{amb} = 25 °C; Δf = 3 MHz; GSM: P_w = -101dBm; $\quad P_{int}$ = -25dBm; note 1	8	-	-	dB
		DCS/PCS: P_w = -101dBm; $\quad P_{int}$ = -28dBm; note 1	8	-	-	
IMrej	image rejection	Δf_{IF} = 200 kHz; T_{amb} = 25 °C; note 1	35	38	-	dB
$\Delta GvRF$	gain mismatch between operation of different bands	note 1	-	-	2	dB
Pins IA, IB, QA and QB (Rx mode)						
Gv_{MIN}	voltage conversion gain	AGC gain set to min.; HGLG=1; notes 1, 6	20	26	32	dB
Gv_{MAX}	voltage conversion gain	AGC gain set to max.; HGLG=1; notes 1, 6	90	94	98	dB
$\Delta GvBW$	gain difference between GSM and EDGE mode	RXBW = 0 <-> 1	-	1.7	-	dB
$\Delta GvIQ$	gain mismatch I and Q paths		-	-	0.5	dB
Gv_{STEP}	voltage conversion gain step	note 6	-	4	-	dB
AGC_{lin}	gain control linearity	T_{amb} = 25 °C; note 6, 7	-2	-	2	dB
		over any 20 dB gain range; note 7	-0.5	-	0.5	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{OUT,lin}$	linear output voltage per pin	R_L = 100 kΩ differential; C_L=10pF differential; THD < 3%; note 8	0.75	-	-	V_{pk}
$V_{OUT,max}$	maximum output voltage per pin	R_L = 100 kΩ differential;	-	-	VCC(IF) / 2	V_{pk}
I_{OUT}	maximum output current per pin		-	-	2000	µA
V_{offset}	differential output offset voltage	in settled conditions	-300	-	+300	mV
$f_{HP,-3dB}$	−3dB high pass corner frequency (dc notch)	FASTSETL=0; STOPSETL=0	4	6	8	kHz
BW_{GSM}	−3dB LOW IF filter bandwidth for GSm operation	100 kHz center frequency GSM mode; RXBW=0	220	240	260	kHz
BW_{EDGE}	−3dB LOW IF filter bandwidth for EDGE operation	100 kHz center frequency EDGE mode; RXBW=1	275	300	325	kHz
$\Delta\tau_{gd}$	group delay variation	30 kHz < f_{OUT} < 170 kHz	-	1.5	2	µs
Att_{GSM}	LOW IF filter attenuation (5th order) in GSM mode	RXBW = 0 f_{OUT} = 100 kHz ± 200 kHz	17	31	-	dB
		f_{OUT} = 100 kHz ± 400 kHz	54	64	-	dB
		f_{OUT} = 100 kHz ± 600 kHz	73	82	-	dB
Att_{EDGE}	LOW IF filter attenuation (5th order) in EDGE mode	RXBW = 1 f_{OUT} = 100 kHz ± 200 kHz	10	19	-	dB
		f_{OUT} = 100 kHz ± 400 kHz	45	54	-	dB
		f_{OUT} = 100 kHz ± 600 kHz	64	73	-	dB

Notes:

1. Measured and guaranteed only on UAA3536 evaluation board.

2. This value excludes printed circuit board and balun losses.

3. No spurs are created as specified in $SPUR_{IN}$.

4. IP3 related to an IM3 measurement with two tones at 800 and 1600kHz offset.

5. IP2 related to an IM2 measurement with two tones at 6 and 6.1MHz offset.

6. Voltage gain defined as the differential baseband RMS output voltage (either at pins IA and IB or pins QA and QB measured in standard load) divided by the RMS input voltage at the RF baluns.

7. Values are not applicable for HGLG=0.

8. Valid for following max. RF input power: HGLG=1: -31 dBm; HGLG=0: -15 dBm

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Transmit modulation loop section

General conditions: V_{mod} = 0.5 V_{pk}; f_{mod} = 67.7 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins IA, IB, QA and QB (mode Tx)						
f_{mod}	modulation frequency range	3 dB low pass cutoff frequency	1	-	-	MHz
V_{mod}	modulation level	single ended; peak value	-	0.5	0.55	Vpk
R_{IN}	dynamic input resistance	single ended	-	14.4	-	kΩ
Offset mixer: pin TXRFI						
f_{RF}	RF input frequency range	GSM DCS PCS	880 1710 1850	- - -	915 1785 1910	MHz
R_{IN}	single ended input resistance	parallel RC input model 900MHz 1900MHz	 - -	 65 35	 - -	Ω
C_{IN}	single ended input capacitance	parallel RC input model 900MHz 1900MHz	 - -	 3.4 2.0	 - -	pF
P_{IN}	input power		-22	-19	-16	dBm
CP1	1 dB input compression point	T_{amb} = 25 °C	-	-22	-	dBm
$SPUR_{IN}$	spurious power level at RF input	LO leakage	-	-50	-45	dBm
		other	-	-	-45	dBm
V_{TXRFI}	range of applied voltage		-0.3	-	VCC(RF) + 0.3	V
Phase detector: pin TXCPO						
I_{CP}	charge pump maximum sink or source current	R_{ext} = 22.6 kΩ (1%); over V_{CP} range; TXI1 = 0; TXI2=0; TXI1 = 1; TXI2=0; TXI1 = 0; TXI2=1; TXI1 = 1; TXI2=1	 0.42 0.63 0.85 1.27	 0.5 0.75 1 1.5	 0.58 0.87 1.15 1.73	mA
f_{TXIF}	TXIF frequency	GSM/PCS DCS	- -	60 114	- -	MHz
$N_{TXIFDIV}$	TXIF divider ratio	GSM/DCS;IFDIV=0 PCS; IFDIV=1	-	16 32	-	-
KΦ	phase frequency detector gain		-	$I_{CP}/2\Pi$	-	A/rad
V_{CP}	charge pump output voltage		0.4	-	V_{CCCP} - 0.4	V
R_{OUT}	output resistance	V_{OUT} = V_{CCCP} / 2	100	-	-	kΩ
$R_{OUT(OFF)}$	output resistance to ground when powered down	TX mode disabled	-	500	-	Ω

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IQ Modulator; f_{mod}=67.7kHz						
Φ_{NOISE} phase noise output power density		T_{amb} = 25 °C; Δf = 400 kHz; note 1, 2; GSM DCS, PCS	-	-122 -118	-120 -116	dBc/Hz
		T_{amb} = 25 °C; Δf = 1.8 MHz; note 1, 2; GSM DCS,PCS	-	-126 -122	-123 -119	dBc/Hz
		T_{amb} = 25 °C; Δf = 20 MHz; note 1, 2; GSM DCS/PCS	-	-	-163 -157	dBc/Hz
LO_{OUT}	local oscillator feedthrough	$f = (F_c + f_{mod})$ +/- f_{mod} ; note 1, 2	-	-40	-32	dBc
IM_{OUT}	image level	$f = (F_c + f_{mod})$ +/− 2 $*$ f_{mod}; note 1, 2	-	-45	-37	dBc
$SPUR4f_m$	spurious level at 4 $*$ f_{mod} offset from wanted	$f = (F_c + f_{mod})$ +/− 4 $*$ f_{mod}; note 1, 2	-	-55	-46	dBc
$SPUR16f_m$	spurious level at 16 $*$ f_{mod} offset from wanted	$f = (F_c + f_{mod})$ +/− 16 $*$ f_{mod}; GSM, DCS; notes 1, 2, 3	-	-	-60	dBc
$SPUR32f_m$	spurious level at 32 $*$ f_{mod} offset from wanted	$f = (F_c + f_{mod})$ +/− 32 $*$ f_{mod}; PCS; notes 1, 2, 3	-	-	-65	dBc
$SPUR_{other}$	spurious level at other frequencies	abs(f-(F_c+f_{mod}))>=400kHz note1, 2	-	-	-70	dBc

Notes

1. Measured and guaranteed only on UAA3536 evaluation board.

2. Measured at external transmit VCO output.

3. Spur is not critical for pseudo random and application modulation spectrum.

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Synthesizer and RF VCO

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF synthesizer; pin RFCPO						
f_{RFLO}	synthesizer frequency range		1774.5	-	2047.5	MHz
f_{compRF}	comparison frequency		-	26	-	MHz
f_{stepRF}	freq. step programmability	f_{comp} = 26 MHz	-	12.4	-	Hz
Φ_{noise}	close-in phase noise	Δf = 2 kHz; note 1, 2	-	-85	-82	dBc/Hz
P_{spur}	spur levels	Δf > 400kHz	-	-	-70	dBc
I_{CP}	Charge pump maximum sink or source current	R_{ext} = 22.6 kΩ (1%); over V_{CP} range; currents set internally: for I_{CP} = 310µA for I_{CP} = 380µA for I_{CP} = 420µA for I_{CP} = 520µA for I_{CP} = 540µA for I_{CP} = 650µA for I_{CP} = 660µA for I_{CP} = 800µA	260 320 350 440 450 540 550 680	310 380 420 520 540 650 660 800	360 440 490 600 630 760 770 920	µA
$K\Phi$	phase freq. detector gain		-	$I_{CP}/2\Pi$	-	A/rad
t_{prech}	loop filter precharge time	after SYNON = 0 -> 1	-	32.5	-	µs
I_{leak}	charge pump leakage current in off state	over full V_{CP} range	-1	-	1	µA
V_{CP}	charge pump output voltage		0.4	-	V_{CCCP} - 0.4	V
$R_{OUT(OFF)}$	output resistance to ground when powered down	SYN mode disabled	-	50	-	Ω
Fractional N Synthesiser						
N	integer divider ratio	f_{comp}=26MHz	8	-	28	
K	fractional divider programming word	f_{comp}=26MHz	524,287	-	1,572,864	
K_{frac}	fractional divider ratio	f_{comp}=26MHz	0.25	-	0.75	
Formulas for frequency calculation: $f(VCO) = fcomp \times \left(\dfrac{N+128}{2} + Kfrac\right)$; $Kfrac = \left(\dfrac{K}{2^{21}} + \dfrac{1}{2^{22}}\right)$;						
Integrated RF VCO: pin RFTUNE						
f_{RF}	RF frequency range		1804	-	1991	MHz
G_{vco}	VCO gain	Vtune=2.0V	15	20	25	MHz/V
$\Delta G_{(VCO*K\Phi)}$	VCO gain times phase freq. detector gain variation	$\Delta G_{(VCO*K\Phi)}$ / $G_{(VCO*K\Phi)}$	-30	-	30	%
R_{tune}	RFTUNE series resistor inside the IC		-	50	-	Ω
C_{tune}	parallel capacitor to ground inside the IC after R_{tune}	freq = 400kHz; 0.4V; freq = 400 kHz; 3.4V	-	20 17	-	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{tune}	tuning voltage range		0.4	-	V_{CCCP} -0.4	V
$\Delta f_{VCC,RFLO}$	pushing		-	-	2	MHz/V
$t_{VCO,cal}$	VCO calibration time	after SYNON = 0 -> 1	-	32.5	-	µs

Notes

1. These performances are measured and guaranteed on evaluation board.

2. For measurement TX mode is activated and signal is taken from TX VCO output.

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Low noise crystal oscillator

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins REFIN, CLKFDBX						
f_{REF}	reference frequency		-	26	-	MHz
R_{REFIN}	input resistance	f=26 MHz	-	2.6	-	kΩ
C_{REFIN}	input capacitance	f=26 MHz	-	0.7	-	pF
V_{REFIN}	intern. supplied DC input voltage		1.0	1.1	1.15	V
$R_{CLKFDBX}$	output resistance	f=26 MHz; CAFC0/.../7=0; f=26 MHz; CAFC0/.../7=1	- -	800 900	- -	Ω
$V_{CLKFDBX}$	DC output voltage		1.8	2.0	2.2	V
$V_{IN(REFIN)}$	input voltage level	note 1	300	-	-	mV$_{pp}$
$V_{CLKFDBX}$	limiting output voltage swing	note 1	-	1700	-	mV$_{pp}$
G_V	small signal voltage gain (REFIN, CLKFDBX)	f=2.6MHz; CAFC0/.../7=0; Pin < -42dBm; note 2	-	26.0	-	dB
$SPUR_{OUT}$	Spurious emission	$f = 2 * f_{REF}$, note 1	-	-32	-20	dBc
	Spurious emission	non harmonics, note 1	-	-	-70	dBc
$\Delta f_{VCC,REF}$	pushing	SYNVCC: 2.6V -> 3.3V	-	-	1	ppm
Coarse AFC						
$C_{CAFC,LO}$	CLKFDBX output capacitance LO	CAFC0/.../7=0	17	19	21	pF
$C_{CAFC,HI}$	CLKFDBX output capacitance HI	CAFC0/.../7=1	32	38	44	pF
$C_{CAFC,LSB}$	LSB for coarse AFC capacitor	CAFC1/.../7 =0 CAFC0 = 0 <-> 1	51	70	86	fF
Pin CAFCSUP						
$I_{CAFCSUP}$	leakage current	V_{CCSYN}=0V; $V_{CAFCSUP}$=2.3V	-	-	100	nA
$V_{store,CAFC}$	CAFCSUP storage voltage	CAFC bits remain stored	0.6	-	-	V
Pin CLKOUT						
f_{CLKOUT}	reference output frequency	note 3	-	13	-	MHz
R_{CLKOUT}	output resistance	at DC output voltage	-	130	-	Ω
V_{CLKOUT}	DC output voltage	note 1	SYNVCC - 1.8	SYNVCC - 1.6	SYNVCC - 1.4	V
V_{CLKOUT}	limiting output voltage swing	notes 1, 3	0.75	1	1.15	Vpp
$S_{CLKOUT,pos}$	positive slew rate	between V_{DC} - 100mV and V_{DC} + 100mV; notes 1, 4	55	-	-	mV/ns
$S_{CLKOUT,neg}$	negative slew rate	between V_{DC} - 100mV and V_{DC} + 100mV; notes 1, 4	-	-	-35	mV/ns
D_{CLKOUT}	duty cycle	note 1	40	-	60	%
$\Phi_{noise-BB}$	phase noise at CLKOUT	Δf = 2 kHz, note 1	-	-	-105	dBc/Hz
$Jitter_{XO}$	timing jitter at CLKOUT	notes 1, 4	-1	-	1	ns
$G_{reverse}$	reverse isolation	to pin CLKFDBX; BW<100MHz; note 1	-	-	-20	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta f_{ref, CAFC}$	residual frequency error	after coarse AFC alignment, T_{amb}=25 °C, quartz specified with max. +/- 10ppm; note 1	-0.5	-	0.5	ppm
$\Delta f/f$ (T)	frequency stability as a function of temperature	over full temperature range, quartz specified with max. +/- 20ppm, note 1	-24	-	24	ppm
$\Delta f/f$ (t)	frequency stability as a function of time	quartz specified with +/- 1ppm, T_{amb}=25 °C, note 1	-1.2	-	1.2	ppm/y

Notes

1. These performances are measured and guaranteed on evaluation board. The 26 MHz quartz is outside the IC. $C_{load, quartz}$=10pF

2. Gain value is also valid for 26MHz not taking into account loading by C_{CAFC} and external capacitor.

3. 26 MHz reference output frequency is available on request.

4. $C_{load,CLKOUT}$= 20pF.

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Timing specifications

| SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{REF,ON}$	Turn on time of reference oscillator	settled to Δf=0.1ppm of final frequency, note 1	-	-	8.6	ms
$t_{VCO, reset}$	VCO calibration reset time	SYNON=0; note 2	10	-	-	μs
$t_{VCO,active}$	active VCO time	VCO remains locked; note 2	6	-	-	ms
$t_{SYN,ON}$	Turn on time of RF synthesiser	settled to Δf=0.1ppm of final frequency; notes 1, 3, 4	–	–	200	μs
$t_{RX,ON}$	RX DC settling time	V(IA-IB) settled to 50mV from final DC value; max. AGC gain; SMARTSETL=0; STOPSETL=0;FASTSETL=0; notes 1, 5	-	-	200	μs
$t_{RX, SMART}$	Activation time of SMART RX DC settling	V(IA-IB) settled to 50mV from final DC value; max. AGC gain; SMARTSETL=1; FASTSETL=1; notes 5, 6	161	-	-	μs
$\Delta t_{SYN-RX, SMART}$	Delay for activation of SMART RX DC settling	SMARTSETL=1; FASTSETL=1	40	-	-	μs
$t_{TX,ON}$	TX loop settling time	setlled to Δf=0.1ppm of final value of $f_{TX,out}$; notes 1, 4 TXI1=TXI2=0 TXI1=TXI2=1	- -	- -	150 80	μs

Notes

1. These performances are measured and guaranteed on evaluation board.

2. RF VCO self calibration needs to be activated for every frequency change. Additionally the dynamically generated internal varactor supply discharges over time and needs recharging. For test purpose permanent varactor supply can be chosen by control bit VARCPVCC. New self calibration and recharging are started with SYNON going from 0 to 1.

3. Only valid after crystal oscillator has locked.

4. Measured acc. GSM specification.

5. A new RXDC settling is provoked when changing AGC bits G2, G3, G4, or G5. No change of RXDC settling will occur after changing AGC bits G0 and G1.

6. For SMARTSETL=1 internally defined timings are chosen with settling mode sequences as shown in table below (timing reference is RXON going from 0 to 1). Normal settling means that the active dc compensation is operating continuously with bandwidth as described in RF receiver section. StopSetl and FastSetl function is described in operating modes section.
    For SMARTSETL=0 the settling mode is defined by user programming of the bits FASTSETL and STOPSETL.

SMARTSETL	FASTSETL	STOPSETL	0-40μs	40-80μs	80-120μs	120-160μs	>160μs
1	0	0	StopSetl	Normal	Normal	Normal	Normal
1	1	0	StopSetl	FastSetl	Normal	Normal	Normal
1	0	1	StopSetl	Normal	Normal	Normal	StopSetl
1	1	1	StopSetl	FastSetl	Normal	Normal	StopSetl
0	X	X	depending on user programming				

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Fig.3 Hardware control timing diagram
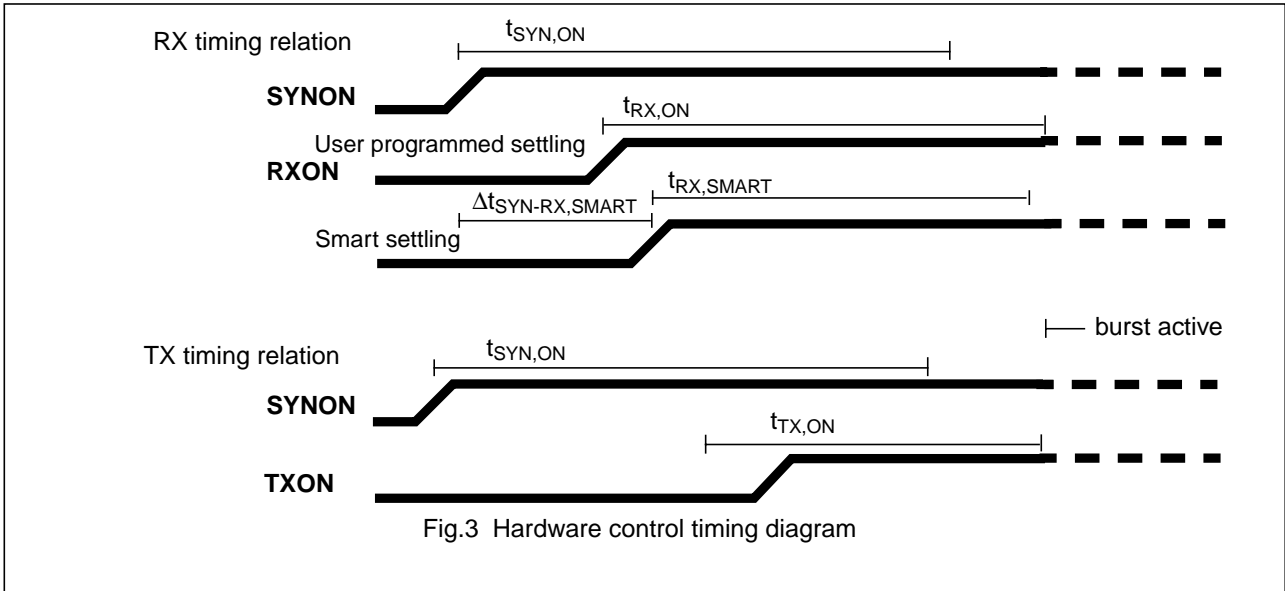
Power supply concept

Three different voltage supplies are needed:
1. For the charge pump blocks: Supply can be turned off in sleep mode.
2. For the reference oscillator (VCCSYN) and other blocks: Supply has to be turned off in sleep mode to turn off the reference oscillator.
3. For TX and RX signal path: Supply can be turned off in sleep mode.

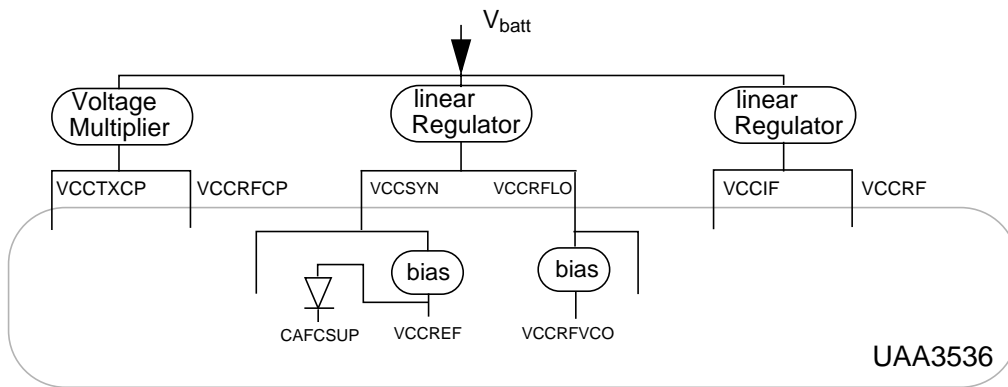The following power supply scheme is proposed:

Fig.4 Power supply concept

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OPERATING MODES

Basic operating mode

The circuit can be powered up into different operating modes depending on the voltage level applied at pins RXON, TXON, SYNON (hardware control) and supply voltage applied. The control bits SYNON, RXON, TXON of the 3-wire bus must be set to logical high accordingly. This defines five main modes called IDLE, REF, SYN, RX and TX mode.

The operation mode status depends on the control pins **SYNON, RXON, TXON and V$_{CC(SYN)}$** according to the table below.

MODE	SYNTHESISER[1] (SYNON)	RECEIVER[2] (RXON)	TRANSMITTER (TXON)	V$_{CC(SYN)}$
IDLE	off	off	off	off
REF	off	off	off	on
SYN	on	off	off	on
RX	on	on	off	on
TX	on	off	on	on

Notes

1. The synthesiser includes the LO buffers common also to the receive and transmit sections.

2. When the receiver is on, it is possible to switch off the low noise amplifier. Refer to receiver control described below.

TX Charge pump current status control

The transmit modulation loop includes a transmit charge pump where sink and source currents are determined by an external resistor. There are four modes with different currents to cope with different transmit VCO gains, e.g. between bands. The selection of these two modes is accomplished by means of the bit TXI1 and TXI2.

The TX charge pump current status depends on the control bit TXI according to the table below.

TXI1 BIT STATUS	TXI2 BIT STATUS	MODE OF OPERATION
0	0	I$_{TXCP}$ = 0.5mA
1	0	I$_{TXCP}$ = 0.75mA
0	1	I$_{TXCP}$ = 1mA
1	1	I$_{TXCP}$ = 1.5mA

TXIF filter status control

The transmit section integrates two switchable low pass filters, one for about 60 MHz IF and the other one for about 114 MHz IF. The selection of these two modes is accomplished by means of the bit FILT.

The transmit filter status depends on the control bit FILT according to the table below.

FILT BIT STATUS	MODE OF OPERATION
0	60 MHz IF
1	114 MHz IF

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TXIF divider ratio status control

The TXIF clock is generated by division of the LO signal of the TX offset mixer. The selection of the division ratios is accomplished by means of the bit IFDIV.

The divider ratios depend on the control bit IFDIV according to the table below.

IFDIV BIT STATUS	MODE OF OPERATION
0	divide by 16 (GSM, DCS)
1	divide by 32 (PCS)

Transmit IF clock I/Q polarity control

The polarity of the I/Q signal for TXIF clock can be changed. The selection of these two modes is accomplished by means of the bit IQPOL.

The TXIF clock I/Q polarity depends on the control bit IQPOL according to the table below.

IQPOL BIT STATUS	MODE OF OPERATION
0	I signal 90 degree before Q
1	Q signal 90 degree before I

Frontend switch control

There are two output pins FESW1 and FESW2 that can supply currents. They are controlled by means of the bits FESW1H, FESW2H, FESW1L and FESW2L combined with the hardware control pin FESWON. This allows to program a changed state to the control register and activate it later on by changing the logic state at the control pin.

The switch status depends on the control bits FESWxx according to the table below.

FESWxH BIT STATUS	FESWxL BIT STATUS	FESWON PIN STATUS	STATUS AT FESWx PIN
X	0	0	tri-state
X	1	0	source current supplied
0	X	1	tri-state
1	X	1	source current supplied

RX gain adjust +2dB status control

The RX gain can be adjusted by +2dB by means of the bit GADJPLUS.

The RX gain adjust +2dB status depends on the control bit GADJPLUS acc. the table below.

GADJPLUS BIT STATUS	MODE OF OPERATION
0	RX gain unchanged
1	RX gain increased by 2dB

RX gain adjust -1dB status control

The RX gain can be adjusted by -1dB by means of the bit GADJMIN.

The RX gain adjust -1dB status depends on the control bit GADJMIN acc. the table below.

GADJMIN BIT STATUS	MODE OF OPERATION
0	RX gain unchanged
1	RX gain decreased by 1dB

LNA gain control

The LNAs have a gain control to switch between a nominal and a low gain state. The low gain state can be used especially to ensure linear operation in case of high input levels with EDGE modulation.

The LNA gain status depends on the control bit HGLG according to the table below.

HGLG BIT STATUS	MODE OF OPERATION
0	low gain
1	high gain

Receiver power status control

When the receiver is on, it is possible to switch off the low noise amplifier separately. Separate control of the low noise amplifier is accomplished by mean of the bit LNA.

The LNA status depends on the control bit LNA according to the table below.

LNA BIT STATUS	POWER STATUS OF LNA
0	off
1	on

Sideband select status control

The receiver includes an image rejection front end which allows the use of a RF LO 100 kHz below the RF input frequency (Infradyne) or 100 kHz above the RF input frequency (supradyne), between these two states the proper image should be selected for rejection. The selection of these two modes is accomplished by mean of the bit SBD.

The sideband status depends on the control bit SBD according to the table below.

SBD BIT STATUS	MODE OF OPERATION
0	supradyne
1	infradyne

RXIF filter bandwidth control

The bandwidth of the RXIF bandpass filter can be switched between 240 and 300kHz. The larger bandwidth can especially be useful for cochannel performance under EDGE modulation. As for higher bandwidth (EDGE operation) the gain of the receive path is 2dB lower compensation can be done with GADJPLUS control.

The RXIF filter bandpass filter bandwidth depends on the control bit RXBW according to the table below.

RXBW BIT STATUS	MODE OF OPERATION
0	240kHz bandwidth
1	300kHz bandwidth

Fast settling mode

The RXIF part contains an active dc compensation (dc notch) that needs significant settling time. To speed it up a fast settling mode is implemented with a higher bandwidth of the notch. In this mode dc settling of the receiver is achieved after max. 50μs. Afterwards it has to be set back again to normal settling to allow proper reception. The mode is controlled by the bit FASTSETL.

The fast settling mode is defined according to the table below.

FASTSETL BIT STATUS	MODE OF OPERATION	BW OF DC NOTCH
0	normal settling	6kHz
1	fast settling	24kHz

Stop settling mode

The active dc compensation (dc notch) of the RXIF part can be switched to static dc compensation. After switching to stop settling the achieved differential offsets at the I/Q output pins are kept and can have little drift through internal leakage. It is controlled by the bit STOPSETL.

The stop settling mode is defined according to the table below.

STOPSETL BIT STATUS	MODE OF OPERATION
0	dc compensation dynamic
1	dc compensation static

Notch remove mode

The active dc compensation (notch) of the RXIF part can be disconnected for test purpose. It is controlled by the bit NTCHREM.

This notch remove mode is defined according the table below.

NTCHREM BIT STATUS	MODE OF OPERATION
0	notch connected
1	notch disconnected

Smart settling mode

The settling of the RXIF part can be switched to internal timing control. The available timing modes can be seen under timing specifications in the IC specification. Internal timing is controlled by the bit SMARTSETL.

The internal timing control can be selected acc. the table below.

SMARTSETL BIT STATUS	MODE OF OPERATION
0	internal timing not activated
1	internal timing activated

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Band status control

The receiver includes three RF front ends and their RF LO sections. For GSM the RF LO signal is divided by two. The selection of the different bands is accomplished by means of the bits BND1/BND2.

The band status depends on the control bits BND1/BND2 according to the table below.

BND1 BIT STATUS	BND2 BIT STATUS	MODE OF OPERATION
1	0	GSM
0	1	DCS
1	1	PCS

Coarse AFC control

The coarse AFC capacitors of the reference oscillator are controlled via the binary weighted bits CAFC0/1/2/3/4/5/6/7.

Their weight is defined according to the table below.

NAME OF THE BIT	VALUE OF THE BIT
CAFC0	LSB
CAFC7	MSB

RF VCO varactor supply control

For normal operation the cathodes of the switched varactors are connected to GND or a dynamically generated internal supply voltage. For test purpose this internal supply voltage can be switched to $V_{CC(RFCP)}$. This selection is accomplished by means of the bit VARCPVCC.

The varactor supply control status depends on the control bit VARCPVCC according to the table below.

VARCPVCC BIT STATUS	MODE OF OPERATION
0	dynamic varactor supply
1	static varactor supply

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PROGRAMMING

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and EN (enable). The data sent to the device is loaded in bursts framed by EN. Programming clock edges are ignored until EN goes active LOW. The programmed information is loaded into the addressed latch when EN returns inactive HIGH. This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of the synthesizer.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of EN. This produces an internal load pulse to store the data in the addressed latch. To ensure that data is correctly loaded on first power-up, EN should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum EN pulse width after data transfer.

Register bit allocation

FIRST							REGISTER ALLOCATION										LAST
BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
X	VAR CP VCC (0)	0 (Vtune meas)	0 (CHG cal1)	0 (CHG cal2)	0 (RFCPI temp LOW)	CAFC 7	CAFC 6	CAFC 5	CAFC 4	CAFC 3	CAFC 2	CAFC 1	CAFC 0	X	X	X	0101
RFK20	RFK19	RFK18	RFK17	RFK16	RFK15	RFK14	RFK13	RFK12	RFK11	RFK10	RFK9	RFK8	RFK7	0 (RFCP I2)	0 (RFCP I1)	0 (RFCP Itest)	0100
RFK6	RFK5	RFK4	RFK3	RFK2	RFK1	RFK0	1 (RFK-1)	RFN5	RFN4	RFN3	RFN2	RFN1	RFN0	BND2	BND1	SYN ON	0011
SMAR TSETL	NTCH REM	STOP SETL	FAST SETL	RXBW	SBD	LNA	HGLG	G 5	G 4	G 3	G 2	G 1	G 0	1 (RXIF ON)	1 (RXRF ON)	RXON	0010
GADJ MIN	GADJ PLUS	X	X	FE SW2H	FE SW1H	X	FE SW2L	FE SW1L	X	X	IQPOL	IF DIV	FILT	TXI2	TXI1	TXON	0001
for test purpose only; all bits must be set to zeros for normal operation; this is forbidden adress																	0000
for test purpose only; all bits must be set to zeros for normal operation; this is forbidden adress																	0110

The fractional-N RF synthesiser is programmed through the integer bits RFN0 ... RFN5 and the fractional bits RFK0 ... RFK20 (see formula on page 15).

X = don't care.

AGC gain lookup table (HGLG fixed to 1); note 1

HGLG[4]	G5[3]	G4[3]	G3	G2	G1	G0	ATTENUATION FROM MAX GAIN (DB)[2]
1	1	1	1	1	1	1	0
1	1	1	1	1	1	0	4
1	1	1	1	1	0	1	8
1	1	1	1	1	0	0	12
1	1	0	1	1	0	1	16
1	1	0	1	1	0	0	20
1	0	1	1	1	0	1	24
1	0	1	1	1	0	0	28
1	0	1	0	1	1	1	32
1	0	1	0	1	1	0	36
1	0	0	0	1	1	1	40
1	0	0	0	1	1	0	44
1	0	0	1	0	0	1	48
1	0	0	1	0	0	0	52
1	0	0	0	0	1	1	56
1	0	0	0	0	1	0	60
1	0	0	0	0	0	1	64
1	0	0	0	0	0	0	68

AGC gain lookup table; note 1

HGLG[4]	G5[3]	G4[3]	G3	G2	G1	G0	ATTENUATION FROM MAX GAIN (DB)[2]
1	1	1	1	1	1	1	0
1	1	1	1	1	1	0	4
1	1	1	1	1	0	1	8
1	1	1	1	1	0	0	12
1	1	1	0	1	1	1	16
1	1	0	1	1	0	0	20
1	1	0	0	1	1	1	24
1	1	0	0	1	1	0	28
1	1	0	0	1	0	1	32
1	1	0	0	1	0	0	36
1	0	1	0	1	0	1	40
1	0	1	0	1	0	0	44
1	0	0	0	1	0	1	48
0	1	0	0	1	0	1	52
0	1	0	0	1	0	0	56
0	0	1	0	1	0	1	60

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HGLG[4]	G5[3]	G4[3]	G3	G2	G1	G0	ATTENUATION FROM MAX GAIN (DB)[2]
0	0	1	0	1	0	0	64
0	0	0	0	1	0	1	68
0	0	0	0	1	0	0	72
0	0	0	0	0	1	1	76
0	0	0	0	0	1	0	80
0	0	0	0	0	0	1	84
0	0	0	0	0	0	0	88

Notes

1. All codes not included in table are forbidden.

2. This is voltage gain attenuation for complete receiver.

3. Steps in front of the bandpass filter.

4. Step in the LNA

Register preset conditions

The UAA3536 programming registers have a preset state. The preset values can be found in the following table. Conditions for guaranteed preset values at power on is as follow:

DATA, CLOCK, EN and RXON, TXON, SYNON, FESWON must be at logic low level.

Preset value is guaranteed 288ms after $SYNV_{CC}$ rising to 90% of 2.6 V.

Frequency is preset for GSM receive, channel 62 (947.4MHz)

AGC is set to maximum gain.

Preset values

FIRST							REGISTER ALLOCATION											LAST
BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
0	0	0	0	0	0	sv	sv	sv	sv	sv	sv	sv	sv	0	0	0	0101
0	1	1	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0100
1	0	0	0	1	0	0	1	0	1	0	0	0	1	0	1	0	0011
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0010
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0001
for test purpose only; all bits are set to zero; this is forbidden address																	0000
for test purpose only; all bits are set to zero; this is forbidden address																	0110

Notes

1. sv means stored values. All control bits that are used for coarse AFC are stored in a memory during the sleep period of the phone and are recalled at turn on of $V_{CC(SYN)}$ so that the reference oscillator restarts with the latest setting. The available storage time depends on the value of the external capacitor at pin CAFCSUP.

SERIAL BUS TIMING CHARACTERISTICS

V_{CC} = 2.6 - 3.3V; T_{amb} = -30 to +70 $^{\circ}$C ; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; pin CLK					
t_r, t_f	input rise and fall times	-	-	20	ns
t_{cy}	clock period	67	-	-	ns
$t_{pu,hi}$	clock pulse width high	30	-	-	ns
$t_{pu,lo}$	clock pulse width low	30	-	-	ns
Enable programming; pin EN					
t_{START}	delay to rising clock edge	200	-	-	ns
t_{END}	delay from last falling clock edge	100	-	-	ns
t_W	minimum inactive pulse width	400	-	-	ns
$t_{SU;EN}$	enable set-up time to next clock edge	200	-	-	ns
Register serial input data; pin DATA					
$t_{SU;DATA}$	input data to clock set-up time	25	-	-	ns
$t_{HD;DATA}$	input data to clock hold time	25	-	-	ns
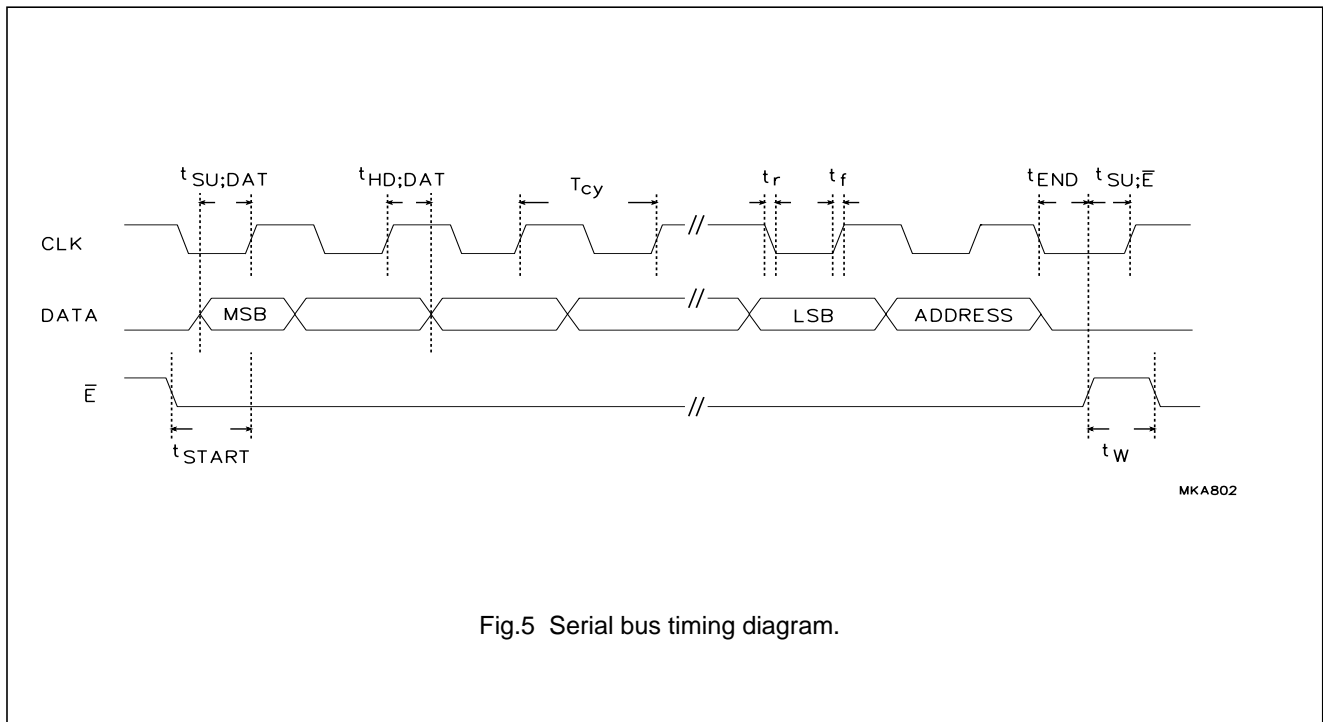
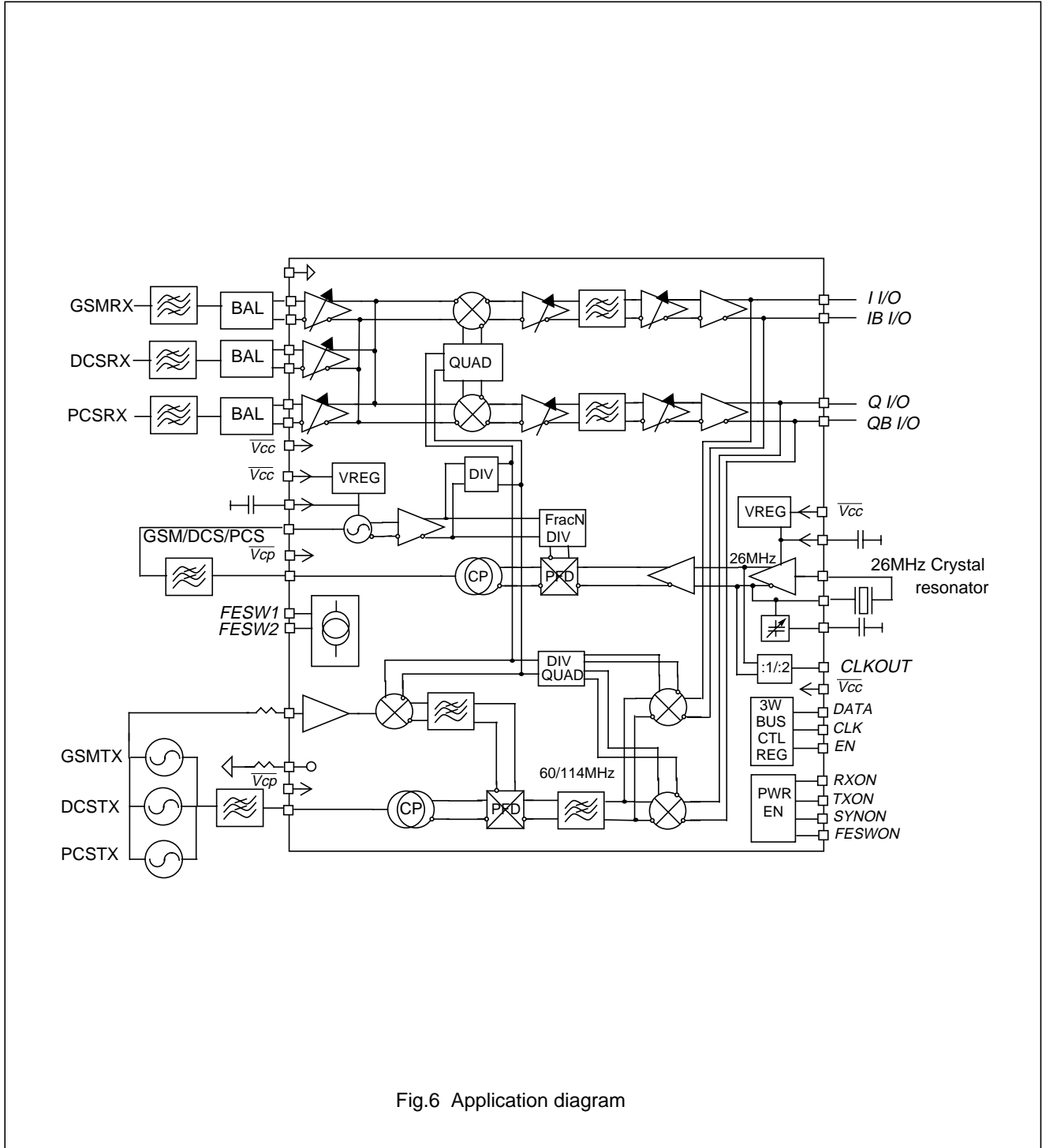Fig.5 Serial bus timing diagram.

APPLICATION INFORMATION
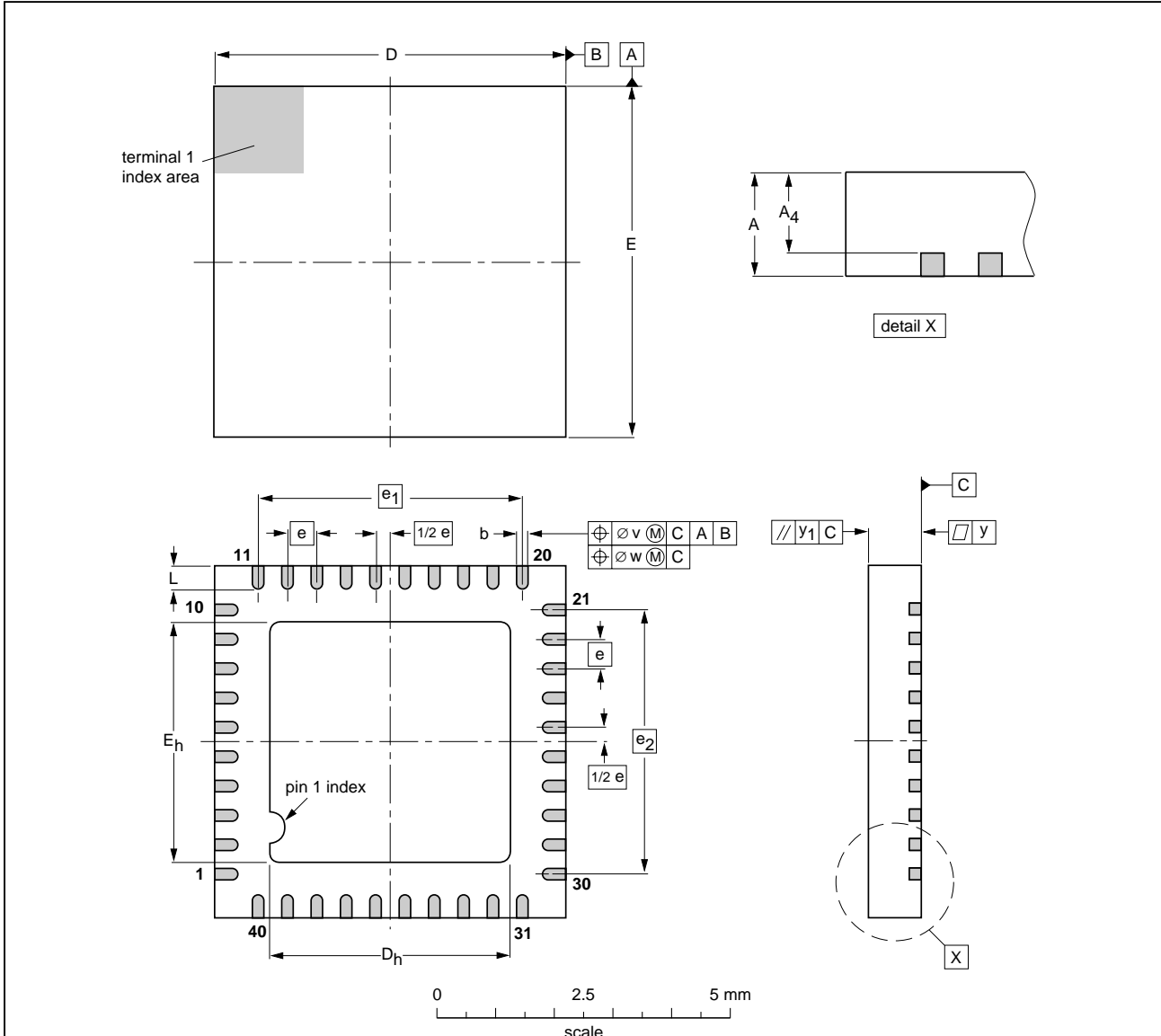

Fig.6 Application diagram

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PACKAGE OUTLINE

HVQFN40: plastic, heatsink very thin quad flat package; no leads;
40 terminals; body 6 x 6 x 0.85 mm

SOT618-1

0   2.5   5 mm

scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₄ max.	b	D$^{(1)}$	D$_h$	E$^{(1)}$	E$_h$	e	e₁	e₂	L	v	w	y	y₁
mm	1.00	0.80	0.35 0.18	6.05 5.95	4.25 3.95	6.05 5.95	4.25 3.95	0.5	4.5	4.5	0.50 0.30	0.2	0.1	0.05	0.1

Note

1. Plastic or metal protrusions of 0.076 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT618-1		MO-220				~~01-06-07~~ 01-08-08

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all HVQFN packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 C.

Wave soldering

Wave soldering is **not** recommended for HVQFN packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45 to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 C within 6seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.