Features

Overall
- IBM Set-Top Box technology
- Four major subsystems integrated with IBM on-chip CoreConnect™ structure.
- Maximum MIPS for OS and application tasks
- Simplified driver and software development
- Scalable, flexible, and extendible
- 54 MHz/57 MIPS
- 3.3 V and 2.5 V power supplies
- IBM CMOS SA-12E process(0.25 µm)
- 352-pin PBGA package

MPEG-2 Digital Audio/Video Subsystem
- MPEG-2 Video Decoder
- MPEG-2 Audio Decoder
- MPEG-2 Transport/DVB Descrambler
- Macrovision Copy Protection on selected parts
- Display Controller
- Digital Encoder (DENC) with six outputs
- Anti-Flicker Filter

PowerPC 401™ Host Processor: PPC401B3 CPU
- 16KB Instruction, 8KB Data caches
- Universal Interrupt Controller

Memory Subsystem
- DMA Controller
- Cross-Bar Switch
- External Bus Interface Unit (EBIU)
- IDE Interface
- One SDRAM Controller

Peripheral Subsystem
- General Purpose Timers (GPTs)
- Pulse Width Modulators
- Smart Card controller
- I^2C Interface
- 16550 Serial Communications Port
- Infrared Serial Communications Port
- General Purpose Inputs/Outputs
- Serial Controller Port
- Modem Serial Interface/Digital Audio Input

Description

IBM STB0210x Digital Set-Top Box Integrated Controller family are highly integrated silicon devices specifically developed for digital set-top box (STB) applications using industry-leading IBM CMOS SA-12E (0.25 µm) process technology.

The STB0210x is part of the second generation of IBM products for digital STB applications. PowerPC processing and peripheral I/O architecture provide a high level of performance and functionality when used in audio and video subsystems. The resulting STB technology is full-functioned and easy to use.

The STB0210x minimizes host processor intervention to maximize MIPS for operating system and application tasks. Most of the features required in the back end of typical midrange and high-end STBs are integrated. Driver and software development is facilitated while preserving scaleability, flexibility, and extendibility.

Architecturally, the devices consist of four subsystems interconnected and tuned using CoreConnect, the IBM multiple-bus, on-chip interconnect structure:
1. PowerPC host processor
2. Digital audio/video
3. Memory interface
4. Peripheral

These high performance subsystems are suited for interactive STBs with demanding software requirements.

Ordering Information

Part Number	Performance (est.)	Clock Speed	Audio	Copy Protection
IBM39STB02100PBA22C	57 MIPS	54 MHz	MPEG	None
IBM39STB02101PBA22C[1]				Macrovision

1. These parts support Macrovision Copy Protection and require that a license be in effect between the purchaser and Macrovision Corporation. Please see “Macrovision Licensing” on page 3.

Conventions and Notation

Throughout this document, standard IBM notation is used, meaning that bits and bytes are numbered in ascending order from left to right. Thus, for a 4-byte word, bit 0 is the most significant bit and bit 31 is the least significant bit.

Overbars, e.g. $\overline{\text{TxEnb}}$, designate signals that are active low.

Numeric notation is as follows:

Hexadecimal values are in single quotes and preceded by "x" or "X." For example: x’0B00’.

Binary values are spelled out (zero and one) or appear in single quotes and preceded by a "b."
For example: b‘10101’.

Settings of a bit or field are binary numbers but are often displayed in tabular form without quotes or the preceding "b."
For example:

00 : 30 frames per second
01 : 15 frames per second
11 : 10 frames per second

Licensing Requirements

Macrovision Licensing

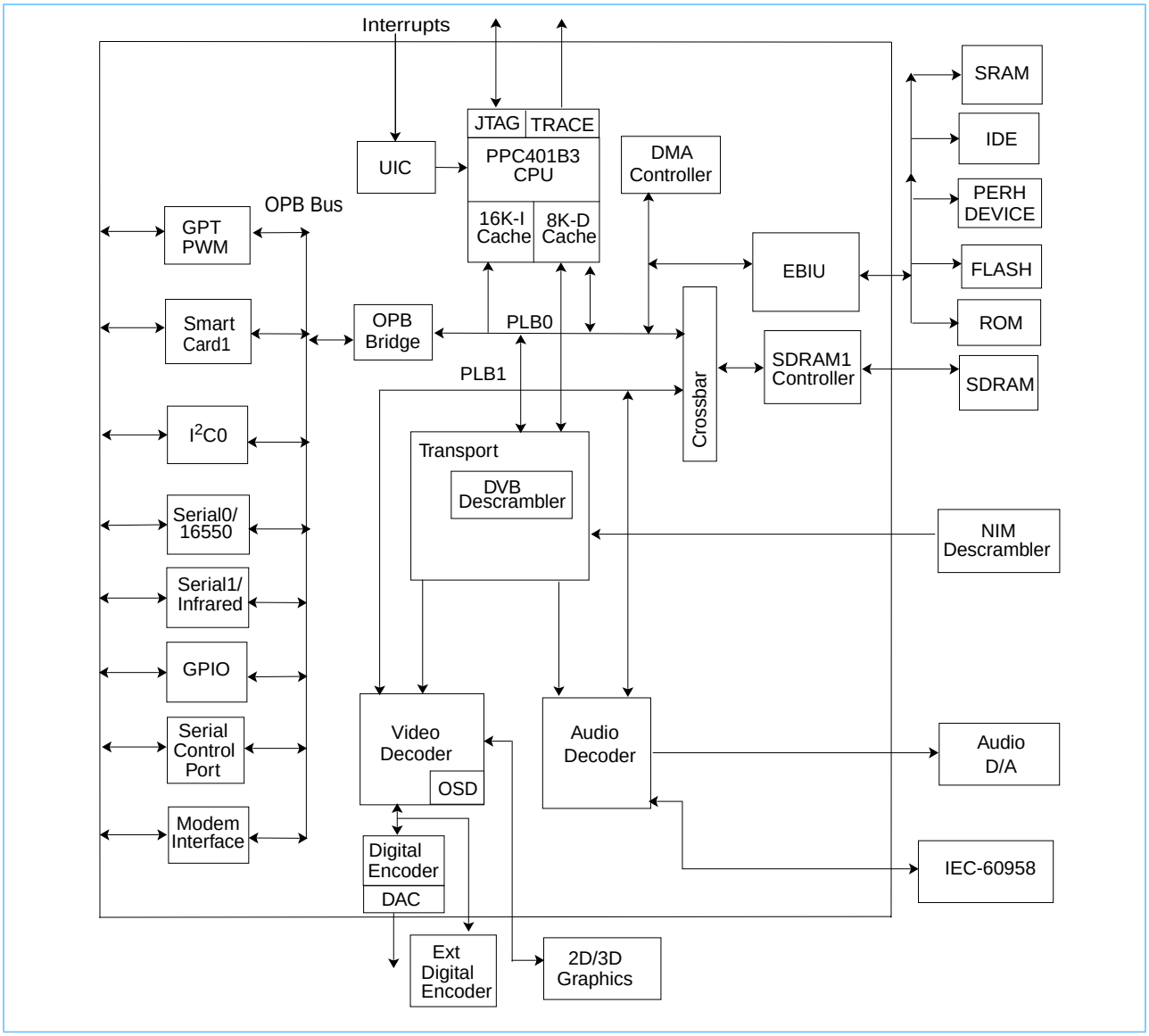
Macrovision Copy Protection is supported in the IBM39STB02101 product. These devices are protected by U.S. patent numbers 4,631,603, 4,577,216, and 4,819,098 and other intellectual property rights. The use of Macrovision's Copy Protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision.

Reverse engineering or disassembly is prohibited. A valid Macrovision license must be in effect between the STB02101 purchaser and Macrovision Corporation. Additional per-chip royalties may be required and are to be paid by the purchaser to Macrovision Corporation.

Macrovision Corporation
1341 Orleans Avenue
Sunnyvale, CA 94089

Architecture and Subsystem Information

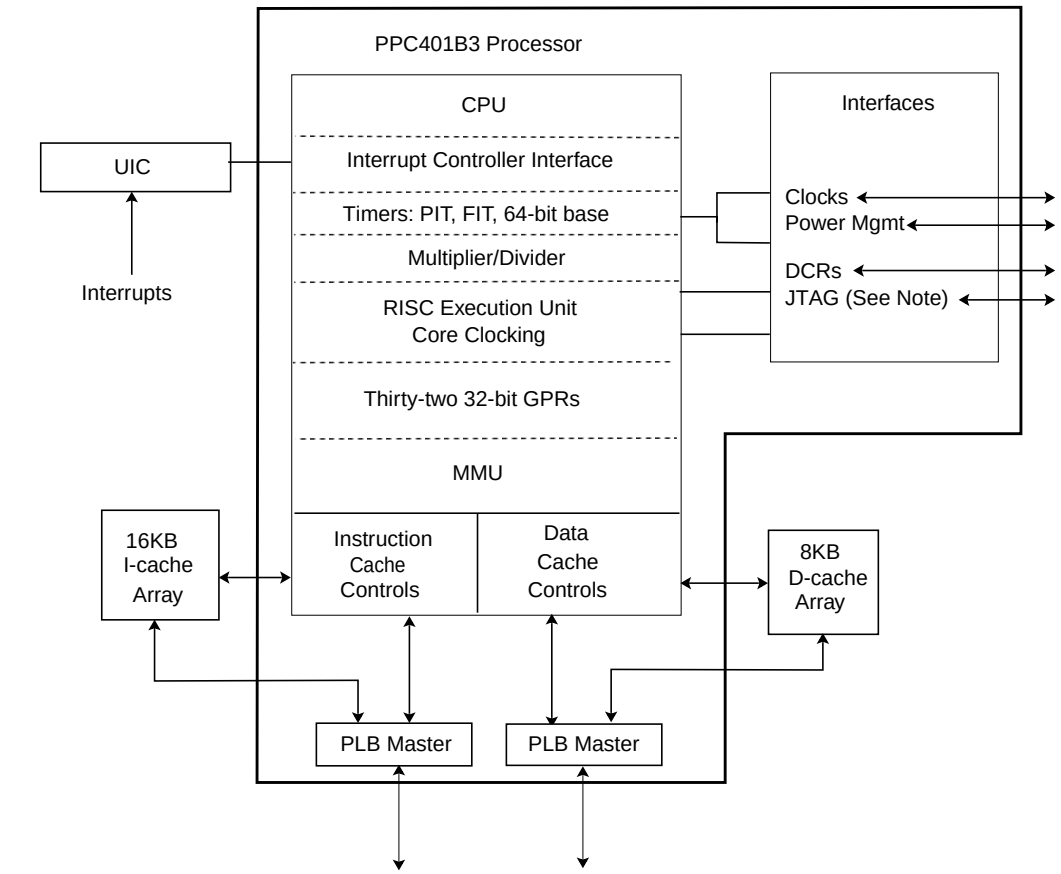
Block Diagram



PowerPC 401B3 Host Processor Subsystem

The PowerPC 401B3 (PPC401B3) subsystem handles all system initialization and control and also provides power and flexibility for product differentiation.

PPC401B3 Subsystem



Note: The JTAG interface is used for development.

PowerPC 401B3 CPU

The PPC401B3 provides high performance and low power consumption. The CPU executes at sustained speeds of greater than one cycle per instruction at 54 MHz. Interrupt latency is three cycles, the best time for critical interrupts.

On-chip instruction is compatible with PowerPC User Instruction Set Architecture. There are 32 x 32 bit general purpose registers. Instruction and data cache arrays improve system throughput. The CPU has a separate two-way set-associative 16KB instruction cache and an 8KB write-back/write-through data cache. Multiply and divide instructions are performed in hardware and are not emulated in software.

Universal Interrupt Controller

The Universal Interrupt Controller (UIC) provides all necessary control, status, and communication functions between all sources of interrupts and the PPC401B3. The UIC combines STB0210x interrupts and presents them to the PPC401B3's critical or non-critical inputs. All interrupts can be programmed to generate either critical or non-critical output. Interrupts can be level- or edge-sensitive and interrupt polarity is programmable.

An optional read-only vector is used to reduce critical interrupt servicing latency. This vector is generated by combining an offset (based on the bit position of the highest priority, enabled, and active critical interrupt) and a vector base address register. A configurable priority control bit determines whether the least significant or most significant bit in the status register has the highest priority.

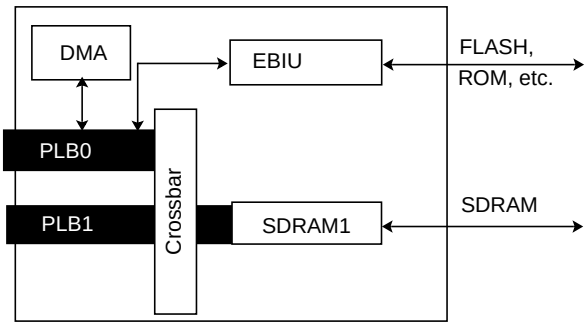
Clock and Power Management

For power-saving purposes, a Clock and Power Management (CPM) input is used to shut down clocks and device functions. A reset is required to activate a unit.

Memory Interface Subsystem

The memory interface subsystem provides the system memory controller interface for SRAM, FLASH Memory, ROM, and SDRAM. It also provides the Direct Memory Access (DMA) interfaces for these memories.

Memory Subsystem



Direct Memory Access Controller

The four-channel DMA controller is a processor local bus master that allows faster data transfer between memory and peripherals than with program control. The controller supports memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. The DMA controller allows the PPC401B3 processor to execute instructions with no bus contention when the PPC401B3 is executing from cache. DMA is useful when the overhead associated with the controller setup is minimal compared to the time it would take to move data using program control load and store instructions.

Each DMA channel has an independent set of registers for data transfer. The registers store data for control, source address, destination address, and transfer count. Each channel also supports chained DMA operations, therefore every channel also includes a chained count register in which case source address registers function as chained address registers. All DMA channels report their status to the DMA execution unit.

The DMA controller also supports:

- Internal DMA channels for smart card interface, 16550 serial communications controller, infrared communications controller, etc.
- 16- and 32-bit peripherals (on-chip peripheral bus and external)
- 32-bit addressing
- Address increment or decrement
- Internal data buffering capability
- Memory-mapped peripherals

Processor Local Bus

The Processor Local Bus (PLB) interfaces directly with the PPC401B3 and the other major subsystems (see “Block Diagram,” on page 4). The STB0210x uses two PLBs to provide high bandwidth between the function masters and the external memory interfaces for ROM, Flash, and SDRAM, etc. The STB0210x PLB architecture includes a crossbar switch to present both memory interfaces as flat, shared memory spaces.

External Bus Interface Unit

The External Bus Interface Unit (EBIU) expands the local bus to transfer data between the PLB and a wide range of memory and peripheral devices attached to the external bus (see the following list). The EBIU can control up to eight devices or banks or regions of FLASH memory (128 MB), and a low latency maximizes system performance.

The EBIU supports:

- A direct connect SRAM/ROM/PIA interface for
  - up to eight SRAM/ROM/PIA banks with programmable address select
  - programmable or device-paced wait states
  - burst mode (BME) and single-cycle transfers
- 16- and 32-bit byte addressable bus width
- Programmable target word first or sequential cache line fills
- DVB Common Interface Support
- IDE interface supports:
  - ATA-3 mode 4, register, and PIO
  - Mode 2 Multiword DMA transfers (see ANSI X3.298-1997, AT Attachment-3 Interface (ATA-3))
  - Multi-word DMA (15.5 MB/s maximum transfer rate)
- External bus master with support for device master and master/slave
- Common bank-specific programmability
- Device-paced ready input

SDRAM Controller

The SDRAM Controller transfers data between the PLB and up to two SDRAM memory banks attached to the external bus. The Controller implements address and data pipelining and supports 16Mb and 64Mb SDRAMS concurrently. It also provides the following:

- Direct-connect SDRAM interface

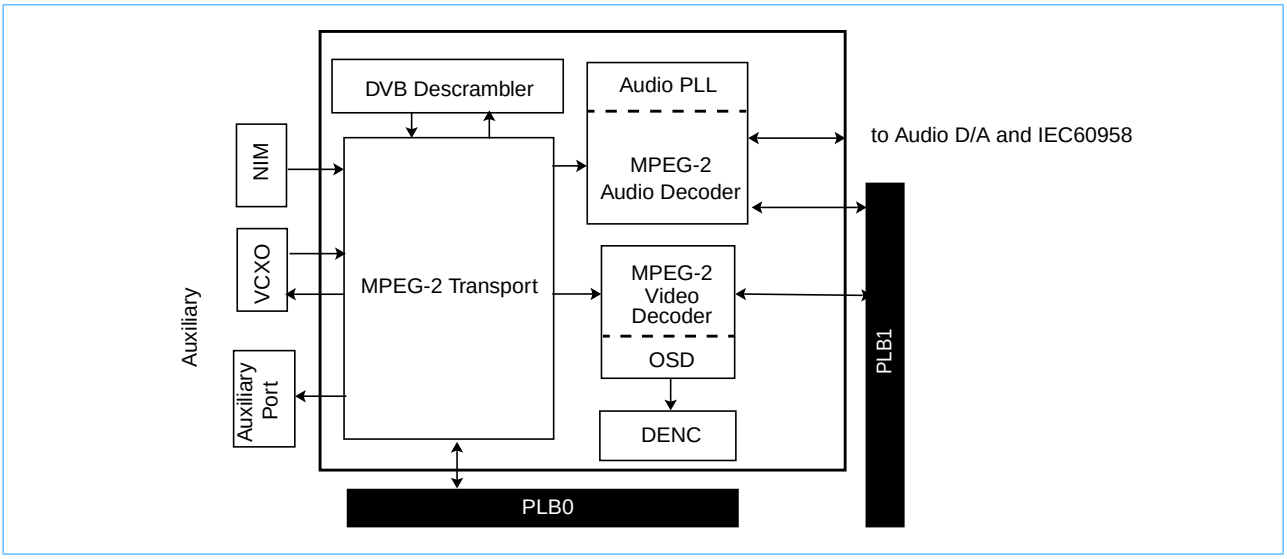
- High bandwidth with a narrow 16-bit interface
- Page interleaving
- Programmable address select
- Programmable rates for automatic SDRAM refresh
- Software-initiated and self refresh modes for power savings

Crossbar Switch

The PLB Crossbar Switch (CBS) creates a flat memory model and implements Unified Memory Architecture (UMA), which connects multiple PLB master buses to the PLB slave buses, thus allowing two sets of PLB buses to intercommunicate. Processor, transport, and the audio and video decoders can access memory through the memory controller.

Digital Audio/Video Subsystem

The MPEG-2 Digital Audio/Video subsystem provides fully-synchronized playback of digital video and audio programs, with a minimum of interaction from the PPC401B3 processor.



MPEG-2 Video Decoder with OSD

The MPEG-2 video decoder provides decompression, decoding, and synchronized playback of digital video streams with a minimum of host support. It produces interlaced video output and can support MPEG-2 compressed data streams up to an average rate of 15 Mbps. The video decoder is also backward compatible to support the ISO/IEC International Standard 11172-2 (11/93) (also called “MPEG-1 Standard”). It supports the ISO/IEC 13818-2 Main Profile at Main Level.

The decoder also supports MPEG-2 MP@ML compliance with 2MB memory. Only 2MB of memory are needed to decode full CCIR601 resolution NTSC and PAL encoded MPEG-2 bitstreams. It performs real-time decoding of all resolutions in 16-pixel multiples, up to and including 720x480x30 or 720x576x25. Horizontal and vertical filters deliver high-quality video. Chrominance filtering and up-sampling to provide CCIR601 4:2:2 video output. Pan and scan are supported in 1/16 pel accuracy for 16:9 source material. Video rates range from 1.5 Mbps to 15 Mbps (higher in bursts).

The MPEG-2 video decoder supports the European DVB standard and accepts Packetized Elementary or Elementary MPEG-2 streams. It uses Packetized Elementary Stream (PES) video decoding to extract the Presentation Time Stamp (PTS), and handles user data and other PES layer bit fields through memory access from the PPC401B3. Input can be from transport or directly from system memory. Outputs are provided for video-only and for video-with-OSD.

The decoder can insert data in the vertical blanking interval (VBI) with VBI Output Support. It supports decoding of still or fixed images and display of scaled video images. It also features:

- Letterbox format display
- Selectable anti-flicker filtering
- Output interface flexibility (programmable controls)
- Composite blanking and Field ID signals
- V-sync and H-sync signals
- CCIR656 master and slave modes
- Programmable signal polarity
- Sophisticated error concealment
- 3:2 pull-down support.
- Closed caption, teletext, or mixed (VPS)
- (1/4x, 1/2x, 2x) and three graphic planes
- Automated video channel change and time-base change features
- Blending of external graphics.

A multi-plane on-screen display (OSD) uses bitmap data in memory to be merged with or displayed in place of the motion video data. Three OSD planes (the cursor, graphics and image planes) are provided for increased display flexibility. The OSD includes:

- Programmable background color
- Multi-region link list graphic and image plane OSD with a color table for each region
- Programmable bitmap resolution on a region-by-region basis
- 64 x 64 pixel, 16-color cursor plane with blending controls
- Overlay and video blending of graphic plane
- Enhanced color mode for 24-bit color (YUV) in Direct Color and CLUT modes with 8-bit alpha blending
- Video shading in graphic plane OSD area
- OSD control output for external multiplexer (picture-in-picture support)
- Tiling capability in image and graphic planes
- Scrolling of image and graphic planes
- Horizontal scaling of image plane bitmaps
- Animation support
- 16 MB OSD addressing range to support more and larger bitmaps.

MPEG-2 Transport and DVB Descrambler

The MPEG-2 transport demultiplexer provides ISO / IEC 13818-1 MPEG-2 transport system layer demultiplexing. Its integrated digital video broadcasting (DVB) descrambler complies with DVB system layer requirements and may be turned off for non-DVB applications. Peak input rates are 100-Mbps (parallel) or 60-Mbps (serial), or 88-Mbps (parallel) or 60-Mbps (serial) with the optional descrambler. Packet Identifier (PID) filtering is based on 32 programmable entries with detection and notification of errors and lost packets. Hardware-based clock recovery on program clock references (PCRs) reduces processor load by:

- Calculating clock difference between PCR and System Time Clock (STC)
- Modulating output to drive an external VCXO
- Using an optional internal clock-recovery algorithm based on clock difference

Transport and descrambler features include:

- Internal DVB (1.0 or 1.1) descrambler, including filtering and storage of eight control word pairs
- Auxiliary output port for real-time data transfers:
  - 8-bit mode at 1X, 1/2X, 1/3X, 1/4X and 1/8X of the system clock speed
- Table section filtering:
  - 64 separate 4-byte filter blocks with bit-level masking with full match/not match capability
  - Multiple filters can be linked to extend filtering depth in 4-byte increments
  - Multiple filters per PID
  - Filters program-specific information (PSI), service information (SI), private tables
  - Handles multiple sections per packet and sections that span packets
  - Optional CRC checking of section data
- Selective routing of some or all packet data to system memory:
  - Based on 32 separate queues (one per PID)
  - Routing entire packets, payloads, adaptation fields, table sections (after filtering) and private data
- Direct transfer of audio / video (PES) data to decoders
- Simplified channel changes, time-base changes and error flagging / concealment through direct communication with decoders

MPEG-2 Audio Decoder

The Audio Decoder receives and decodes either ES (Elementary Stream) or PES (Packetized Elementary Stream) audio data. The audio compute engine is a generic DSP processor that decodes MPEG, or 16-, 18- or 20-bit unformatted Pulse Code Modulation (PCM) audio data via individual software programs.

The host processor downloads each program load to the Audio Decoder following initialization. The Audio Decoder generates up to two channels of decoded PCM for MPEG and PCM audio playback output. It provides 2-channel MPEG audio to two channels output. Unpacketized PCM (UPCM) plays back at sampling frequencies of 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz, along with quantization sample width selections of 16-, 18-, or 20-bit input and 16 or 20-bit output.

The Audio Decoder:

- Decodes MPEG-1 and MPEG-2 audio, Layers I and II and 2-channel output, including single channel, stereo, joint stereo, and dual channel modes.
- Performs MPEG-1 and MPEG-2 PES audio parsing, and also accepts audio elementary streams. Parses and stores ancillary data into external memory for later use by the host processor.
- Supports 16-kHz, 22.05-kHz, 24-kHz, 32-kHz, 44.1-kHz, and 48-kHz audio sampling frequencies.
- Supports audio/video synchronization through PTS/STC comparison with each audio frame.
- Supports an encoded audio bit rate up to 640 Kbps. This bit rate only pertains to encoded bitstream data.
- Includes Audio Clip Mode for PES, ES, and PCM formats with byte address granularity and 2MB maximum per clip buffer.
- Supports expandable rate buffer size selectable from 4K to 64K (in 4K increments).
- Uses a re-locatable rate buffer region, with a programmable base register (128-byte location granularity).
- Has a re-locatable PTS Value and Ancillary data region, using a programmable base register with 128-byte location granularity.

- Uses a locatable Audio Temporary Data and Decoded Audio Data Bank region (programmable base register with 128-byte location granularity with additional offset register).
- Includes 256x and 512x DAC sampling clock frequency configurations.
- Has a programmable stream ID register with corresponding 8-bit enable field.
- Provides three PCM output formats in 16- or 20-bit precision:
  - I^2S
  - Left-justified
  - Right-justified
- Performs audio bitstream error concealment, either by frame repeats or muting, due to loss of synchronization or detection of CRC errors.
- Performs MPEG error checking using frame size calculation for each frame.
- Provides a programmable interface that supports the following:
  - Play, stop, and mute
  - Rate buffer purge to support channel and mode changes
  - Provides compressed buffer empty/full indicators
  - Synchronization enable/disable for PTS-STC comparison
  - Provides buffer fullness value
- Includes SPDIF meeting IEC61937 specs.
- Supports enhanced IEC61937 S/P DIF Channel Status bit by including 16 SPDIF Channel Status bits, with host control over most of the bits.
- Inserts host-controlled validity bit into SPDIF sub-frame via DCR register.
- Performs audio attenuation in 64 steps, with smooth transitions between steps.
- Provides tone generation with up to 128 generated tones at 31 different durations with seven levels of attenuation via processor command.
- Supports automated channel change.
- Supports automated time base change.

NTSC/PAL Digital Encoder Unit with Macrovision Copy Protection[1]

The multi-standard Digital Encoder converts digital audio/video data into analog National Television System Committee (NTSC) or Phase Alternate Line (PAL) data output formats (see Macrovision Licensing on page 3). It provides up to six concurrent analog video outputs, including S-Video, composite video, YPbPr, and RGB. The encoder is compatible with SCART connectors, with support for Macrovision Copy Protection Revision 7. Analog outputs are driven by 10-bit D/A converters, operating at 27 MHz. The outputs drive standard video levels into 75-Ω loads. It supports closed caption, teletext insertion, and Line 23 WSS (Wide-screen Signaling) per ITU-R BT.1119. There is a switchable pedestal with gain compensation. Playback of synchronized video data can be locked to the incoming composite video stream.

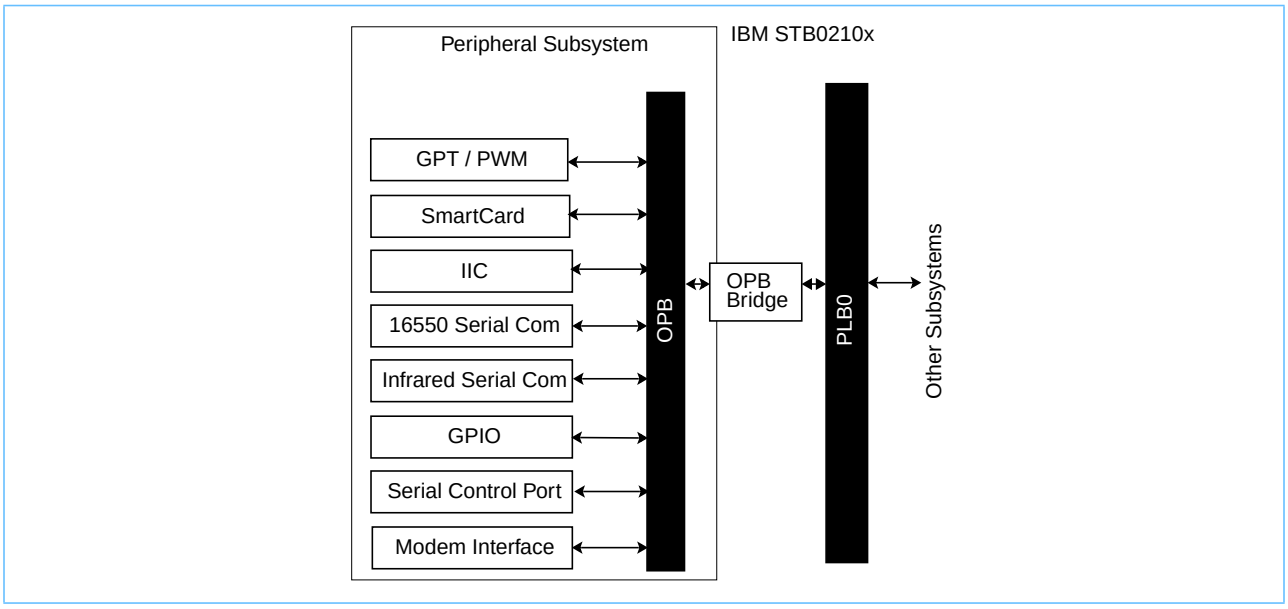
1. This feature is available only on STB02101, Macrovision license required.

Additional Interfaces

External Graphics and Video (EGV) Port

External Graphics and Video (EGV) ports provide flexibility for interfacing external graphics and video components. When the EGV is used as an output, its signals may be routed to an external graphics device or DENC. When used as an input, either the internal OSD graphics can be replaced with data from an external graphics device, or external digital video data (from an analog signal converted to digital via DSMD, for example) could replace the internally decoded MPEG video. In the latter case, the external digital video can be merged/blended with the internal OSD graphics.

Peripheral Subsystem



General Purpose Timer

The General Purpose Timer (GPT) is an on-chip peripheral bus (OPB) function that provides a separate time base counter and additional system timers beyond those defined in the PPC401B3.

Three Inter-Character (IC) time-out timers are also implemented in this functional unit in the GPT. These timers receive the count signal inputs from other units they are timing. Each timer is a 10-bit down counter loaded with a programmable value (TOUT) upon the active edge of the count signal input. Once loaded, the IC timer counts down TOUT number of TCLK cycles until it reaches zero (that is, when the IC timer has expired). When a timer expires, it sets its corresponding bit in the IC interrupt status register.

There is a separate time base inside the GPT, distinct from the time base within the PPC401B3. Two event timers capture unique input events and there are two compare timers with unique outputs. Separately configurable and programmable synchronization controls edge detection and output levels. There are two reset inputs, one for the entire GPT unit, and one for the time base.

Pulse Width Modulation

The pulse width modulation (PWM) function produces two square wave outputs with a variable duty cycle under program control. The duty cycle varies from 100 percent to zero percent in steps of 1/256. There is a control register with two bits for each PWM. This register controls the active status of the PWM, and determines what its inactive output level should be. When the PWM control register is set to disable a PWM, the 8-bit period counter will be inactive to minimize power.

The pulse width modulation portion of the GPT contains two identical blocks, each containing an 8-bit programmable and reloadable down counter and control logic. A time-base generator that is a free-running counter (TCLK based) generates the frequency of the pulse-width modulated output.

IInter-Integrated Circuit (IIC) Unit

The IIC unit is used to provide a simple to use, highly programmable interface between the OPB and the industry standard IIC serial bus. They provide full management of all IIC bus protocols, compliant with Phillips Semiconductors I^2C Specification, dated 1995, and support a fixed V_{DD} IIC interface. It can be programmed to operate as master, as slave, or as both master and slave on the IIC interface. In addition to sophisticated IIC bus protocol management, the IIC provide full data buffering between the OPB and the IIC bus.

The IIC unit offers 5 V tolerant I/O for both 100- and 400-kHz operation with 8-bit data transfers and 7-bit and 10-bit address decode/generation. There is one programmable interrupt request signal, two independent 4 x 1-byte data buffers, and 12 memory-mapped, fully programmable configuration registers.

Smart Card Interface Unit

The Smart Card Interface Unit handles communications between an Integrated Circuit Card and the host CPU. These 5 V tolerant I/O devices have a software-based control structure and are designed for use with asynchronous transmissions. It features hardware activation/deactivation and reset with software overrides and byte-wide FIFO support. It is compatible with ISO/IEC 7816-3 and support T0 and T1 protocols. The Interface Unit support 2-channel DMA with 8-bit memory-mapped registers and hardware error checking. An Inter-Character Time-out Facility provides timing support from the GPT/PWM.

16550 Serial Communication Controller

The 16550 Serial Communication Controller is a universal asynchronous receiver/transmitter (UART) with FIFOs, and is compatible with the 16550 part numbers manufactured by National Semiconductor (NS) Corporation. It is also compatible with National Semiconductor 16450 (non-FIFO version). Serial interface characteristics are fully programmable with complete modem control functions and status reporting capability. The controller supports:

- 5-, 6-, 7-, or 8-bit characters
- Even, odd, or no parity bit generation and detection
- 1-, 1.5-, or 2-stop-bit generation
- Variable baud rate and a programmable baud rate generator

There is also support for two DMA channels with a 16-byte FIFO for transmit/receive path. Internal loopback is provided for diagnostics and an Inter-Character Timeout Facility provides timing support from the GPT/PWM.

Infrared Serial Communications Controller

In addition to standard UART functions, the Serial/Infrared Communications Controller can use an alternate mode (IrDA mode) to transfer and receive infrared characters. IrDA transmissions are specified by the Infrared Data Association (IrDA) Specification 1.1. IrDA mode supports RS-232 and infrared communications up to 1.152 Mbps with automatic insertion/removal of standard ASYNC communication bits. The controller includes:

- A programmable baud rate generator
- Individual enable for receiver and transmitter interrupts
- Internal loopback and auto-echo modes
- Full-duplex operation
- Programmable serial interface
- Status reporting capability
- Individual receiver and transmitter DMA support
- Auto-handshaking mode for receiver and transmitter
- Transmitter pattern generation capability
- Serial clock frequency up to 1/2 system clock frequency
- Inter-Character Timeout Facility support from the GPT/PWM

Modem Interface

The Modem Interface provides a glueless communication from the device to and from many standard and economical telephony CODECs (Note: CODECs are the Audio ADC/DAC devices). The PPC401B3 CPU and applicable software can be used to implement an inexpensive interface for a modem. The external interface supports industry standard 4-wire parameters, consisting of transmit data, receive data, clock, and frame sync. Two channels of DMA allow off-loading data from the CPU. The Modem Interface supports digital audio MIC input, status reporting, and interrupt generation.

Serial Control Port

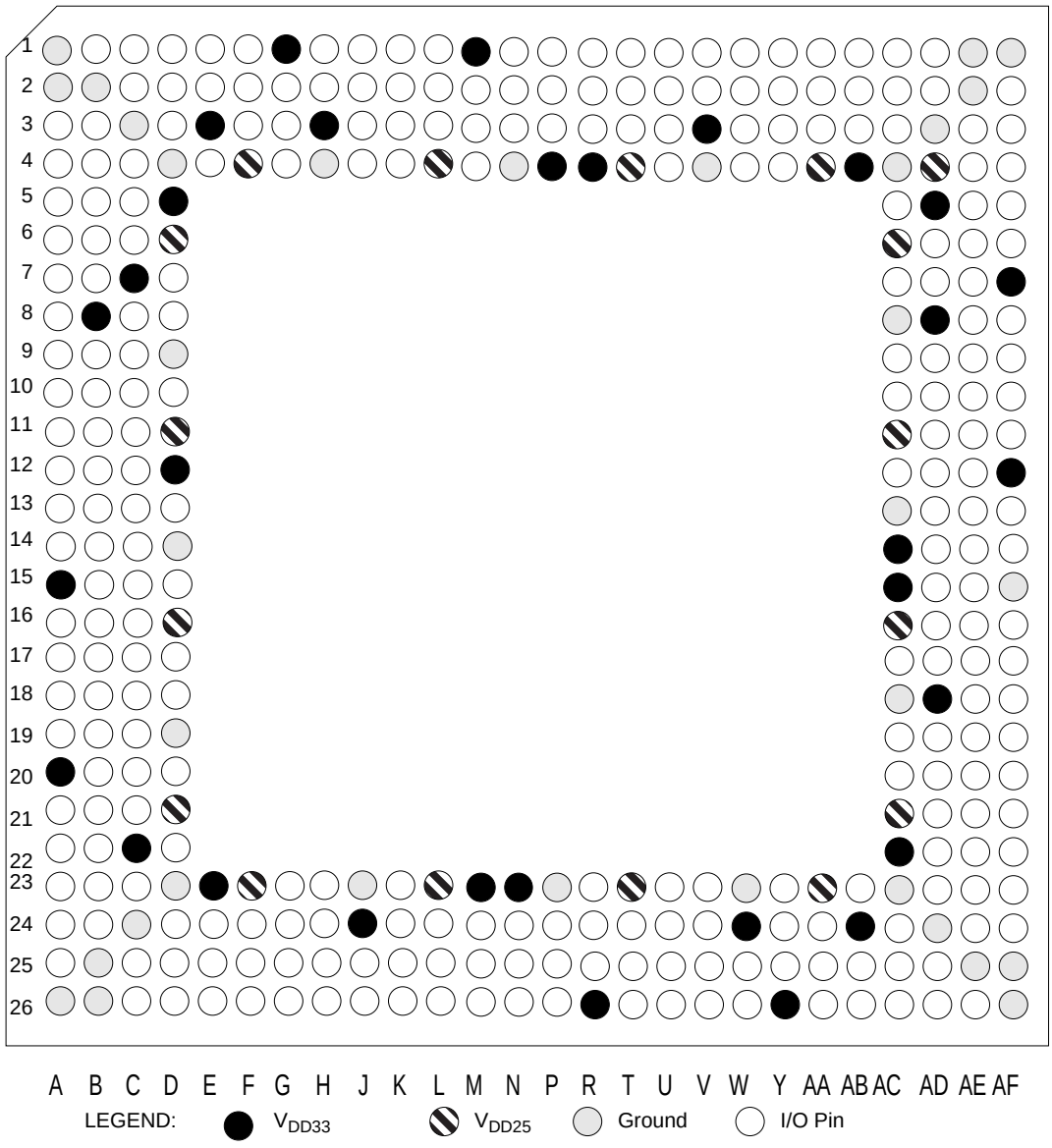
The Serial Control Port (SCP) is a full-duplex, synchronous, character-oriented (byte) port that allows the exchange of data with other SCP bus-compatible serial devices. The SCP is a slave device to the OPB bus, and supports a three-wire interface to the serial port (receive, transmit, and clock). It provides a glueless serial interface to many microcontrollers, with clock inversion and reverse data. The port includes a programmable clock rate divider (Sysclk/4 to Sysclk/1024), and bit rate is supported up to 1/4 the frequency of the system clock.

General Purpose I/O Controller

The General Purpose I/O (GPIO) controller enables the multiplexing of module I/Os, with functions that include programmable open-drain output conversion, registered input and output functions, and simplified GPIO definition.

Pin and I/O Information

Pinout Diagram



Signal Pins Sorted by Signal Name

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
AUD_VDDA0	AF15	PLL Analog PWR + GND	BI_DATA2	AD16	Bus Interface
AUD_VDDA1	AE12	PLL Analog PWR + GND	BI_DATA3	AD15	Bus Interface
BI_ADDRESS8 (MSB)	AF11	Bus Interface	BI_DATA4	AE15	Bus Interface
BI_ADDRESS9	AD10	Bus Interface	BI_DATA5	AE16	Bus Interface
BI_ADDRESS10	AE10	Bus Interface	BI_DATA6	AE17	Bus Interface
BI_ADDRESS11	AE9	Bus Interface	BI_DATA7	AF19	Bus Interface
BI_ADDRESS12	AC9	Bus Interface	BI_DATA8	AE18	Bus Interface
BI_ADDRESS13	AE11	Bus Interface	BI_DATA9	AC17	Bus Interface
BI_ADDRESS14	AD4	Bus Interface	BI_DATA10	AF16	Bus Interface
BI_ADDRESS15	AF4	Bus Interface	BI_DATA11	AD14	Bus Interface
BI_ADDRESS16	AE5	Bus Interface	BI_DATA12	AF14	Bus Interface
BI_ADDRESS17	AC5	Bus Interface	BI_DATA13	AD13	Bus Interface
BI_ADDRESS18	AC7	Bus Interface	BI_DATA14	AF18	Bus Interface
BI_ADDRESS19	AD6	Bus Interface	BI_DATA15	AE20	Bus Interface
BI_ADDRESS20	AD7	Bus Interface	BI_DATA16	AD25	Bus Interface
BI_ADDRESS21	AE8	Bus Interface	BI_DATA17	AD23	Bus Interface
BI_ADDRESS22	AD9	Bus Interface	BI_DATA18	AE23	Bus Interface
BI_ADDRESS23	AC10	Bus Interface	BI_DATA19	AE22	Bus Interface
BI_ADDRESS24	AF9	Bus Interface	BI_DATA20	AD19	Bus Interface
BI_ADDRESS25	AF8	Bus Interface	BI_DATA21	AF21	Bus Interface
BI_ADDRESS26	AE7	Bus Interface	BI_DATA22	AD21	Bus Interface
BI_ADDRESS27	AF6	Bus Interface	BI_DATA23	AE26	Bus Interface
BI_ADDRESS28	AF5	Bus Interface	BI_DATA24	AE24	Bus Interface
BI_ADDRESS29	AE3	Bus Interface	BI_DATA25	AD22	Bus Interface
BI_ADDRESS30	AF3	Bus Interface	BI_DATA26	AF22	Bus Interface
BI_ADDRESS31 (LSB)/BI_WBE1	AF2	Bus Interface	BI_DATA27	AC20	Bus Interface
$\overline{\text{BI\_CS0}}$	AD11	Bus Interface	BI_DATA28	AC19	Bus Interface
$\overline{\text{BI\_CS1}}$	AF13	Bus Interface	BI_DATA29	AF20	Bus Interface
$\overline{\text{BI\_CS2}}$	AB3	Bus Interface	BI_DATA30	AF24	Bus Interface
$\overline{\text{BI\_CS3}}$	AC1	Bus Interface	BI_DATA31	AD26	Bus Interface
BI_DATA0 (MSB)	AE19	Bus Interface	$\overline{\text{BI\_OE}}$	AE13	Bus Interface
BI_DATA1	AD17	Bus Interface	BI_READY	AC12	Bus Interface

Signal Pins Sorted by Signal Name (Continued)

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
BI_R$\overline{W}$	AE14	Bus Interface	DAC1_ROUT	C14	Video and Graphics
$\overline{BI\_WBE0}$	AD12	Bus Interface	DAC1_RREF_OUT	A9	Video and Graphics
CI_CLOCK	F26	Channel Interface	DAC1_VREF_IN	C10	Video and Graphics
CI_DATA0 (MSB)	C25	Channel Interface	DAC2_AGND0	B13	DAC Analog PWR + GND
CI_DATA1	D24	Channel Interface	DAC2_AGND1	B16	DAC Analog PWR + GND
CI_DATA2	G23	Channel Interface	DAC2_AGND2	D18	DAC Analog PWR + GND
CI_DATA3	A24	Channel Interface	DAC2_AVDD0	A14	DAC Analog PWR + GND
CI_DATA4	E26	Channel Interface	DAC2_AVDD1	C16	DAC Analog PWR + GND
CI_DATA5	B24	Channel Interface	DAC2_AVDD2	D17	DAC Analog PWR + GND
CI_DATA6	G26	Channel Interface	DAC2_AVDD3	C19	DAC Analog PWR + GND
CI_DATA7 (LSB)	E24	Channel Interface	DAC2_BOUT	A19	Video and Graphics
CI_DATA_ENABLE	H24	Channel Interface	DAC2_BREF_OUT	B19	Video and Graphics
CLK_VDDA	AC2	PLL Analog PWR + GND	DAC2_GOUT	B15	Video and Graphics
DA_BIT_CLOCK	P1	Audio	DAC2_GREF_IN	D15	Video and Graphics
DA_IEC_958	M3	Audio	DAC2_ROUT	C15	Video and Graphics
DA_LR_CHANNEL_CLOCK	M4	Audio	DAC2_RREF_OUT	B18	Video and Graphics
DA_OVERSAMPLING_CLOCK	P2	Audio	DAC2_VREF_IN	B17	Video and Graphics
DA_SERIAL_DATA0	R2	Audio	DV1_DATA0 (MSB)	C5	Video and Graphics
DAC1_AGND0	D13	DAC Analog PWR + GND	DV1_DATA1	B5	Video and Graphics
DAC1_AGND1	B10	DAC Analog PWR + GND	DV1_DATA2	C8	Video and Graphics
DAC1_AGND2	D8	DAC Analog PWR + GND	DV1_DATA3	B4	Video and Graphics
DAC1_AVDD0	B12	DAC Analog PWR + GND	DV1_DATA4	C6	Video and Graphics
DAC1_AVDD1	B11	DAC Analog PWR + GND	DV1_DATA5	C4	Video and Graphics
DAC1_AVDD2	D10	DAC Analog PWR + GND	DV1_DATA6	B3	Video and Graphics
DAC1_AVDD3	C9	DAC Analog PWR + GND	DV1_DATA7 (LSB)	A4	Video and Graphics
DAC1_BOUT	B7	Video and Graphics	DV1_HSYNC	A8	Video and Graphics
DAC1_BREF_OUT	A7	Video and Graphics	DV1_PIXEL_CLOCK	A6	Video and Graphics
DAC1_GOUT	A11	Video and Graphics	DV1_VSYNC	A3	Video and Graphics
DAC1_GREF_OUT	C13	Video and Graphics	G_SYSTEM_CLOCK	AC3	Global

Signal Pins Sorted by Signal Name (Continued)

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
$\overline{\text{G\_SYSTEM\_RST}}$	G3	Global	GPIO_5	C23	General Purpose I/O
GND	P23	Ground	GPIO_6	Y4	General Purpose I/O
GND	V4	Ground	GPIO_7	AA1	General Purpose I/O
GND	A1	Ground	GPIO_8	W3	General Purpose I/O
GND	A2	Ground	GPIO_9	L2	General Purpose I/O
GND	A26	Ground	GPIO_10	K3	General Purpose I/O
GND	AC4	Ground	GPIO_11	G2	General Purpose I/O
GND	AC8	Ground	GPIO_12	M2	General Purpose I/O
GND	AC13	Ground	GPIO_13	L3	General Purpose I/O
GND	AC18	Ground	GPIO_14	H1	General Purpose I/O
GND	AC23	Ground	GPIO_15	N2	General Purpose I/O
GND	AD3	Ground	GPIO_16	AA25	General Purpose I/O
GND	AD24	Ground	GPIO_17	Y23	General Purpose I/O
GND	AE1	Ground	GPIO_18	A22	General Purpose I/O
GND	AE2	Ground	GPIO_19	D20	General Purpose I/O
GND	AE25	Ground	GPIO_20	C21	General Purpose I/O
GND	AF1	Ground	GPIO_21	B21	General Purpose I/O
GND	AF25	Ground	GPIO_22	B20	General Purpose I/O
GND	AF26	Ground	GPIO_23	A21	General Purpose I/O
GND	B2	Ground	GPIO_24	A16	General Purpose I/O
GND	B25	Ground	GPIO_25	B14	General Purpose I/O
GND	B26	Ground	GPIO_26	A12	General Purpose I/O
GND	C3	Ground	GPIO_27	C12	General Purpose I/O
GND	C24	Ground	GPIO_28	C11	General Purpose I/O
GND	D4	Ground	GPIO_29	J2	General Purpose I/O
GND	D9	Ground	GPIO_30	AB1	General Purpose I/O
GND	D19	Ground	GPIO_31	AB2	General Purpose I/O
GND	D23	Ground	I2C0_SCL	N1	Inter-Integrated Circuit)
GND	H4	Ground	I2C0_SDA	N3	Inter-Integrated Circuit
GND	J23	Ground	INT0	AC24	Interrupt
GND	N4	Ground	INT1	C26	Interrupt
GND	D14	Ground	INT2	AD2	Interrupt
GND	W23	Ground	INT3	AD1	Interrupt
GPIO_2	B9	General Purpose I/O	MUX1_0	AB25	Multiplexed I/O
GPIO_3	AB26	General Purpose I/O	MUX1_1	AB23	Multiplexed I/O
GPIO_4	P26	General Purpose I/O	MUX1_2	AC26	Multiplexed I/O

Signal Pins Sorted by Signal Name (Continued)

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
MUX2_0	C2	Multiplexed I/O	SD1_CLK	R23	SDRAM1 Controller
MUX2_1	D1	Multiplexed I/O	$\overline{\text{SD1\_CS0}}$	N26	SDRAM1 Controller
MUX2_2	E4	Multiplexed I/O	SD1_DATA0 (MSB)	AA26	SDRAM1 Controller
MUX2_3	E1	Multiplexed I/O	SD1_DATA1	Y24	SDRAM1 Controller
MUX3_0	V2	Multiplexed I/O	SD1_DATA2	W26	SDRAM1 Controller
MUX3_1	V1	Multiplexed I/O	SD1_DATA3	V25	SDRAM1 Controller
MUX3_2	P3	Multiplexed I/O	SD1_DATA4	V24	SDRAM1 Controller
MUX3_3	U3	Multiplexed I/O	SD1_DATA5	U25	SDRAM1 Controller
MUX3_4	U2	Multiplexed I/O	SD1_DATA6	U24	SDRAM1 Controller
MUX3_5	U4	Multiplexed I/O	SD1_DATA7	T26	SDRAM1 Controller
MUX3_6	T3	Multiplexed I/O	SD1_DATA8	U23	SDRAM1 Controller
MUX3_7	T2	Multiplexed I/O	SD1_DATA9	T25	SDRAM1 Controller
MUX3_8	T1	Multiplexed I/O	SD1_DATA10	U26	SDRAM1 Controller
MUX3_9	R3	Multiplexed I/O	SD1_DATA11	V26	SDRAM1 Controller
MUX3_10	R1	Multiplexed I/O	SD1_DATA12	V23	SDRAM1 Controller
Reserved (Tie to 3.3V)	F3	Global	SD1_DATA13	W25	SDRAM1 Controller
SC0_CLK	Y2	Smart Card Interface 0	SD1_DATA14	Y25	SDRAM1 Controller
SC0_DETECT	Y1	Smart Card Interface 0	SD1_DATA15 (LSB)	AA24	SDRAM1 Controller
SC0_IO	W4	Smart Card Interface 0	SD1_DQMH	P25	SDRAM1 Controller
SC0_RESET	W1	Smart Card Interface 0	SD1_DQML	T24	SDRAM1 Controller
SC0_VCC_COMMAND	W2	Smart Card Interface 0	$\overline{\text{SD1\_RAS}}$	N25	SDRAM1 Controller
SD1_ADDRESS0 (MSB)	M25	SDRAM1 Controller	$\overline{\text{SD1\_WE}}$	R25	SDRAM1 Controller
SD1_ADDRESS1	N24	SDRAM1 Controller	$\overline{\text{SERIAL1/INFRARED\_CTS}}$	F2	Serial1 / Infrared
SD1_ADDRESS2	P24	SDRAM1 Controller	$\overline{\text{SERIAL1/INFRARED\_RTS}}$	D36	Serial1 / Infrared
SD1_ADDRESS3	M26	SDRAM1 Controller	SERIAL1/INFRARED_RXD	G4	Serial1 / Infrared
SD1_ADDRESS4	L25	SDRAM1 Controller	SERIAL1/INFRARED_TXD	C1	Serial1 / Infrared
SD1_ADDRESS5	M24	SDRAM1 Controller	VDD25	AA4	2.5 V Power
SD1_ADDRESS6	K23	SDRAM1 Controller	VDD25	AA23	2.5 V Power
SD1_ADDRESS7	K24	SDRAM1 Controller	VDD25	AC6	2.5 V Power
SD1_ADDRESS8	J26	SDRAM1 Controller	VDD25	AC11	2.5 V Power
SD1_ADDRESS9	H26	SDRAM1 Controller	VDD25	AC16	2.5 V Power
SD1_ADDRESS10	J25	SDRAM1 Controller	VDD25	AC21	2.5 V Power
SD1_ADDRESS11	L24	SDRAM1 Controller	VDD25	D6	2.5 V Power
SD1_ADDRESS12	K25	SDRAM1 Controller	VDD25	D11	2.5 V Power
SD1_ADDRESS13 (LSB)	L26	SDRAM1 Controller	VDD25	D16	2.5 V Power
$\overline{\text{SD1\_CAS}}$	R24	SDRAM1 Controller	VDD25	D21	2.5 V Power

Signal Pins Sorted by Signal Name (Continued)

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
VDD25	F4	2.5 V Power	VDD33	AC14	3.3 V Power
VDD25	F23	2.5 V Power	VDD33	AC15	3.3 V Power
VDD25	L4	2.5 V Power	VDD33	AD18	3.3 V Power
VDD25	L23	2.5 V Power	VDD33	AC22	3.3 V Power
VDD25	T4	2.5 V Power	VDD33	AB24	3.3 V Power
VDD25	T23	2.5 V Power	VDD33	Y26	3.3 V Power
VDD33	E3	3.3 V Power	VDD33	W24	3.3 V Power
VDD33	G1	3.3 V Power	VDD33	R26	3.3 V Power
VDD33	H3	3.3 V Power	VDD33	N23	3.3 V Power
VDD33	M1	3.3 V Power	VDD33	M23	3.3 V Power
VDD33	P4	3.3 V Power	VDD33	J24	3.3 V Power
VDD33	R4	3.3 V Power	VDD33	E23	3.3 V Power
VDD33	V3	3.3 V Power	VDD33	C22	3.3 V Power
VDD33	AB4	3.3 V Power	VDD33	A20	3.3 V Power
VDD33	AD5	3.3 V Power	VDD33	A15	3.3 V Power
VDD33	AF7	3.3 V Power	VDD33	D12	3.3 V Power
VDD33	AD8	3.3 V Power	VDD33	D5	3.3 V Power
VDD33	AF12	3.3 V Power	VDD33	B8	3.3 V Power
			VDD33	C7	3.3 V Power

Signal Pins Sorted by Pin Number

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
A1	GND	Ground	B10	DAC1_AGND1	DAC Analog PWR + GND
A2	GND	Ground	B11	DAC1_AVDD1	DAC Analog PWR + GND
A3	DV1_VSYNC	Video and Graphics	B12	DAC1_AVDD0	DAC Analog PWR + GND
A4	DV1_DATA7(LSB)	Video and Graphics	B13	DAC2_AGND0	DAC Analog PWR + GND
A5			B14	GPIO_25	General Purpose I/O
A6	DV1_PIXEL_CLOCK	Video and Graphics	B15	DAC2_GOUT	Video and Graphics
A7	DAC1_BREF_OUT	Video and Graphics	B16	DAC2_AGND1	DAC Analog PWR + GND
A8	DV1_HSYNC	Video and Graphics	B17	DAC2_VREF_IN	Video and Graphics
A9	DAC1_RREF_OUT	Video and Graphics	B18	DAC2_RREF_OUT	Video and Graphics
A10	NC		B19	DAC2_BREF_OUT	Video and Graphics
A11	DAC1_GOUT	Video and Graphics	B20	GPIO_22	General Purpose I/O
A12	GPIO_26	General Purpose I/O	B21	GPIO_21	General Purpose I/O
A13	NC		B22	NC	
A14	DAC2_AVDD0	DAC Analog PWR + GND	B23	NC	
A15	VDD33	3.3 V Power	B24	CI_DATA5	Channel Interface
A16	GPIO_24	General Purpose I/O	B25	GND	Ground
A17	NC		B26	GND	Ground
A18	NC		C1	$\overline{\text{SERIAL1/INFRARED\_TXD}}$	Serial1 / Infrared
A19	DAC2_BOUT	Video and Graphics	C2	MUX2_0	Multiplexed IO
A20	VDD33	3.3 V Power	C3	GND	Ground
A21	GPIO_23	General Purpose I/O	C4	DV1_DATA5	Video and Graphics
A22	GPIO_18	General Purpose I/O	C5	DV1_DATA0	Video and Graphics
A23	NC		C6	DV1_DATA4	Video and Graphics
A24	CI_DATA3	Channel Interface	C7	VDD33	3.3 V Power
A25	NC		C8	DV1_DATA2	Video and Graphics
A26	GND	Ground	C9	DAC1_AVDD3	DAC Analog PWR + GND
B1	NC		C10	DAC1_VREF_IN	Video and Graphics
B2	GND	Ground	C11	GPIO_28	General Purpose I/O
B3	DV1_DATA6	Video and Graphics	C12	GPIO_27	General Purpose I/O
B4	DV1_DATA3	Video and Graphics	C13	DAC1_GREF_OUT	Video and Graphics
B5	DV1_DATA1	Video and Graphics	C14	DAC1_ROUT	Video and Graphics
B6	NC		C15	DAC2_ROUT	Video and Graphics
B7	DAC1_BOUT	Video and Graphics	C16	DAC2_AVDD1	DAC Analog PWR + GND
B8	VDD33	3.3 V Voltage	C17	NC	
B9	GPIO_2	General Purpose I/O	C18	NC	

Signal Pins Sorted by Pin Number (Continued)

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
C19	DAC2_AVDD3	DAC Analog PWR + GND	E2	NC	
C20	NC		E3	VDD33	3.3 V Power
C21	GPIO_20	General Purpose I/O	E4	MUX2_2	Multiplexed IO
C22	VDD33	3.3 V Power	E23	VDD33	3.3 V Power
C23	GPIO_5	General Purpose I/O	E24	CI_DATA7	Channel Interface
C24	GND	Ground	E25	NC	
C25	CI_DATA0(MSB)	Channel Interface	E26	CI_DATA4	Channel Interface
C26	INT1	Interrupts	F1	NC	
D1	MUX2_1	Multiplexed IO	F2	$\overline{\text{SERIAL1/INFRARED\_CTS}}$	Serial/Infared
D2	NC		F3	Reserved (Tie to 3.3V)	Global
D3	$\overline{\text{SERIAL1/INFRARED\_RTS}}$	Serial1 / Infrared	F4	VDD25	2.5 V Power
D4	GND	Ground	F23	VDD25	2.5 V Power
D5	VDD33	3.3 V Power	F24	NC	
D6	VDD25	2.5 V Power	F25	NC	
D7	NC		F26	CI_CLOCK	Channel Interface
D8	DAC1_AGND2	DAC Analog PWR + GND	G1	VDD33	3.3 V Power
D9	GND	Ground	G2	GPIO_11	General Purpose I/O
D10	DAC1_AVDD2	DAC Analog PWR + GND	G3	$\overline{\text{G\_SYSTEM\_RST}}$	Global
D11	VDD25	2.5 V Power	G4	$\overline{\text{SERIAL1/INFRARED\_RXD}}$	Serial/Infared
D12	VDD33	3.3 V Power	G23	CI_DATA2	Channel Interface
D13	DAC1_AGND0	DAC Analog PWR + GND	G24	NC	
D14	GND	Ground	G25	NC	
D15	DAC2_GREF_IN	Video and Graphics	G26	CI_DATA6	Channel Interface
D16	VDD25	2.5 V Power	H1	GPIO_14	General Purpose I/O
D17	DAC2_AVDD2	DAC Analog PWR + GND	H2	NC	
D18	DAC2_AGND2	DAC Analog PWR + GND	H3	VDD33	3.3 V Power
D19	GND	Ground	H4	GND	Ground
D20	GPIO_19	General Purpose I/O	H23	NC	
D21	VDD25	2.5 V Power	H24	CI_DATA_ENABLE	Channel Interface
D22	NC		H25	NC	
D23	GND	Ground	H26	SD1_ADDRESS9	SDRAM1 Controller
D24	CI_DATA1	Channel Interface	J1	NC	
D25	NC		J2	GPIO_29	General Purpose I/O
D26	NC		J3	NC	
E1	MUX2_3	Multiplexed IO	J4	NC	

Signal Pins Sorted by Pin Number (Continued)

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
J23	GND	Ground	N26	$\overline{\text{SD1\_CS0}}$	SDRAM1 Controller
J24	VDD33	3.3 V Power	P1	DA_BIT_CLOCK	Audio
J25	SD1_ADDRESS10	SDRAM1 Controller	P2	DA_OVERSAMPLING_CLOCK	Audio
J26	SD1_ADDRESS8	SDRAM1 Controller	P3	MUX3_2	Multiplexed IO
K1	NC		P4	VDD33	3.3 V Power
K2	NC		P23	GND	Ground
K3	GPIO_10	General Purpose I/O	P24	SD1_ADDRESS2	SDRAM1 Controller
K4	NC		P25	SD1_DQMH	SDRAM1 Controller
K23	SD1_ADDRESS6	SDRAM1 Controller	P26	GPIO_4	General Purpose I/O
K24	SD1_ADDRESS7	SDRAM1 Controller	R1	MUX3_10	Multiplexed IO
K25	SD1_ADDRESS12	SDRAM1 Controller	R2	DA_SERIAL_DATA0	Audio
K26	NC		R3	MUX3_9	Multiplexed IO
L1	NC		R4	VDD33	3.3 V Power
L2	GPIO_9	General Purpose I/O	R23	SD1_CLK	SDRAM1 Controller
L3	GPIO_13	General Purpose I/O	R24	$\overline{\text{SD1\_CAS}}$	SDRAM1 Controller
L4	VDD25	2.5 V Power	R25	$\overline{\text{SD1\_WE}}$	SDRAM1 Controller
L23	VDD25	2.5 V Power	R26	VDD33	3.3 V Power
L24	SD1_ADDRESS11	SDRAM1 Controller	T1	MUX3_8	Multiplexed IO
L25	SD1_ADDRESS4	SDRAM1 Controller	T2	MUX3_7	Multiplexed IO
L26	SD1_ADDRESS13(LSB)	SDRAM1 Controller	T3	MUX3_6	Multiplexed IO
M1	VDD33	3.3 V Power	T4	VDD25	2.5 V Power
M2	GPIO_12	General Purpose I/O	T23	VDD25	2.5 V Power
M3	DA_IEC_958	Audio	T24	SD1_DQML	SDRAM1 Controller
M4	DA_LR_CHANNEL_CLOCK	Audio	T25	SD1_DATA9	SDRAM1 Controller
M23	VDD33	3.3 V Power	T26	SD1_DATA7	SDRAM1 Controller
M24	SD1_ADDRESS5	SDRAM1 Controller	U1	NC	
M25	SD1_ADDRESS0	SDRAM1 Controller	U2	MUX3_4	Multiplexed IO
M26	SD1_ADDRESS3	SDRAM1 Controller	U3	MUX3_3	Multiplexed IO
N1	I2C0_SCL	Inter-Integrated Circuit	U4	MUX3_5	Multiplexed IO
N2	GPIO_15	General Purpose I/O	U23	SD1_DATA8	SDRAM1 Controller
N3	I2C0_SDA	Inter-Integrated Circuit	U24	SD1_DATA6	SDRAM1 Controller
N4	GND	Ground	U25	SD1_DATA5	SDRAM1 Controller
N23	VDD33	3.3 V Power	U26	SD1_DATA10	SDRAM1 Controller
N24	SD1_ADDRESS1	SDRAM1 Controller	V1	MUX3_1	Multiplexed IO
N25	$\overline{\text{SD1\_RAS}}$	SDRAM1 Controller	V2	MUX3_0	Multiplexed IO

Signal Pins Sorted by Pin Number (Continued)

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
V3	VDD33	3.3 V Power	AB24	VDD33	3.3 V Power
V4	GND	Ground	AB25	MUX1_0	Multiplexed IO
V23	SD1_DATA12	SDRAM1 Controller	AB26	GPIO_3	General Purpose I/O
V24	SD1_DATA4	SDRAM1 Controller	AC1	$\overline{\text{BI\_CS3}}$	Bus Interface
V25	SD1_DATA3	SDRAM1 Controller	AC2	CLK_VDDA	PLL Analog PWR + GND
V26	SD1_DATA11	SDRAM1 Controller	AC3	G_SYSTEM_CLOCK	Global
W1	SC0_RESET	Smart Card Interface 0	AC4	GND	Ground
W2	SC0_VCC_COMMAND	Smart Card Interface 0	AC5	BI_ADDRESS17	Bus Interface
W3	GPIO_8	General Purpose I/O	AC6	VDD25	2.5 V Power
W4	SC0_IO	Smart Card Interface 0	AC7	BI_ADDRESS18	Bus Interface
W23	GND	Ground	AC8	GND	Ground
W24	VDD33	3.3 V Power	AC9	BI_ADDRESS12	Bus Interface
W25	SD1_DATA13	SDRAM1 Controller	AC10	BI_ADDRESS23	Bus Interface
W26	SD1_DATA2	SDRAM1 Controller	AC11	VDD25	2.5 V Power
Y1	SC0_DETECT	Smart Card Interface 0	AC12	BI_READY	Bus Interface
Y2	SC0_CLK	Smart Card Interface 0	AC13	GND	Ground
Y3	NC		AC14	VDD33	3.3 V Power
Y4	GPIO_6	General Purpose I/O	AC15	VDD33	3.3 V Power
Y23	GPIO_17	General Purpose I/O	AC16	VDD25	2.5 V Power
Y24	SD1_DATA1	SDRAM1 Controller	AC17	BI_DATA9	Bus Interface
Y25	SD1_DATA14	SDRAM1 Controller	AC18	GND	Ground
Y26	VDD33	3.3 V Power	AC19	BI_DATA28	Bus Interface
AA1	GPIO_7	General Purpose I/O	AC20	BI_DATA27	Bus Interface
AA2	NC		AC21	VDD25	2.5 V Power
AA3	NC		AC22	VDD33	3.3 V Power
AA4	VDD25	2.5 V Power	AC23	GND	Ground
AA23	VDD25	2.5 V Power	AC24	INT0	Interrupts
AA24	SD1_DATA15	SDRAM1 Controller	AC25	NC	
AA25	GPIO_16	General Purpose I/O	AC26	MUX1_2	Multiplexed IO
AA26	SD1_DATA0	SDRAM1 Controller	AD1	INT3	Interrupts
AB1	GPIO_30	General Purpose I/O	AD2	INT2	Interrupts
AB2	GPIO_31	General Purpose I/O	AD3	GND	Ground
AB3	$\overline{\text{BI\_CS2}}$	Bus Interface	AD4	BI_ADDRESS14	Bus Interface
AB4	VDD33	3.3 V Power	AD5	VDD33	3.3 V Power
AB23	MUX1_1	Multiplexed IO	AD6	BI_ADDRESS19	Bus Interface

Signal Pins Sorted by Pin Number (Continued)

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
AD7	BI_ADDRESS20	Bus Interface	AE16	BI_DATA5	Bus Interface
AD8	VDD33	3.3 V Power	AE17	BI_DATA6	Bus Interface
AD9	BI_ADDRESS22	Bus Interface	AE18	BI_DATA8	Bus Interface
AD10	BI_ADDRESS9	Bus Interface	AE19	BI_DATA0	Bus Interface
AD11	$\overline{\text{BI\_CS0}}$	Bus Interface	AE20	BI_DATA15	Bus Interface
AD12	$\overline{\text{BI\_WBE0}}$	Bus Interface	AE21	NC	
AD13	BI_DATA13	Bus Interface	AE22	BI_DATA19	Bus Interface
AD14	BI_DATA11	Bus Interface	AE23	BI_DATA18	Bus Interface
AD15	BI_DATA3	Bus Interface	AE24	BI_DATA24	Bus Interface
AD16	BI_DATA2	Bus Interface	AE25	GND	Ground
AD17	BI_DATA1	Bus Interface	AE26	BI_DATA23	Bus Interface
AD18	VDD33	3.3 V Power	AF1	GND	Ground
AD19	BI_DATA20	Bus Interface	AF2	BI_ADDRESS31	Bus Interface
AD20	NC		AF3	BI_ADDRESS30	Bus Interface
AD21	BI_DATA22	Bus Interface	AF4	BI_ADDRESS15	Bus Interface
AD22	BI_DATA25	Bus Interface	AF5	BI_ADDRESS28	Bus Interface
AD23	BI_DATA17	Bus Interface	AF6	BI_ADDRESS27	Bus Interface
AD24	GND	Ground	AF7	VDD33	3.3 V Power
AD25	BI_DATA16	Bus Interface	AF8	BI_ADDRESS25	Bus Interface
AD26	BI_DATA31	Bus Interface	AF9	BI_ADDRESS24	Bus Interface
AE1	GND	Ground	AF10	NC	
AE2	GND	Ground	AF11	BI_ADDRESS8	Bus Interface
AE3	BI_ADDRESS29	Bus Interface	AF12	VDD33	3.3 V Power
AE4	NC		AF13	$\overline{\text{BI\_CS1}}$	Bus Interface
AE5	BI_ADDRESS16	Bus Interface	AF14	BI_DATA12	Bus Interface
AE6	NC		AF15	AUD_VDDA0	PLL Analog PWR + GND
AE7	BI_ADDRESS26	Bus Interface	AF16	BI_DATA10	Bus Interface
AE8	BI_ADDRESS21	Bus Interface	AF17	NC	
AE9	BI_ADDRESS11	Bus Interface	AF18	BI_DATA14	Bus Interface
AE10	BI_ADDRESS10	Bus Interface	AF19	BI_DATA7	Bus Interface
AE11	BI_ADDRESS13	Bus Interface	AF20	BI_DATA29	Bus Interface
AE12	AUD_VDDA1	PLL Analog PWR + GND	AF21	BI_DATA21	Bus Interface
AE13	$\overline{\text{BI\_OE}}$	Bus Interface	AF22	BI_DATA26	Bus Interface
AE14	$\overline{\text{BI\_RW}}$	Bus Interface	AF23	NC	
AE15	BI_DATA4	Bus Interface	AF24	BI_DATA30	Bus Interface

Signal Pins Sorted by Pin Number (Continued)

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
AF25	GND	Ground	AF26	GND	Ground

STB0210x Multiplexed I/O Signal Table

STB0210x has four sets of multiplexed I/O signals: Mux0, Mux1, Mux2, and Mux3. At reset, the multiplexed I/O signals are tristated, unless noted.

The muxtiplexed I/O can be selected by column in the following tables. For example, if Input/Output 1 is selected, Input/Output 2 and Input/Output 3 are not available.

Blank entries indicate reserved multiplexing.

Multiplexed I/O Signal Table - Mux1

Bit #	Input/Output 1	I/O	Input/Output 2	I/O	Input/Output 3	
00	EDMAC2_ACK	O	EBM_HOLDACK	I/O	IDE_REQ	I
01	EDMAC2_REQ	I	EBM_HOLDREQ	I/O	IDE_ACK	O
02	EDMAC2_EOT	I/O	EBM_BUSREQ	I/O		

Multiplexed I/O Signal Table - Mux2

Bit #	Input/Output 1	I/O	Input/Output 2	I/O
00	SERIAL0/16550_TXD	O	SSP_TXD	O
01	SERIAL0/16550_RXD	I	SSP_RXD	I
02	SERIAL0/16550_CTS	I	SSP_CLK	I
03	SERIAL0/16550_RTS	O	SSP_FS	I/O

Multiplexed I/O Signal Table - Mux3

Bit #	Input/Output 1	I/O	Input/Output 2	I/O	Input/Output 3	I/O	Input/Output 4	I/O
00	HSP_DATA0	O			SERIAL1/INFRARED_DSR (through GPIO bit 31 alt rcv 2)	I		
01	HSP_DATA1	O			SERIAL1/INFRARED_DTR	O		
02	HSP_DATA2	O			RW_TMS (through GPIO bit 11 alt rcv 1	I	RT_TS1E	O
03	HSP_DATA3	O			RW_TDI (through GPIO bit 12 alt rcv 1)	I	RT_TS2E	O
04	HSP_DATA4	O			RW_TCK (through GPIO bit 13 alt rcv 1)	I	RT_TS3	O
05	HSP_DATA5	O			RW_TDO	O	RT_TS4	O

Multiplexed I/O Signal Table - Mux3 (Continued)

Bit #	Input/Output 1	I/O	Input/Output 2	I/O	Input/Output 3	I/O	Input/Output 4	I/O
06	HSP_DATA6	O			RW_HALT (through GPIO bit 15 alt rcv 1)	I	RT_TS5	O
07	HSP_DATA7	O			SERIAL0/16550_DSR (through GPIO bit 5 alt rcv 3)	I	RT_TS6	O
08	HSP_CLOCK	O			SERIAL0/16550_DTR	O		
09	HSP_DATA_ ENABLE	O			SERIAL0/16550_DCD (through GPIO bit 6 alt rcv 3)	I		
10	HSP_PACKET_ START	O			SERIAL0/16550_RI (through GPIO bit 8 alt rcv 3)	I		

General Purpose I/O (GPIO)

The following table describes the GPIO bits. For each GPIO bit only one signal can be selected at a time.

Each table row lists the signal associated with each logical GPIO bit number. The first column lists the GPIO bit number. The second column lists the signal connected as input or output to the first alternate GPIO multiplexer. The signal name is listed first, followed by the signal description. The third column gives the direction of the signal listed in column 2. The same format is used for columns 4 through 7.

Blank entries indicate reserved GPIO multiplexing.

GPIO bit number refers to the device GPIO signal name, not the physical device pin number.

After reset all GPIOs are programmed as inputs, with the exception of GPIO0 bit 29 (PWM output), which defaults to an open-drain output, and GPIO bit 14 (JTAG TDO output), which defaults to an output (if BI_DATA[4] is set to ‘0’ during reset).

General Purpose I/O Bits

Bit #	Input/Output Mux 1	Type	Input/Output Mux 2	Type	Input/Output Mux 3	Type
00						
01						
02	AV_CSYNC $\overline{\text{BI\_CS4}}$	I O	GPT_FreqGenOut	O	INT4	I
03	SYS_CLK	O	$\overline{\text{BI\_CS5}}$	O	INT5	I
04	$\overline{\text{EDMAC0\_REQ}}$	I	$\overline{\text{SD1\_CS1}}$	O	$\overline{\text{SERIAL0/16550\_DTR}}$	O
05	$\overline{\text{EDMAC0\_ACK}}$	O			$\overline{\text{SERIAL0/16550\_DSR}}$	I
06	SCP_TXD	O	CI_PACKET_START	I	$\overline{\text{SERIAL0/16550\_DCD}}$	I
07	SCP_RXD	I	CI_DATA_ERROR	I	TS_BCLKEN	I
08	SCP_CLK	O	$\overline{\text{TS\_REQ}}$	O	$\overline{\text{SERIAL0/16550\_RI}}$	I
09	PWM0	O	GPT_COMP0	O	GPT_CAPT0 $\overline{\text{BI\_CS6}}$	I O
10	PWM1	O	GPT_COMP1	O	GPT_CAPT1 $\overline{\text{BI\_CS7}}$	I O
11	RW_TMS	I	SSP_TXD	O	$\overline{\text{BI\_CS6}}$	O
12	RW_TDI	I	SSP_RXD	I	$\overline{\text{BI\_CS7}}$	O
13	RW_TCK	I	SSP_CLK	I	INT6	I
14	RW_TDO	O	SSP_FS	I/O	INT7	I
15	$\overline{\text{RW\_HALT}}$	I	SERIAL0/16550_CLK - External SERIAL0/16550 Clock Input	I	SYS_CLK	O
16			$\overline{\text{BI\_CS4}}$	O		
17			$\overline{\text{BI\_CS5}}$	O	HSP_ERROR	O
18	DV_TRANSPARENCY_ GATE	I/O	DV2_PIXEL_CLOCK	I	SERIAL1/INFRARED_CLK - External SERIAL1/INFRARED Clock Input	I
19	TTX_REQ	I/O	DV2_VSYNC	I/O		

General Purpose I/O Bits (Continued)

Bit #	Input/Output Mux 1	Type	Input/Output Mux 2	Type	Input/Output Mux 3	Type
20	TTX_DATA	I/O	DV2_HSYNC	I/O		
21	DV2_DATA0 (MSB)	I/O			INT8	I
22	DV2_DATA1	I/O			INT9	I
23	DV2_DATA2	I/O				
24	DV2_DATA3	I/O				
25	DV2_DATA4	I/O				
26	DV2_DATA5	I/O				
27	DV2_DATA6	I/O				
28	DV2_DATA7	I/O				
29	DENC_PWM_OUTPUT	O	XPT_PWM_OUTPUT	O		
30	$\overline{\text{EDMAC1\_REQ}}$ $\overline{\text{BI\_WBE2}}$	I O	$\overline{\text{SERIAL1/INFRARED\_DTR}}$	O		
31	$\overline{\text{EDMAC1\_ACK}}$	O	$\overline{\text{SERIAL1/INFRARED\_DSR}}$ $\overline{\text{BI\_WBE3}}$	I O		

Electrical Information

The following tables give the absolute ratings for various electrical characteristics.

Drivers/Receivers

Four types of I/O drivers and receivers are used on the STB0210x device, as follows:

I/O Driver Types

Driver/ Receiver Type	Characteristics	Used on I/O signals:
BP3365	5 V tolerant, no pull-up or pull-down (external pull-up is required)	$\overline{\text{G\_SYSTEM\_RESET}}$, GPIO[2], GPIO[29], SC0_IO, SC0_CLK, SC0_DETECT, SC0_RESET, SC0_VCC_COMMAND, BI_READY
BP3335	5 V tolerant, no pull-up or pull-down (external pull-up is required)	I2C0_SDA, I2C0_SCL
BT3350PU	3.3 V I/O with pull-up	BI_DATA[0:31]
BT3365PU	3.3 V I/O with pull-up	all other digital I/O signals

DC Electrical Characteristics

The table, “DC Electrical Characteristics,” gives the absolute ratings for various electrical characteristics. The temperature is 70° C in all cases.

DC Electrical Characteristics

Driver / Receiver	Symbol	Parameter	Conditions	Min	Typ	Max	Units
BP3335	V_{IH}	High Level Input Voltage		2.00		5.50[1]	V
	V_{IL}	Low Level Input Voltage		-0.60[2]		0.80	V
	V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = 17.0 mA	2.40			V
	V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 11.0 mA			0.4	V
BP3365	V_{IH}	High Level Input Voltage		2.00		5.50[1]	V
	V_{IL}	Low Level Input Voltage		-0.60[2]		0.80	V
	V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = 9.0 mA	2.40			V
	V_{OL}	Low Level Output Voltagec	V_{CC} = Min, I_{OL} = 6.0 mA			0.4	V

1. Maximum V_{IH} applies to overshoot only.
2. Minimum V_{IL} applies to undershoot only.

DC Electrical Characteristics (Continued)

Driver / Receiver	Symbol	Parameter	Conditions	Min	Typ	Max	Units
BT3350PU	V_{IH}	High Level Input Voltage		2.00		4.0[1]	V
	V_{IL}	Low Level Input Voltage		-0.60[2]		0.80	V
	V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = 12.0 mA	2.40			V
	V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL}= 8.0 mA			0.4	V
BT3365PU	V_{IH}	High Level Input Voltage		2.00		4.0[1]	V
	V_{IL}	Low Level Input Voltage		-0.60[2]		0.80	V
	V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = 9.0 mA	2.40			V
	V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL}= 6.0 mA			0.4	V
BT3350PU, BT3365PU	I_I	Maximum Input Current	V_{IN} = 0 V			-250	µA
BP3335, BP3365	I_I	Maximum Input Current				0	µA
N/A	I_{CC}	Supply Current, 2.5 V	V_{CC} = Max			TBD	mA
N/A	I_{CC330}	Supply Current, 3.3 V	V_{CC330} = Max			TBD	mA
All	C_I	Input Capacitance	V_{CC} = Nom, V_I = Nom			2.6	pF
All	ESD	Electro Static Discharge		TBD		TBD	V
N/A	PD	Power Dissipation			2.5		W

1. Maximum V_{IH} applies to overshoot only.
2. Minimum V_{IL} applies to undershoot only.

The absolute maximum ratings in the following table are stress ratings only. Operation at or beyond these maximum ratings may cause permanent damage to the device.

Absolute Maximum Ratings

Parameter	Maximum Rating
Supply voltage with respect to GND, 2.5 V supply	3.0 V
Supply voltage with respect to GND, 3.3 V supply	3.9 V
Case temperature under bias	TBD
Storage temperature	-65° C to 150° C

Operating Conditions

The STB0210x Digital Set-Top Box Integrated Controller can interface to either 3.3 V or 5 V technologies. 5 V interfaces are supported only for drivers/receivers supporting 5 V tolerance (see *Drivers/Receivers*). The range for supply voltages is specified for five-percent margins relative to a nominal 2.5 V and 3.3 V power supply.

Note: Device operation beyond the conditions specified in the table below is not recommended. Extended operation beyond the recommended conditions may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage, 2.5 V	2.38	2.62	V
V_{CC330}	Supply Voltage, 3.3 V	3.14	3.47	V
T_A	Operating Free Air Temperature	0°	70°	C

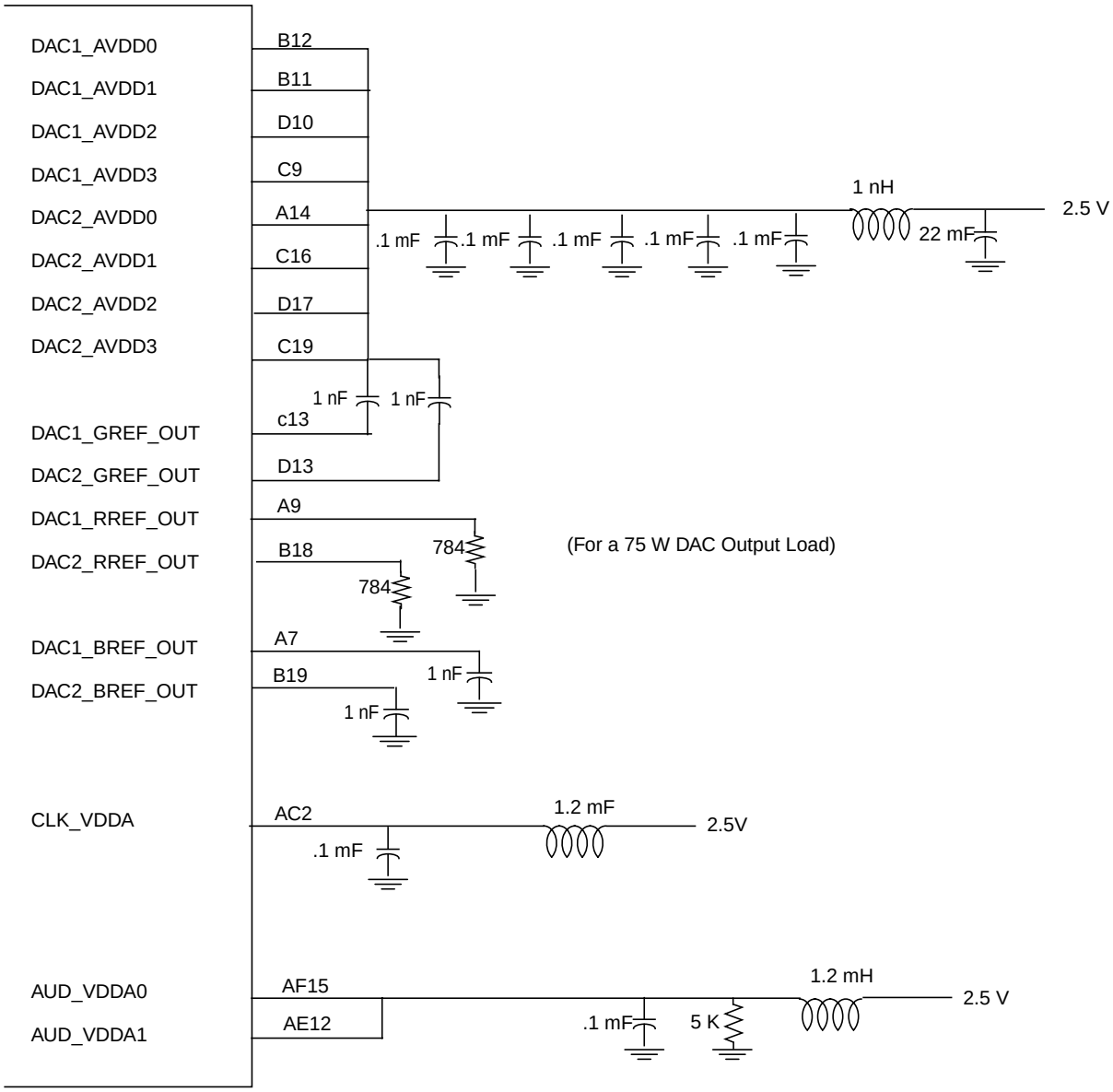
Power Considerations

Power dissipation is determined by operating frequency, temperature, and supply voltage, as well as external source/sink current requirements.

Recommended Connections

Power and ground pins should all be connected to separate power and ground planes in the circuit board to which the STB0210x is mounted. Unused input pins must be tied inactive, either high or low.

Recommended Connections for Analog I/O Pins



I/O Timing Diagrams

AC Specification

Timings are being developed and will be added when available. They should be similar to STB03xxx.

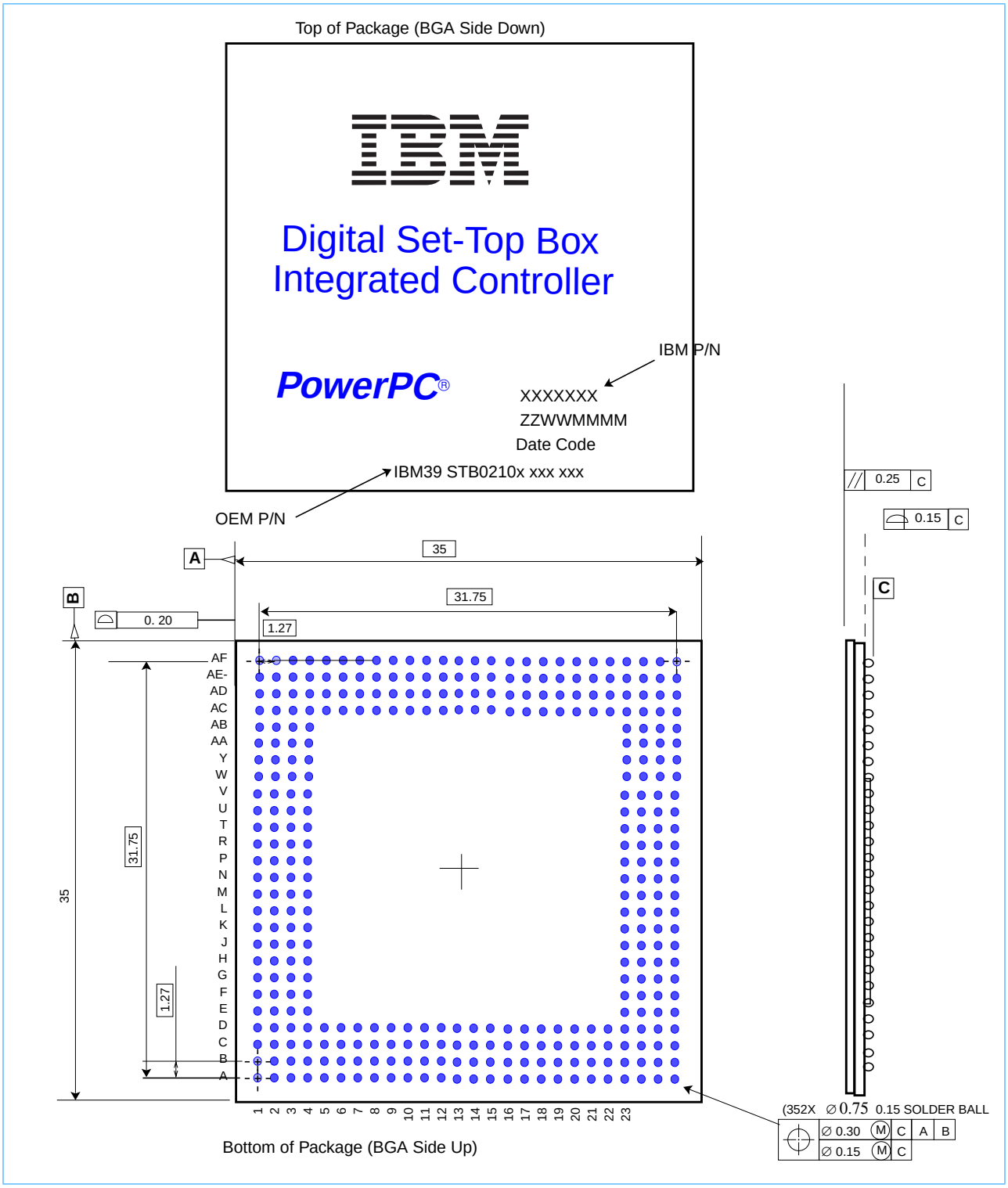
Note:

Additional Timing Information

Interface	Timing Information
IIC	Compliant with Philips Semiconductors I^2C Specification, dated 1995. Interface is asynchronous Direct connect
Smart Card (SC)	Compatible with ISO/IEC 7816-3. Interface is asynchronous Direct connect
Serial0/16550	Functionally identical to National Semiconductor NS16450 in character mode (after reset). Interface is asynchronous External transceiver logic is required
Serial1/Infrared	Functionally identical to IBM PowerPC403™ Serial Port Unit (SPU) (after reset). Compatible with the IrDA Specification 1.1 IrDA 1.0 SIR with data rates up to 115.2 Kbps IrDA 1.1 FIR with data rates up to 1.152 Mbps Interface is asynchronous External transceiver logic is required
External Interrupts	Inputs are asynchronous
DMA	External DMA request inputs are asynchronous
GPT	Capture timer inputs are asynchronous
External Bus Master	Interface is asynchronous
RISCWatch	Compatible with IBM RISCWatch probe Direct connect to probe Contact your IBM Applications Engineer for more information
RISCTrace	Compatible with IBM RISCTrace probe Direct connect to probe Contact your IBM Applications Engineer for more information

Mechanical Information

Package Diagram



Development Support

With IBM tools and the IBM PowerPC Embedded Tools Program, you receive the support you need to develop and debug your STB applications quickly.

IBM Tools

IBM offers Windows® 95/98–hosted development tools for STB applications that include:

- STB and processor reference design and evaluation kits, including board, compiler, debugger, ROM source, schematics, etc.
- RISCWatch debugger, with in-circuit, ROM monitor, RTOS-aware debugging and real-time non-invasive trace capability
- Metaware High C/C++ compiler, highly optimized for the PowerPC processors

Debug

The STB0210x facilitates development through its JTAG test access port.

With IBM RISCWatch or other third-party debugger on a workstation, you can single-step the processor and interrogate the internal processor state.

Additionally, the real-time debug port supports tracing the executed instruction stream out of the instruction cache. The trace status signals provide trace information in real-time instruction trace debug mode. This mode does not alter the performance of the processor.

Third-Party Tool Support

Through the IBM PowerPC Embedded Tools Program, you have access to hundreds of tools offered by over 75 industry-leading vendors. Often, the tools you currently use support PowerPC embedded processor products, such as the IBM STB010XX Digital Set-Top Box Integrated Controllers. For a list of the tools that are offered, visit IBM's tool support Web page at:

http://www.chips.ibm.com/products/powerpc/tools/

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Revision Log

Revision	Contents of Modification
March 24, 2000	Initial release (revision 00).
March 27, 2000	Update to GPIO Table (revision 01)

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