Dual Pixel LVDS Transmitter
EP387A

User Guide
V0.7

Revised: Nov. 29, 2005

Original Release Date: January 30, 2003

Explore Microelectronics, Taiwan

Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Jan/30/2003	--	Initial Version
0.1	Feb/18/2003	--	Correct pin names
0.2	Jun/17/2003	--	Power Consumption Measurement
0.3	Aug/14/2003	--	Correct ambiguous sentence
0.4	Dec/14/2004	Ether Lai	Update Electrical Characteristics & Add Package Information
0.5	Jun/02/2005	Ether Lai	Additional Function in 2nd Link; ID Position Change
0.6	Jul/15/2005	Ether Lai	Add ESD Rating
0.7	Nov/29/2005	Ether Lai	Change Package Marking

Section 1 Introduction

1.1 Overview

The EP387A supports dual LVDS links transmission between the host and the flat panel display up to QXGA resolutions. The transmitter converts 48 bits (24-bit color, dual pixel) of CMOS/TTL data and 3 control bits into 8 LVDS (Low Voltage Differential Signal) data streams. At a maximum input clock rate of 112MHz in the dual pixel mode, each LVDS differential data pair speed is 784Mbps, providing a total throughput of 5.4Gbps. Two additional modes are supported. One of them converts 24 bits (24-bit color, single pixel) data input into dual LVDS links and the input clock rate can be up to 165MHz. The other mode converts 24 bits data input into single LVDS link in order to support the inter-operability with the conventional LVDS application. The configurable pre-emphasis feature is provided to support additional output strength to reduce the cable loading effects. The EP387A provides a second LVDS output clock pair. Both LVDS clocks pairs are identical. This feature supports backward compatibility with the previous generation of single pixel LVDS transmitter. The second clock allows the transmitter to interface to panel using a "dual pixel" configuration of two 24-bit or 18-bit LVDS receivers.

1.2 Features

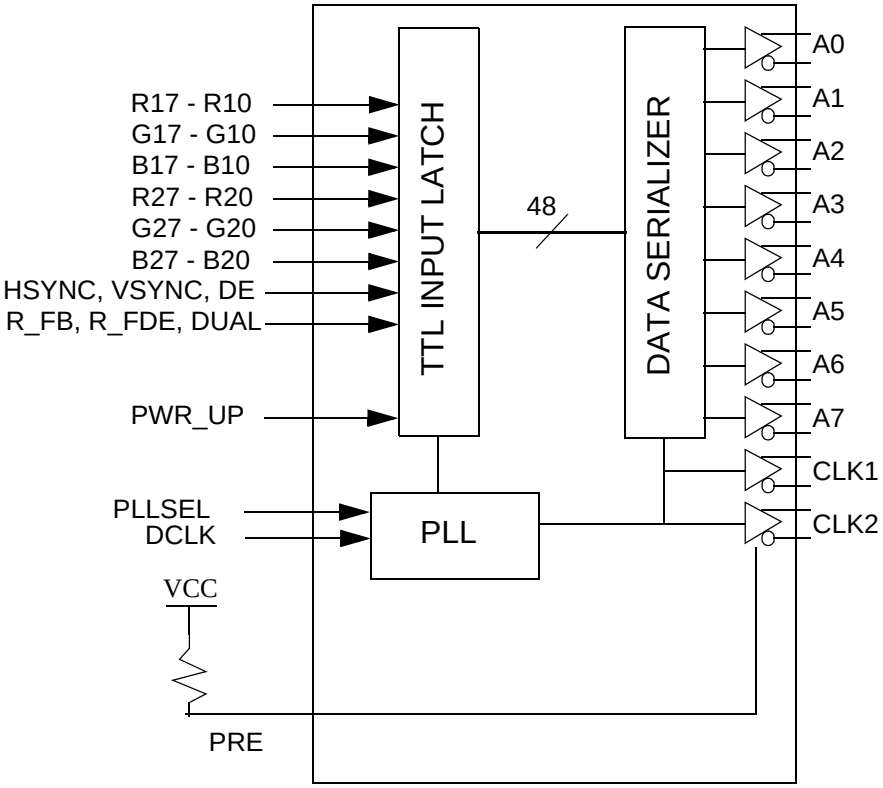
The EP387A includes the following distinctive features:

- Supports SVGA through QXGA resolutions
- Support 32.5MHz to 112/170MHz clock rates
- Up to 5.4Gbps bandwidth
- Pre-emphasis reduces cable loading effects
- Programmable Interface to timing controller, dual-in/dual-out, single-in/dual-out and single-in/single-out.
- Cycle-to-cycle jitter rejection
- 5V tolerant on data and control input pins
- Programmable data and control strobe select
- Compatible with ANSI/TIA/EIA-644 LVDS standard
- Compatible with National DS90C387A
- Single 3.3V CMOS design
- 100-pin LQFP (Pb Free, compliant to JEDEC/IPC J-STD-006)

Section 2 Overview

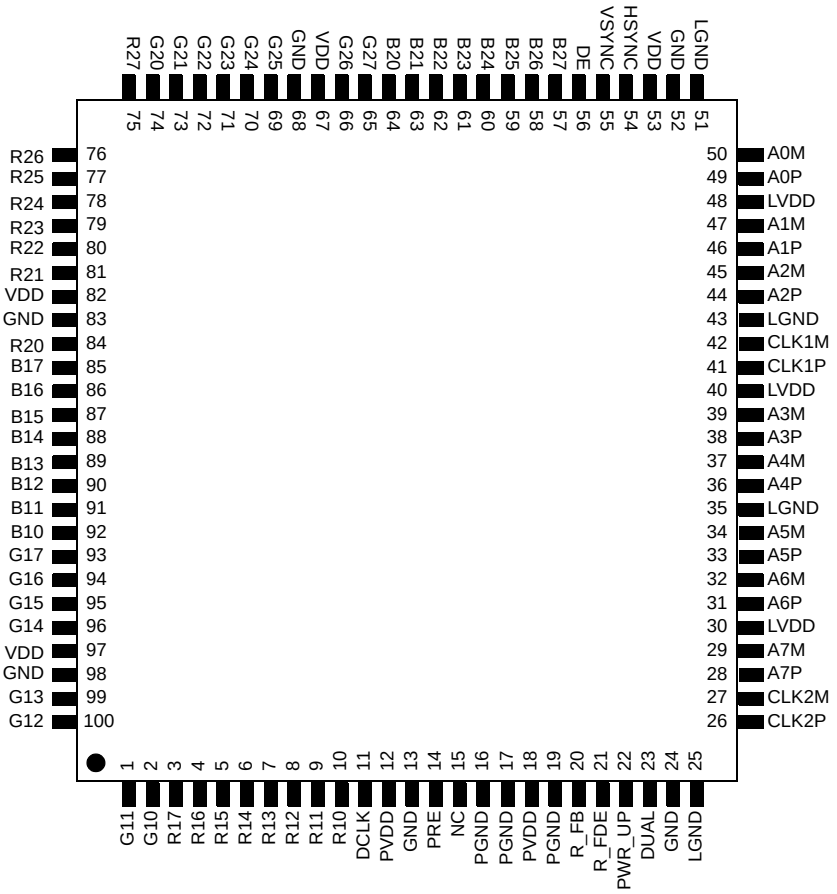
2.1 Block Diagram

Figure 2-1 Block Diagram of LVDS Transmitter EP387A



2.2 Pin Diagram

Figure 2-2 Pin Diagram of EP387A LVDS Transmitter



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 Input Control/Data/CLK Pins

NAME	PIN #	IN/OUT	DESCRIPTION
R17~R10 G17~G10 B17~B10	3~10 93~96,99~100, 1, 2 85~92	IN	Pixel Data Inputs for dual pixel input mode or single pixel input mode.
R27~R20 G27~G20 B27~B20	75~81, 84 65~66,69~74 57~64	IN	Pixel Data Inputs for dual pixel input mode.
DE	56	IN	Data Enable Input.
HSYNC	54	IN	Horizontal Sync Input.
VSYNC	55	IN	Vertical Sync Input.
DCLK	11	IN	Data Clock Input.
R_FB	20	IN	Programmable data strobe select. Rising data strobe edge selected when input is high.
R_FDE	21	IN	Programmable DE strobe select. Tied HIGH for data active when DE is high.
NC	15	IN	Not used.
PRE	14	IN	Pre-emphasis level select. Pre-emphasis is active when input is tied to VDD through external pull-up resistor. Resistor value determines pre-emphasis level. For normal LVDS drive level, leave this pin open (do not tie to ground).
DUAL	23	IN	Three modes selectable from this pin configuration. 1. dual pixel in, dual link out (DUAL = VDD) 2. single pixel in, dual link out (DUAL = 1/2 VDD) 3. single pixel in, single link out (DUAL = GND). Only LVDS channels A0 thru A3 and CLK1 are active for power saving.
PWR_UP	22	IN	Power Up.

Table 2-2 LVDS Output Pins

NAME	PIN #	IN/OUT	DESCRIPTION
AnP	28, 31, 33, 36, 38, 44, 46, 49	OUT	Positive LVDS differential data output.
AnM	29, 32, 34, 37, 39, 45, 47, 50	OUT	Negative LVDS differential data output.
CLK1P	41	OUT	Positive LVDS differential clock output.
CLK1M	42	OUT	Negative LVDS differential clock output.
CLK2P	26	OUT	Additional Positive LVDS differential clock output. Identical to CLK1P. No connect if not used.
CLK2M	27	OUT	Additional Negative LVDS differential clock output. Identical to CLK1M. No connect if not used.

Table 2-3 Power and Ground Pins

NAME	PIN #	IN/OUT	DESCRIPTION
VDD	53, 67, 82, 97	PWR	Digital VDD, 3.3V
VSS	13, 24, 52, 68, 83, 98	GND	Digital Ground.
LVDD	30, 40, 48	PWR	Analog VDD, 3.3V
LGND	25, 35, 43	GND	Analog Ground.
PVDD	12, 18	PWR	PLL VDD, 3.3V
PVSS	16, 17, 19	GND	PLL Ground.

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc} + 0.3	V
V_{OD}	LVDS Driver Output Voltage	-0.3		V_{cc} + 0.3	V
T_J	Junction Temperature	-25		125	℃
T_{STG}	Storage Temperature	-65		150	℃
θ_{JA}	Thermal Resistance (Junction to Ambient)		49		℃/W
ESD	Human Body Model (MIL-STD-883F 3015.7)	3			KV

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	-10	25	70	℃

CMOS/TTL DC Specifications (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0		Vcc	V
V_{IL}	Low-level Input Voltage		GND		0.8	V
I_{INC}	Input Current	0 <= V_{IN} <= Vcc			+/- 10	uA

LVDS Transmitter DC Specifications (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	R_L = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states				35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in V_{OC} between complimentary output states				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100 Ω			-10	mA
I_{OZ}	Output Tri-State Current	PWR_UP = 0V, V_{OUT} = 0V or VCC		+/- 1	+/- 10	uA

Supply Current (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{TCCG}	Transmitter Supply Current Worst Case	R_L = 100 Ω, C_L = 5 pF, Worst Case Pattern, DUAL = VCC	F = 32.5 MHz		48		mA
			F = 67.5 MHz		65		mA
			F = 82.5 MHz		72		mA
			F = 112 MHz		96		mA
	Transmitter Supply Current 16 Grayscale	R_L = 100 Ω, C_L = 5 pF, 16 Grayscale Pattern, DUAL = VCC	F = 32.5 MHz		42		mA
			F = 67.5 MHz		54		mA
			F = 82.5 MHz		58		mA
			F = 112 MHz		75		mA
I_{TCCZ}	Transmitter Supply Current Power Down	PWR_UP = 0, Input Source is Tri-stated			28		uA

Figure 2-3 Worst Case Pattern

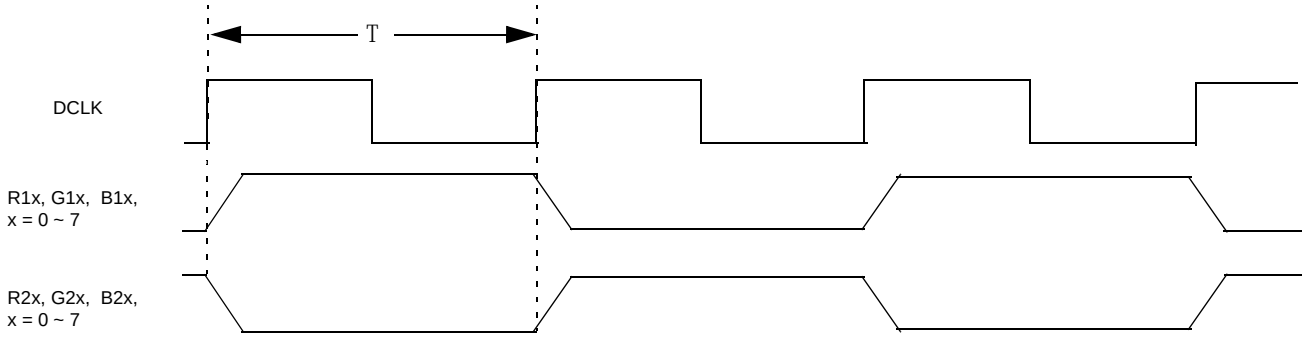
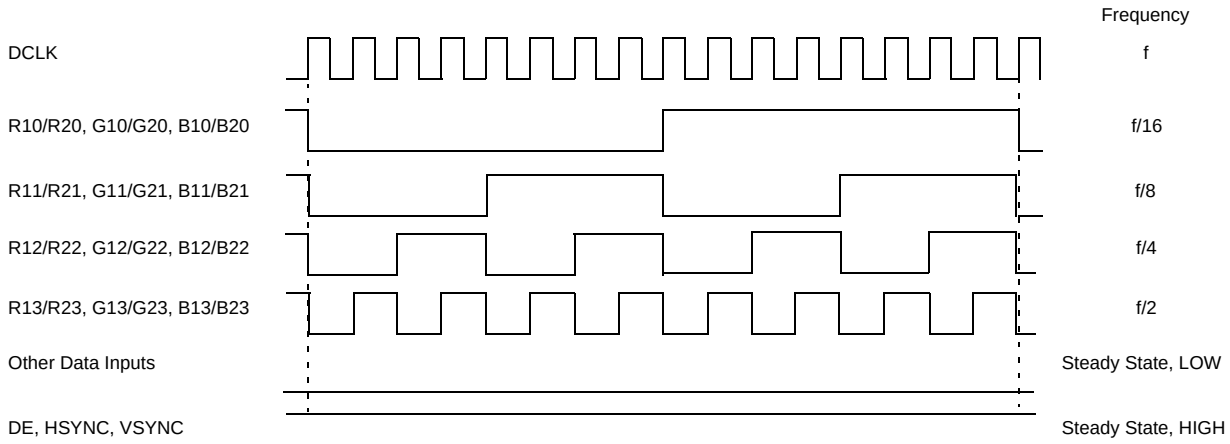


Figure 2-4 16 Grayscale Pattern



Recommended Transmitter Input Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{CIT}	DCLK IN Transition Time	DUAL = GND or VCC	1.0	2.0	3.0	ns
		DUAL = 1/2 VCC	1.0	1.5	1.7	ns
T_{CIP}	DCLK IN Period	DUAL = GND or VCC	8.928		30.77	ns
		DUAL = 1/2 VCC	5.88		15.38	ns
T_{TCH}	DCLK IN High Time		0.35T	0.5T	0.65T	ns
T_{TCL}	DCLK IN Low Time		0.35T	0.5T	0.65T	ns

Transmitter AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{LLHT}	LVDS Low-to-High Transition Time	PRE = 0.75V		0.14	0.7	ns
		PRE = VCC		0.11	0.6	ns
T_{LHLT}	LVDS High-to-Low Transition Time	PRE = 0.75V		0.16	0.8	ns
		PRE = VCC		0.11	0.7	ns
T_{TS}	TTL Data Setup to DCLK IN		3.0			ns
T_{TH}	TTL Data Hold from DCLK IN		0			ns
T_{PLLS}	PLL Set Time				10	ms
T_{PDO}	Power Down Delay				100	ns

2.5 Timing Diagrams

Figure 2-5 LVDS Output Timing Definition

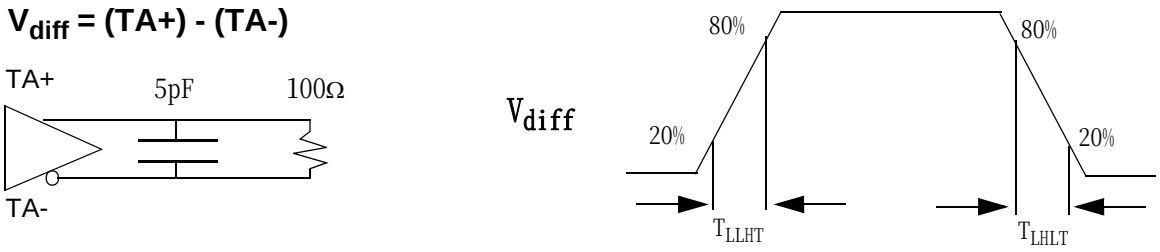


Figure 2-6 TTL Input Timing Definition

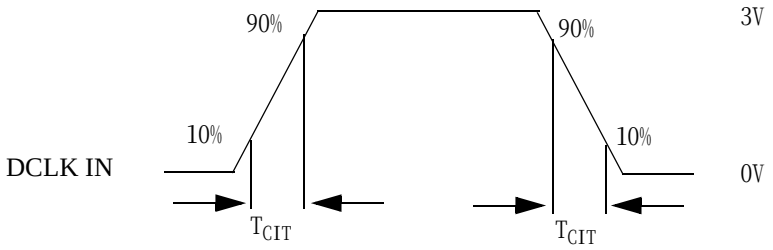


Figure 2-7 Setup/Hold and High/Low Timing Definition (Falling Edge Strobe)

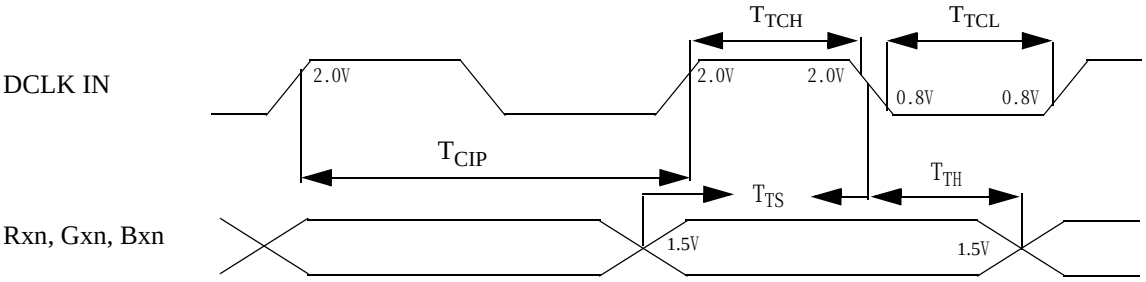


Figure 2-8 Phase Lock Loop Set Time Definition

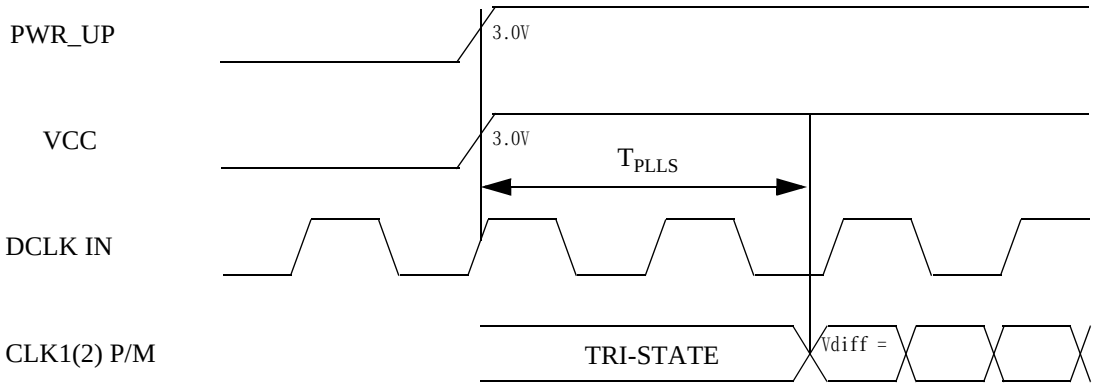
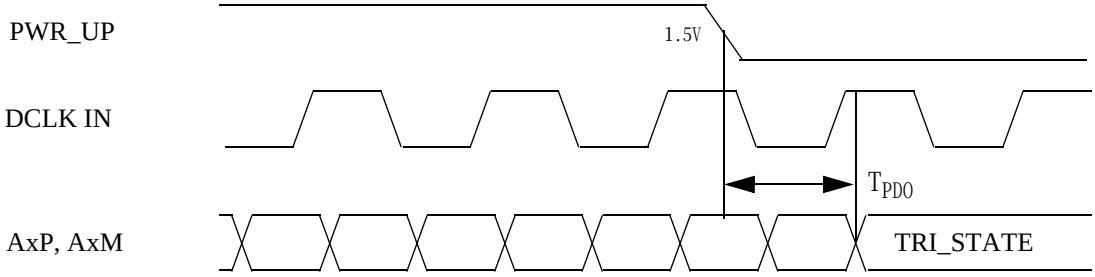


Figure 2-9 Power Down Delay Timing Definition



2.6 LVDS Outputs / TTL Data Inputs Mapping

The LVDS Clock waveshape is shown in the following figure. Note that the rising edge of the LVDS clock occurs two LVDS sub symbols before the current cycle of data. The clock is composed of a 4 LVDS sub symbol HIGH time and a 3 LVDS sub symbol LOW time.

The respective pin names are shown in the figure and these names are not the color mapping information but pin names only. Input B17 and B27 are double wide bits. The DE signal is mapped to two LVDS sub symbols and two LVDS clocks are provided for the backward compatibility. Also, there are two reserved bits and their corresponding receiver outputs has to be left open.

1

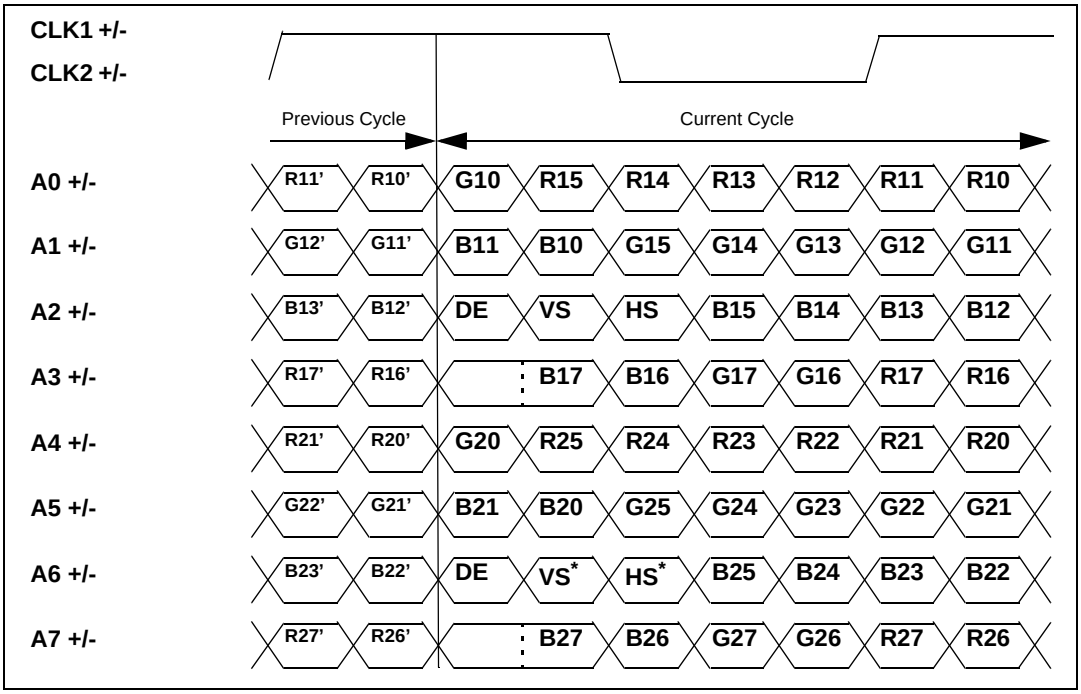


Figure 2-10 LVDS Outputs / TTL Inputs Data Mapping

NOTES:
1. * means "valid for the new design (contact sales for more details)"

2.7 Functional Descriptions

The EP387A is designed to reject cycle-to-cycle jitter which may be seen at the input clock. Very low cycle-to-cycle jitter is passed on to the transmitter outputs. This significantly reduces the impact of jitter provided by the input clock source and improve the accuracy of data sampling.

The EP387A offers the programmable edge data strobes selection for convenient interface with a variety of the graphic controllers. The different edge strobe can be programmed for rising edge strobe or falling edge strobe through a dedicated pin. A rising edge strobed transmitter will inter-operate with a falling edge receiver without any translation logic.

Pre-emphasis adds extra current during LVDS logic transition to reduce the additional cable loading effects. Pre-emphasis strength is set via a DC voltage level applied from min to max (0.75V to VCC) at the "PRE" pin. A higher input voltage on the "PRE" pin increases the magnitude of the dynamic current during data transition. The "PRE" pin requires one external pull-up resistor to VCC in order to set the expected DC level. There is an internal resistor network, which cause a voltage drop. Refer to the following table to set the expected voltage level.

Table 2-4 Pre-emphasis DC Voltage Level Setting

External Resistor in PRE	Resulting Voltage	Effects
1M-ohm or NC	0.75V	Standard LVDS
50k-ohm	1.0V	
9k-ohm	1.5V	50% pre-emphasis
3k-ohm	2.0V	
1K-ohm	2.6V	
100 ohm	VCC	100% pre-emphasis

The EP387A can be configured to different operating modes:

1. Dual pixel input, Dual LVDS output
2. Single pixel input, Single LVDS output
3. Single pixel input, Dual LVDS output

The first "dual-in, dual-out" mode can be selected by applying VCC to the control pin "DUAL". In dual mode, the transmitter outputs two LVDS clock in order to drive the traditional single-channel receiver.

The second "single-in, single-out" mode can be selected by applying GND to the control pin "DUAL". In single mode, the LVDS output data pairs "A4" to "A7" and the LVDS clock pairs "CLK2" are disabled to reduce the power dissipation.

The third "single-in, dual-out" mode can be selected by applying 1/2VCC (1.65V) level to the control pin "DUAL". In this mode, the input signals are splitted into odd and even pixel starting with the odd (first) pixel outputs to "A0" -- "A3" pairs and the next even (second) pixel outputs to "A4" -- "A7" pairs. The splitting of the data signals also starts with DE (Data Enable) transitioning from logic LOW to HIGH indicating active data. The "R_FDE" pin must be set high in this case. The number of clock cycles during blanking time must be EVEN number.

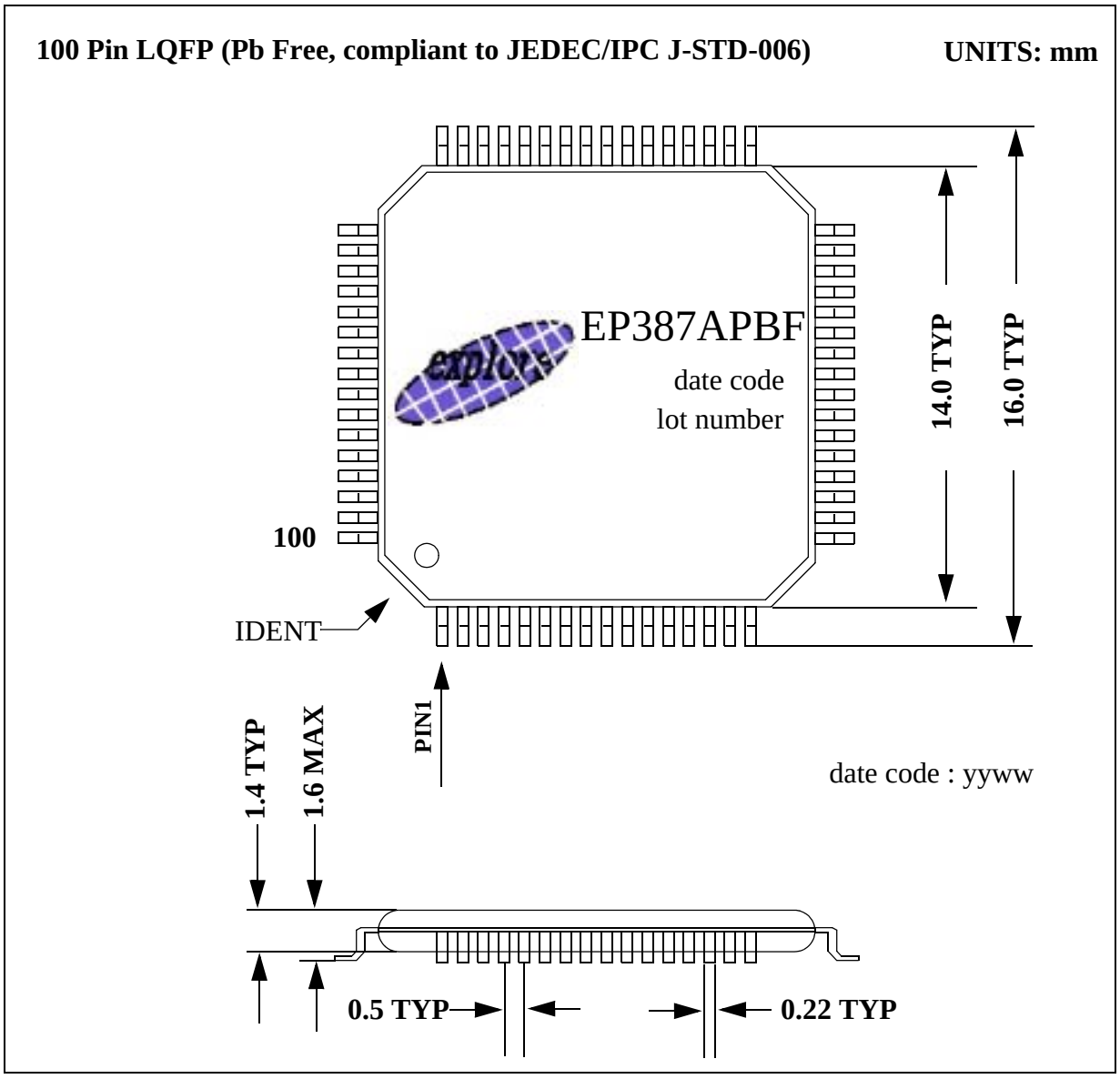
The following table provides the summary of the possible operating modes:

Table 2-5 Summary of the Operating Mode Configuration

Pin	Condition	Operating Mode
R_FB	R_FB = Vcc	Rising Edge Input Data Strobe
	R_FB = GND	Falling Edge Input Data Strobe
R_FDE	R_FDE = Vcc	Active data DE = HIGH
	R_FDE = GND	Active data DE = LOW
DUAL	DUAL = Vcc	Dual pixel Input, Dual LVDS Output
	DUAL = GND	Single pixel Input, Single LVDS Output
	DUAL = 1/2 Vcc	Single pixel Input, Dual LVDS Output

The transmitter provides the power down feature in order to save the total system power. When the power down feature enabled, the current draw from the supply pins is minimized and the PLLs are shut down. The LVDS outputs are tri-stated. This feature is enabled by setting the PWR_UP pin to LOW. This pin should be driven HIGH to enable the device once applied VCC is stable.

2.8 Package


100 Pin LQFP (Pb Free, compliant to JEDEC/IPC J-STD-006)
UNITS: mm
EP387APBF
date code
lot number
14.0 TYP
16.0 TYP
100
IDENT
PIN1
1.4 TYP
1.6 MAX
date code : yyww
0.5 TYP
0.22 TYP

User Guide End Sheet

FINAL PAGE OF
20
PAGES