# THOMSON COMPOSANTS MILITAIRES ET SPATIAUX

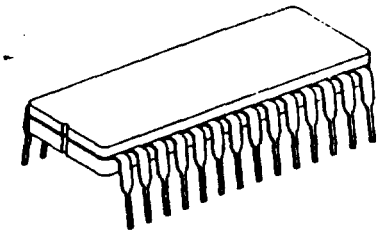
# EF 6840

## NMOS PROGRAMMABLE TIMER MODULE (PTM)

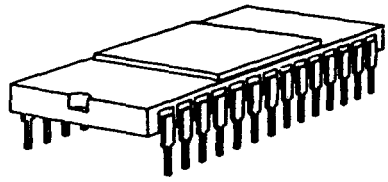
### DESCRIPTION

The EF 6840 is a programmable subsystem component of the 6800 family designed to provide variable system time intervals.

The EF 6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The EF 6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for squatre wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.



**J suffix**
**DIL 28**
Cerdip package



**C suffix**
**DIL 28**
Ceramic Side Brazed package

**E suffix**
**LCCC 28**
Leadless Ceramic Chip Carrier package

See the ordering information page 21.

Pin connection : see page 20.

### MAIN FEATURES

- Operates from a single 5 V power supply.
- Fully TTL compatible.
- Single system clock required (enable).
- Selectable prescaler on timer 3 capable of 4 MHz for the EF 6840, 6 MHz for the EF 68A40 and 8 MHz for the EF 68B40.
- Programmable interrupts ($\overline{IRQ}$) output to MPU.
- Readable down counter indicates counts to go to time-out.
- Selectable gating for frequency or pulse-width comparison.
- RESET input.
- Three asynchronous external clock and gate/trigger inputs internally synchronized.
- Three maskable outputs.
- Three available versions :
  EF 6840 (1.0 MHz),
  EF 68A40 (1.5 MHz),
  EF 68B40 (2 MHz) - (0°C to +70°C only).

### SCREENING / QUALITY

This product is manufactured in full compliance with either :

- MIL-STD-883 (class B).
- NFC 96863 class G.
- or according to TMS standards.



THCSS00157

## SUMMARY

## A - GENERAL DESCRIPTION

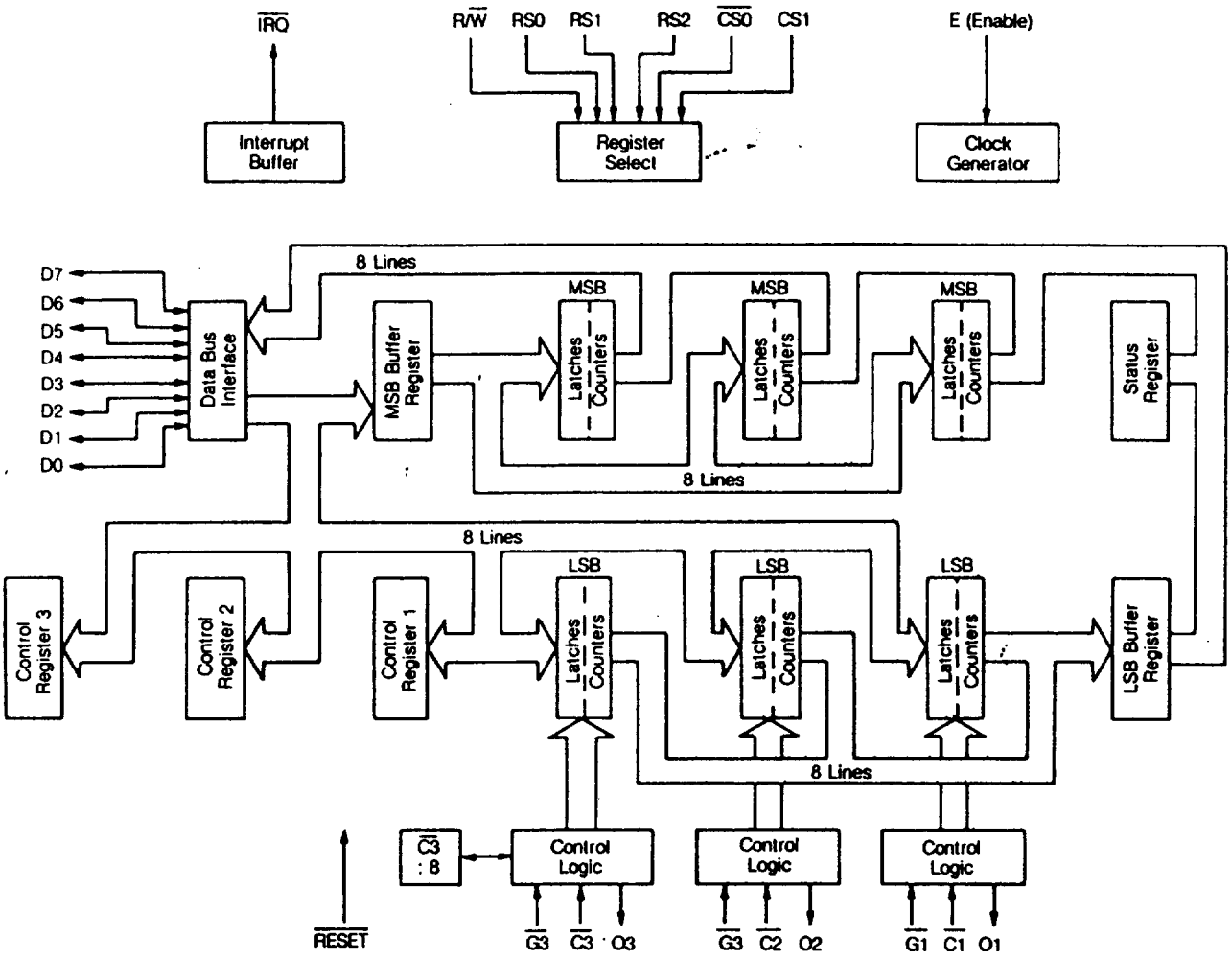



**Figure 1 : Block diagram.**

# B - DETAILED SPECIFICATIONS

## 1 - SCOPE

This drawing describes the specific requirements for the peripherals EF 6840, 1, 1.5 and 2 MHz, in compliance either with MIL-STD-883 class B and TMS standards.

## 2 - APPLICABLE DOCUMENTS

### 2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics
2) MIL-M-38510 : general specifications for microcircuits

## 3 - REQUIREMENTS

### 3.1 - *General*

The microcircuits are in accordance with the applicable document and as specified herein.

### 3.2 - Design and construction

#### *3.2.1 - Terminal connections*

Depending on the package, the terminal connections shall be is shown in § 10.1 and § 10.2.

#### *3.2.2 - Lead material and finish*

Lead material and finish shall be any option of MIL-M-38510 except finish C (as described in 3.5.6.1 of 38510).

#### *3.2.3 - Package*

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-M-38510 appendix C (when defined) :

- 28 leads - DIL Ceramic Side Brazed
- 28 leads - DIL Ceramic Cerdip
- 28 leads - LCCC leadless Ceramic Chip Carrier

The precise case outlines are described on § 9.

### 3.3 - Electrical characteristics

#### *3.3.1 - Absolute maximum ratings (see Table 1)*

**Table 1**

| Symbol | Parameter | | Test conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | −0.3 | +7.0 | V |
| $V_I$ | Input voltage | | | −0.3 | +7.0 | V |
| $P_{dmax}$ | Max Power dissipation | | $T_{case}$ = −55°C | | 0.7 | W |
| | | | $T_{case}$ = +125°C | | 0.4 | W |
| $T_{case}$ | Operating temperature | M suffix : EF 6840/EF 68A40 | f = 1 and 1.5 MHz | −55 | +125 | °C |
| | | V suffix : EF 6840/EF 68A40 | f = 1 and 1.5 MHz | −40 | +85 | °C |
| | | No suffix : EF 6840/EF 68A40/EF 68B40 | f = 1, 1.5 and 2 MHz | 0 | +70 | °C |
| $T_{stg}$ | Storage temperature | | | −55 | +150 | °C |
| $T_j$ | Junction temperature | | | | +160 | °C |
| $T_{leads}$ | Lead temperature | | Max 5 sec. soldering | | +270 | °C |

**Note** : This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{CC}$).

### 3.4 · Thermal characteristics (at 25°C)

Table 2

| Package | Symbol | Parameter | Value | Unit |
|---|---|---|---|---|
| DIL 28 | $\theta_{JA}$ | Thermal resistance · Ceramic junction to ambient | 56 | °C/W |
| | $\theta_{JC}$ | Thermal resistance · Ceramic junction to case | 10 | °C/W |
| LCCC 28 | $\theta_{JA}$ | Thermal resistance · Ceramic junction to ambient | 86 | °C/W |
| | $\theta_{JC}$ | Thermal resistance · Ceramic junction to case | 10 | °C/W |

**Power considerations**

The average chip-junction temperature, $T_J$, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

$T_A$ = Ambient Temperature, °C

$\theta_{JA}$ = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

The total thermal resistance of a package ($\theta_{JA}$) can be separated into two components, $\theta_{JC}$ and $\theta_{CA}$, representing the barrier to heat flow from the semiconductor junction to the package (case), surface ($\theta_{JC}$) and from the case to the outside ambient ($\theta_{CA}$). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

$\theta_{JC}$ is device related and cannot be influenced by the user. However, $\theta_{CA}$ is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce $\theta_{CA}$ so that $\theta_{JA}$ approximately equals $\theta_{JC}$. Substitution of $\theta_{JC}$ for $\theta_{JA}$ in equation (1) will result in a lower semiconductor junction temperature.

### 3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

### 3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

***3.6.1 · Thomson logo***

***3.6.2 · Manufacturer's part number***

***3.6.3 · Class B identification***

***3.6.4 · Date-code of inspection lot***

***3.6.5 · ESD identifier if available***

***3.6.6 · Country of manufacturing***

## 4 · QUALITY CONFORMANCE INSPECTION

### 4.1 · MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

## 5 - ELECTRICAL CHARACTERISTICS

### 5.1 - General requirements

All static and dynamic electrical characteristics specified. For inspection purpose, refer to relevant specification :

Table 3 : Static electrical characteristics for all electrical variants. See § 5.2.

Tables 4, 5 : Dynamic electrical characteristics. See § 5.3.

For static characteristics, test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to loading network in § 5.4.

### 5.2 - Static characteristics

**Table 3**

$V_{CC}$ = 5.0 $V_{dc}$ ±5% ; $V_{SS}$ = 0 $V_{dc}$ ; $T_C$ = −55°C / +125°C or −40°C / +85°C or 0°C / +70°C
(See Figures 2 and 6)

| Symbol | Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | $V_{SS}$ + 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input low voltage | | $V_{SS}$ − 0.3 | | $V_{SS}$ + 0.8 | V |
| $I_{in}$ | Input leakage current ($V_{in}$ = 0 to 5.25 V) | | | 1.0 | 2.5 | µA |
| $I_{TSI}$ | Hi-Z (off state) input current ($V_{in}$ = 0.5 to 2.4 V) | D0-D7 | | 2.0 | 10 | µA |
| $V_{OH}$ | Output high voltage<br>($I_{load}$ = −205µA)<br>($I_{load}$ = −200µA) | <br>D0-D7<br>Other outputs | <br>$V_{SS}$ + 2.4<br>$V_{SS}$ + 2.4 | | | V |
| $V_{OL}$ | Output low voltage<br>($I_{load}$ = 1.6 mA)<br>($I_{load}$ = 3.2 mA) | <br>$\overline{IRQ}$, D0-D7<br>O1-O3 | | | <br>$V_{SS}$ + 0.4<br>$V_{SS}$ + 0.4 | V |
| $I_{LOH}$ | Output leakage current (off state) ($V_{OH}$ = 2.4 V) | $\overline{IRQ}$ | | 1.0 | 10 | µA |
| $P_{INT}$ | Internal power dissipation (measured at $T_A$ = $T_L$) | | | 470 | 700 | mW |
| $C_{in}$ | Input capacitance<br>($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | <br>D0-D7<br>All others | | | <br>12.5<br>7.5 | <br>pF<br>pF |
| $C_{out}$ | Output capacitance<br>($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | <br>$\overline{IRQ}$<br>O1, O2, O3 | | | <br>5.0<br>10 | <br>pF<br>pF |

### 5.3 - Dynamic (switching) characteristics

The limits and values given in this section apply over the full case temperature range −55°C to +125°C or 0°C to +70°C and $V_{CC}$ in the range 4.75 V to 5.25 V $V_{IL}$ = 0.8 V and $V_{IH}$ = 2.0 V.

Table 4 - **AC operating characteristics** - (See Figures 3 and 8)

| Symbol | Characteristic | EF 6840 | | EF 68A40 | | EF 68B40 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_r$, $t_f$ | Input rise and fall times (Figures 3 and 4) $\overline{C}$, $\overline{G}$, and $\overline{RESET}$ | | 1.0* | | 0.666* | | 0.500* | µs |
| $PW_L$ | Input pulse width low (Figure 3) (Asychronous input) $\overline{C}$, $\overline{G}$, $\overline{RESET}$ | $t_{cycE} + t_{su} + t_{hd}$ | | $t_{cycE} + t_{su} + t_{hd}$ | | $t_{cycE} + t_{su} + t_{hd}$ | | ns |
| $PW_H$ | Input pulse width high (Figure 4) (Asychronous input) C, G | $t_{cycE} + t_{su} + t_{hd}$ | | $t_{cycE} + t_{su} + t_{hd}$ | | $t_{cycE} + t_{su} + t_{hd}$ | | ns |
| $t_{su}$ | Input setup time (Figure 5) (Synchronous input) $\overline{C}$, $\overline{G}$, and $\overline{RESET}$ | 200 | | 120 | | 75 | | ns |
| $t_{hd}$ | Input hold time (Figure 5) (Synchronous input) $\overline{C}$, $\overline{G}$, and $\overline{RESET}$ | 50 | | 50 | | 50 | | ns |
| $t_{sync}$ | Input synchronization time (Figure 8) $\overline{C3}$ (–8 prescaler mode only) | 250 | | 200 | | 175 | | ns |
| $PW_L$, $PW_H$ | Input pulse width $\overline{C3}$ (–8 prescaler mode only) | 120 | | 80 | | 60 | | ns |
| $t_{co}$ | Output delay, O1, O3 (Figure 6) ($V_{OH}$ = 2.4 V, load B) TTL | | 700 | | 460 | | 340 | ns |
| $t_{cm}$ | ($V_{OH}$ = 2.4 V, load D) MOS | | 450 | | 450 | | 340 | ns |
| $t_{cmos}$ | ($V_{OH}$ = 0.7 $V_{DD}$, load D) CMOS | | 2.0 | | 1.35 | | 1.0 | µs |
| $t_{IR}$ | Interrupt release time | | 1.2 | | 0.9 | | 0.7 | µs |

* $t_r$ and $t_f \leq t_{cycE}$

Table 5 - **Bus timing characteristics** - see Notes 1, 2 and 3

| Ident. Number | Symbol | Characteristic | EF 6840 | | EF 68A40 | | EF 68B40 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | $t_{cyc}$ | Cycle time | 1.0 | 10 | 0.67 | 10 | 0.5 | 10 | µs |
| 2 | $PW_{EL}$ | Pulse width, E low | 430 | 9500 | 280 | 9500 | 210 | 9500 | ns |
| 3 | $PW_{EH}$ | Pulse width, E high | 450 | 9500 | 280 | 9500 | 220 | 9500 | ns |
| 4 | $t_r$, $t_f$ | Clock rise and fall time | | 25 | | 25 | | 20 | ns |
| 9 | $t_{AH}$ | Address hold time | 10 | | 10 | | 10 | | ns |
| 13 | $t_{AS}$ | Address setup time before E | 80 | | 60 | | 40 | | ns |
| 14 | $t_{CS}$ | Chip select setup time before E | 80 | | 60 | | 40 | | ns |
| 15 | $t_{CH}$ | Chip select hold time | 10 | | 10 | | 10 | | ns |
| 18 | $t_{DHR}$ | Read data hold time | 20 | 50* | 20 | 50* | 20 | 50* | ns |
| 21 | $t_{DHW}$ | Write data hold time | 10 | | 10 | | 10 | | ns |
| 30 | $t_{DDR}$ | Peripheral output data delay time | | 290 | | 180 | | 150 | ns |
| 31 | $t_{DSW}$ | Peripheral input data setup time | 165 | | 80 | | 60 | | ns |

* The data bus output buffers are not longer sourcing or sinking current by $t_{DHR}$ max (high impedance).

**Note 1**: Not all signals are applicable to every part.

**Note 2**: Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.

**Note 3**: Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

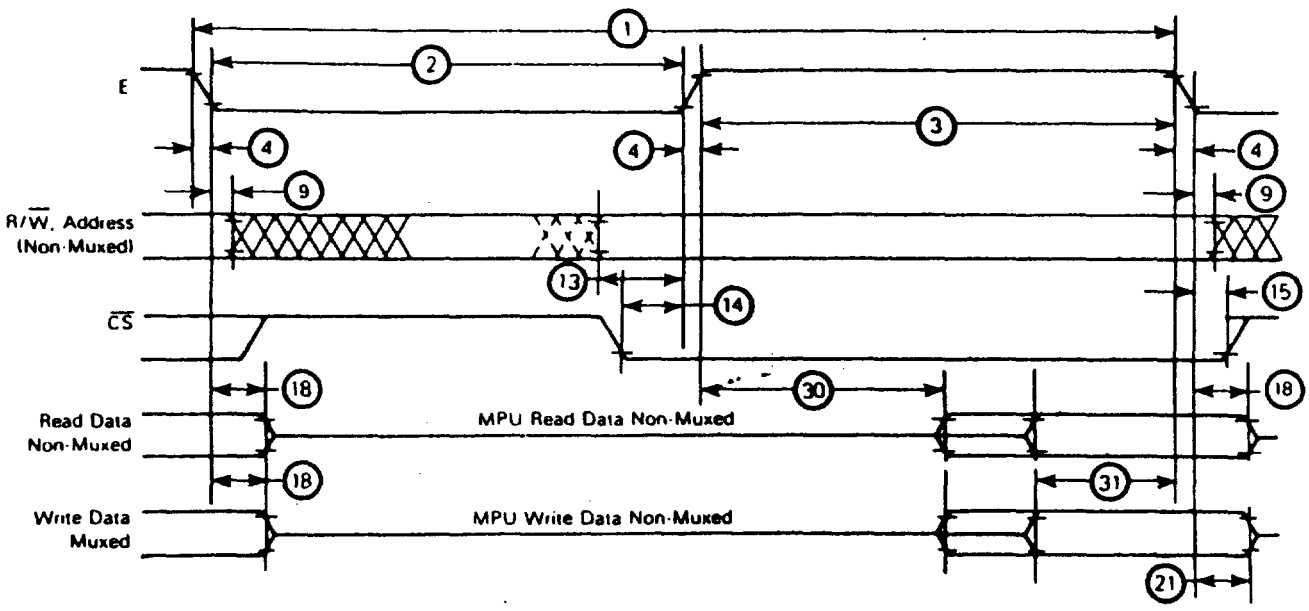



Figure 2 : Bus timing.

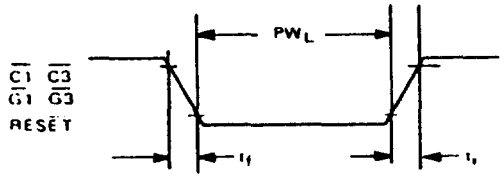



Figure 3 : Input pulse width low.

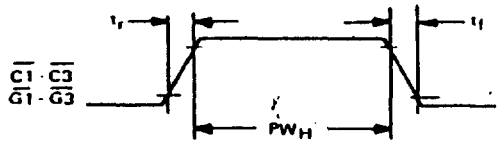



Figure 4 : Input pulse width high.

NOTES
1 Not all signals are applicable to every part
2 Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified
3 Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified

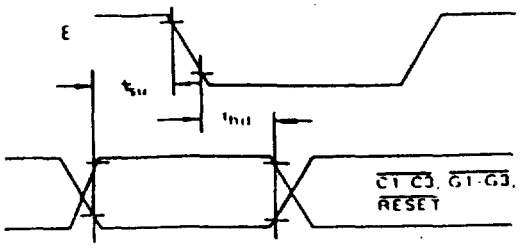



Figure 5 : Input setup and hold times.

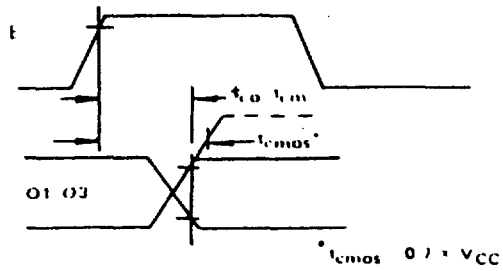



Figure 6 : Output delay.

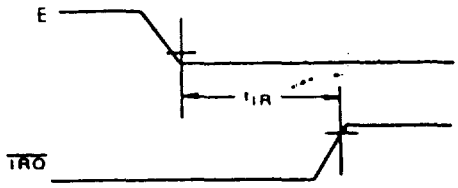



Figure 7 : IRQ release time.

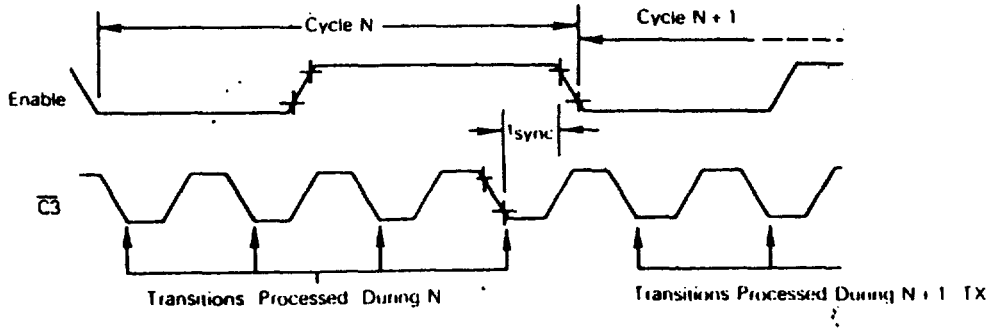
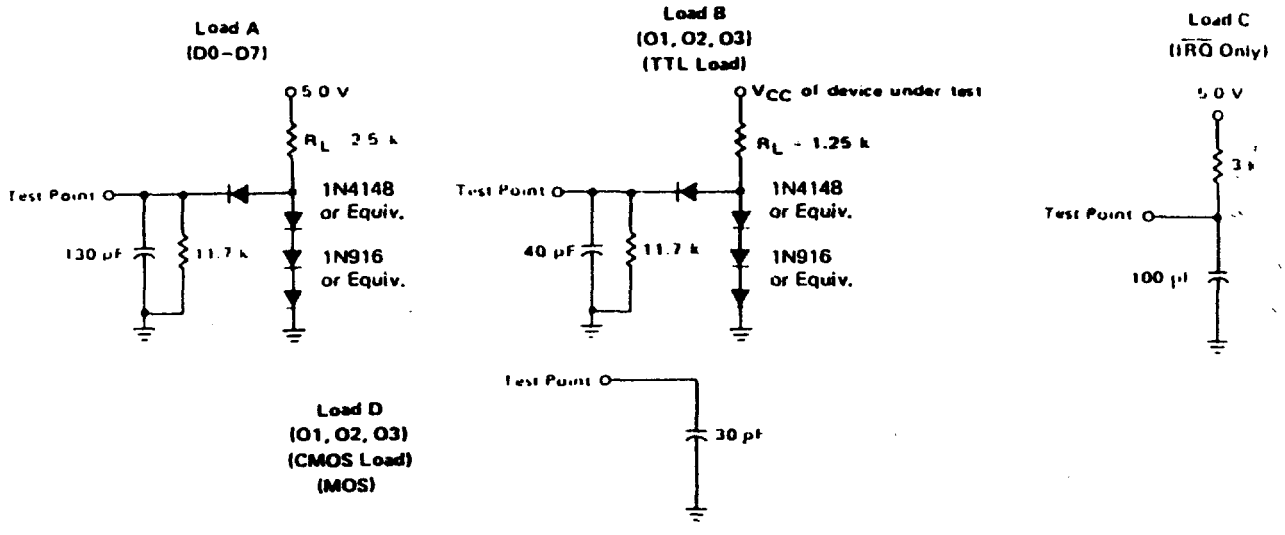



Figure 8 : $\overline{C3}$ input synchronization time (÷8 prescaler mode only).

### 5.4 - Test conditions specific to the device

#### *5.4.1 - Loading network*

Figure 9 here below shows the loading network applicable to the timing tables.




NOTE Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

Figure 9 : Bus timing test loads.

## 6 · FUNCTIONAL DESCRIPTION

### 6.1 · Device operation

The EF 6840 is part of the 6800 micoprocessor family and is fully bus compatible with 6800 systems. The three timers in the EF 6840 operate independently and in several distinct modes to fit a wide variety of measurement and systhesis applications.

The EF 6840 is an integrated set of three distinct counter/timers (Figure 1). It consists of three 16-bit data latches, three 16-bit counters (clocked independently), and the comparison and enable cicuitry necessary to implement various measurement and synthesis functions. In addition, it contains interrupt drivers to alert the processor that a particular function has been completed.

In a typical application, a timer will be loaded by first storing two bytes of data into an associated counter latch. This data is then transferred into the counter via a counter initialization cycle. If the counter is enabled, the counter decrements on each subsequent clock period which may be an external clock, or Enable (E) until one of several predetermined conditions causes it to halt or recycle. The timers are thus programmable, cyclic in nature, controllable by external inputs or the MPU program, and accessible by the MPU at any time.

#### BUS INTERFACE

The programmable timer module (PTM) interfaces to the EF 6800 bus with an 8-bit bidirectional data bus, two chip select lines, a read/write line, a clock (Enable) line, and interrupt request line, an external reset line, and three register select lines. VMA should be utilized in conjunction with an MPU address line into a chip select of the PTM when using the EF 6800/6802.

#### BIDIRECTIONAL DATA (D0-D7)

The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and PTM. The data bus output drivers are three-state devices which remain in the high-impedance (off) state except when the MPU performs a PTM read operation (read/write and enable lines high and PTM chip selects activated).

#### CHIP SELECT ($\overline{CS0}$, CS1)

These two signals are used to activate the data bus interface and allow transfer of data from the PTM. With $\overline{CS0}$ = 0 and CS1 = 1, the device is selected and data transfer will occur.

#### READ/WRITE (R/$\overline{W}$)

This signal is generated by the MPU to control the direction of data transfer on the data bus. With the PTM selected, a low state on the PTM R/$\overline{W}$ line enables the input buffers and data is transferred from the MPU to the PTM on the trailing edge of the E (enable) clock. Alternately, (under the same conditions) R/W = 1 and enable high allows data in the PTM to be read by the MPU.

#### ENABLE (E CLOCK)

The E clock signal synchronizes data transfer between the MPU and the PTM. It also performs an équivalent synchronization function on the external clock, reset, and gate inputs of the PTM.

#### INTERRUPT REQUEST ($\overline{IRQ}$)

The active low interrupt request signal is normally tied directly (or through priority interrupt circuitry) to the $\overline{IRQ}$ input of the MPU. This is an «open drain» output (no load device on the chip) which permits other similar interrupt request lines to be tied together in a wire-OR configuration.

The $\overline{IRQ}$ line is activated if, and only if, the composite interrupt flag (bit 7 of the internal status register) is asserted. The conditions under which the $\overline{IRQ}$ line is activated are discussed in conjunction with the status register.

#### $\overline{RESET}$

A low level at this input is clocked into the PTM by the E (enable) input. Two enable pulses are required to sycnhronize and process the signal. The PTM then recognizes the active «low» or iniactive «high» on the third enable pulse. If the $\overline{RESET}$ signal is asynchronous, an additional enable period is required if setup times are not met. The $\overline{RESET}$ input must be stable high/low for the minimum time stated in the AC operating characteristics.

Recognition of a low level at this input by the PTM causes the following action to occur :

a. All counter latches are preset to their maximum count values.

b. All control register bits are cleared with the exception of CR10 (internal reset bit) which is set.

c. All counters are preset to the contents of the latches.

d. All counter outputs are reset and all counter clocks are disabled.

e. All status register bits (interrupt flags (are cleared).

#### REGISTER SELECT LINES (RS0, RS1, RS2)

These inputs are used in conjunction with the R/$\overline{W}$ line to select the internal registers, counters and latches as shown in Table 6.

**Note** : The PTM is accessed via MPU load and store operations in much the same manner as a memory device. The instructions available with the 6800 family of MPUs which perform read-modify-write operations on memory should not be used when the PTM is accessed. These instructions actually fetch a byte from memory, perform an operation, then restore it to the same address location. Since the PTM uses the R/$\overline{W}$ line as an additional register select input, the modified data will not be restored to the same register if these instructions are used.

## CONTROL REGISTER

Each timer in the EF 6840 has a corresponding write-only control register. Control register = 2 has a unique address space (RS0 = 1, RS = 0, RS2 = 0) and therrefore may be written into at any time. The remaining control registers (= 1 and = 3) share the address space selected by a logic zero on all register select inputs.

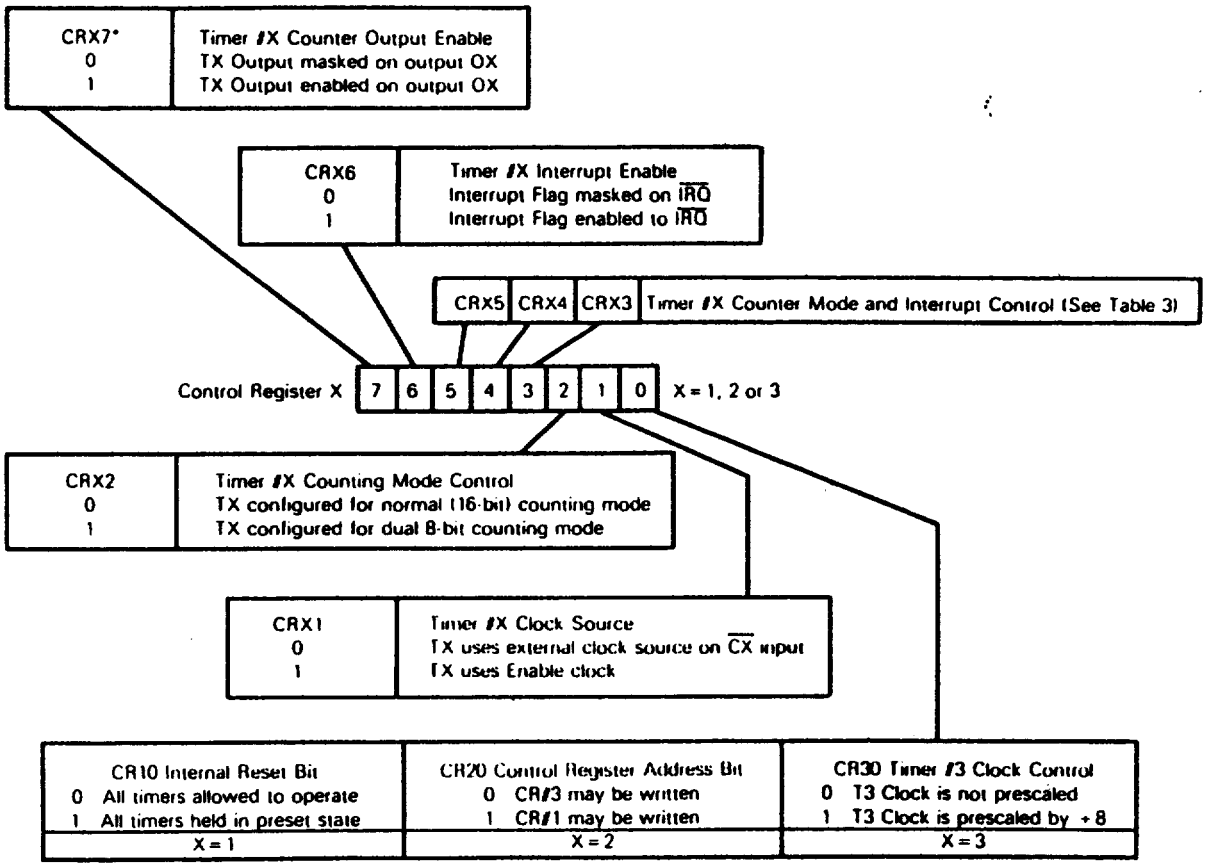
### CR20

The lesat-significant bit of control register = 2 (CR20) is used as an additional addressing bit for control registers = 1 and = 3. Thus, with all register selects and R/W inputs at logic zero, control register = 1 will be written into if CR20 is a logic one. Under the same conditions, control register = 3 can also be written into after a RESET low condition has occurred, since all control register bits (except CR10) are cleared. Therefore, one may write in the sequence CR3, CR2, CR1.

**Table 6 - Register selection**

| Register Select Inputs | | | Operations | |
|---|---|---|---|---|
| RS2 | RS1 | RS0 | R/$\overline{W}$ = 0 | R/$\overline{W}$ = 1 |
| 0 | 0 | 0 | CR20 = 0 Write Control Register #3<br>CR20 = 1 Write Control Register #1 | No Operation |
| 0 | 0 | 1 | Write Control Register #2 | Read Status Register |
| 0 | 1 | 0 | Write MSB Buffer Register | Read Timer #1 Counter |
| 0 | 1 | 1 | Write Timer #1 Latches | Read LSB Buffer Register |
| 1 | 0 | 0 | Write MSB Buffer Register | Read Timer #2 Counter |
| 1 | 0 | 1 | Write Timer #2 Latches | Read LSB Buffer Register |
| 1 | 1 | 0 | Write MSB Buffer Register | Read Timer #3 Counter |
| 1 | 1 | 1 | Write Timer #3 Latches | Read LSB Buffer Register |

**Table 7 - Control register bits**



### CR10

The least significant bit of control register = 1 is used as an internal reset bit. When this bit is a logic zero, all timers are allowed to operate in the modes prescribed by the remaining bits of the control registers. Wrinting a «one» into CR10 causes all counters to be preset with the contents of the corresponding counter latches, all counter clocks to be disabled, and the timer outputs and interrupt flags (status register) to be reset. Counter latches and control registers are undisturbed by an internal reset and may be written into regardless of the state of CR10.

The least significant bit of control register = 3 is used as a selector for a : 8 prescaler which is available with timer = 3 only. The prescaler, if selected, is effectively placed between the clock input circuitry and the input to counter = 3. It can therefore be used with either the internal clock (enable) or an external clock source.

Note : When initializing timer 3 into the divide-by-eight mode on consecutive E-cycles (i.e., with DMA), control register 3 must be initialized after timer latch = 3 to insure proper timer initialization.

### CR30

The functions depicted in the foregoing discussions are tabulated in Table 7 for ease of reference.

Control register bits CR10, CR20, and CR30 are unique in that each selects a different function. The remaining bits (1 through 7) of each control register select common functions, with a particular control register affecting only its corresponding timer.

### CRX1

Bit 1 of control register = 1 (CR11) selects whether an internal or external clock source is to be used with timer = 1. Similarly, CR21 selects the clock source for timer = 2, and CR31 performs this function for timer = 3. The function of each bit of control register «X» can therefore be defined as shown in the remaining section of Table 7.

### CRX2

Control register bit 2 selects whether the binary information contained in the counter latches (and subsequently loaded into the counter) is to be treated as a single 16-bit word or two 8-bit bytes. In the single 16-bit counter modes (CRX2 = 0) the counter will decrement to zero after N + 1 enabled (G = 0) clock periods, where N is defined as the 16-bit number in the counter latches. With CRX2 = 1, a similar time out will occur after (L + 1) • (M + 1) enabled clock periods, where L and M, respectively, refer to the LSB and MSB bytes in the counter latches.

### CRX3-CRX7

Control register bits 3, 4 and 5 are explained in detail in the timer operating mode section. Bit 6 is an interrupt mask bit which will be explained more fully in conjunction with the status register, and bit 7 is used to enable the corresponding timer ouput. A summary of the control register programming modes i shown in Table 8.

### STATUS REGISTER/INTERRUPT FLAGS

The EF 6840 has an internal read-only status register which contains four interrupt flags. (The remaining four bits of the register are not used, and defaults to zeros when being read). Bits 0, 1 and 2 are assigned to timers 1, 2 and 3, respectively, as individual flag bits, while bit 7 is a composite interrupt flag. This flag bit will be asserted if any of the individual flag bits is set while bit 6 of the corresponding control register is at a logic one. The conditions for asserting the composite interrupt flag bit can therefore be expressed as :

$I,TY = I1 \cdot CR16 + I2 \cdot CR26 + I3 \cdot CR36$

where INT = Composite interrupt flag (bit 7)
I1 = timer = 1 interrupt flag (bit 0)
I2 = timer = 2 interrupt flag (bit 1)
I3 = timer = 3 interrupt flag (bit 2)

An interrupt flag is cleared by a timer reset condition, i.e., external $\overline{RESET}$ = 0 or internal reset bit (CR10) = 1. It will also be cleared by a read timer counter command provided that the status register has previously been read while the interupt flag was set. This condition on the read status register-read timer counter (RS-RT) sequence is designed to prevent missing interrupts which might occur after the status register is read, but prior to reading the timer counter.

An individual interrupt flag is also cleared by a write timer latches (W) command or a counter initialization (CI) sequence, provided that W or CI affects the timer corresponding to the individual interrupt flag.

**Table 8 - PTM operating mode selection**

| CRX3 | CRX4 | CRX5 | |
|---|---|---|---|
| 0 | 0 | 0 | Continuous Operating Mode: Gate 1 or Write to Latches or Reset Causes Counter Initialization |
| 1 | 0 | 0 | Frequency Comparison Mode: Interrupt If Gate ⎍ is < Counter Time Out |
| 0 | 1 | 0 | Continuous Operating Mode: Gate 1 or Reset Causes Counter Initialization |
| 1 | 1 | 0 | Pulse Width Comparison Mode: Interrupt if Gate ⎍ is < Counter Time Out |
| 0 | 0 | 1 | Single Shot Mode: Gate 1 or Write to Latches or Reset Causes Counter Initialization |
| 1 | 0 | 1 | Frequency Comparison Mode: Interrupt If Gate ⎍ is > Counter Time Out |
| 0 | 1 | 1 | Single Shot Mode: Gate 1 or Reset Causes Counter Initialization |
| 1 | 1 | 1 | Pulse Width Comparison Mode: Interrupt If Gate ⎍ is > Counter Time Out |

### COUNTER LATCH INITIALIZATION

Each of the three independent timers consists of a 16-bit addressable counter and a 16-bit addressable latch. The counters are preset to the binary numbers stored in the latches. Counter initialization results in the transfer of the latch contents to the counter. See notes in Table 9 regarding the binary number N, L, or M placed into the latches and their relationship to the output waveforms and counter time-outs.

Since the PTM data bus is 8-bits wide and the counters are 16-bits wide, a temporary register (MSB buffer register) is provided. This «write only» register is for the most-significant-byte of the desired latch data. Three addresses are provided for the MSB buffer register (as indicated in Table 6), but they all lead to the same buffer. Data from the MSB buffer will automatically be transferred into the most-significant byte of timer = X when a write timer = X latches command is performed. So it can be seen that the EF 6840 has been designed to allow transfer fo two bytes of data into the counter latches provided that the MSB is transferred first. The storage order must be observed to ensure proper latch operation.

In many applications, the source of the data will be a 6800 family MPU. It should be noted that the 16-bit store operations of the 6800 family microprocessors (STS and STX) transfer data in the order required by the PTM. A store index register instruction, for example, results in the MSB of the X register being transferred to the selected address, then the LSB of the X register being written into the next higher location. Thus, either the index register or stack pointer may be transferrred directly into a selected counter latch with a single instruction.

A logic zero at the $\overline{\text{RESET}}$ input also initializes the counter latches. In this case, all latches will assume a maximum count of $65{,}535_{10}$. It is important to note that an internal reset (bit zero of control register 1 set) has no effect on the counter latches.

### COUNTER INITIALIZATION

Counter initialization is defined as the transfer of data from the latches to the counter with subsequent clearing of the individual interrupt flag associated with the counter. Counter initialization always occurs when a reset condition ($\overline{\text{RESET}}$ = 0 or CR10 = 1) is recognized. It can also occur - depending on timer mode - with a write timer latches command or recognition of a negative transition of the gate input.

Counter recycling or re-intialization occurs when a negative transition of the clock input is recognized after the counter has reached an all-zero state. In this case, data is transferred from the latches to the counter.

### ASYNCHRONOUS INPUT/OUTPUT LINES

Each of the three timers within the PTM has external clock and gate inputs as elle a counter output line. The inputs are high-impedance, TTL-compatible lines and outputs are capable of driving two standard TTL loads.

### CLOCK INPUTS ($\overline{C1}$, $\overline{C2}$ and $\overline{C3}$)

Input pins $\overline{C1}$, $\overline{C2}$ and $\overline{C3}$ will accept asynchronous TTL voltage level signals to decrement timers 1, 2, and 3, respectively. The high and low levels of the external clocks must each be stable for at least one system clock period plus the sum of the setup and hold times for the clock inputs. The asynchronous clock rate can vary from dc to the limit imposed by the enable clock setup, and hold times.

The external clock inputs are clocked in by enable pulses. Three enable periods are used to synchronize and process the external clock. The fourth enable pulse decrements the internal counter. This does not affect the input frequency, it merely creates a delay betweet a clock input transition and internal recognition of that transition by the PTM. All references to C inputs in this document relate to internal recognition of the input transition. Note that a clock high or low level which does not meet setup and hold time specifications may require an additional enable pulse for recognition. When observing recurring events, a lack of synchronization will result in «jitter» being observed on the output of the PTM when using asynchronous clocks and gate input signals. There are two types of jitter. «System jitter» is the result of the input signals being out of synchronization with enable, permitting signals with marginal setup and hold time to be recognized by either the bit time nearest the input transition or the subsequent bit time.

«Input jitter» can be as great as the time between input signal negative going transitions plus the system jitter, if the first transition is recognized during one system cycle, and not recognized the next cycle, or vice versa. See Figure 10.

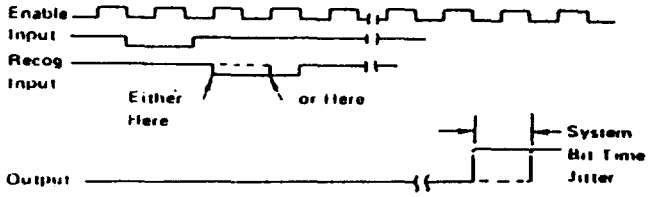



**Figure 10 :** Input jitter.

### CLOCK INPUT $\overline{C3}$ (: 8 PRESCALER MODE)

External clock input $\overline{C3}$ represents a special cas when timer = 3 is programmed to utilize its optional : 8 prescaler mode.

The divide-by-8 prescaler contains an asynchronous ripple counter ; thus, input setup ($t_{su}$) and hold times ($t_{hd}$) do not apply. As long as minimum input pulse widths are maintained, the counter will recognize and process all input clock ($\overline{C3}$) transitions. However, in order to guarantee that a clock transition is processed during the current E cycle, a certain amount of synchronization time ($t_{sync}$) is required between the $\overline{C3}$ transition and the falling edge of enable (see Figure 8). If the synchronization time requirement is not met, it is possible that the $\overline{C3}$ transition will not be processed until the following E cycle.

The maximum input frequency and allowable duty cycles for the : 8 prescaler mode are specified under the AC operating characterisitcs. Internally, the : 8 prescaler output is treated in the same manner as the previously discussed clock inputs.

### GATE INPUTS ($\overline{G1}$, $\overline{G2}$, $\overline{G3}$)

Input pins $\overline{G1}$, $\overline{G2}$, and $\overline{G3}$ accept asynchronous TTL-compatible signals which are used as triggers or clock gating functions to timers, 1, 2, and 3, respectively. The gating inputs are clocked into the PTM by the E (enable) clock in the same manner as the previously discussed clock inputs. That is, a gate transition is recognized by the PTM on the fourth enable pulse (provided setup and hold time requirements are met), and the high or low levels of the gate input must be stable for at least one system clock period plus the sum of setup and hold times. All references to G transistion in this document relate to internal recognition of the input transition.

The gate inputs of all timers directly affect the internal 16-bit counter. The operation of $\overline{G3}$ is therefore independent of the : 8 prescaler selection.

### TIMER OUTPUTS (O1, O2, O3)

Timer outputs O1, O2, and O3 are capable of driving up to two TTL loads and produce a defined output waveform for either continuous or single-shot timer modes. Output waveform definition is accomplished by selecting either single 16-bit or dual 8-bit operating modes. The single 16-bit mode will produce a square-wave output in the continuous mode and a single pulse in the single-shot mode. The dual 8-bit mode will produce a variable duty cycle pulse in both the continuous and single-shot timer modes. One bit of each control register (CRX7) is used to enable the corresponding output. If this bit is cleared, the output will remain low ($V_{OL}$) regardless of the operating mode. If it is cleared while the ouput is high the output will go low during the first enable cycle following a write to the control register.

The continuous and single-shot timer modes are the only ones for which output response is defined in this data sheet. Refer to the programmable timer fundamentals and applications manual for a discussion of the output signals in other modes. Signals appear at the outputs (unless CRX7 = 0) during frequency and pulse width comparison modes, but the actual waveform is not predictable in typical applications.

### TIMER OPERATING MODES

The EF 6840 has been designed to operate effectively in a wide variety of applications. This is accomplished by using three bits of each control register (CRX3, CRX4, and CRX5) to define different operating modes of the timers. These modes are divided into WAVE SYNTHESIS and WAVE MEASUREMENT modes, and are outlined in Table 9.

One of the WAVE SYNTHESIS modes is the continuous operating mode, which is useful for cyclic wave generation. Either symmetrical or variable duty-cycle waves can be generated in this mode. The other wave synthesis mode, the single-shot mode, is similar in use to the continuous operating mode, however, a single pulse is generated, with a programmable preset width.

The WAVE MEASUREMENT modes include the frequency comparison and pulse width comparison modes which are used to measure cyclic and singular pulse widths, respectively.

In addition to the four timer modes in table 9, the remaining control register bit is used to modify counter initialization and enabling or interrupt conditions.

**Table 9 - Operating modes**

| Control Register | | | Timer Operating Mode | |
|---|---|---|---|---|
| CRX3 | CRX4 | CRX5 | | |
| 0 | * | 0 | Continuous | Synthesizer |
| 0 | * | 1 | Single Shot | |
| 1 | 0 | * | Frequency Comparison | Measurement |
| 1 | 1 | * | Pulse Width Comparison | |

*Defines Additional Timer Function Selection

## WAVE SYNTHESIS MODES

### CONTINUOUS OPERATING MODE (Table 10)

The continuous mode will synthesize a continuous wave with a period proportional to the preset number in the particular timer latches. Any of the timers in the PTM may be programmed to operate in a continuous mode by writing zeroes into bits 3 and 5 of the corresponding control register. Assuming that the timer output is enabled (CRX7 = 1), either a square wave or a variable duty cycle waveform will be generated at the timer output, OX. The type of output is selected via control register bit 2.

Either a timer reset (CR10 = 1 or external reset = 0) condition or internal recognition of a negative transition of the gate input results in counter initialization. A write timer latches command can be selected as a counter initialization signal by clearing CRX4.

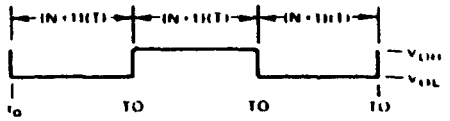
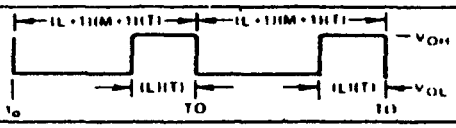
The counter is enabled by an absence of a timer reset condition and a logic zero at the gate input. In the 16-bit mode, the counter will decrement on the first clock cycle during or after the counter initialization cycle. It continues to decrement on each clock signal so long as G remains low and no reset condition exists. A counter time out (the first clock after all counter bits = 0) results in the individual interrupt flag being set and reinitialization of the counter.

In the dual 8-bit mode (CRX2 = 1) [refer to the example in Figure 9 and Tables 10 and 11] the MSB decrements once for every full countdown of the LSB + 1. When the LSB = 0, the MSB is unchanged; on the next clock pulse the LSB is reset to the count in the LSB latches, and the MSB is decremented by 1 (one). The output, if enabled, remains low during and after initialization and will remain low until the counter MSB is all zeroes. The output will go high at the beginning of the next clock pulse. The output remains high until both the LSB and MSB of the counter are all zeroes. At the beginning of the next clock pulse the defined time out (TO) will occur and the output will go low. In the dual 8-bit mode the period of the output of the example in Figure 11 would span 20 clock pulses as opposed to 1546 clock pulses using the normal 16-bit mode.

A special time-out condition exists for the dual 8-bit mode (CRX2 = 1) if L = 0. In this case, the counter will revert to a mode, similar to the single 16-bit mode except time out occurs after M + 1* clock pulses. The ouput, if enabled, goes low during the counter initialization cycle and reverses state at each time out. The counter remains cyclical (is re-initialized at each time out) and the individual interrupt flag is set when time out occurs. If M = L = 0, the internal counters do not change, but the output toggles at a rate of 1/2 the clock frequency.

The discussion of the continuous mode has assumed that the application requires an output signal. It should be noted that the timer operates in the same manner with the output disabled (CRX7 = 0). A read timer counter command is valid regardless of the state of CRX7.

*Table 10 - Continuous operating modes*

| Synthesis Modes | | CONTINUOUS MODE (CRX3 = 0, CRX5 = 0) | |
|---|---|---|---|
| Control Register | | Initialization/Output Waveforms | |
| CRX2 | CRX4 | Counter Initialization | *Timer Output (OX) (CRX7 = 1) |
| 0 | 0 | $\overline{G}_I$+W+R |  |
| 0 | 1 | $\overline{G}_I$+R | |
| 1 | 0 | $\overline{G}_I$+W+R |  |
| 1 | 1 | $\overline{G}_I$+R | |

### SINGLE-SHOT TIMER MODE

This mode is identical to the continuous mode with three exceptions. The first of these is obvious from the name-the output returns to a low level after the initial time out and remains low until another counter initialization cycle each occurs.

As indicated in Table 11, the internal counting mechanism remains cyclical in the single-shot mode. Each time out of the counter results in the setting of an individual interrupt flag and re-initialization of the counter.

The second major difference between the single-shot and continuous modes is that the internal counter enable is not dependent on the gate input level reamining in the low state for the single-shot mode.

Another special condition is introduced in the single-shot mode. If L = M = 0 (dual 8-bit) or N = 0 (single 16-bit), the output goes low on the first clock received during or after counter initialization. The output remains low until the operating mode is changed or nonzero data is written into the counter latches. Time outs continue to occur at the end of each clock period.

The three differences between single-shot and continous timer mode can be summarized as attributes of the single-shot ode :

1. Output is enabled for only one pulse until it is reinitialized.
2. Counter enable is independent of gate.
3. L = M = 0 or N = 0 disables output.

Aside from these differences, the two modes are identical.

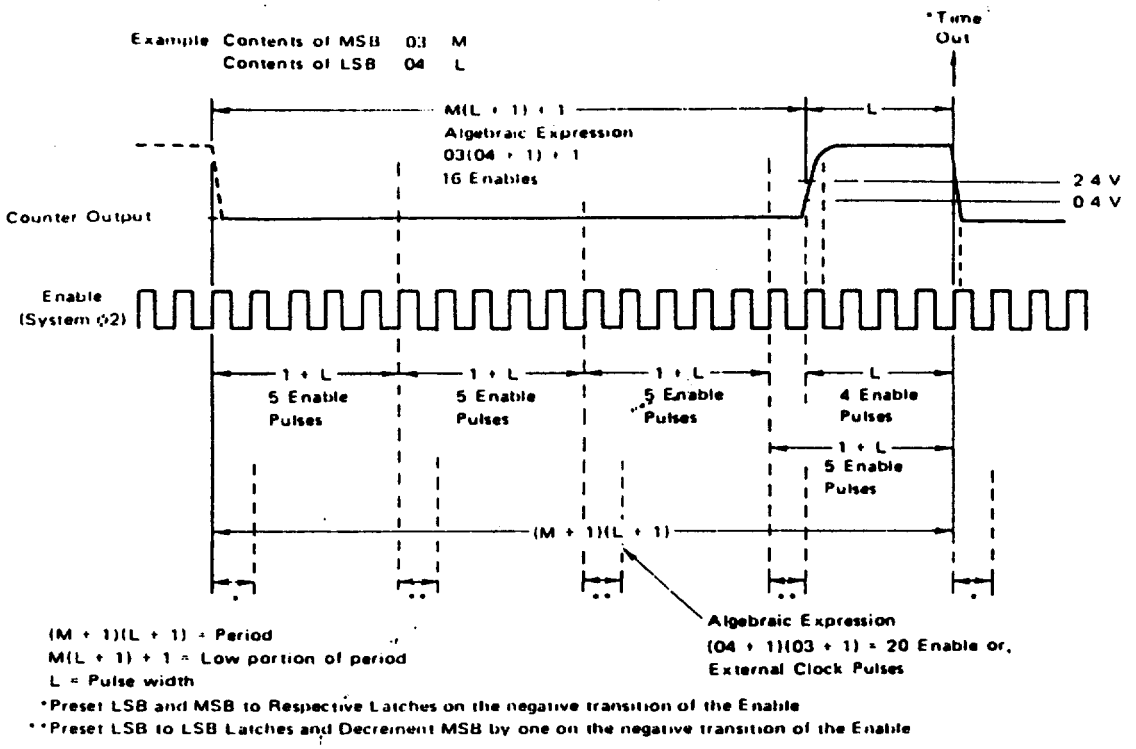
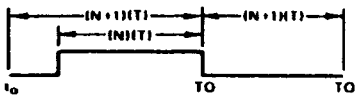
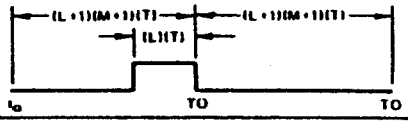



Figure 11 : Timer output waveform example (continuous dual 8-bit mode using internal enable).

**Table 11 - Single-shot operating modes**

| Synthesis Modes | | SINGLE-SHOT MODE (CRX3 = 0, CRX7 = 1, CRX5 = 1) | |
|---|---|---|---|
| Control Register | | Initialization/Output Waveforms | |
| CRX2 | CRX4 | Counter Initialization | Timer Output (OX) |
| 0 | 0 | $\overline{G}$↓+W+R |  |
| 0 | 1 | $\overline{G}$↓+R | |
| 1 | 0 | $\overline{G}$↓+W+R |  |
| 1 | 1 | $\overline{G}$↓+R | |



Symbols are as defined in Table 5.

## WAVE MEASUREMENT MODES

### TIME INTERVAL MODES

The time internal modes are the frequency (period) measurement and pulse width comparison modes, and are provided for those applications which require more flexibility of interrupt generation and counter initialization. Individual interrupt flags are set in these modes as a function of both counter time out and transitions of the $\overline{Gate}$ input. Counter initialization is also affected by interrupt flag status.

A timer's output is normally not used in a Wave Measurement mode, but it is defined. If the output is enabled, it will operate as follows. During the period between reinitialization of the time and the first time out, the output will be a logical zero. If the first time out is completed (regardless of its method of generation), the output will go high. If further TO's occur, the output will change state at each completion of a time-out.

The counter does operate in either single 26-bit or dual 8-bit modes as programmed by CRX2. Other features of the wave measurement modes are outlined in Table 12.

**Frequency comparison or period measurement mode (CRX3 = 1, CRX4 = 0)**

The frequency comparison mode with CRX5 = 1 is straightforward. If time out occurs prior to the first negative transition of the $\overline{Gate}$ input after a counter intialization cycle, an individual interrupt flag is set. The counter is disabled, and a counter initialization cycle cannot begin until the interrupt flag is cleared and a negative transition on $\overline{G}$ is detected.
If CRX5 = 0, as shown in Tables 12 and 13, an interrupt is generated if $\overline{Gate}$ input returns low prior to a time out. If a counter time out occurs first, the counter is recycled and continues to decrement. A bit is set within the timer on the initial time out which precludes further individual interrupt generation until a new counter initialization cycle has been completed. When this internal bit is set, a negative transition of the $\overline{Gate}$ input starts a new counter initialization cycle. (The condition of $\overline{GI} \bullet I \bullet \overline{TO}$ *is satisfied, since a time out has occured and no individual interrupt has been generated.*)
Any of the timers within the PTM may be programmed to compare the period of a pulse (giving the frequency after calculations) at the $\overline{Gate}$ input with the time period requested for counter time out. A negative transition of the $\overline{Gate}$ input enables the counter and starts a counter initialization cycle - provided that other conditions, as noted in Table 13, are satisfied. The counter decrements on each clock signal recognized during or after counter initialization until an interrupt is generated, a write timer latches command is issued, or a timer reset condition occurs. It can be seen from Table 13 that an interrupt condition will be generated if CRX5 = 0 and the period of the pulse (single pulse or measured separately repetitive pulses) at the gate input is less than the counter time out period. If CRX5 = 1, an interrupt is generated if the reverse is true.
Assume now with CRX5 = 1 that a counter initialization has occured and that the gate input has returned low prior to counter time out. Since there is no individual interrupt flag generated, this automatically starts a new counter initialization cycle. The process will continue with frequency comparison being performed on each gate input cycle until the mode is changed, or a cycle is determined to be above the predetermined limit.

**Pulse width comparison mode (CRX3 = 1, CRX4 = 1)**

This mode is similar to the frequency comparison mode except for a positive, rather than negative, transition of the gate input terminates the count. With CRX5 = 0, an individual interrupt flag will be generated if the zero level pulse applied to the gate input is less than the time period required for counter time out. With CRX5 = 1, the interrupt is generated when the reverse condition is true.
As can be seen in Table 13, a positive transition of the gate input disables the counter. With CRX5 = 0, it is therefore possible to directly obtain the width of any pulse causing an interrupt. Similar data for other time interval modes and conditions can be obtained, if two sections of the PTM are dedicated to the purpose.

Table 12 - Output delay

| CRX3 = 1 | | | |
|---|---|---|---|
| CRX4 | CRX5 | Application | Condition for Setting Individual Interrupt Flag |
| 0 | 0 | Frequency Comparison | Interrupt Generated if $\overline{Gate}$ Input Period (1/F) is less than Counter Time Out (TO) |
| 0 | 1 | Frequency Comparison | Interrupt Generated if $\overline{Gate}$ Input Period (1/F) is greater than Counter Time Out (TO) |
| 1 | 0 | Pulse Width Comparison | Interrupt Generated if $\overline{Gate}$ Input "Down Time" is less than Counter Time Out (TO) |
| 1 | 1 | Pulse Width Comparison | Interrupt Generated if $\overline{Gate}$ Input "Down Time" is greater than Counter Time Out (TO) |

Table 13 · Frequency comparison mode

| Mode | Bit 3 | Bit 4 | Control Reg. Bit 5 | Counter Initialization | Counter Enable Flip-Flop Set (CE) | Counter Enable Flip-Flop Reset (CE) | Interrupt Flag Set (I) |
|---|---|---|---|---|---|---|---|
| Frequency | 1 | 0 | 0 | $\overline{G}\downarrow \cdot I \pm (\overline{CE} + TO) + R$ | $\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$ | W • R • I | G↓ Before TO |
| Comparison | 1 | 0 | 1 | $\overline{G}\downarrow \cdot \overline{I} + R$ | $\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$ | W • R • I | TO Before $\overline{G}\downarrow$ |
| Pulse width | 1 | 1 | 0 | $\overline{G}\downarrow \cdot \overline{I} + R$ | $\overline{G}\downarrow \overline{W} \cdot \overline{R} \cdot \overline{I}$ | W • R • I • G | $\overline{G}\uparrow$ Before TO |
| Comparison | 1 | 1 | 1 | $\overline{G}\downarrow \cdot \overline{I} + \overline{R}$ | $\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$ | W • R • I • G | $\overline{G}\uparrow$ Before TO |

$\overline{G}\downarrow$ = Negative transition of $\overline{Gate}$ input.
W = Write Timer Latches Command.
R = Timer Reset (CR10 = 1 or External $\overline{RESET}$ = 0).
N = 16-Bit Number in Counter Latch.
TO = Counter Time Out (All Zero Condition).
I = Interrupt for a given timer.

* All time intervals shown above assume the Gate ($\overline{G}$) and Clock ($\overline{C}$) signals are synchronized to the system clock. (E) with the specified setup and hold time requirements.

## 7 · PREPARATION FOR DELIVERY

### 7.1 · Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

### 7.2 · Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

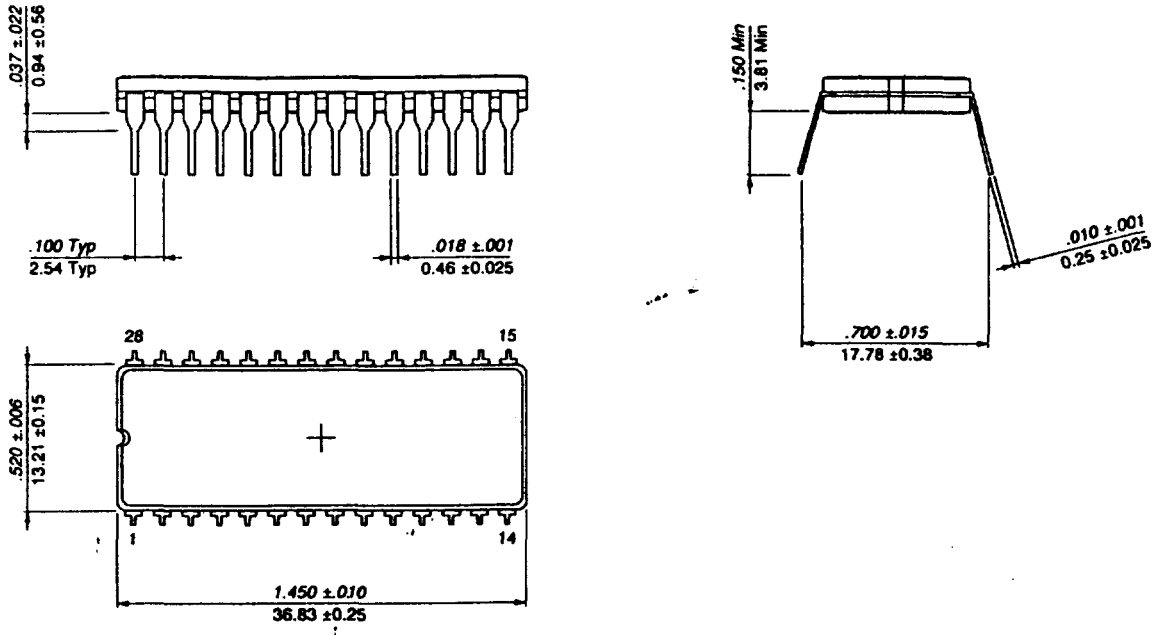
## 8 · HANDLING

MOS device must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

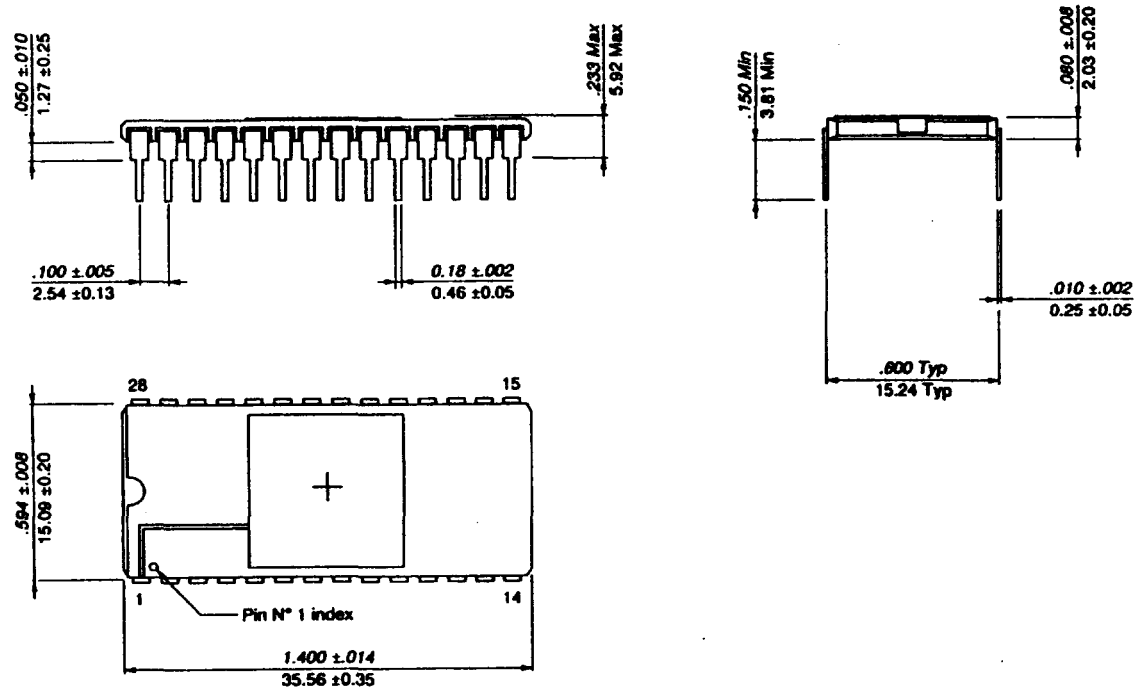
a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 %, if pratical.

## 9 - PACKAGE MECHANICAL DATA

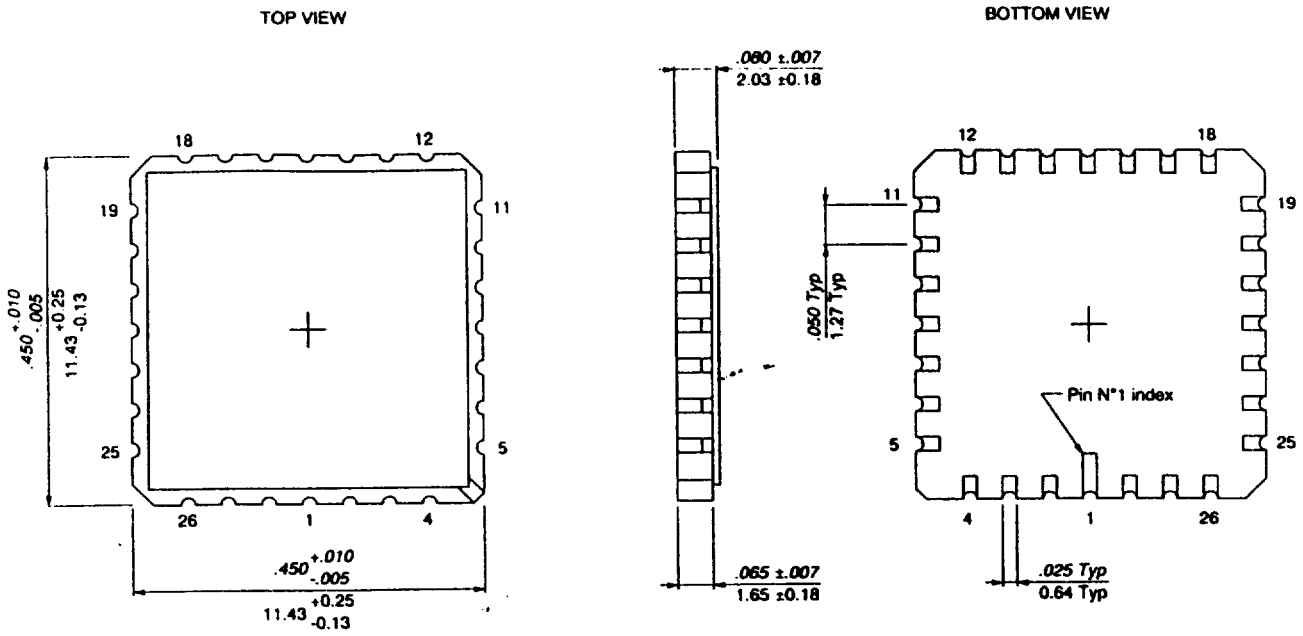
### 9.1 - 28 pins - DIL Ceramic Side Brazed Package




### 9.2 - 28 pins - DIL Cerdip Package

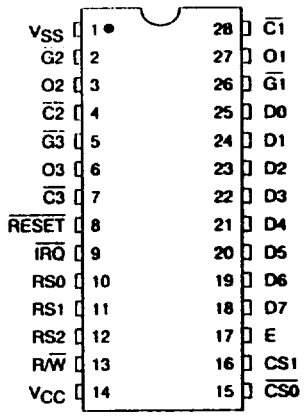


### 9.3 · 28 pins · Leadless Ceramic Chip Carrier

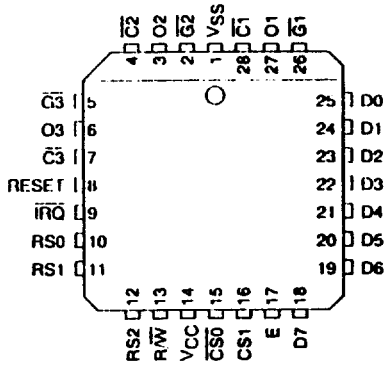



## 10 · TERMINAL CONNECTIONS

### 10.1 · 28 pins · Pin assignment (DIL)




### 10.2 · 28 pins · Leadless Ceramic Chip Carrier (LCCC)



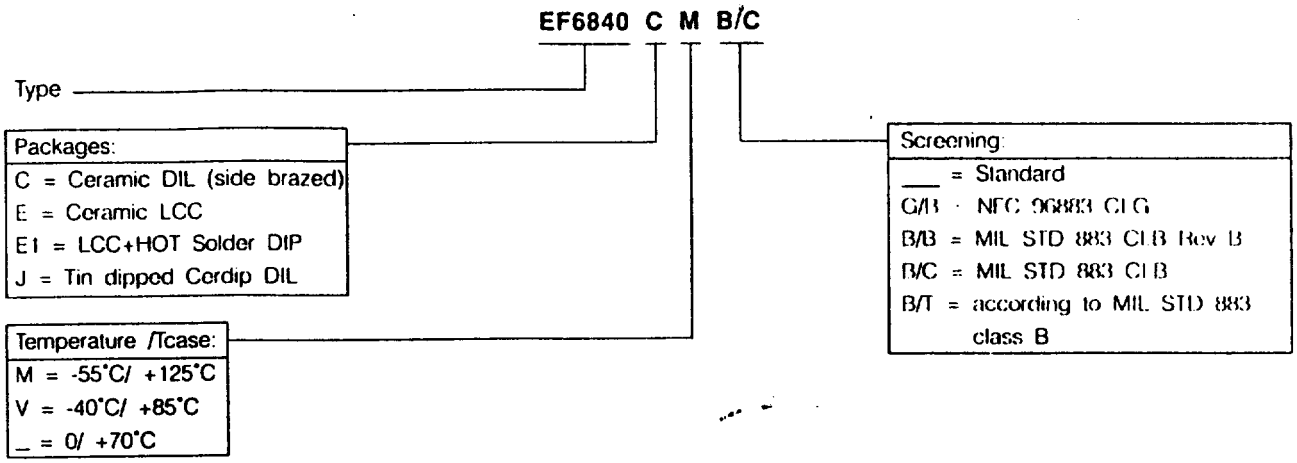
## 11 · ORDERING INFORMATION

### 11.1 · Hi-REL product

| Commercial TMS Part-Number (see Note) | Norms | Package | Temperature range $T_C$ (°C) | Frequency (MHz) | Drawing number |
|---|---|---|---|---|---|
| EF6840JMG/B | NFC 96863 class G | DIL Cerdip | −55 / +125 | 1 | Data sheet |
| EF6840CMG/B | NFC 96863 class G | DIL Side Brazed | −55 / +125 | 1 | Data sheet |
| EF6840EMG/B | NFC 96863 class G | LCCC | −55 / +125 | 1 | Data sheet |
| EF68A40JMG/B | NFC 96863 class G | DIL Cerdip | −55 / +125 | 1.5 | Data sheet |
| EF68A40CMG/B | NFC 96863 class G | DIL Side Brazed | −55 / +125 | 1.5 | Data sheet |
| EF68A40EMG/B | NFC 96863 class G | LCCC | −55 / +125 | 1.5 | Data sheet |
| EF6840JMB/C | MIL-STD-883 class B | DIL Cerdip | −55 / +125 | 1 | Data sheet |
| EF6840CMB/C | MIL-STD-883 class B | DIL Side Brazed | −55 / +125 | 1 | Data sheet |
| EF6840E1MB/C | MIL-STD-883 class B | LCCC | −55 / +125 | 1 | Data sheet |
| EF68A40JMB/C | MIL-STD-883 class B | DIL Cerdip | −55 / +125 | 1.5 | Data sheet |
| EF68A40C1MB/C | MIL-STD-883 class B | DIL Side Brazed | −55 / +125 | 1.5 | Data sheet |
| EF68A40EMB/T | According to MIL-STD-883 class B | LCCC | −55 / +125 | 1.5 | Data sheet |
| **Note :** THOMSON COMPOSANTS MILITAIRES ET SPATIAUX. | | | | | |

### 11.2 · Standard product

| Commercial TMS Part-Number (see Note) | Norms | Package | Temperature range $T_C$ (°C) | Frequency (MHz) | Drawing number |
|---|---|---|---|---|---|
| EF6840CV | TMS standard | DIL Side Brazed | −40 / +85 | 1 | Data sheet |
| EF6840JV | TMS standard | DIL Cerdip | −40 / +85 | 1 | Data sheet |
| EF68A40CV | TMS standard | DIL Side Brazed | −40 / +85 | 1.5 | Data sheet |
| EF68A40JV | TMS standard | DIL Cerdip | −40 / +85 | 1.5 | Data sheet |
| EF6840JM | TMS standard | DIL Cerdip | −55 / +125 | 1 | Data sheet |
| EF6840CM | TMS standard | DIL Side Brazed | −55 / +125 | 1 | Data sheet |
| EF6840EM | TMS standard | LCCC | −55 / +125 | 1 | Data sheet |
| EF68A40JM | TMS standard | DIL Cerdip | −55 / +125 | 1.5 | Data sheet |
| EF68A40CM | TMS standard | DIL Side Brazed | −55 / +125 | 1.5 | Data sheet |
| EF68A40EM | TMS standard | LCCC | −55 / +125 | 1.5 | Data sheet |
| EF6840C | TMS standard | DIL Side Brazed | 0 / +70 | 1 | Data sheet |
| EF6840J | TMS standard | DIL Cerdip | 0 / +70 | 1 | Data sheet |
| EF68A40C | TMS standard | DIL Side Brazed | 0 / +70 | 1.5 | Data sheet |
| EF68B40J | TMS standard | DIL Cerdip | 0 / +70 | 2 | Data sheet |
| **Note :** THOMSON COMPOSANTS MILITAIRES ET SPATIAUX. | | | | | |


EF6840 C M B/C
Type
Packages:
C = Ceramic DIL (side brazed)
E = Ceramic LCC
E1 = LCC+HOT Solder DIP
J = Tin dipped Cerdip DIL
Temperature /Tcase:
M = -55°C/ +125°C
V = -40°C/ +85°C
_ = 0/ +70°C
Screening:
___ = Standard
G/B = NFC 96883 Cl G
B/B = MIL STD 883 Cl B Rev B
B/C = MIL STD 883 Cl B
B/T = according to MIL STD 883 class B

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