Product Specification

27C1024

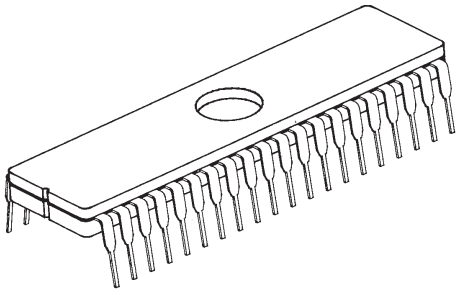
1024 K (64 K X 16) CMOS UV ERASABLE AND OTP ROM PROM

DESCRIPTION

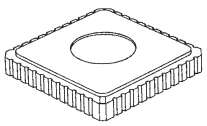
The 27C1024 is a 1,048,576-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 16 bits. The 27C1024 with its single + 5 V power supply and with an access time of 80 ns, is ideal for use in 16 bit microprocessor system allowing full speed operation without WAIT states. In high performance CPU's (10 MHz), the 27C1024 has an important feature which is to separate the output control, Output Enable (OE) from the Chip Enable control (CE). The OE control eliminates bus contention in multiple bus microprocessor systems. The 27C1024 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 40 mA while the maximum standby current is only 0.2 mA. The standby mode is achieved by applying a TTL-high signal to the CE input. The 27C1024 enables implementation of new, advanced systems with firmware intensive architectures.

The combination of the 27C1024s high density, and new advanced microprocessors having mega-bit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The 27C1024 large storage capability enables it to function as a high density software carrier. The 27C1024 has an «Electronic Signature» that allows programmers to automatically identify device type and pinout.

PACKAGE DIMENSIONS



Q suffix
40 pins CERDIP



EQ suffix
44 pins LCCC

MAIN FEATURES

- Very fast access time : 90 ns.
- Compatible to high speed microprocessors zero wait state.
- Low «CMOS» consumption :
  active current : 40 mA max.
  standby current : 0.2 mA max.
- Programming voltage : 12.5 V.
- Electronic signature for automated programming.
- Programming time in the 6 seconds range (presto II algorithm).
- 40/44 pins JEDEC approved pin-out.
- Power supply : V_{CC} = 5 V_{DC} ± 10 %.
- Military temperature range : T_C = −55, +125°C.

SCREENING / QUALITY

This product is manufactured according to :

- MIL–STD–883 QML
- TCS Standard
- DSCC drawing 5962–86805

January 2000

SUMMARY

A - GENERAL DESCRIPTION

INTRODUCTION

The 27C1024 series are 1,048 576-bit, ultraviolet-light, erasable, electrically programmable read-only memories. These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The 27C1024 is pin compatible with existing 40-pin ROMs and EPROMs. It is offered in both dual-in-line and leadless chip carrier ceramic package (Q and EQ suffix) rated for operation from $-55°C$ to $+125°C$.

Since these EPROMs operate from a single 5 V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming but all programming signals are TTL level.

There are seven modes of operation for the 27C1024. Read mode requires a single 5 V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

The 27C1024 has a standby mode that reduces the maximum power dissipation. But in this case the read access of the memory is not possible.

Maximum operating power dissipation : 500 mW at 5 V.

Maximum standby power dissipation : 1 mW at 5 V.

This memory has static operation : no clocks no refresh.

This memory is fully compatible with TTL families S, LS, AS, ALS.

1 - DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

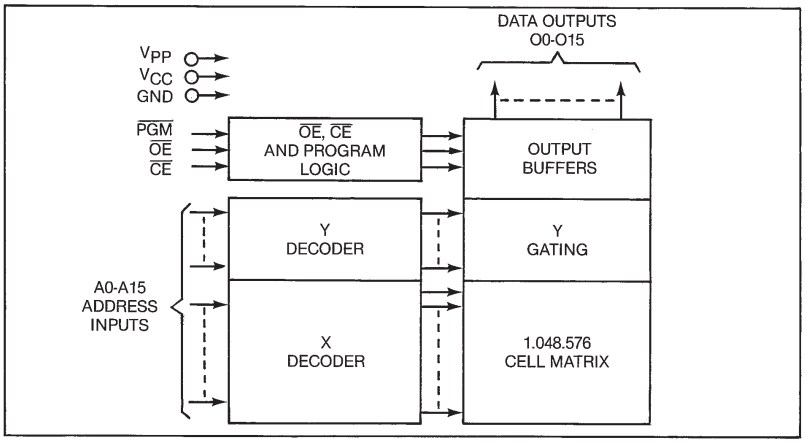
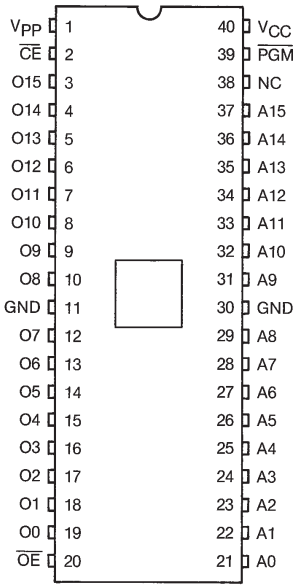


FIGURE 1 - 27C1024 BLOCK DIAGRAM.

2 - PIN ASSIGNEMENTS

CERDIP PACKAGE



LCCC PACKAGE

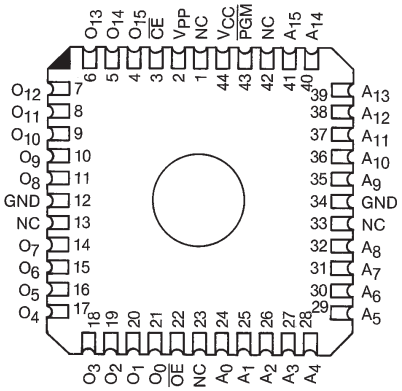


FIGURE 2 - PIN CONFIGURATION.

3 - TERMINAL DESIGNATIONS

The function and relevant symbol of each terminal of the device are given in the Figure 3 below.

PIN FUNCTIONS

A0-A15	Address Input
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program
O0-O15	Data Input / Output
NC	No Connected

FIGURE 3

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the CMOS UV erasable PROM memories 27C1024, in compliance either with MIL-STD-883 class B ı

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : Test methods and procedures for electronics
2) MIL-PRF-38535 : Integrated circuits (micro-circuits) manufacturing.

3 – REQUIREMENTS

3.1 – General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 – Design and construction

3.2.1 – Terminal connections

Depending on the package, the terminal connections shall be is shown in figure 2.

3.2.2 – Lead material and finish

Lead material and finish shall be any option of MIL–STD–1835 tin dipped.

3.2.3 – Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL–STD–1835 :
– 40 lead DIL, Dual In Line,
– 44 lead LCCC.
The precise case outlines are described into MIL–STD–1835, and also §9.

3.3 Electrical characteristics

3.3.1 – Absolute maximum ratings (Table 1)

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.
If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 1 – Absolute maximum ratings
Unless otherwise stated, all voltages are referenced to the reference terminal as defined in Figure 3.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	–0.6	7	V
V_{PP}	Programming supply voltage	–0.6	14	V
V_I	Input voltages (Except A9) (A9)	–0.6 –0.6	6.5 13.5	V V
V_O	Output voltages	–0.6	V_{CC} + 1	V
V_{OZ}	Off–state voltage	–0.6	V_{CC} + 1	V
I_O	Output curents		5	mA
I_I	Input currents		15	mA
P_D max.	Max. power–dissipation		250	mW
T_{stg}	Storage temperature	– 65	+ 150	°C
T_{lead}	Lead temperature (soldering : 10 s)		+ 300	°C

Note : Stresses above those listed under ”Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.3.2 – Recommended conditions of use and guaranteed characteristics

a) Guaranteed characteristics (Tables 4 and 5)

The characteristics associated to a specified meaxurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification in guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommanded operating ranges specified below.

b) Recommended conditions of use (Table 2)

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

The conditions shall not be for inspection purposes.

Some recommanded values may, however, be taken in other parts of this specification as detail conditions for an applicable test (Table 4).

All voltages are referenced to a reference terminal (V_{SS}, GND, etc...).

Table 2

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.5	5.5	V
V_{IL}	Low level input voltage	−0.1	0.8	V
V_{IH}	High level input voltage	2	V_{CC} +0.5	V
T_{case}	Operating temperature	−55	+125	°C

3.4 - Thermal characteristics

Table 3

Package	Symbol	Parameter	Value	Unit
CERDIP DIL 40		**Thermal resistance - Ceramic**		
	$\theta_{J\text{-}A}$	Junction-to-Ambient	45	°C/W
	$\theta_{J\text{-}C}$	Junction-to-Case	5	°C/W
LCCC 44		**Thermal resistance - Ceramic**		
	$\theta_{J\text{-}A}$	Junction-to-Ambient	50	°C/W
	$\theta_{J\text{-}C}$	Junction-to-Case	10	°C/W

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output

Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in «Thermal Resistance Measurement Method for EF 68xx Microcomponent Devices», and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - QML / MIL-STD-883

Is in accordance with MIL-PRF-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 4 : Static electrical characteristics for the electrical variants.
- Table 5 : Dynamic electrical characteristics.

For static characteristics (Table 4), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause § 5.4 of this specification (Table 5).

5.2 - Static characteristics

All voltages are referenced to GND.

Table 4 - Read mode DC characteristics Note 1

$-55°C \leqslant T_C \leqslant +125°C$ $V_{CC} = 5\ V \pm 10\ \%$

Symbol	Parameter	Test conditions	Min	Max	Unit
I_{LI}	Input leakage current	$0\ V \leqslant V_{IN} \leqslant V_{CC}$		± 10	μA
I_{LO}	Output leakage current	$0\ V \leqslant V_{OUT} \leqslant V_{CC}$		± 10	μA
I_{CC}	Supply current	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$, $I_{OUT} = 0\ mA$, $f = 5\ MHz$		40	mA
I_{CC1}	Supply current (standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply cuurent (standby) CMOS	$\overline{E} > V_{CC} - 0.2\ V$		200	μA
I_{PP}	Program current	$V_{PP} = V_{CC}$		100	μA
V_{IL}	Input low voltage		-0.3	0.8	V
V_{IH} Note 2	Input high voltage		2	$V_{CC} + 1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1\ mA$		0.45	V
V_{OH}	Output high voltage TTL	$I_{OH} = -400\ \mu A$	2.4		V
	Ouput high voltage CMOS	$I_{OH} = -100\ \mu A$	$V_{CC} - 0.7$		V

Note 1 : V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
Note 2 : Maximum DC voltage on output is $V_{CC} + 0.5$ V.

5.3 Dynamic characteristics

Table 5A – Read mode AC characteristics Note 1

–55°C ≤ Tc ≤ +125°C Vcc = 5 V ± 10 %

Symbol	Alt	Parameter	Test conditions	27C1024				Unit
				–90		–10		
				Min	**Max**	**Min**	**Max**	
t_{AVQV}	t_{ACC}	Address valid to output valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		90		100	ns
t_{ELQV}	t_{CE}	Chip enable low to output valid	$\overline{G} = V_{IL}$		90		100	ns
t_{GLQV}	t_{OE}	Output enable low to output valid	$\overline{E} = V_{IL}$		45		50	ns
t_{EHQZ} Note 2	t_{DF}	Chip enable high to output Hi–Z	$\overline{G} = V_{IL}$	0	30	0	30	ns
t_{GHQZ} Note 2	t_{DF}	Output enable high to output HI–Z	$\overline{E} = V_{IL}$	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address transition to output transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0	0	ns

Note 1 : V_{CC} must be appllied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
Note 2 : Sampled only, not 100 % tested.

Table 5B – Read mode AC characteristics Note 1

–55°C ≤ T_c ≤ +125°C V_{CC} = 5 V ± 10%

Symbol	Alt	Parameter	Test conditions	27C1024						Unit
				–12		–15		–20/–25		
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{AVQV}	t_{ACC}	Address valid to output valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		120		150		200	ns
t_{ELQV}	t_{CE}	Chip enable low to output valid	$\overline{G} = V_{IL}$		120		150		200	ns
t_{GLQV}	t_{OE}	Output enable low to output valid	$\overline{E} = V_{IL}$		60		60		70	ns
t_{EHQZ} Note 2	t_{DF}	Chip enable high to output Hi–Z	$\overline{G} = V_{IL}$	0	40	0	50	0	60	ns
t_{GHQZ} Note 2	t_{DF}	Output enable high to output HI–Z	$\overline{E} = V_{IL}$	0	40	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address transition to output transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Note 1 : V_{CC} must be appllied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
Note 2 : Sampled only, not 100 % tested.

5.4 - Test conditions specific to the device

Output load	1 TTL gate and CL = 100 pF
Input rise and fall times	⩽ 10 ns
Input pulse levels	0.45 V to 2.4 V
Timing measurement reference level inputs, outputs	0.8 V and 2 V

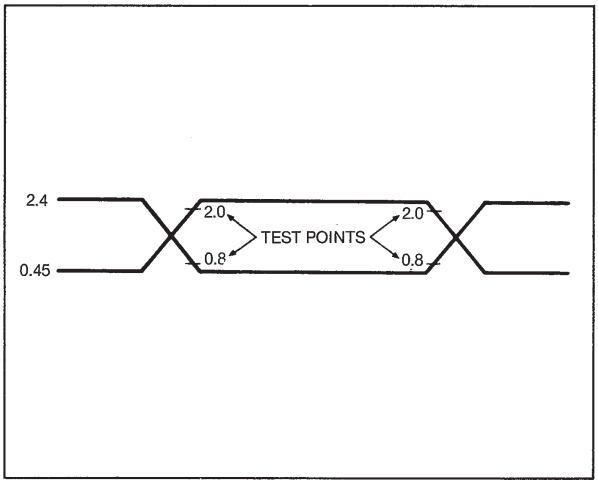


FIGURE 4 - AC TESTING INPUT / OUPUT WAVEFORM.

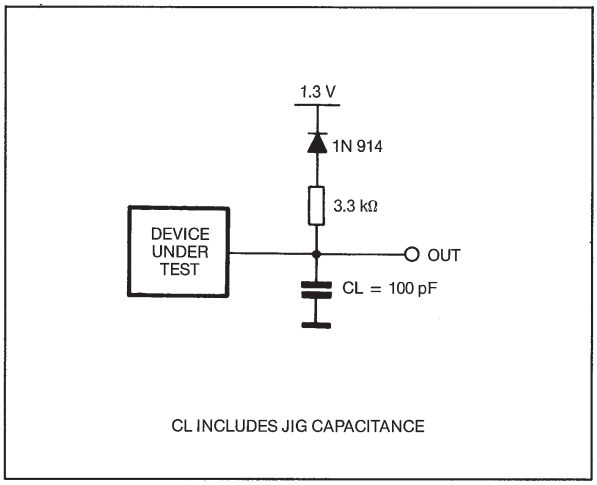


FIGURE 5 - AC TESTING LOAD CIRCUIT.

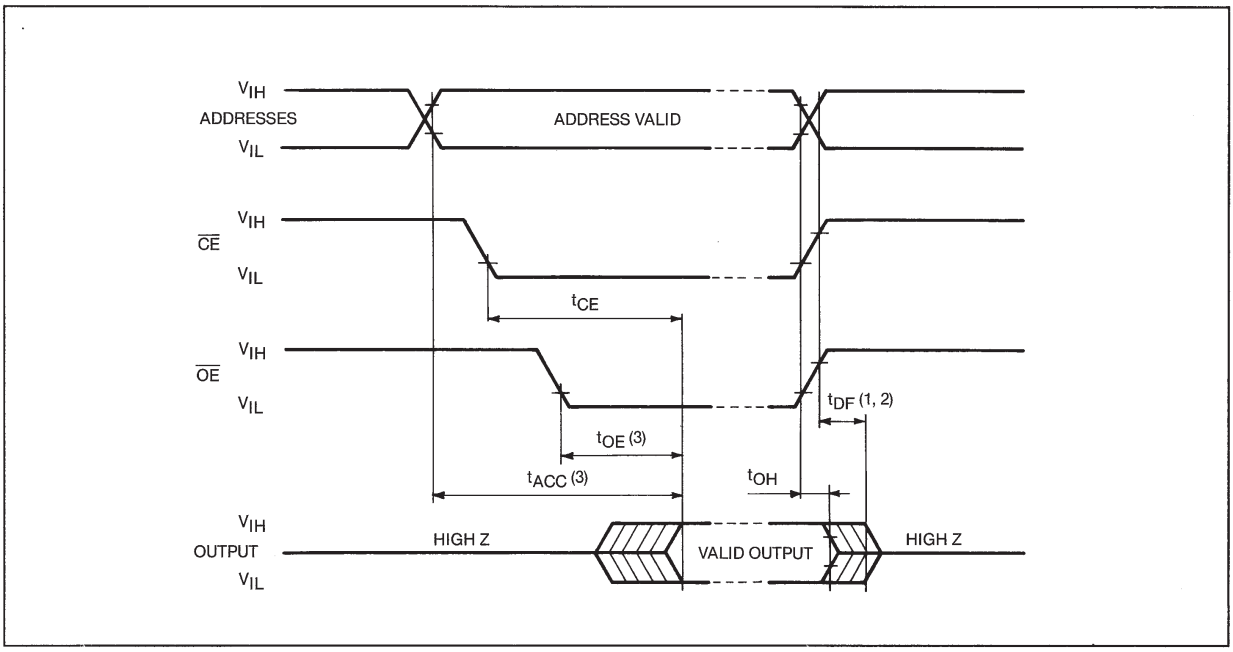


FIGURE 6 - AC WAVEFORMS.

Note 1 : This parameter is only sampled and not 100 % tested.
Note 2 : t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.
Note 3 : $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{CE}.

5.5 - Capacitance (see note)
(T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Test conditions	Min	Typ. (Note)	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		8	12	pF

Note : Typical values are for T_{amb} = 25°C and nominal supply voltages.
These parameters are only sampled and not 100 % tested.

5.6 - Burn-in conditions

5.6.1 - In Cerdip

Power :
V_{SS} = 0 V V_{CC} = 5 V
Frequency : 500 kHz Level «0» : 0 V Level «1» : 5 V

5.6.2 - In LCCC

Power :
V_{SS} = 0 V V_{CC} = 5.5 V
Frequency : 500 kHz Level «0» : 0 V Level «1» : 5.5 V

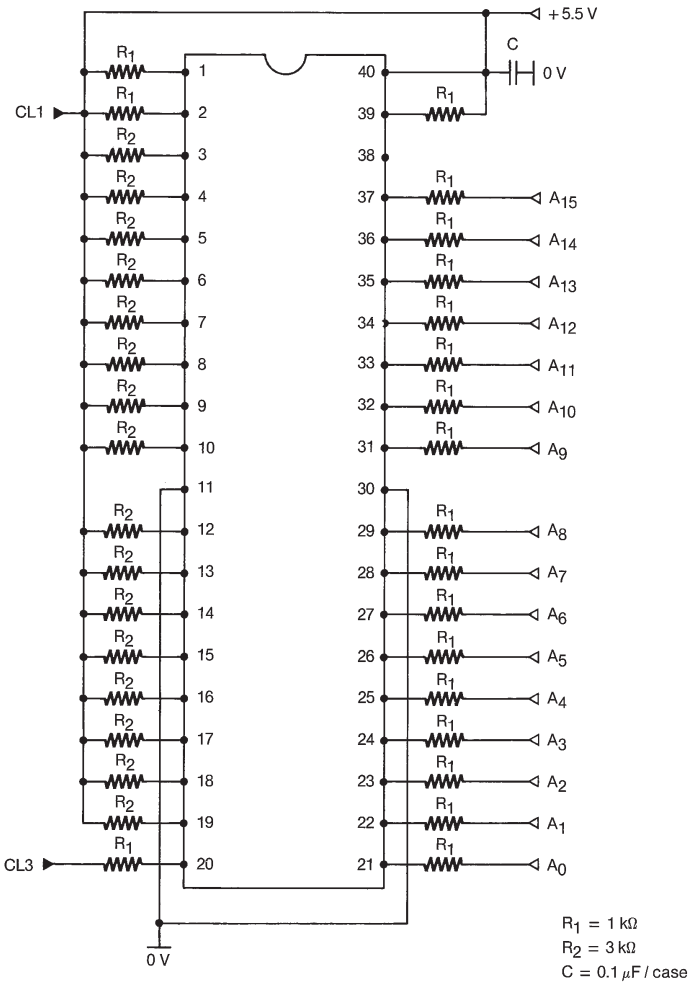


FIGURE 7

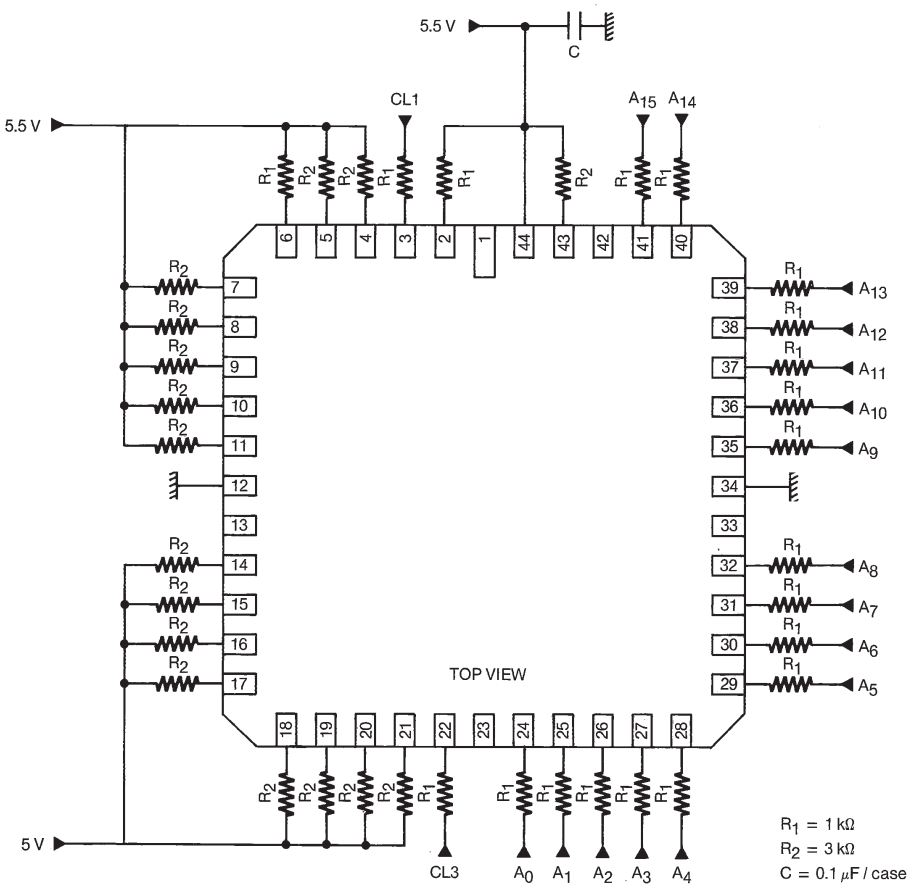


FIGURE 8

6 · FUNCTIONAL DESCRIPTION

6.1 · Device operation

The modes of operation of the 27C1024 are listed in the function table (see § 6.5). A single 5 V power supply is required in the read mode. All inputs are TTL levels except for 12 V on A9 for Electronic Signature.

Read mode

The 27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby mode

The 27C1024 has a standby mode which reduces the maximum active current from 40 mA to 0.2 mA. The 27C1024 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two line output control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

System considerations

The power switching characteristics of CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the actice current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the ouput capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array.

The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

6.2 · Programming

Caution : exceeding 14 V on V_{PP} pin will permanently damage the 27C1024.

When delivered, and after each erasure, all bits of the 27C1024 are in the «1» state. Data is introduced by selectively programming «0s» into the desired bit locations. Although only «0s» will be programmed, both «1s» and «0s» can be present in the data word. The only way to change a «0» to a «1» is by ultraviolet light erasure.

The 27C1024 is in the programming mode when the V_{PP} input is at 12.75 V and $\overline{CE}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data iputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

Very fast and reliable programming algorithm = PRESTO II

PRESTO II programming algorithm is available for the 27C1024.

During programming and verify operation a MARGIN MODE™ Circuit is automatically activated. It provides adequate margin on threshold voltage of programmed cells, thus writing margin is independent from V_{CC} in verify mode and over program pulse is not necessary, reducing programming time down to a theoretical value of 6 seconds.

Program inhibit

Programming of multiple 27C1024s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel 27C1024 may be common. A TTL low-level pulse applied to a 27C1024's $\overline{CE}$ input, with V_{PP} at 12.75 V, will program that 27C1024. A high level $\overline{CE}$ input inhibits the order 27C1024s from being programmed. V_{CC} is specified to be 6.25 V ±0.25 V.

Program verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.75 V and V_{CC} at 6.25 V ±0.25 V.

Electronic signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its mannufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the 27C1024. To activate this mode the programming equipment must force 11.5 V to 12.5 V on address line A9 of the 27C1024. Two identifier bytes may then be sequenced from the device outputs by toggling address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the TCS 27C1024, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7 while outputs O_8 to O_{15} are don't care.

ELECTRONIC SIGNATURE MODE

Identifier \ Pins	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
Device code	V_{IH}	1	0	0	0	1	1	0	0	8C

Notes : A9 = 12 V ±0.5 V ; $\overline{CE}$, $\overline{OE}$ = V_{IL} ; A1-A8, A10-A15 = V_{IL}.

PROGRAMMING OPERATION (T_C = 25°C ±5°C, V_{CC} (1) = 6.25 V ±0.25 V, V_{PP} (1) = 12.75 V ±0.25 V)
DC and operating characteristic

Symbol	Parameter	Test conditions see Note	Min	Max	Unit
I_{LI}	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input low level (all inputs)		−0.1	0.8	V
V_{IH}	Input high level		2.0	V_{CC} +0.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = −400 µA	2.4		V
I_{CC2}	V_{CC} supply current			50	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 electronic signature voltage		11.5	12.5	V

Note : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC characteristics

Symbol	Parameter	Test conditions Note 1	Min	Max	Unit
t_{AS}	Address setup time		2		µs
t_{OES}	$\overline{OE}$ setup time		2		µs
t_{DS}	Data setup time		2		µs
t_{AH}	Address hold time		0		µs
t_{DH}	Data hold time		2		µs
t_{DFP} Note 2	Output enable output float delay		0	130	ns
t_{VPS}	V_{PP} setup time		2		µs
t_{VCS}	V_{CC} setup time		2		µs
t_{CES}	$\overline{CE}$ setup time		2		µs
t_{PW}	$\overline{PGM}$ initial program puls width		95	105	µs
t_{OE}	Data valid from $\overline{OE}$			100	ns

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
Note 2 : This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

6.3 - High speed programming

6.3.1 - PRESTO II programming algorithm flow chart

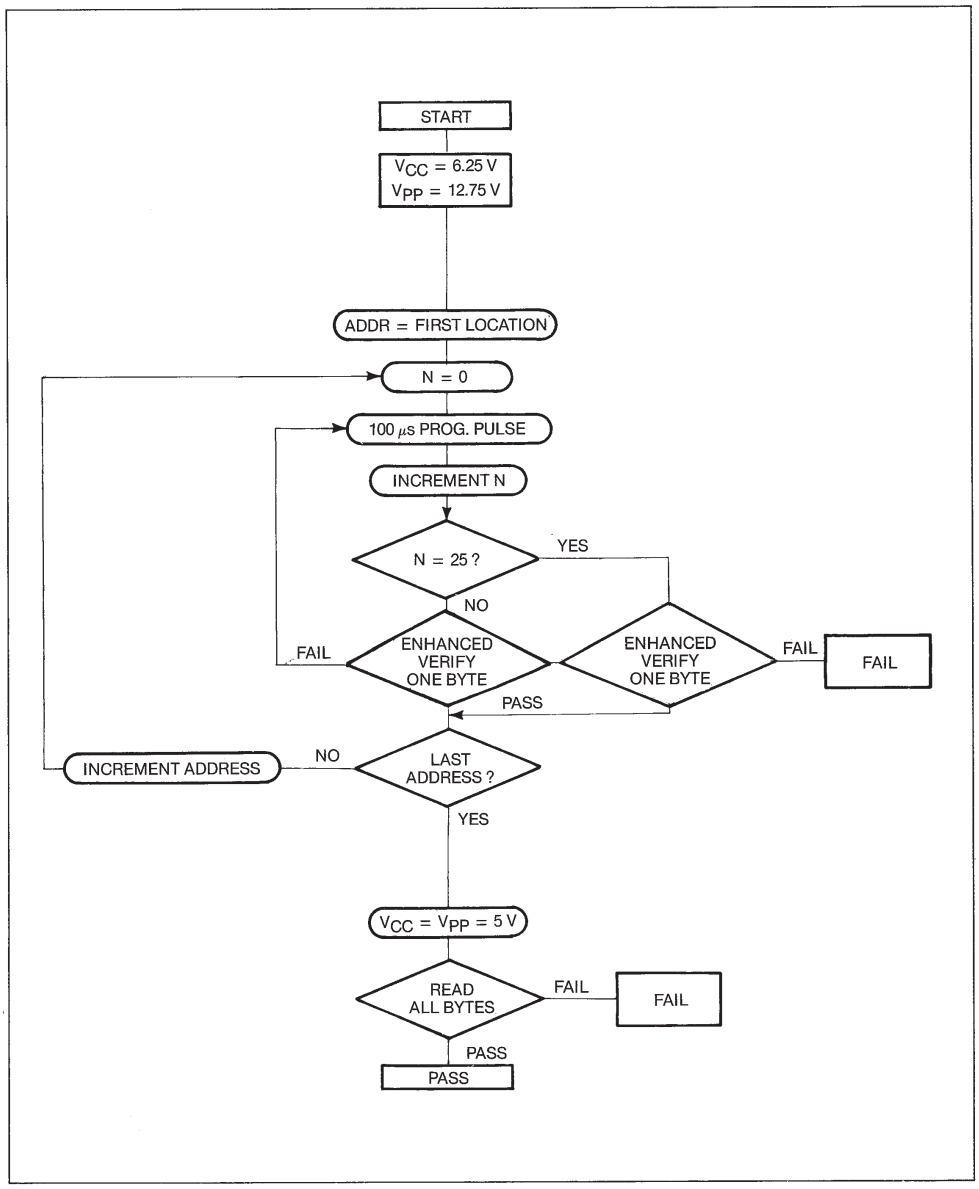
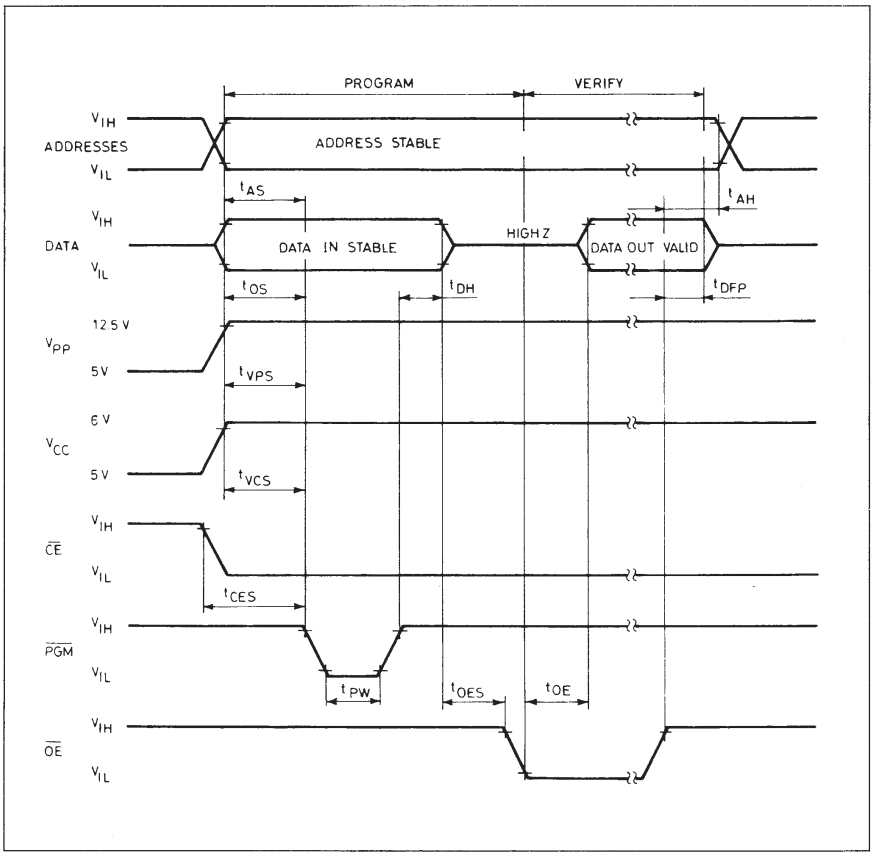


FIGURE 9

6.3.2 - Wave forms



Note 1 : The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.

Note 2 : t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Note 3 : When programming the 27C1024, a 0.1 μF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

FIGURE 10 - PROGRAMMING WAVEFORMS

6.4 - Erasing

The erasure characteristic of the 27C1024 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom A. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical 27C1024 in about 3 years, while it would take approximately 1 week cause erasure when expose to direct sunlight. If the 27C1024 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the 27C1024 window to prevent unintentional erasure. The recommended erasure procedure for the 27C1024 is exposure to short wave ultraviolet light which has wavelength 2537 A. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm² power rating. The 27C1024 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

6.5 - Function table

OPERATING MODES

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	A9	$\overline{PGM}$	V_{PP}	OUTPUTS
Read	L	L	X	H	V_{CC}	D_{OUT}
Output disable	L	H	X	X	V_{CC}	High Z
Standby	H	X	X	X	V_{CC}	High Z
Program	L	X	X	L	V_{PP}	D_{IN}
Program verify	L	L	X	H	V_{PP}	D_{OUT}
Program inhibit	H	X	X	X	V_{PP}	High Z
Electronic signature	L	L	V_H	H	V_{CC}	CODE

Notes : X = Don't care ; V_H = 12 V ±0.5 V ; H = High ; L = Low.

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuits are prepared for delivery in accordance with MIL-STD-883.

7.2 - Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

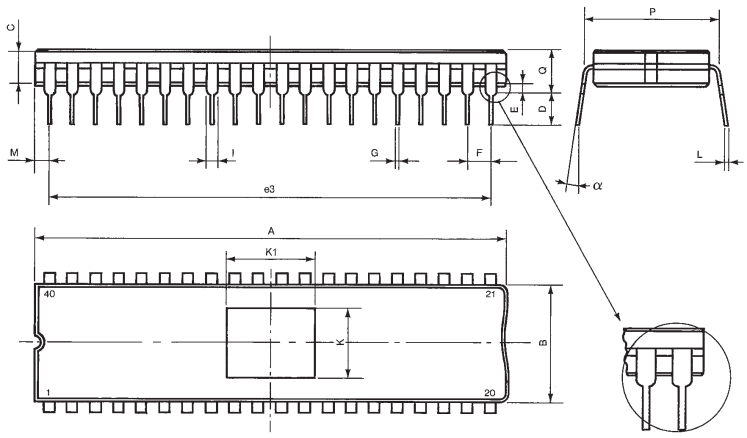
8 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devices should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 percent if practical.

9 - PACKAGE MECHANICAL DATA

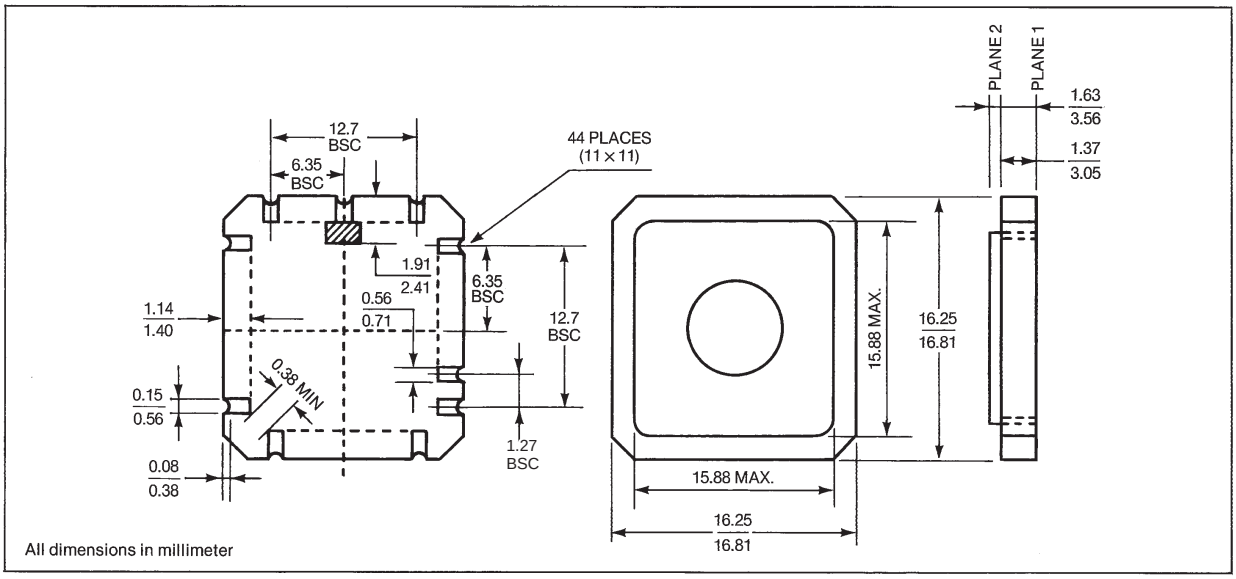
9.1 - DIL CERDIP with window package 40 pins



Symbol	Millimeters		
	Min	Typ	Max
A			53.24
B	12.95		15.75
C	3.90		5.08
D	3.18		5
E	0.38		1.78
e3		48.26	
F		2.54	
G	0.36		0.58
I	0.96		1.65
L	0.20		0.38
M			2.49
P	14.90		16
Q			5.71
K	7.90		8.38
K1	10.41		10.92
α	0		15°

FIGURE 11 - 40-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)

9.2 - 44 pins Leadless Ceramic Chip Carrier



10 – ORDERING INFORMATION

10.1 Hi REL product

TCS part number	norms	package	temperature range (T°C)	Tacc (ns)	Drawing number
27C1024MQB/C90	MILSTD 883 Class B	Cerdip 40	–55/+125	90	TCS datasheet
27C1024MQB/C10	MILSTD 883 Class B	Cerdip 40	–55/+125	100	TCS datasheet
27C1024MQB/C12	MILSTD 883 Class B	Cerdip 40	–55/+125	120	TCS datasheet
27C1024MQB/C15	MILSTD 883 Class B	Cerdip 40	–55/+125	150	TCS datasheet
27C1024MQB/C20	MILSTD 883 Class B	Cerdip 40	–55/+125	200	TCS datasheet
27C1024MQB/C25	MILSTD 883 Class B	Cerdip 40	–55/+125	250	TCS datasheet
27C1024MEQ1B/C90	MILSTD 883 Class B	LCCC44	–55/+125	90	TCS datasheet
27C1024MEQ1B/C10	MILSTD 883 Class B	LCCC44	–55/+125	100	TCS datasheet
27C1024MEQ1B/C12	MILSTD 883 Class B	LCCC44	–55/+125	120	TCS datasheet
27C1024MEQ1B/C15	MILSTD 883 Class B	LCCC44	–55/+125	150	TCS datasheet
27C1024MEQ1B/C20	MILSTD 883 Class B	LCCC44	–55/+125	200	TCS datasheet
27C1024MEQ1B/C25	MILSTD 883 Class B	LCCC44	–55/+125	250	TCS datasheet

TCS part number	norms	package	temperature range (Tc°C)	Tacc (ns)	Drawing number
27C1024DESC02QA	DSCC	Cerdip 40	–55/+125	250	5962–8680502QA
27C1024DESC03QA	DSCC	Cerdip 40	–55/+125	200	5962–8680503QA
27C1024DESC05QA	DSCC	Cerdip 40	–55/+125	150	5962–8680505QA
27C1024DESC06QA	DSCC	Cerdip 40	–55/+125	120	5962–8680506QA
27C1024DESC07QA	DSCC	Cerdip 40	–55/+125	90	5962–8680507QA
27C1024DESC02XA	DSCC	LCCC 44	–55/+125	250	5962–8680502XA
27C1024DESC03XA	DSCC	LCCC 44	–55/+125	200	5962–8680503XA
27C1024DESC05XA	DSCC	LCCC 44	–55/+125	150	5962–8680505XA
27C1024DESC06XA	DSCC	LCCC 44	–55/+125	120	5962–8680506XA
27C1024DESC07XA	DSCC	LCCC 44	–55/+125	90	5962–8680507XA

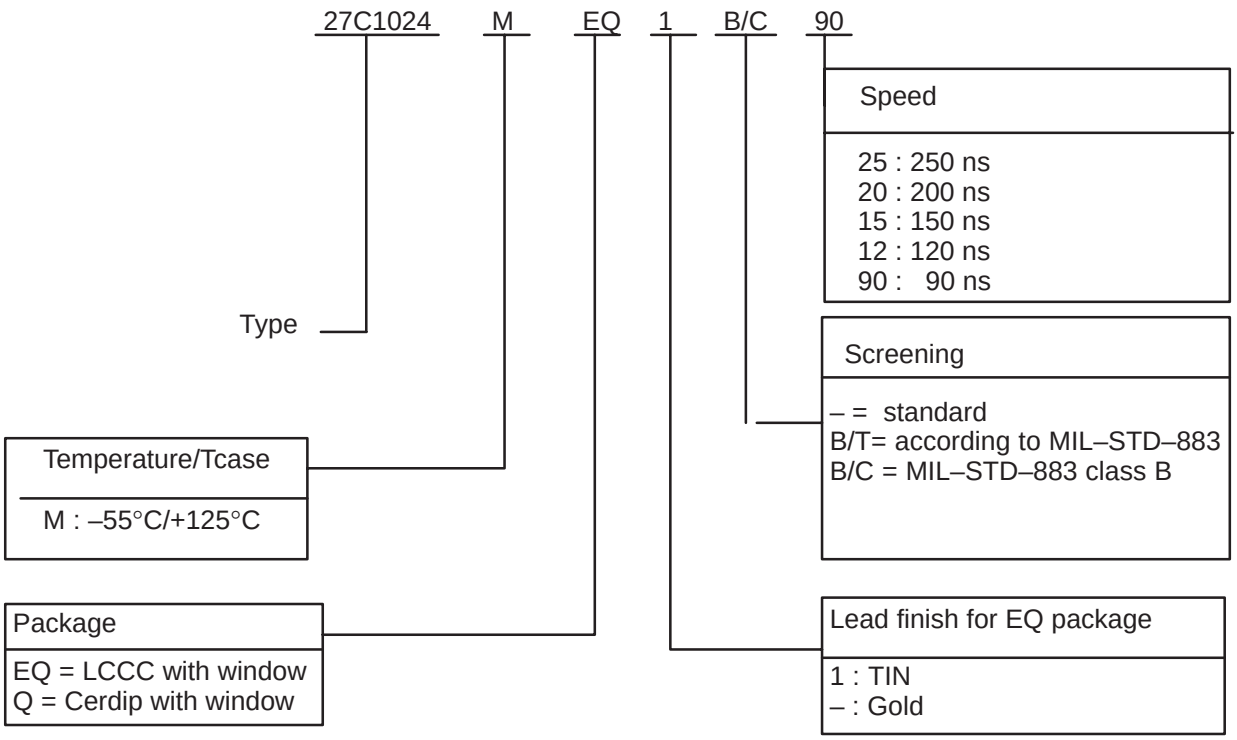
TCS part number	norms	package	temperature range (Tc°C)	Tacc (ns)	Drawing number
27C1024MQB/Txx (see note1)	According to MIL–STD–883	Cerdip 40	–55/+125	See note 1	TCS datasheet
27C1024MEQ1B/Txx (see note 1)	According to MIL–STD–883	LCCC 44	–55/+125	See note 1	TCS datasheet

10.2 Standard product

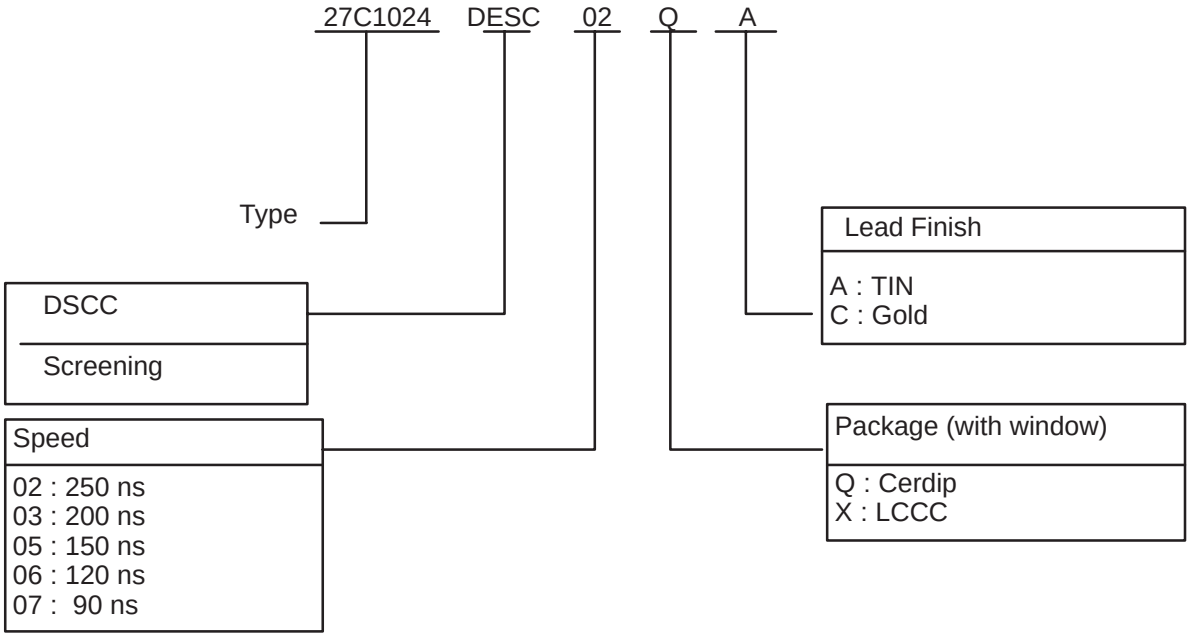
TCS part number	norms	package	temperature range (Tc°C)	Tacc (ns)	Drawing number
27C1024MQxx (see note1)	TCS Standard	Cerdip 40	–55/+125	See note 1	TCS datasheet
27C1024MEQxx (see note 1)	TCS Standard	LCCC 44	–55/+125	See note 1	TCS datasheet

note 1 : xx = 90 (Tacc = 90ns)
xx = 10 (Tacc = 100 ns)
xx = 12 (Tacc = 120 ns)
xx = 15 (Tacc = 150 ns)
xx = 20 (Tacc = 200 ns)
xx = 25 (Tacc = 250 ns)

10.3 MIL STD 883 and TCS Standard



10.4 DSCC Drawing 86805



This product is manufactured and commercialized by THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - PO Box 123 - 38521 SAINT-EGREVE Cedex - FRANCE.

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