

# UT8ER512K32 Monolithic 16M RadHard SRAM



## FEATURES

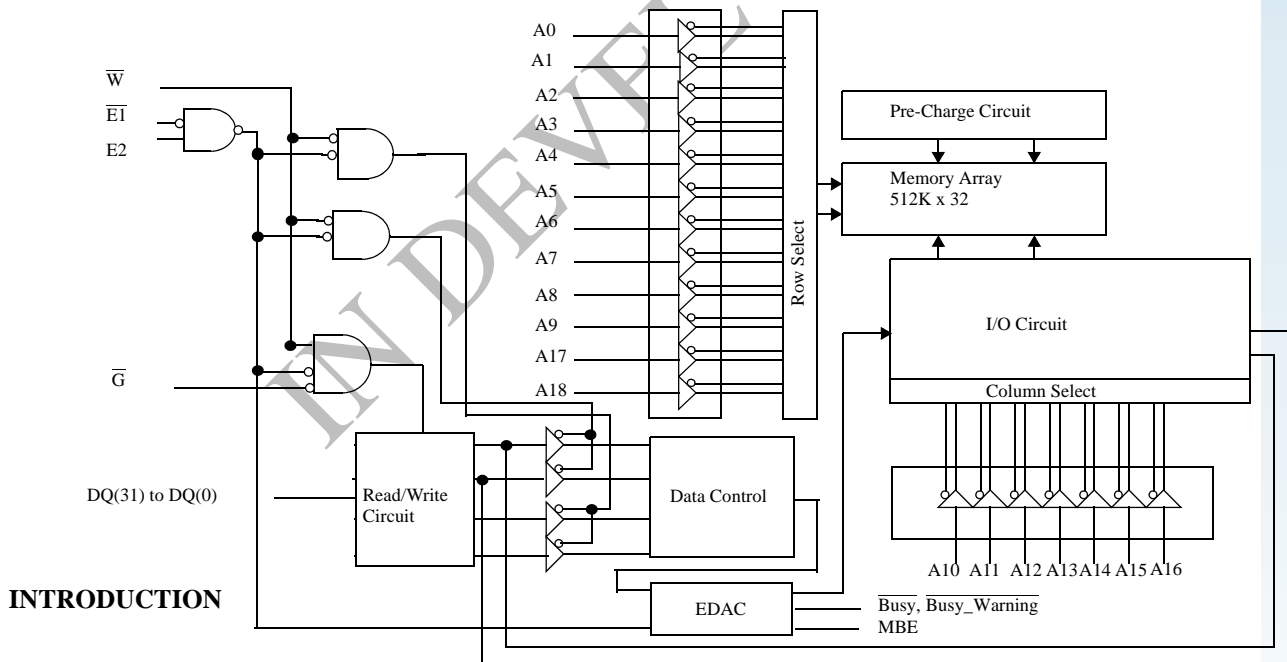
- ❑ 20ns maximum access time
- ❑ Asynchronous operation, functionally compatible with industry-standard 512K x 32 SRAMs
- ❑ CMOS compatible inputs and output levels, three-state bidirectional data bus
  - 3.3 volt IO, 1.8 volt core
- ❑ Radiation performance
  - Total-dose: >100Krad(Si)
  - SEL Immune: 100MeV-cm<sup>2</sup>/mg
  - SEU error rate = 2.9x10<sup>-16</sup> errors bit/day assuming geosynchronous orbit, Adam's 90% worst environment, and 312KHz default scrub rate (=99.4% SRAM availability)
  - Neutron Fluence: 3.0E14n/cm<sup>2</sup>
  - Dose Rate
    - Upset TBD rad(Si)/sec
    - Latchup TBD rad(Si)/sec
- ❑ Packaging options:
  - 68-lead ceramic quad flatpack (6.898 grams)
- ❑ Standard Microcircuit Drawing TBD
  - QML compliant part

The UT8ER512K32 is a high-performance CMOS static RAM organized as 524,288 words by 32 bits. Easy memory expansion is provided by active LOW and HIGH chip enables ( $\overline{E1}$ , E2), an active LOW output enable ( $\overline{G}$ ), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to the device is accomplished by driving chip enable one ( $\overline{E1}$ ) input LOW, chip enable two (E2) HIGH and write enable ( $\overline{W}$ ) input LOW. Data on the 32 I/O pins (DQ0 through DQ31) is then written into the location specified on the address pins (A0 through A8). Reading from the device is accomplished by taking chip enable one ( $\overline{E1}$ ) and output enable ( $\overline{G}$ ) LOW while forcing write enable ( $\overline{W}$ ) and chip enable two (E2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 32 input/output pins (DQ0 through DQ31) are placed in a high impedance state when the device is deselected ( $\overline{E1}$  HIGH or E2 LOW), the outputs are disabled ( $\overline{G}$  HIGH), or during a write operation ( $\overline{E1}$  LOW, E2 HIGH and  $\overline{W}$  LOW).

To reduce bit error rates caused by single event phenomenon in space, the UT8ER512K32 employs an embedded EDAC (error detection and correction) having code engine with auto scrubbing. When a double bit error occurs in a word, the UT8ER512K32 asserts an  $\overline{MBE}$  output to the host.



## INTRODUCTION

Figure 1. UT8ER512K32 SRAM Block Diagram

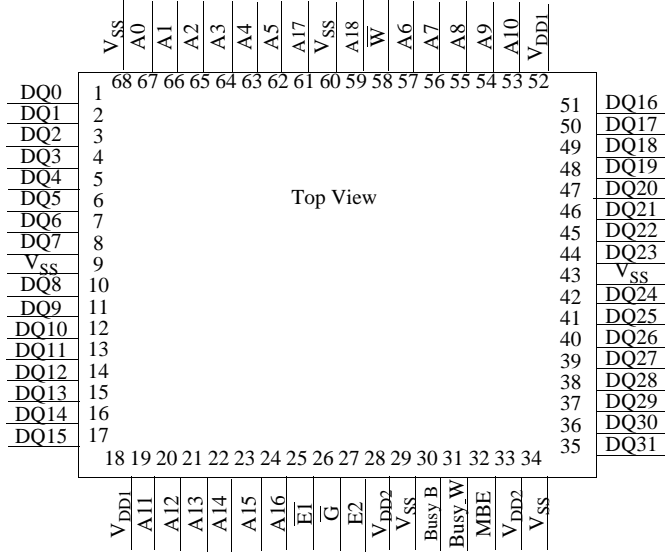


Figure 2. 25ns SRAM Pinout (68)

**PIN NAMES**

|                                   |                            |
|-----------------------------------|----------------------------|
| A(18:0)                           | Address                    |
| DQ(31:0)                          | Data Input/Output          |
| $\overline{E1}$                   | Enable (Active Low)        |
| E2                                | Enable (Active High)       |
| $\overline{W}$                    | Write Enable               |
| $\overline{G}$                    | Output Enable              |
| V <sub>DD1</sub>                  | Power (1.8)                |
| V <sub>DD2</sub>                  | Power (3.3V)               |
| V <sub>SS</sub>                   | Ground                     |
| MBE                               | Multiple Bit Error         |
| $\overline{\text{Busy B}}$        | Device Status              |
| $\overline{\text{Busy\_Warning}}$ | Advanced for Device Status |

**DEVICE OPERATION**

The UT8ER512K32 has four control inputs called Enable 1 ( $\overline{E1}$ ), Enable 2 (E2), Write Enable ( $\overline{W}$ ), and Output Enable ( $\overline{G}$ ); 19 address inputs, A(18:0); and 32 bidirectional data lines, DQ(31:0).  $\overline{E1}$  and E2 device enables control device selection, active, and standby modes. Asserting  $\overline{E1}$  and E2 enables the device, causes I<sub>DD</sub> to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory.  $\overline{W}$  controls read and write operations. During a read cycle,  $\overline{G}$  must be asserted to enable the outputs.

Table 1. SRAM Device Operation Truth Table

| $\overline{G}$ | $\overline{W}$ | E2 | $\overline{E1}$ | I/O Mode                | Mode       |
|----------------|----------------|----|-----------------|-------------------------|------------|
| X              | X              | X  | H               | DQ(31:0)<br>3-State     | Standby    |
| X              | X              | L  | X               | DQ(31:0)<br>3-State     | Standby    |
| L              | H              | H  | L               | DQ(31:0)<br>Data Out    | Word Read  |
| X              | L              | H  | L               | DQ(31:0)<br>Data In     | Word Write |
| H              | H              | H  | L               | DQ(31:0)<br>All 3-State | 3-State    |

**Notes:**

1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

Table 2. EDAC Control Pin Operation Truth Table

| MBE | Busy B | Busy_W | I/O Mode       | Mode                                      |
|-----|--------|--------|----------------|---|
| H   | H      | H      | Read           | Uncorrectable Bit Error                   |
| L   | H      | H      | Read           | Valid Data Out                            |
| X   | H      | H      | X              | Device Ready                              |
| X   | H      | L      | X              | Device Ready / Early Scrub Request Coming |
| X   | L      | X      | Not Accessible | Device Busy                               |

**Notes:**

1. "X" is defined as a "don't care" condition

## READ CYCLE

A combination of  $\overline{W}$  and E2 greater than  $V_{IH}$  (min) and  $\overline{E1}$  and  $\overline{G}$  less than  $V_{IL}$  (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs while the chip is enabled with  $\overline{G}$  asserted and  $\overline{W}$  deasserted. Valid data appears on data outputs DQ(31:0) after the specified  $t_{AVQV}$  is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time ( $t_{AVAV}$ ).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b, is initiated by the latter of either  $\overline{E1}$  and E2 going active while  $\overline{G}$  remains asserted,  $\overline{W}$  remains deasserted, and the addresses remain stable for the entire cycle. After the specified  $t_{ETQV}$  is satisfied, the 32-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(31:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by  $\overline{G}$  going active while  $\overline{E1}$  and E2 are asserted,  $\overline{W}$  is deasserted, and the addresses are stable. Read access time is  $t_{GLQV}$  unless  $t_{AVQV}$  or  $t_{ETQV}$  (reference Figure 3b) have not been satisfied.

SRAM EDAC Status Indications during a Read Cycle, if MBE is Low, the data is good. If MBE is High the data is corrupted.

## WRITE CYCLE

A combination of  $\overline{W}$  and  $\overline{E1}$  less than  $V_{IL}$  (max) and E2 greater than  $V_{IH}$  (min) defines a write cycle. The state of  $\overline{G}$  is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either  $\overline{G}$  is greater than  $V_{IH}$  (min), or when  $\overline{W}$  is less than  $V_{IL}$  (max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by  $\overline{W}$  going high, with  $\overline{E1}$  and E2 still active. The write pulse width is defined by  $t_{WLWH}$  when the write is initiated by  $\overline{W}$ , and by  $t_{ETWH}$  when the write is initiated by  $\overline{E1}$  and E2. Unless the outputs have been previously placed in the high-impedance state by  $\overline{G}$ , the  $t_{WLQZ}$  before applying data to the 32 bidirectional pins DQ(31:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by the latter of  $\overline{E1}$  or E2 going inactive. The write pulse width is defined by  $t_{WLEF}$  when the write is initiated by  $\overline{W}$ , and by  $t_{ETEF}$  when the write

is initiated by either  $\overline{E1}$  or E2 going active. For the  $\overline{W}$  initiated write, unless the outputs have been previously placed in the high-impedance state by  $\overline{G}$ , the user must wait  $t_{WLQZ}$  before applying data to the thirty-two bidirectional pins DQ(31:0) to avoid bus contention.

## MEMORY SCRUBBING/CYCLE STEALING

The UT8ER512K32 SRAM uses architectural improvements and embedded error detection and correction to maintain unsurpassed levels of SEU protection. This is accomplished by what Aeroflex refers to as Cycle Stealing. When the device asserts  $\overline{BUSY\_WARNING}$  followed by  $\overline{BUSY}$ , the user must de-assert  $\overline{E1}$  or E2 within the minimum specification for an access cycle ( $t_{AVAV}$ ). To minimize the system design impact for reduced speed operation, the edge relationship between  $\overline{BUSY\_WARNING}$  and  $\overline{BUSY}$  is programmable via the sequence described in figure 5a.

The effective error rate will be flux dependent (rate at which radiation is applied) and not simply LET dependent. As a result, some users may desire an increased scrub rate to lower the error rate at the sacrifice of reduced total throughput, while others may desire a lower scrub rate to increase the total throughput and accept a higher error rate in a low flux environment. This rate at which the SRAM controller will correct errors from the memory is user programmable. The required sequence is described in figure 5a.

Data is corrected not only during the internal scrub, but again during a user requested read cycle. If the MBE signal is asserted once the data is valid ( $t_{AVAV}$ ), if the data presented contains at least two errors and should be considered corrupt.

## RADIATION HARDNESS

The UT8ER512K32 SRAM incorporates special design, layout, and process features which allows operation in a limited radiation environment.

**Table 3. Radiation Hardness Design Specifications<sup>1</sup>**

|                                   |      |                |
|-----------------------------------|------|----------------|
| Total Dose                        | 100K | rad(Si)        |
| Heavy Ion Error Rate <sup>2</sup> | TBD  | Errors/Bit-Day |

**Notes:**

1. The SRAM is immune to latchup to particles >100MeV-cm<sup>2</sup>/mg.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

## SUPPLY SEQUENCING

No supply voltage sequencing is required between  $V_{DD1}$  and  $V_{DD2}$ .

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(Referenced to  $V_{SS}$ )

| SYMBOL        | PARAMETER   | LIMITS        |
|---------------|---|---------------|
| $V_{DD1}$     | DC supply voltage                                 | -0.3 to 2.0V  |
| $V_{DD2}$     | DC supply voltage                                 | -0.3 to 3.8V  |
| $V_{IO}$      | Voltage on any pin                                | -0.3 to 3.8V  |
| $T_{STG}$     | Storage temperature                               | -65 to +150°C |
| $P_D$         | Maximum power dissipation                         | 1.2W          |
| $T_J$         | Maximum junction temperature                      | +150°C        |
| $\Theta_{JC}$ | Thermal resistance, junction-to-case <sup>2</sup> | 5°C/W         |
| $I_I$         | DC input current                                  | ±5 mA         |

### Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Test per MIL-STD-883, Method 1012.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL    | PARAMETER               | LIMITS   |
|-----------|-------------------------|--|
| $V_{DD1}$ | Positive supply voltage | 1.7 to 1.9V  |
| $V_{DD2}$ | Positive supply voltage | 3.0 to 3.6V  |
| $T_C$     | Case temperature range  | (C) Screening: -55 to +125°C<br>(W) Screening: -40 to +125°C |
| $V_{IN}$  | DC input voltage        | 0V to $V_{DD2}$  |

**DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)\***

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening)

| SYMBOL                              | PARAMETER  | CONDITION   | MIN                 | MAX                 | UNIT |
|-------------------------------------|--|---|---------------------|---------------------|------|
| V <sub>IH</sub>                     | High-level input voltage                           |   | .7*V <sub>DD2</sub> |                     | V    |
| V <sub>IL</sub>                     | Low-level input voltage                            |   |                     | .3*V <sub>DD2</sub> | V    |
| V <sub>OL</sub>                     | Low-level output voltage                           | I <sub>OL</sub> = 8mA, V <sub>DD2</sub> = V <sub>DD2</sub> (min)  |                     | .2*V <sub>DD2</sub> | V    |
| V <sub>OH</sub>                     | High-level output voltage                          | I <sub>OH</sub> = -4mA, V <sub>DD2</sub> = V <sub>DD2</sub> (min)   | .8*V <sub>DD2</sub> |                     | V    |
| C <sub>IN</sub> <sup>1</sup>        | Input capacitance                                  | f = 1MHz @ 0V   |                     | 12                  | pF   |
| C <sub>IO</sub> <sup>1</sup>        | Bidirectional I/O capacitance                      | f = 1MHz @ 0V   |                     | 12                  | pF   |
| I <sub>IN</sub>                     | Input leakage current                              | V <sub>IN</sub> = V <sub>DD2</sub> and V <sub>SS</sub>  | -2                  | 2                   | μA   |
| I <sub>OZ</sub>                     | Three-state output leakage current                 | V <sub>O</sub> = V <sub>DD2</sub> and V <sub>SS</sub><br>V <sub>DD2</sub> = V <sub>DD2</sub> (max), $\bar{G}$ = V <sub>DD2</sub> (max)  | -2                  | 2                   | μA   |
| I <sub>OS</sub> <sup>2, 3</sup>     | Short-circuit output current                       | V <sub>DD2</sub> = V <sub>DD2</sub> (max), V <sub>O</sub> = V <sub>DD2</sub><br>V <sub>DD2</sub> = V <sub>DD2</sub> (max), V <sub>O</sub> = V <sub>SS</sub>   | -100                | +100                | mA   |
| I <sub>DD1</sub> (OP <sub>1</sub> ) | V <sub>DD1</sub> Supply current operating @ 1MHz   | Inputs : V <sub>IL</sub> = V <sub>SS</sub> + 0.2V,<br>V <sub>IH</sub> = V <sub>DD2</sub> - 0.2V, I <sub>OUT</sub> = 0<br>V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max) |                     | 25                  | mA   |
| I <sub>DD1</sub> (OP <sub>2</sub> ) | V <sub>DD1</sub> Supply current operating @ 50MHz, | Inputs : V <sub>IL</sub> = V <sub>SS</sub> + 0.2V,<br>V <sub>IH</sub> = V <sub>DD2</sub> - 0.2V, I <sub>OUT</sub> = 0<br>V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max) |                     | 200                 | mA   |
| I <sub>DD2</sub> (OP <sub>1</sub> ) | V <sub>DD2</sub> Supply current operating @ 1MHz   | Inputs : V <sub>IL</sub> = V <sub>SS</sub> + 0.2V,<br>V <sub>IH</sub> = V <sub>DD2</sub> - 0.2V, I <sub>OUT</sub> = 0<br>V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max) |                     | 1                   | mA   |
| I <sub>DD2</sub> (OP <sub>2</sub> ) | V <sub>DD2</sub> Supply current operating @ 50MHz, | Inputs : V <sub>IL</sub> = V <sub>SS</sub> + 0.2V,<br>V <sub>IH</sub> = V <sub>DD2</sub> - 0.2V, I <sub>OUT</sub> = 0<br>V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max) |                     | 12                  | mA   |
| I <sub>DD1</sub> (SB) <sup>4</sup>  | Supply current standby @ 0Hz                       | CMOS inputs , I <sub>OUT</sub> = 0<br>$\bar{E}1$ = V <sub>DD2</sub> - 0.2, E2 = GND<br>V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max)                                   |                     | 25                  | mA   |
| I <sub>DD2</sub> (SB) <sup>4</sup>  |  |   |                     | 100                 | μA   |
| I <sub>DD1</sub> (SB) <sup>4</sup>  | Supply current standby A(16:0) @ 50MHz             | CMOS inputs , I <sub>OUT</sub> = 0<br>$\bar{E}1$ = V <sub>DD2</sub> - 0.2, E2 = GND,<br>V <sub>DD1</sub> = V <sub>DD1</sub> (max), V <sub>DD2</sub> = V <sub>DD2</sub> (max)                                  |                     | 25                  | mA   |
| I <sub>DD2</sub> (SB) <sup>4</sup>  |  |   |                     | 100                 | μA   |

**Notes:**

\* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 3.0E5 rad(Si).

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.

2. Supplied as a design limit but not guaranteed or tested.

3. Not more than one output may be shorted at a time for maximum duration of one second.

4. V<sub>IH</sub> = V<sub>DD2</sub> (max), V<sub>IL</sub> = 0V.

**AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)\***

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening,  $V_{DD1} = V_{DD1}(\text{min})$ ,  $V_{DD2} = V_{DD2}(\text{min})$ )

| SYMBOL           | PARAMETER   | UT8ER512 |     | UNIT | FIGURE |
|------------------|---|----------|-----|------|--------|
|                  |   | MIN      | MAX |      |        |
| $t_{AVAV}^1$     | Read cycle time                                     | 20       |     | ns   | 3a     |
| $t_{AVQV}$       | Address to data valid from address change           |          | 20  | ns   | 3c     |
| $t_{AXQX}^2$     | Output hold time                                    | 3        |     | ns   | 3a     |
| $t_{GLQX}^{1,2}$ | $\overline{G}$ -controlled output enable time       | 0        |     | ns   | 3c     |
| $t_{GLQV}$       | $\overline{G}$ -controlled output data valid        |          | 7   | ns   | 3c     |
| $t_{GHQZ}^2$     | $\overline{G}$ -controlled output three-state time  |          | 7   | ns   | 3c     |
| $t_{ETQX}^{2,3}$ | E-controlled output enable time                     | 5        |     | ns   | 3b     |
| $t_{ETQV}^3$     | E-controlled access time                            |          | 20  | ns   | 3b     |
| $t_{EFQZ}^4$     | E-controlled output three-state time <sup>2</sup>   |          | 7   | ns   | 3b     |
| $t_{ETMV}$       | E-controlled error flag time                        |          | 20  | ns   | 3b     |
| $t_{AVMV}$       | Address to error flag valid                         | 20       |     | ns   | 3a     |
| $t_{AXMX}$       | Address to error flag hold time from address change | 3        |     | ns   | 3a     |
| $t_{GLMV}$       | $\overline{G}$ -controlled error flag valid         |          | 7   | ns   | 3c     |
| $t_{GLMX}$       | $\overline{G}$ -controlled error flag enable time   | 5        |     | ns   | 3c     |
| $t_{ETMX}$       | E-controlled error flag enable time                 | 5        |     | ns   | 3b     |

**Notes:**

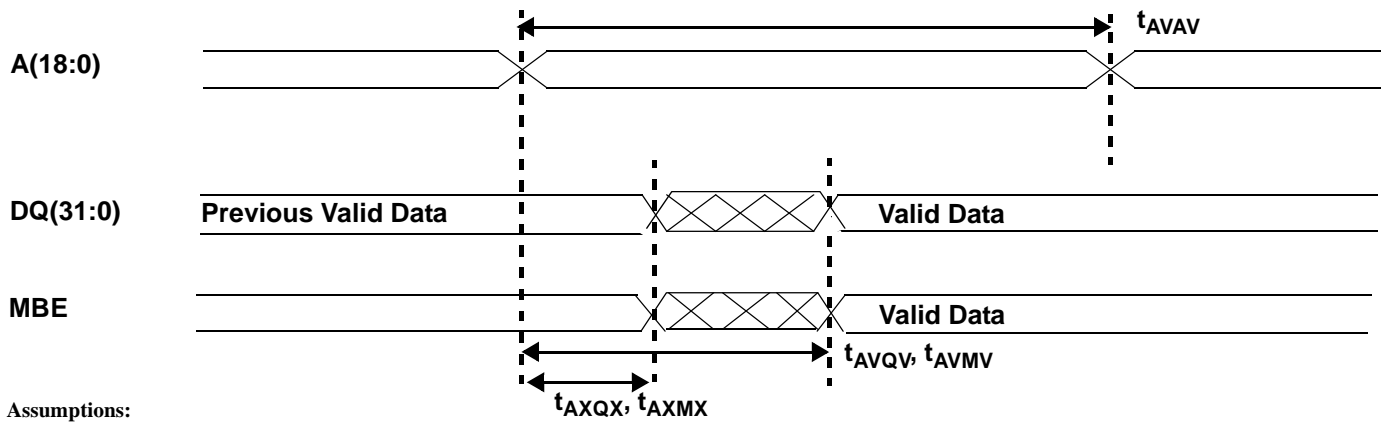
\* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Guaranteed but not tested.

2. Three-state is defined as a 200mV change from steady-state output voltage.

3. The ET (enable true) notation refers to the latter falling edge of E1 or rising edge of E2.

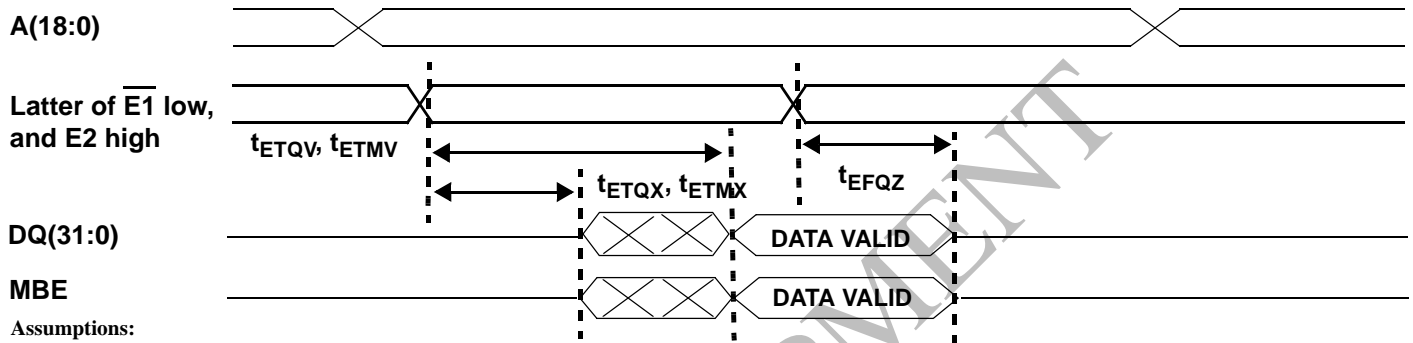
4. The EF (enable false) notation refers to the latter rising edge of E1 or falling edge of E2.



**Assumptions:**

1.  $\overline{E1}$  and  $\overline{G} \leq V_{IL}$  (max) and  $E2$  and  $\overline{W} \geq V_{IH}$  (min)
2.  $\text{Busy} \geq V_{OH}$  (min)

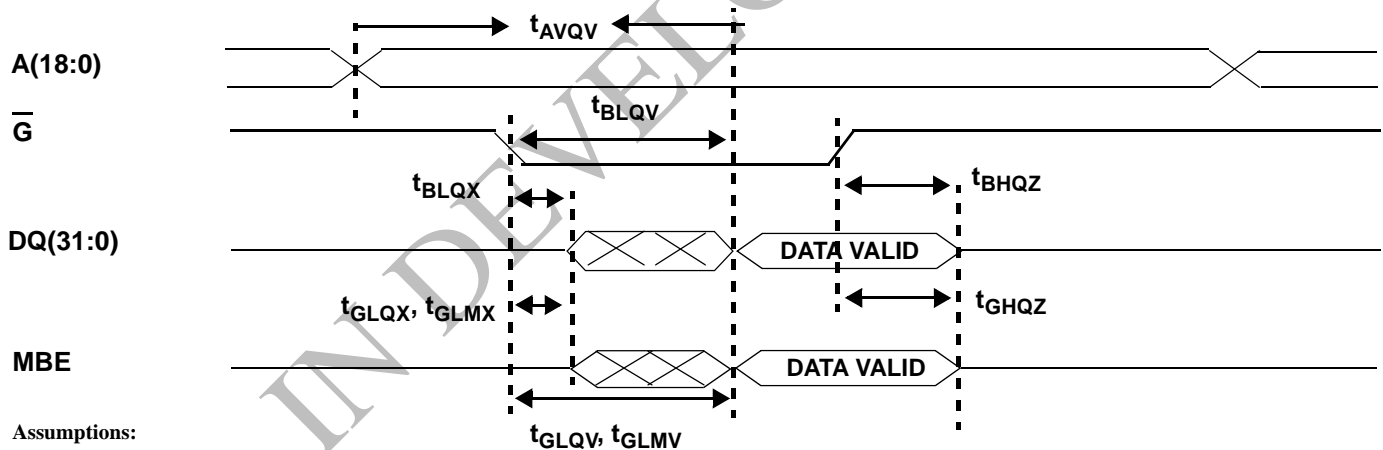
Figure 3a. SRAM Read Cycle 1: Address Access



**Assumptions:**

1.  $\overline{G} \leq V_{IL}$  (max) and  $\overline{W} \geq V_{IH}$  (min)
2.  $\text{Busy} \geq V_{OH}$  (min)

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



**Assumptions:**

1.  $\overline{E1} \leq V_{IL}$  (max),  $E2$  and  $\overline{W} \geq V_{IH}$  (min)
2.  $\text{Busy} \geq V_{OH}$  (min)

Figure 3c. SRAM Read Cycle 3: Output Enable Access

**AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)\***

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening,  $V_{DD1} = V_{DD1}(\text{min})$ ,  $V_{DD2} = V_{DD2}(\text{min})$ )

| SYMBOL       | PARAMETER  | MIN MAX |     | UNIT | FIGURE |
|--------------|--|---------|-----|------|--------|
|              |  | MIN     | MAX |      |        |
| $t_{AVAV}^1$ | Write cycle time   | 20      |     | ns   | 4a/4b  |
| $t_{ETWH}$   | Device enable to end of write  | 17      |     | ns   | 4a     |
| $t_{AVET}$   | Address setup time for write ( $\overline{E1}/E2$ - controlled)        | 0       |     | ns   | 4b     |
| $t_{AVWL}$   | Address setup time for write ( $\overline{W}$ - controlled)            | 0       |     | ns   | 4a     |
| $t_{WLWH}$   | Write pulse width  | 17      |     | ns   | 4a     |
| $t_{WHAX}$   | Address hold time for write ( $\overline{W}$ - controlled)             | 0       |     | ns   | 4a     |
| $t_{EFAX}$   | Address hold time for device enable ( $\overline{E1}/E2$ - controlled) | 0       |     | ns   | 4b     |
| $t_{WLQZ}^2$ | $\overline{W}$ - controlled three-state time                           |         | 7   | ns   | 4a/4b  |
| $t_{WHQX}^2$ | $\overline{W}$ - controlled output enable time                         | 6       |     | ns   | 4a     |
| $t_{ETEF}$   | Device enable pulse width ( $\overline{E1}/E2$ - controlled)           | 17      |     | ns   | 4b     |
| $t_{DVWH}$   | Data setup time  | 12      |     | ns   | 4a     |
| $t_{WHDX}$   | Data hold time   | 0       |     | ns   | 4a     |
| $t_{WLEF}$   | Device enable controlled write pulse width                             | 17      |     | ns   | 4b     |
| $t_{DVEF}$   | Data setup time  | 12      |     | ns   | 4a/4b  |
| $t_{EFDX}$   | Data hold time   | 0       |     | ns   | 4b     |
| $t_{AVWH}$   | Address valid to end of write  | 17      |     | ns   | 4a     |
| $t_{WHWL}^1$ | Write disable time   | 5       |     | ns   | 4a     |

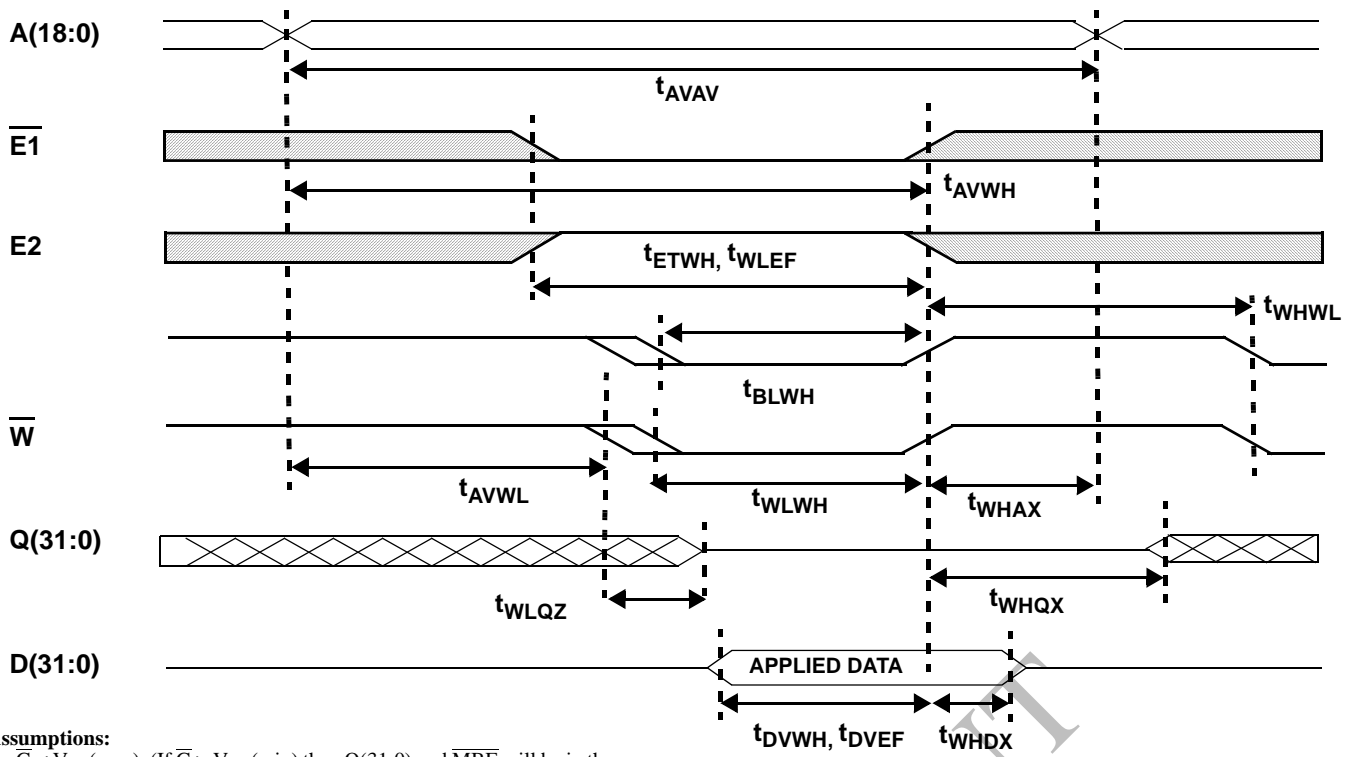
**Notes:**

\* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Tested with  $\overline{G}$  high.

2. Three-state is defined as 200mV change from steady-state output voltage.

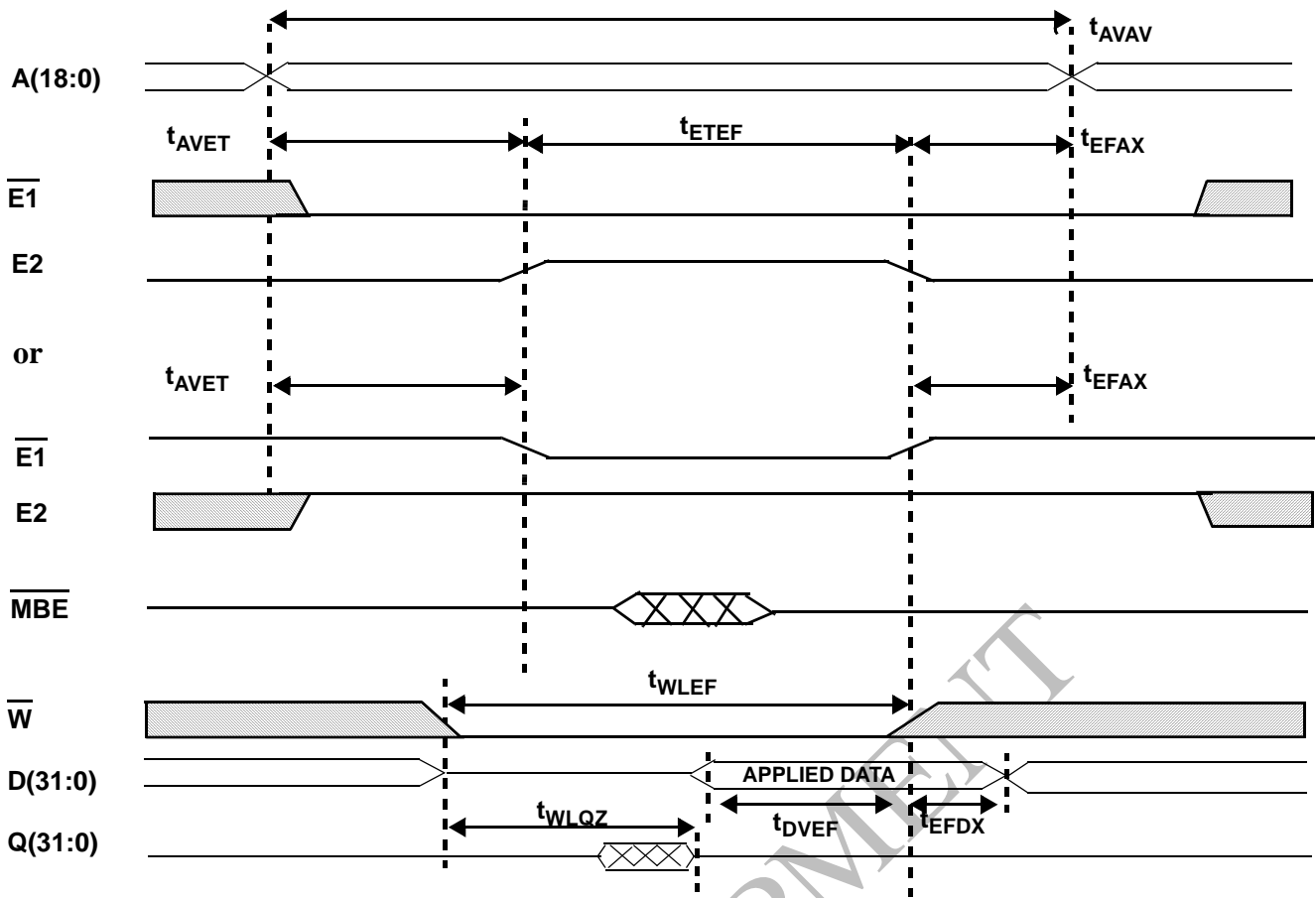




**Assumptions:**

1.  $\overline{G} \leq V_{IL}(\text{max})$ . (If  $\overline{G} \geq V_{IH}(\text{min})$  then Q(31:0) and  $\overline{MBE}$  will be in three-state for the entire cycle.)
2.  $\overline{\text{Busy}} \geq V_{OH}(\text{min})$

Figure 4a. SRAM Write Cycle 1:  $\overline{W}$  - Controlled Access



**Assumptions & Notes:**

1.  $\overline{G} \leq V_{IL}(\text{max})$ . (If  $\overline{G} \geq V_{IH}(\text{min})$  then Q(31:0) and  $\overline{MBE}$  will be in three-state for the entire cycle.)
2. Either  $\overline{E1}$  / E2 scenario can occur.
3.  $\overline{\text{Busy}} \geq V_{OH}(\text{min})$

**Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access**

**AC CHARACTERISTICS for EDAC FUNCTION (Pre and Post-Radiation)\***

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening,  $V_{DD1} = V_{DD1}(\text{min})$ ,  $V_{DD2} = V_{DD2}(\text{min})$ )

| SYMBOL       | PARAMETER                                    | MIN MAX     |     | UNIT | FIGURE |
|--------------|--|-------------|-----|------|--------|
|              |  | MIN         | MAX |      |        |
| $t_{AVAV1}$  | Address valid to address valid               |             | 100 | ns   | 5a     |
| $t_{AVCL}$   | Address valid to control low                 |             | 100 | ns   | 5a     |
| $t_{AVEX}$   | Address valid to enable valid                |             | 200 | ns   | 5a     |
| $t_{WTBL}^1$ | User Programmable - warning true to busy low | See Table 4 |     |      | 5b     |
| $t_{BLEX}$   | Busy low to enable true                      |             | 25  | ns   | 5b     |
| $t_{BLBH}$   | Busy low to busy high                        | 50          | 75  | ns   | 5b     |
| $t_{BHEV}$   | Busy high to enable valid                    | 0           |     | ns   | 5b     |
| $t_{BHWf}$   | Busy high warning false                      |             | 25  | ns   | 5b     |

Notes:

\* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. See Table 4 for User Programmable information.

**Table 4: EDAC Programming Configuration Table**

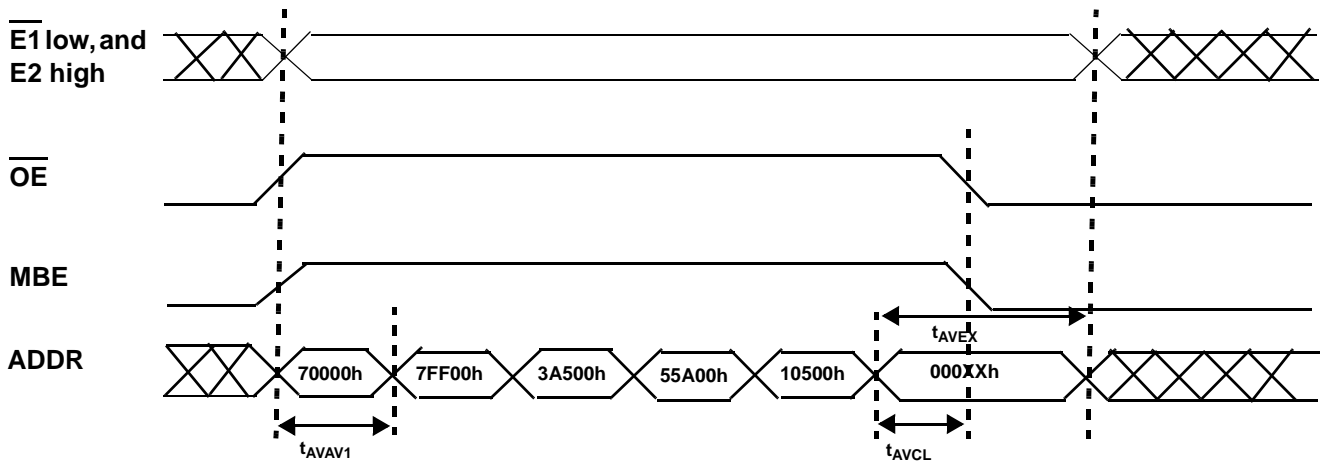
| DATA BIT | PARAMETER                     | MIN MAX |    | FUNCTION   |
|----------|-------------------------------|---------|----|--|
| A 0 - 3  | Scrub Rate <sup>1</sup>       | 0       | 15 | As Scrub Rate changes from 0 - 15, then the interval between Scrub cycles will change as follows:<br>0 = 20 MHz      6 = 312 kHz      11 = 9.76 kHz<br>1 = 10 MHz      7 = 156 kHz      12 = 4.88 kHz<br>2 = 5 MHz      8 = 78 kHz      13 = 2.44 kHz<br>3 = 2.5 MHz      9 = 39 kHz      14 = 1.22 kHz<br>4 = 1.25 MHz      10 = 19.5 kHz      15 = .61 kHz<br>5 = 625 kHz    |
| A 4 - 7  | Busy Warning <sup>2</sup>     | 0       | 15 | If Busy Warning changes from 0 - 15, then the interval $t_{WTBL}$ between Busy and Busy Warning will change as follows:<br>0 = 0 ns      6 = 300 ns      11 = 550 ns<br>1 = 50 ns      7 = 350 ns      12 = 600 ns<br>2 = 100 ns      8 = 400 ns      13 = 650 ns<br>3 = 150 ns      9 = 450 ns      14 = 700 ns<br>4 = 200 ns      10 = 500 ns      15 = 750 ns<br>5 = 250 ns |
| A 8      | Bypass EDAC Bit <sup>3</sup>  | 0       | 1  | If 0, then normal EDAC operation will occur.<br>If 1, then EDAC will be bypassed.  |
| A 9      | Read / Write Control Register | 0       | 1  | If 0, then DQ 0 - 8 will be written into the Control Register<br>If 1, then DQ 0 - 8 will be asserted on the Data Buss   |

Notes:

1. Default Scrub Rate is 312 KHz.

2. The default for  $t_{WTBL}$  is 500 ns.

3. The default state for A8 is 0.



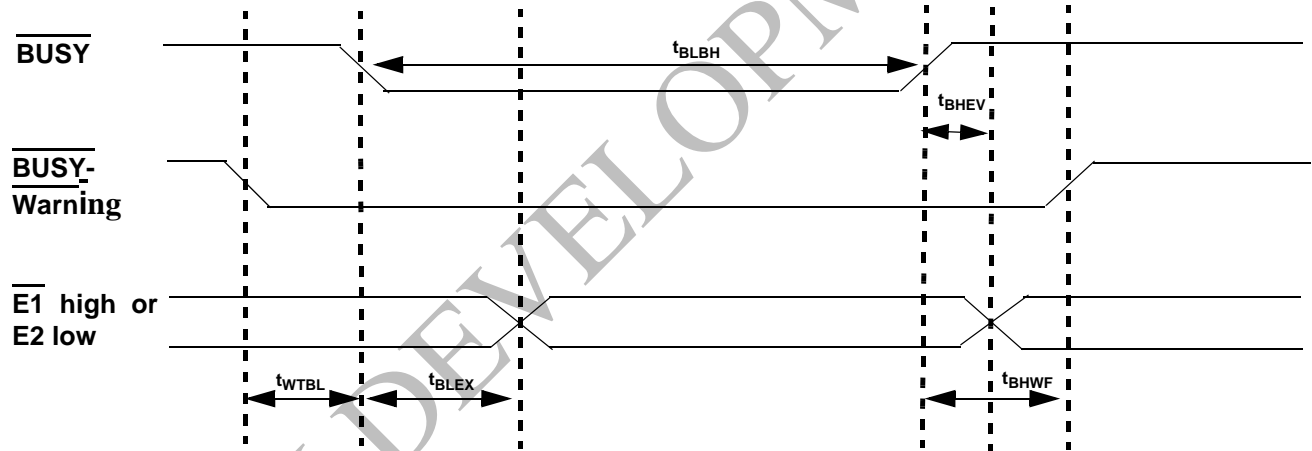
**Note:**

1.  $\overline{MBE}$  is driven high by the user.
2. Lower 8 bits of the last address are used to configure the control register.

**Assumptions:**

1.  $\overline{Busy} \geq V_{OH}$  before the start of the configuration cycle. Ignore  $\overline{Busy}$  during configuration cycle.

Figure 5a. Writing Control Register



**Assumptions:**

1. The conditions pertain to both a Read or Write.

Figure 5b. Scrub Cycle

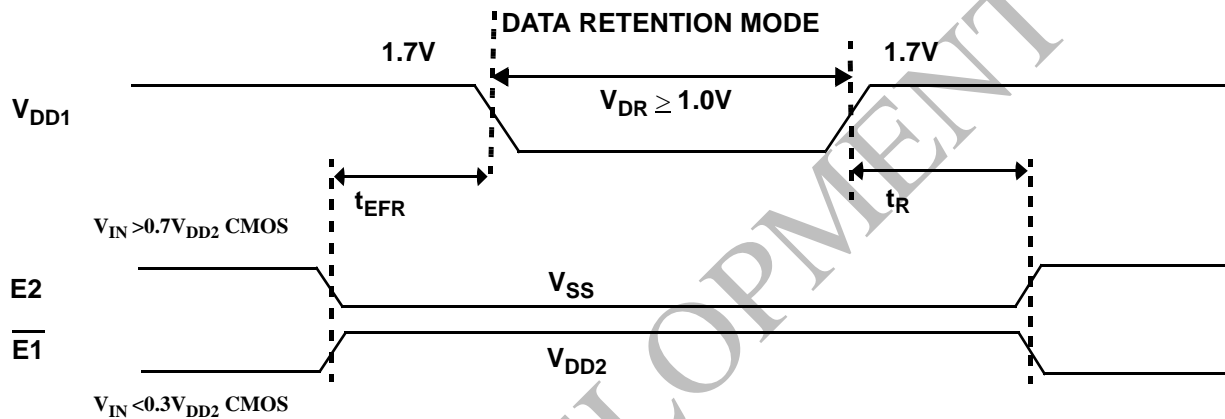
**DATA RETENTION CHARACTERISTICS (Pre and Post-Radiation)\* ( $V_{DD2} = V_{DD2}(\text{min})$ , 1 Sec DR Pulse)**

| SYMBOL          | PARAMETER                            | MINIMUM    | MAXIMUM | UNIT          |
|-----------------|--------------------------------------|------------|---------|---------------|
| $V_{DR}$        | $V_{DD1}$ for data retention         | 1.0        |         | V             |
| $I_{DDR}^1$     | Data retention current               |            | 600     | $\mu\text{A}$ |
|                 | -40°C                                |            | 600     | $\mu\text{A}$ |
|                 | -55°C                                |            | 600     | $\mu\text{A}$ |
|                 | 25°C                                 |            | 600     | $\mu\text{A}$ |
|                 | 125°C                                |            | 12      | mA            |
| $t_{EFR}^{1,2}$ | Chip deselect to data retention time | 0          |         | ns            |
| $t_R^{1,2}$     | Operation recovery time              | $t_{AVAV}$ |         | ns            |

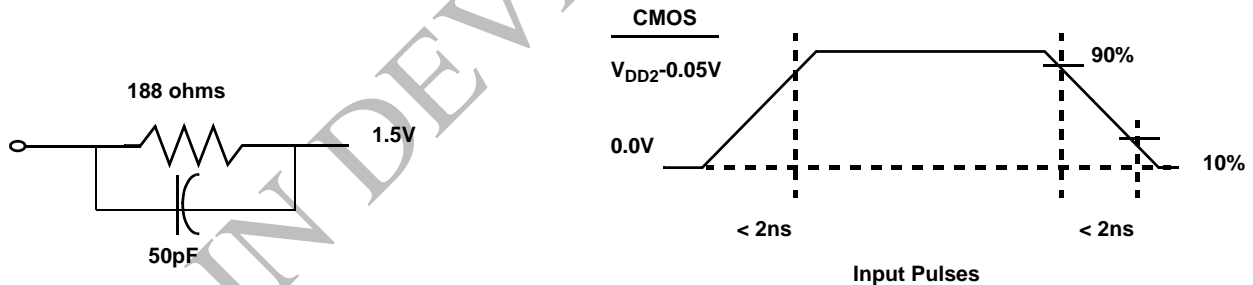
**Notes:**

\* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

- $\overline{E1} = V_{DD2}$  or  $E2 = V_{SS}$  all other inputs =  $V_{DD2}$  or  $V_{SS}$
- $V_{DD2} = 0$  volts to  $V_{DD2}(\text{max})$



**Figure 6. Low  $V_{DD}$  Data Retention Waveform**

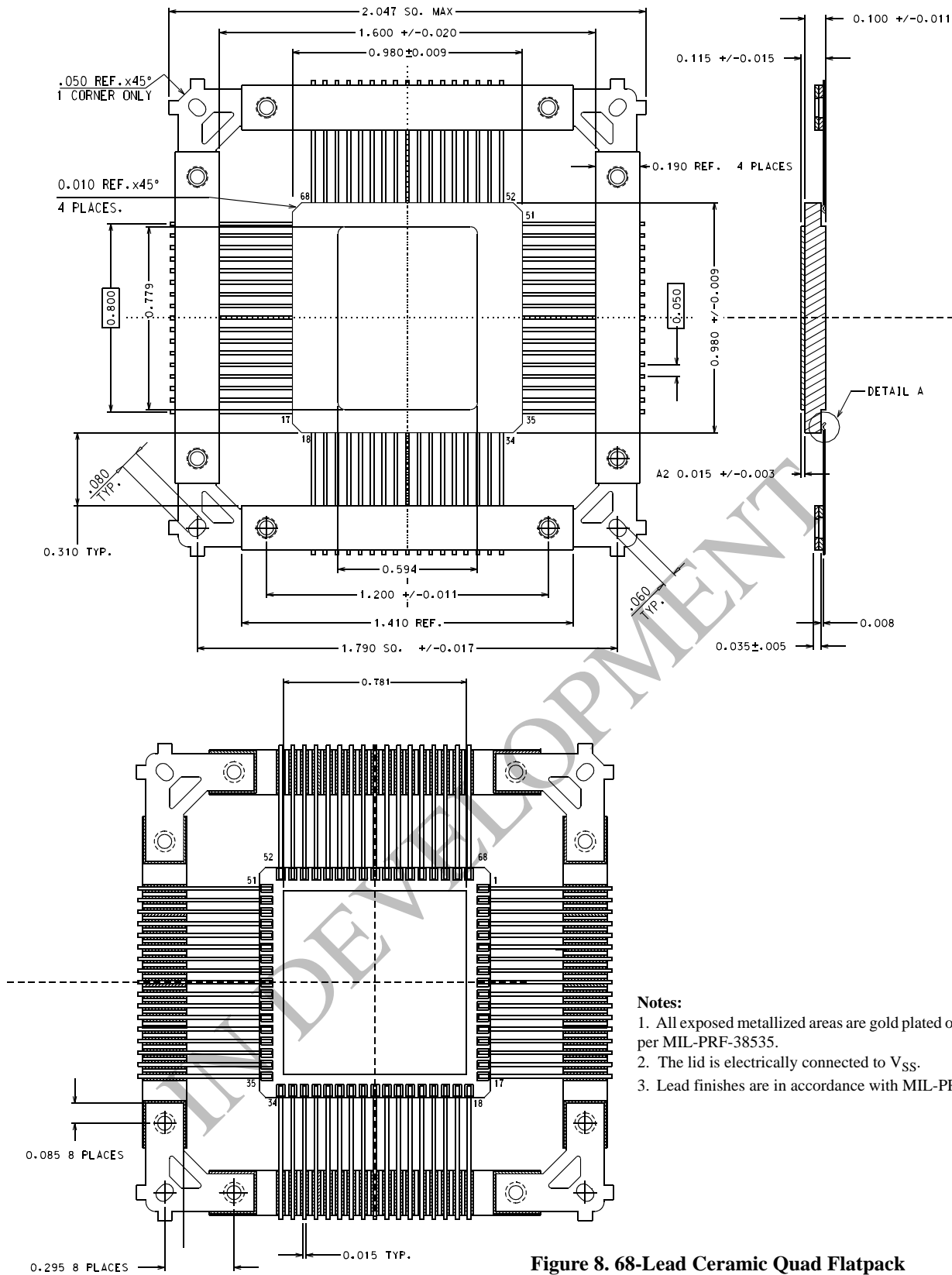


**Notes:**

- 50pF including scope probe and test socket.
- Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input =  $V_{DD2}/2$ ).

**Figure 7. AC Test Loads and Input Waveforms**

PACKAGING

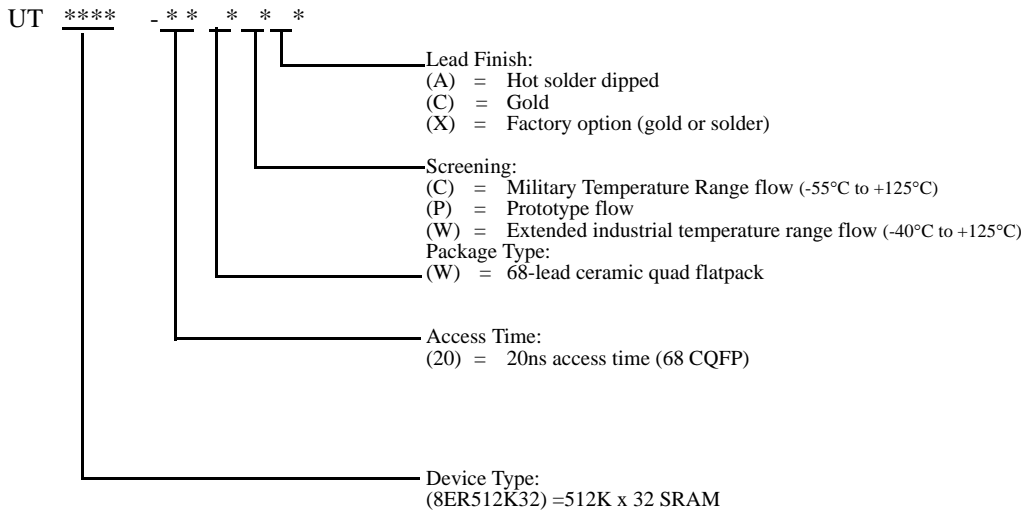


- Notes:**
1. All exposed metallized areas are gold plated over nickel per MIL-PRF-38535.
  2. The lid is electrically connected to  $V_{SS}$ .
  3. Lead finishes are in accordance with MIL-PRF-38535.

Figure 8. 68-Lead Ceramic Quad Flatpack

## ORDERING INFORMATION

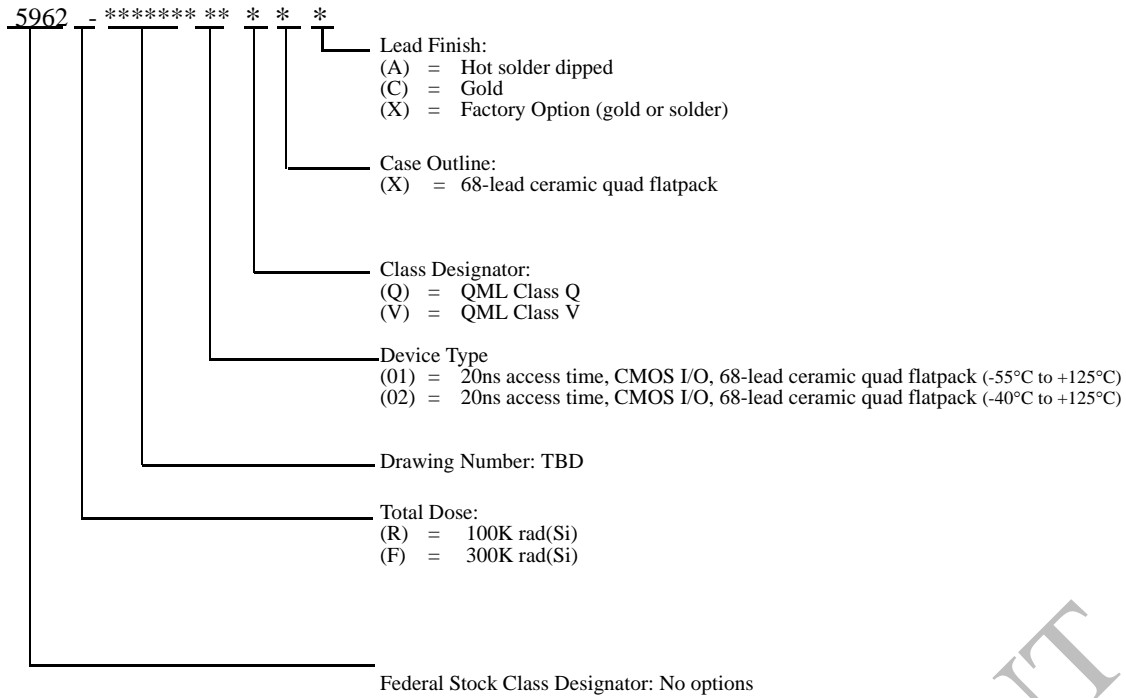
### 512K x 32 SRAM



#### Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

**512K x 32 SRAM: SMD**



**Notes:**

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

IN DEVELOPMENT



NOTES

IN DEVELOPMENT

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