ANALOG DEVICES

DAC-210

11-BIT VOLTAGE-OUTPUT D/A CONVERTER (10 BITS PLUS SIGN)

Precision Monolithics Inc.

FEATURES

- Complete ..... Includes Reference and Op Amp
- Bipolar Output ..... ±10V
- Sign-Magnitude Coding
- No Bipolar Offset Adjustment Required
- 10-Bit Linearity Maintained over Full Temperature
- Multiplying Operation
- Fast ..... 1.5μs Settling Time
- Monotonicity Guaranteed
- Reliable ..... 100% Burned-In
- Available in Die Form

GENERAL DESCRIPTION

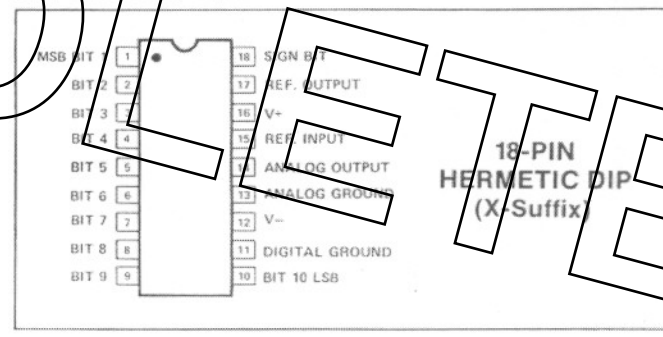
The DAC-210 is a complete, monolithic 10-bit plus sign DAC with a ±10V output. A precision voltage reference, a logic controlled polarity switch and output amplifier are included. Linearity, monotonicity, and full-scale temperature coefficient are guaranteed over the full operating temperature range. Ease of application is achieved by the **total** D/A system specs given for nonlinearity and zero-scale offset. System specs eliminate the complex error budget analysis required by less "complete" DACs. Sign-magnitude coding minimizes the "major-carry" zero-code errors inherent in offset coding schemes.

ORDERING INFORMATION†

TEMPCO (ppm/°C)	NL %FS	COMMERCIAL TEMPERATURE
±40	±0.05	DAC210EX
±60	±0.05	DAC210FX
±30 Typ	±0.10	DAC210GX

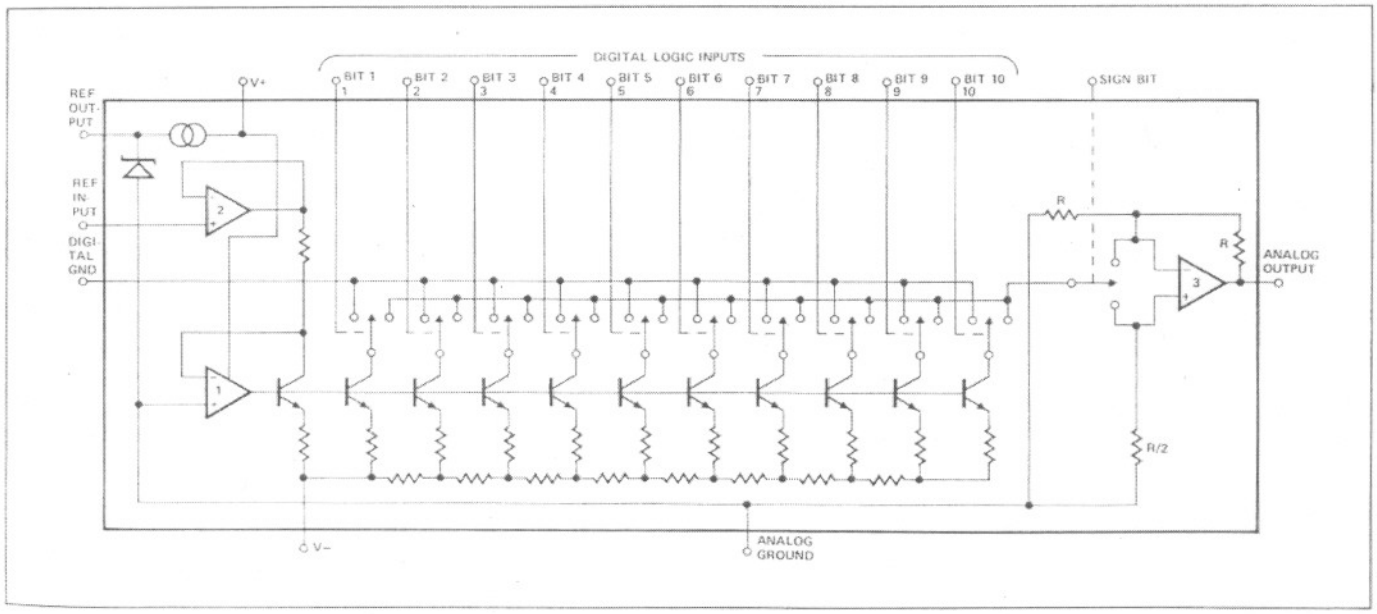
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

PIN CONNECTION



18-PIN HERMETIC DIP (X-Suffix)

SIMPLIFIED SCHEMATIC



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DIGITAL-TO-ANALOG CONVERTERS

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$ for E, F and G grades, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-210E MIN	DAC-210E TYP	DAC-210E MAX	DAC-210F MIN	DAC-210F TYP	DAC-210F MAX	DAC-210G MIN	DAC-210G TYP	DAC-210G MAX	UNITS
Resolution		Including Sign	11	—	—	11	—	—	11	—	—	Bits
Monotonicity			10	—	—	10	—	—	9	—	—	Bits
Nonlinearity	NL	$T_A = 25°C$	—	—	±0.05	—	—	±0.05	—	—	±0.10	%FS
		T_A = Full Range	—	—	±0.05	—	—	±0.10	—	—	—	
Zero-Scale Offset Voltage	V_{ZS}	$T_A = 25°C$	—	—	±0.05	—	—	±0.1	—	—	—	%FS
		T_A = Full Range	—	—	±0.06	—	—	±0.1	—	—	—	
Bipolar Full Range Voltage Symmetry ($\lvert V_{FR+} \rvert - \lvert V_{FR-} \rvert$)	V_{FRS}	$T_A = 25°C$	—	—	40	—	—	60	—	—	80	mV
		T_A = Full Range	—	—	50	—	—	70	—	50	—	
Zero-Scale Voltage Symmetry ($\lvert V_{ZS+} \rvert - \lvert V_{ZS-} \rvert$)	V_{ZSS}	T_A = Full Range	—	—	1	—	—	1	—	—	2	mV
Gain Tempco	T_C	Internal Reference	—	—	±40	—	—	±60	—	±30	—	ppm/°C
		External Reference	—	±15	—	—	±30	—	—	±30	—	
Output Voltage Range	V_{OR+}	R_L = 2kΩ	+10.0	—	+11.5	+10.0	—	+11.5	+10.0	—	+11.5	V
	V_{OR-}		−11.5	—	−10.0	−11.5	—	−10.0	−11.5	—	−10.0	
Differential Nonlinearity	DNL	$T_A = 25°C$	—	—	±1	—	—	±1	—	—	±1	LSB
Settling Time	T_S	(Note 4)	—	1.5	—	—	1.5	—	—	1.5	—	µs
Reference Input Slew Rate	SR_{REF}		—	1.5	—	—	1.5	—	—	1.5	—	V/µs
Reference Input Impedance	Z_{IN}		—	200	—	—	200	—	—	200	—	MΩ
Reference Input Multiplying Range	IVR_m	For 0.1% Typical Nonlinearity (Note 1)	3	—	10	3	—	10	3	—	10	V
Reference Amplifier Bandwidth	BW		—	1	—	—	1	—	—	1	—	MHz
Reference Output Voltage	V_{REF}	(Note 5)	—	7.6	—	—	7.6	—	—	7.6	—	V
DAC Output Current	I_O	(Note 3)	0	—	5	0	—	5	0	—	5	mA
Reference Output Current	I_{REF}		—	100	—	—	100	—	—	100	—	µA
Output Slew Rate	SR_O		—	10	—	—	10	—	—	10	—	V/µs
Logic Input Current	I_{IN}	$-5V \le V_I \le V+$	—	±2	±10	—	±2	±10	—	±2	±10	µA
Logic "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	—	—	0.8	V
Logic "1" Input Voltage	V_{INH}		2.0	—	—	2.0	—	—	2.0	—	—	V
Power Supply Sensitivity (Note 2)	P_{SS}	$T_A = 25°C$	—	0.015	0.05	—	0.015	0.05	—	0.015	0.1	$\%V_{FS}/V$
		T_A = Full Range	—	0.015	0.1	—	0.015	0.1	—	0.015	0.1	
Positive Supply Current	I+		—	7	9	—	7	9	—	7	9	mA
Negative Supply Current	I−		—	−10	−12	—	−10	−12	—	−10	−12	mA

NOTES:
1. Guaranteed by design.
2. Power Supplies – The DAC-210 will operate within specifications for power supplies ranging from ±12V to ±18V. Power supplies should be bypassed near the package with a 0.1µF disk capacitor.
3. Guaranteed by V_{OR} test, R_L = 2kΩ.
4. To within ±5mV of final settled value, (±10 volt output step, R_L = 2kΩ.)
5. For applications where long-term stability is critical, an external voltage reference is recommended (See PMI REF01/02).

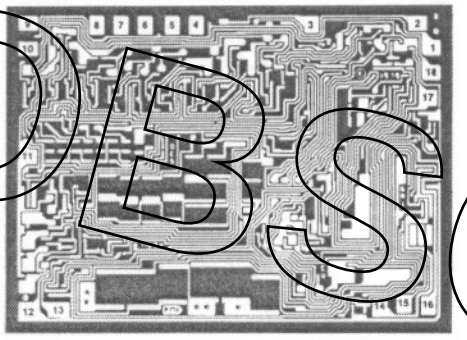
ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
DAC-210E, F, G ..... 0°C to +70°C
Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
V+ Supply to Analog Ground ..... 0 to +18V
Analog Ground to Digital Ground ..... 0 to ±0.5V
Logic Inputs to Digital Ground ..... –5V to (V+ –0.7V)
V+ Supply to V– Supply 36V
Internal Reference Output Current 300µA
Reference Input Voltage ..... 0 to +10V
Lead Temperature (Soldering, 60 sec) ..... 300°C
Output Short-Circuit Duration ..... Indefinite
(Short-circuit may be ground to either supply)

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	79	11	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

DICE CHARACTERISTICS



1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6
7. B7
8. B8
9. B9
10. B10 (LSB)
11. DIGITAL GROUND
12. V–
13. ANALOG GROUND
14. ANALOG OUTPUT
15. REFERENCE INPUT
16. V+
17. REFERENCE OUTPUT
18. SIGN BIT

NOTE: For 5 volt output option (+5V only) * is connected to analog output. ** is connected to analog ground.

DIE SIZE 0.118 × 0.087 inch, 10,266 sq. mils
(2.997 × 2.210 mm, 6.623 sq. mm)
For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, +10V full-scale output, $T_A = 25°C$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC-210N LIMIT	DAC-210G LIMIT	DAC-210GR LIMIT	UNITS
Resolution	Bipolar Output	11	11	11	Bits MAX
	Unipolar Output	10	10	10	
Monotonicity		10	9	8	Bits MIN
Nonlinearity		±0.05	±0.1	±0.2	%FS MAX
Zero-Scale Offset	Sign-Bit High, All Other Inputs Low	±5	±10	±10	mV MAX
Zero-Scale Symmetry	$V_{ZS+} - V_{ZS-}$	±1	±2	±2	mV MAX
Full-Scale Bipolar Symmetry	±10V Full-Scale	±40	±80	±80	mV MAX
Power Supply Rejection	$V_S = \pm 12V$ to $\pm 18V$	0.05	0.05	0.1	$\%V_{FS}/V$ MAX
Power Consumption	$I_{OUT} = 0$	300	300	300	mW MAX
Logic Input "0"		0.8	0.8	0.8	V MAX
Logic Input "1"		2	2	2	V MIN
Analog Output Voltage (All Bits High)	V+ (Sign-Bit High)	11.5	11.5	11.5	V MAX
		10	10	10	V MIN
	V– (Sign-Bit Low)	–10	–10	–10	V MAX
		–11.5	–11.5	–11.5	V MIN
Differential Nonlinearity		±1	±1	±1	LSB MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

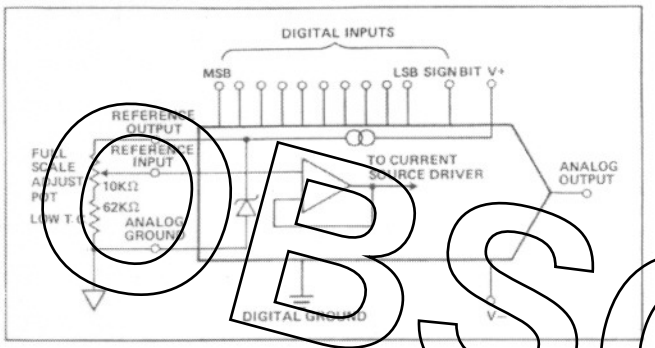
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and +10V full-scale output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-210N TYPICAL	DAC-210G TYPICAL	DAC-210GR TYPICAL	UNITS
Full-Scale Tempco	TCV_{FS}	Internal Reference	15	30	30	ppm/°C
Settling Time ($T_A = 25°C$)	t_S	To ±1/2 LSB 10 Volt Step	1.5	1.5	1.5	µs
Logic Input Current	I_{IN}	$T_A = 25°C$	1	1	1	µA

CONNECTION INFORMATION

FULL-SCALE ADJUSTMENT — Full-scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of ≥ 75kΩ may be used.

FULL SCALE ADJUSTMENT CIRCUIT



REFERENCE INPUT BYPASS — Lowest noise and fastest settling operation will be obtained by bypassing the reference input to analog ground with a 0.01μF disk capacitor.

VARIABLE REFERENCES — Operation as a two-quadrant multiplying DAC is achieved by applying an analog input varying between 0 and +10V to the reference input terminal. The DAC output is then the scaled product of this voltage and the digital input.

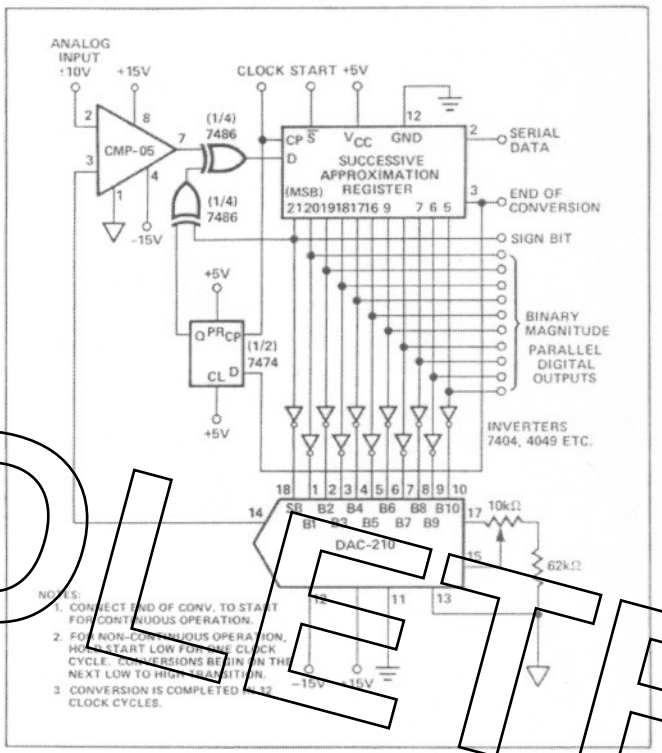
GROUNDING — For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the power supply, so that the large digital currents do not flow through the analog ground path.

SIGN — MAGNITUDE CODING TABLE

	SIGN-BIT	MSB									LSB
+FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	1	1	1
+HALF-SCALE	1	1	0	0	0	0	0	0	0	0	0
ZERO-SCALE (+)	1	0	0	0	0	0	0	0	0	0	0
ZERO-SCALE (−)	0	0	0	0	0	0	0	0	0	0	0
−HALF-SCALE	0	1	0	0	0	0	0	0	0	0	0
−FULL-SCALE +1 LSB	0	1	1	1	1	1	1	1	1	1	1

TYPICAL APPLICATIONS

10-BIT SIGN-MAGNITUDE ADC



APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATION — For applications not requiring full 10-bit resolution, unused logic inputs should be tied to ground.

CAPACITIVE LOADING — The output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE OUTPUT — For best results, reference output current should not exceed 100μA.

INTERFACING WITH CMOS LOGIC — The DAC-210's logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+. This wide input voltage range allows direct CMOS Interface with no additional components.

USE WITH EXTERNAL REFERENCES — Positive polarity external reference voltages referred to analog ground may be applied to the reference input terminal to improve full-scale tempco, to provide tracking to other system elements, or to slave a number of DAC-210's to the reference output of any one of them.