U74AHCT3G06

CMOS IC

INVERTER WITH OPEN-DRAIN OUTPUT

TSSOP-8

■ DESCRIPTION

The **U74AHCT3G06** is a high-speed Si-gate CMOS device which provides three inverting buffers with open-drain outputs. For digital operation this device must have a pull-up resistor to establish a logic HIGH-level.

The **U74AHCT3G06** is compatible of TTL input switching levels and has supply voltage range from 4.5V to 5.5V.

■ FEATURES

* Low power supply 1.0μA at 5.5V
* Up to 5.5V inputs accept voltages
* Low power dissipation
* Balanced propagation delays
* High noise immunity
* Output capability standard (open drain)

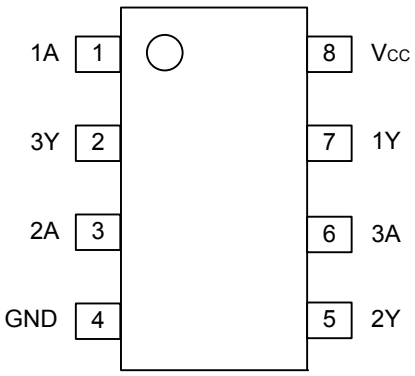
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHCT3G06L-P08-R	U74AHCT3G06G-P08-R	TSSOP-8	Tape Reel
U74AHCT3G06L-P08-T	U74AHCT3G06G-P08-T	TSSOP-8	Tube

U74AHCT3G06L-P08-R
(1)Packing Type
(2)Package Type
(3)Lead Free

(1) R: Tape Reel, T: Tube
(2) P08: TSSOP-8
(3) G: Halogen Free, L: Lead Free

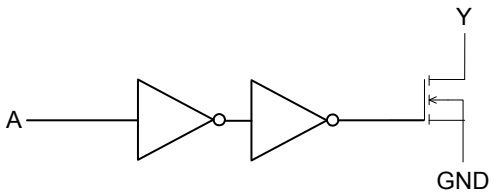
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	OUTPUT(Y)
L	Z
H	L

■ LOGIC DIAGRAM (each gate)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ 7.0	V
Output Voltage	V_{OUT}	-0.5 ~ 7.0(active mode)	V
Output Voltage		-0.5 ~ 7.0(high-impedance mode)	V
V_{CC} or GND Current	I_{CC}	±75	mA
Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OUT}	±20	mA
Operating Temperature	T_{OPR}	-40 ~ + 85	
Storage Temperature	T_{STG}	-65 ~ + 150	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	Active mode	0		V_{CC}	V
		High-impedance mode	0		6.0	V
Input Rise or Fall Times	t_R, t_F	V_{CC} = 5.0 ± 0.5V			20	ns/V

■ ELECTRICAL CHARACTERISTICS(T_A=25)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC} = 4.5 V to 5.5 V		2.0			V
Low-Level Input Voltage	V_{IL}	V_{CC} = 4.5 V to 5.5 V				0.8	V
Low-Level Output Voltage	V_{OL}	V_{CC} =4.5V,	I_O = 50 μA		0	0.1	V
		V_I = V_{IH} or V_{IL}	I_O = 8.0 mA			0.36	
Input Leakage Current	$I_{I(LEAK)}$	V_I =5.5V or GND,V_{CC}=0V to 5.5V				0.1	μA
3-State output OFF-State Current	I_{OZ}	V_{CC}=5.5V,V_I =V_{IH} or V_{IL},V_O=V_{CC} or GND				±.025	μA
Quiescent Supply Current	I_{CC}	V_{CC} =5.5V,V_I = V_{CC} or GND, I_O = 0				1.0	μA
Additional Quiescent Supply Current	ΔI_{CC}	V_{CC}=5.5V,One input at 3.4V, Other inputs at V_{CC} or GND, I_{OUT} = 0				1.35	mA
Input Capacitance	C_{IN}	V_I=V_{CC} or GND			1.5	10	pF

■ SWITCHING CHARACTERISTICS (T_A=25 , $t_R = t_F \leq 3.0$ ns)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay from Input (A) to Output(Y)	t_{PZL}	V_{CC} 4.5V to 5.5V	C_L 15pF	-	3.0	5.3	ns
	t_{PLZ}			-	3.2	4.6	
	t_{PZL}		C_L 50pF	-	4.2	7.5	ns
	t_{PLZ}			-	4.5	7.0	

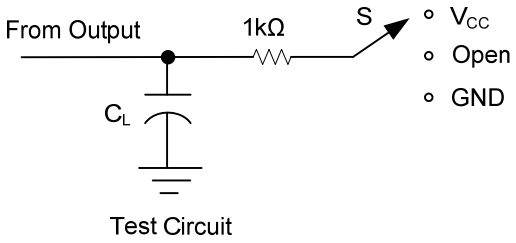
■ OPERATING CHARACTERISTICS (T_A =25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNIT
Power Dissipation Capacitance	C_{PD}	C_L=50pF, f=1MHz (Note1, 2)	4.5	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = number of inputs switching;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

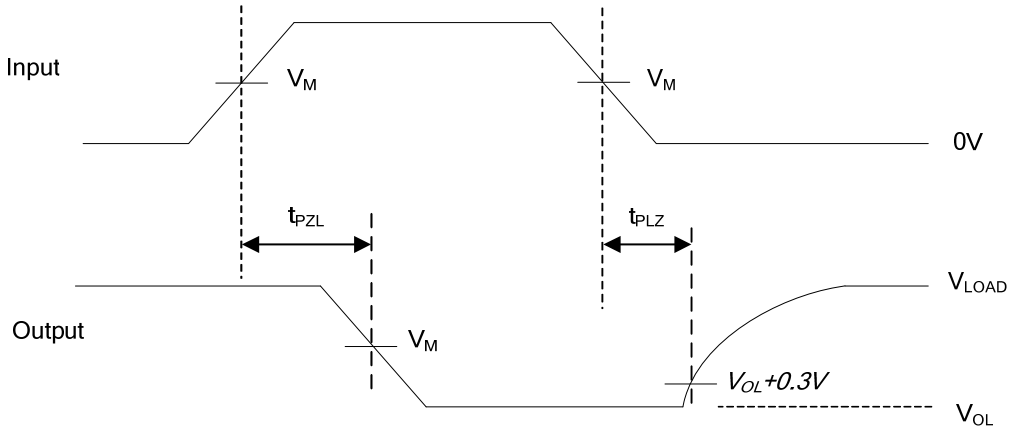
■ TEST CIRCUIT AND WAVEFORMS



Test Circuit

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{CC}

V_I	V_M	V_M
GND to V_{CC}	50%V_{CC}	50%V_{CC}



Voltage Waveforms Enable and Disable Times

Note: C_L includes probe and jig capacitance.
P_{RR} ≤1MHz, Z_O = 50Ω, t_R ≤3ns, t_F ≤3ns.