

ML67Q4060/61/50/51

32-bit General-Purpose ARM-Based Microcontroller

OVERVIEW

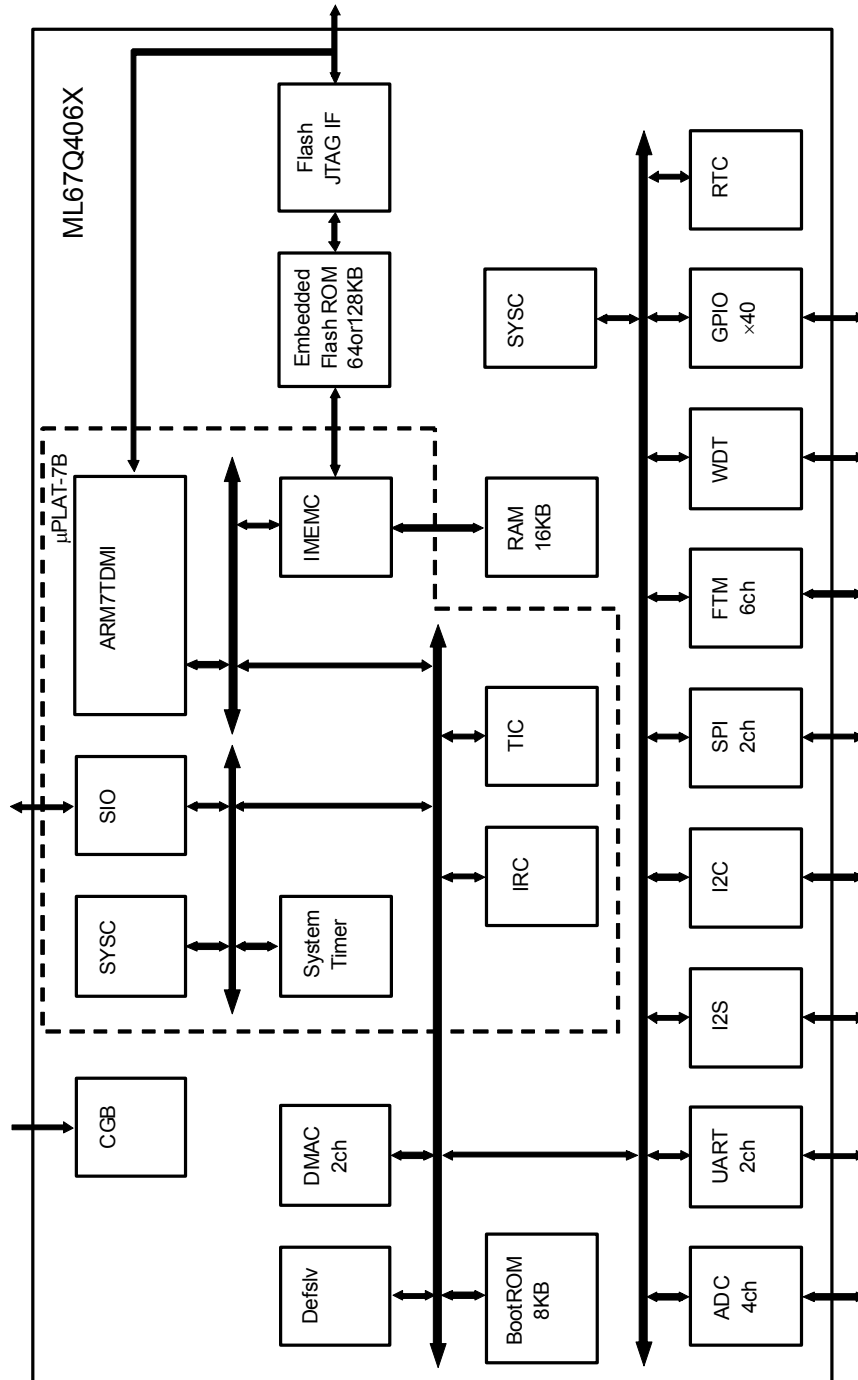
This LSI is a general-purpose microcontroller that integrates peripheral functions such as I2C, I2S, and various serial interfaces. It uses the ARM7TDMI 32-bit RISC CPU developed by ARM Limited as its core. The following describes the features of the ML67Q4050/ML67Q4060 Series.

FEATURES

- CPU ATM7TDMI up to 33.33MHz
- Internal memory 16KB RAM processor bus connection
Built-in Flash ROM processor bus connection of the 128KB(ML67Q4051 and ML67Q4061) or 64KB (ML67Q4050 and ML67Q4060)
- External memory controller (Function for the ML67Q4050 series only)
Setting of programmable access timing for each space
ROM (FLASH) access function
SRAM access function
External I/O access function
- Interrupt controller/extended interrupt controller
FIQ: 1 source (NMI pin)
IRQ: 31 sources (40 sources for the ML67Q4050 Series)
Seven levels of interrupt priorities can be set for each interrupt source.
- System timer 16-bit auto-reload timer: × 1ch
- SIO (UART) Full-duplex start-stop synchronization method
- DMA controller 2ch
- Watchdog timer 16-bit timer
- A/D converter 10-bit sequential comparison type × 4ch
- I2C bus controller Philips I2C bus specification Ver 2.1 conformed controller
- Flexible timer 16-bit timer × 6ch
Operable in each of the modes, Auto Reload Timer (ART)/Compare Out (CMO)/Pulse Width Modulation (PWM)/Capture (CAP)
- RTC Generates 1 second from 32.768 kHz
- I2S transmit/receive Connection interface for general-purpose DACs/ADCs. Conforms to Philips I2S (the Inter-IC Sound) specification
- GPIO Built-in GPIO of 8 bits × 1ch, 7 bits × 2ch, and 6 bits × 3ch
- UART 2 channels of serial communication function with FIFO
- SPI 2 channel of full duplex serial peripheral interface
- Clock Main clock oscillator (16 to 33.333MHz)
RTC clock oscillator (32.768kHz clock)
- Power management Power saving mode
CPU halt mode: Stops only the CPU clock.
STOP mode: Stops all the clocks of the chip except RTC
- Package 64pin TQFP(TQFP64-P-1010-0.50-K)
84pin LFBGA(P-LFBGA84-0909-0.80)
64pin WCSP(P-VFBGA64-5.09 × 4.84-0.50-W, P-VFLGA64-5.09 × 4.84-0.50-W)
144pin LQFP(LQFP144-P-2020-0.50-ZK)
144-pin LFBGA (P-LFBGA144-1111-0.80)

BLOCK DIAGRAM

ML67Q4060 Series



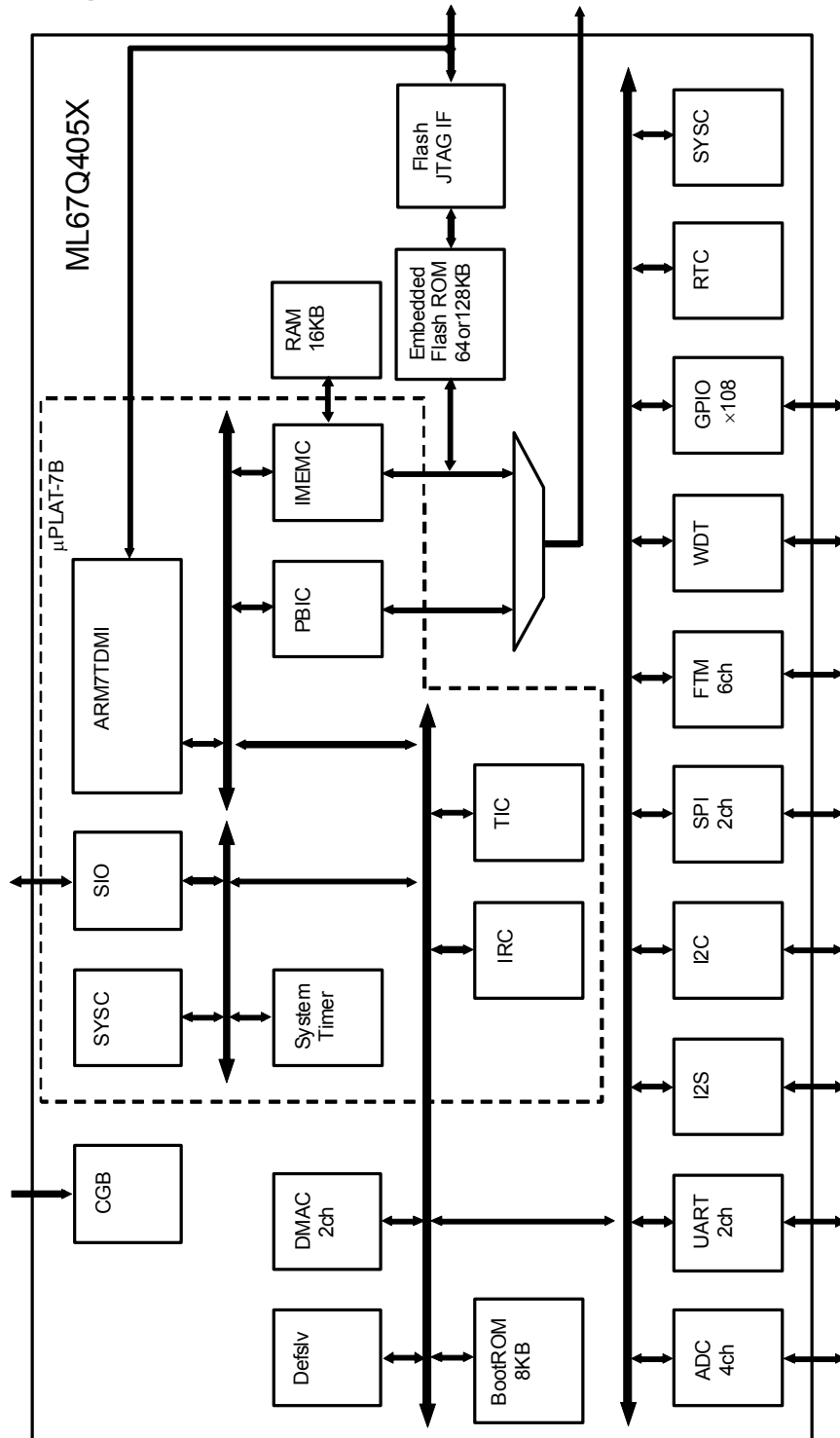
ML67Q4060 Series Block Diagram

Note:

ML67Q4060: Flash ROM 64KB

ML67Q4061: Flash ROM 128KB

ML67Q4050 Series



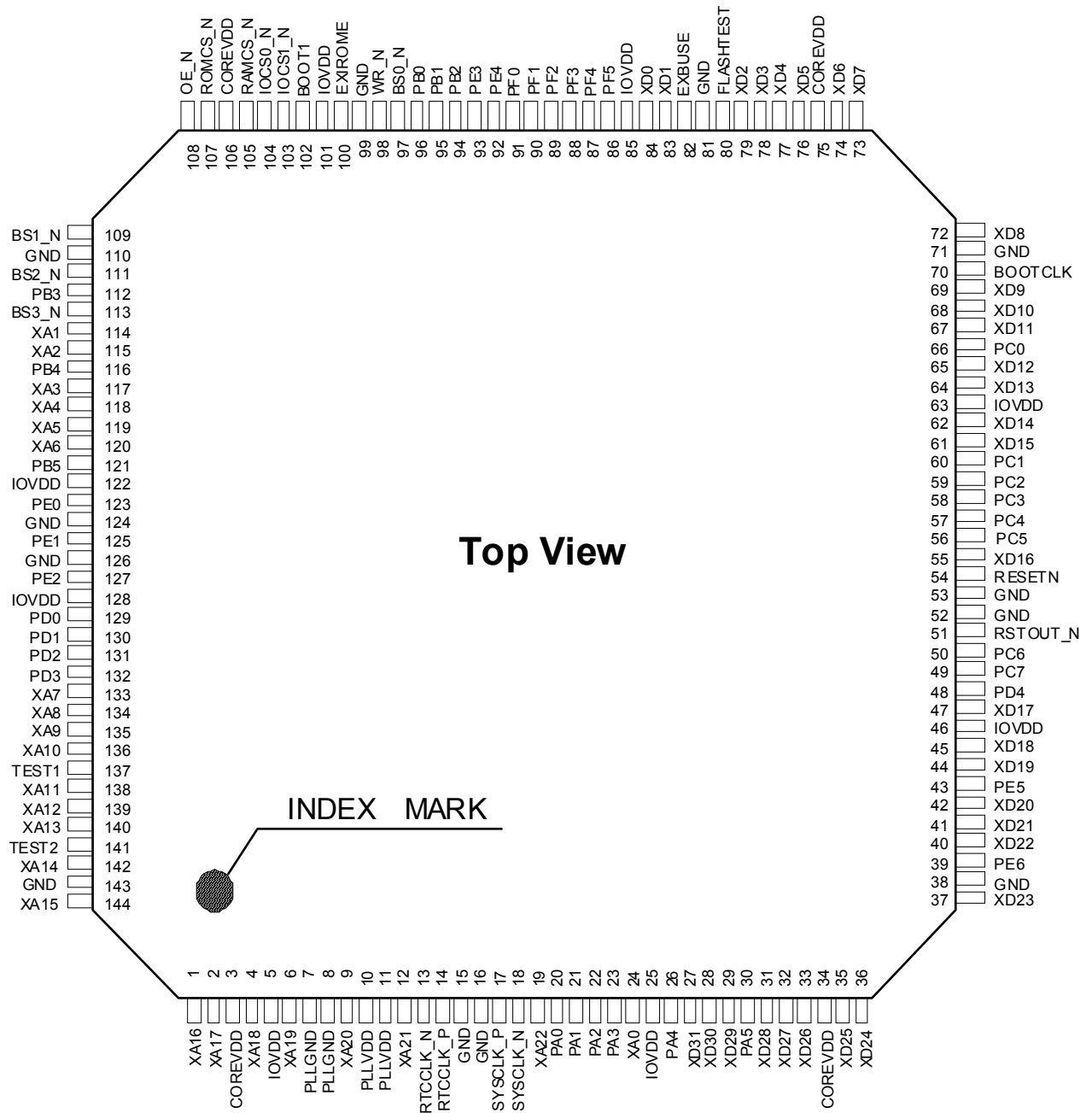
ML67Q4050 Series Block Diagram

Note:

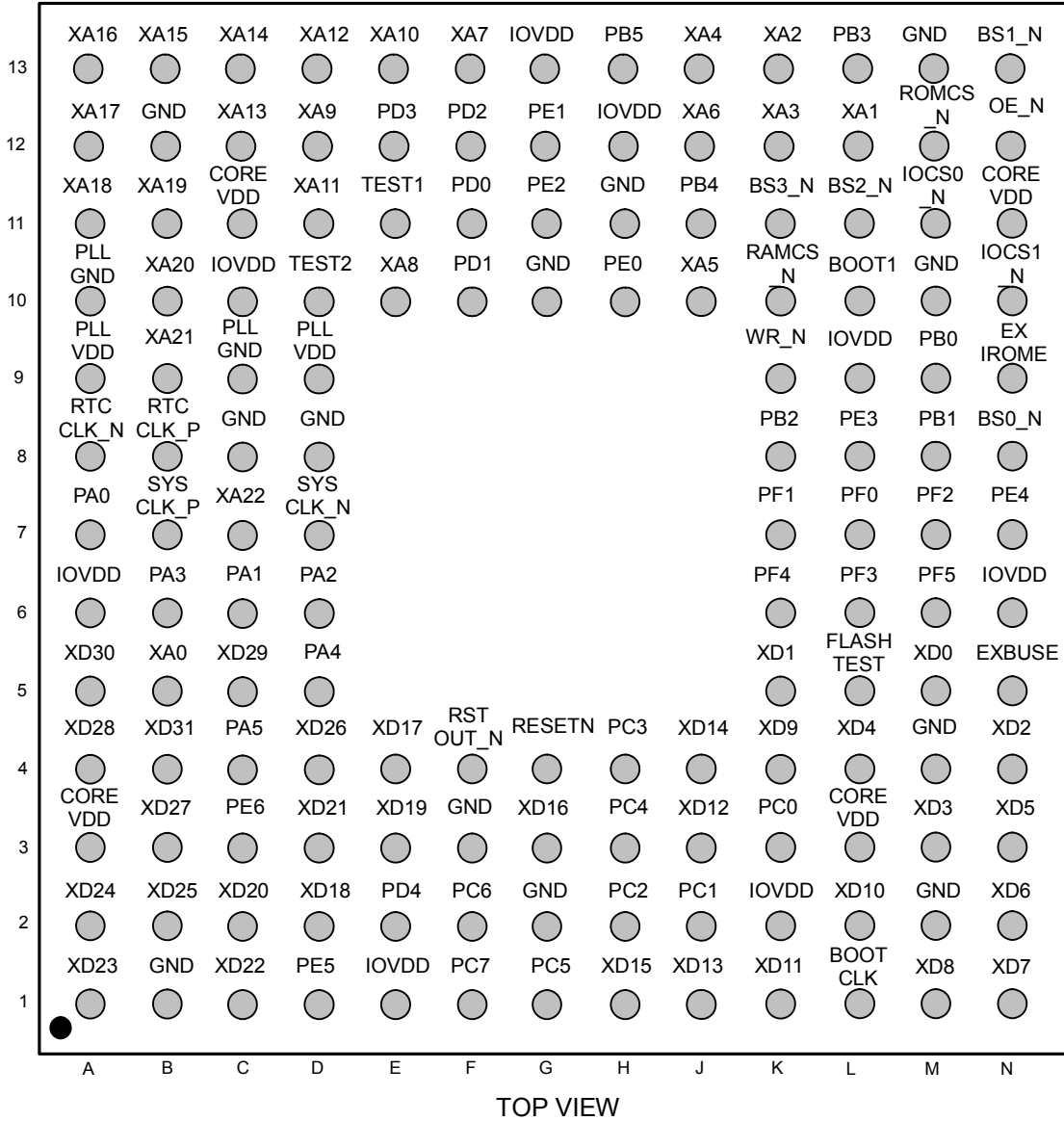
- ML67Q4050: Flash ROM 64KB
- ML67Q4051: Flash ROM 128KB

PIN CONFIGURATION

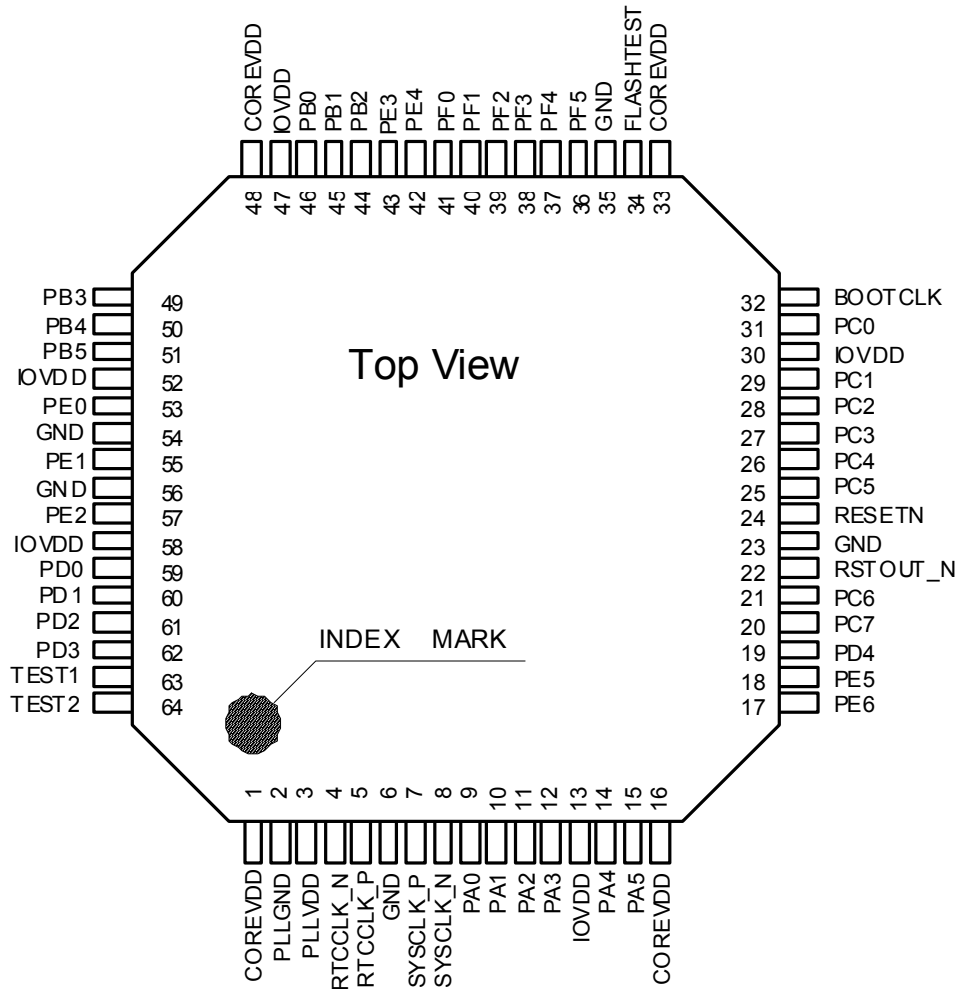
144pin LQFP (LQFP144-P-2020-0.50-ZK)



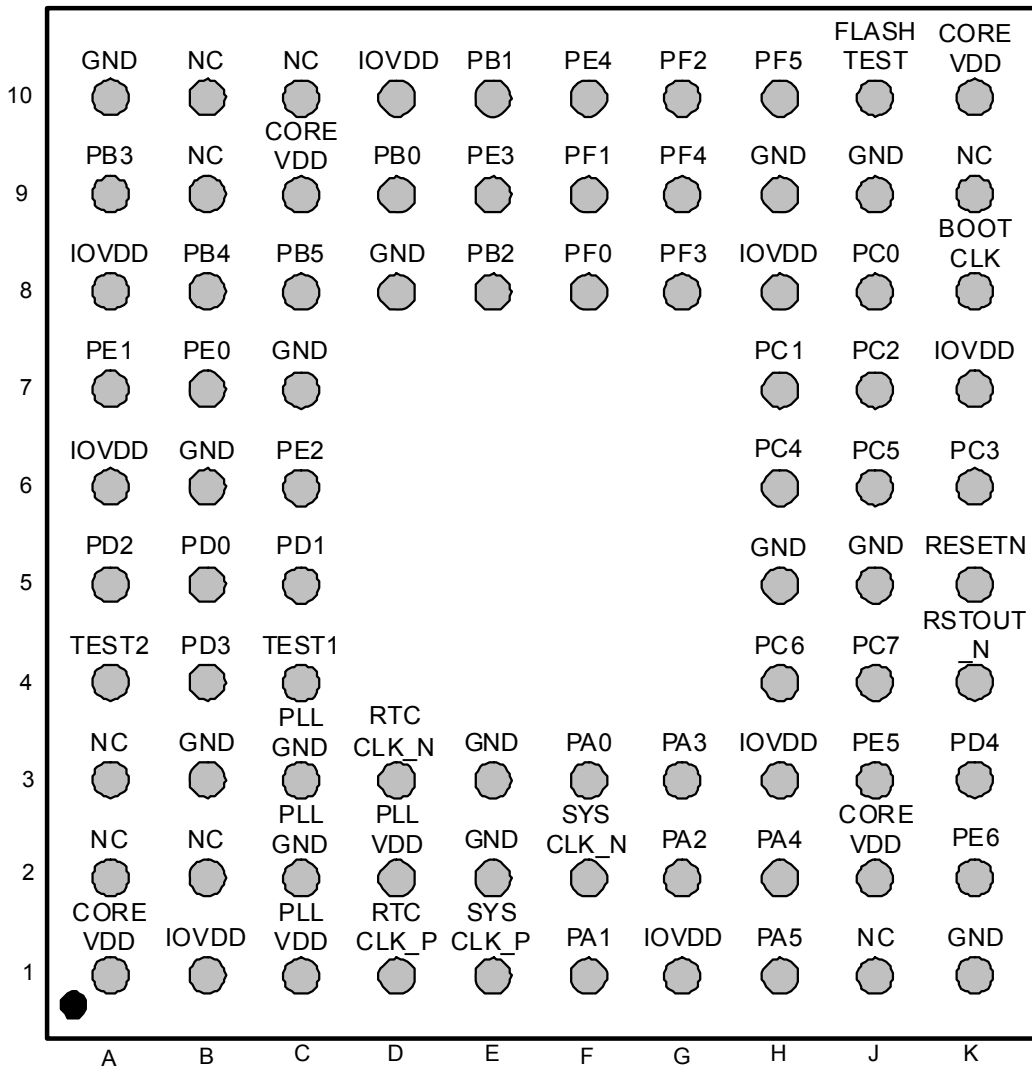
144pin LFBGA (P-LFBGA144-1111-0. 80)



64pin TQFP (TQFP64-P-1010-0.50-K)

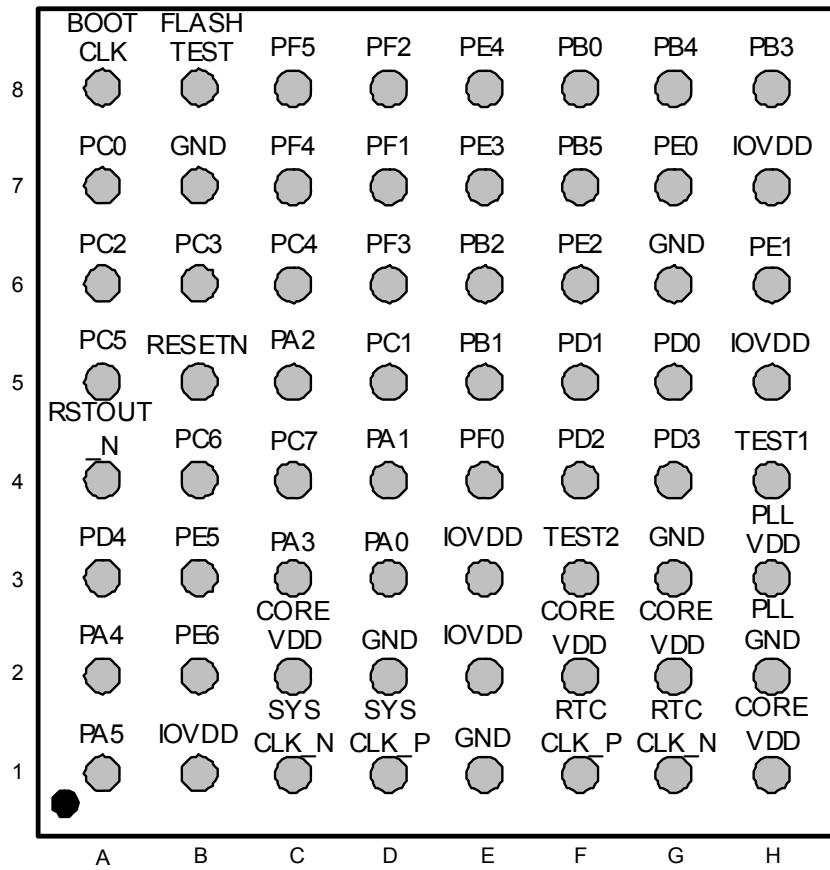


84pin LFBGA (P-LFBGA84-0909-0.80)



TOP VIEW

64pin WCSP (P-VFBGA64-5.09×4.84-0.50-W, P-VFLGA64-5.09×4.84-0.50-W)



TOP VIEW

PIN DESCRIPTIONS

Table 1-1 list the functions of all pins in the ML67Q4050/ML67Q4060 Series.

“I”, “O”, and “I/O” in each input/output column signify an input pin, output pin and input/output pin, respectively. IPU stands for “Internally Pulled Up”.

Table 1-1 List of ML67Q4050/ML67Q4060 Series Pin Functions (1 of 6)

Pin name	Primary function		Secondary function			Tertiary function			Setting at reset			IPU	Schmitt trigger circuit	Sink current [mA]	Pin assignment				
	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description				144 QFP	144 BGA	64 QFP	84 BGA	64 WCSP
RESETN	I	Reset input										○	○	—	54	G4	24	K5	B5
SYSCLK_P	I	Main clock										—	—	—	17	B7	7	E1	D1
SYSCLK_N	O	Main clock										—	—	—	18	D7	8	F2	C1
RTCCLK_P	I	RTC clock										—	—	—	14	B8	5	D1	F1
RTCCLK_N	O	RTC clock										—	—	—	13	A8	4	D3	G1
TEST1	I	Test pin 1										—	—	—	137	E11	63	C4	H4
TEST2	I	Test pin 2										—	—	—	141	D10	64	A4	F3
IOVDD	-	I/O power supply										—	—	—	*[1]	*[6]	*[11]	*[14]	*[19]
COREVDD	-	Internal power supply										—	—	—	*[2]	*[7]	*[12]	*[15]	*[20]
GND	-	GND										—	—	—	*[3]	*[8]	*[13]	*[16]	*[21]
PLLVD	-	PLL power supply										—	—	—	*[4]	*[9]	3	*[17]	H3
PLLGND	-	PLL GND										—	—	—	*[5]	*[10]	2	*[18]	H2
FLASHTEST	-	Test pin (NC)										—	—	—	80	L5	34	J10	B8

144QFP

*[1] IOVDD: 5, 25, 46, 63, 85, 101, 122, 128

*[2] COREVDD: 3, 34, 75, 106

*[3] GND: 15, 16, 38, 52, 53, 71, 81, 99, 110, 124, 126, 143

*[4] PLLVDD: 10, 11

*[5] PLLGND: 7, 8

144BGA

*[6] IOVDD: A6, C10, E1, G13, H12, K2, L9, N6

*[7] COREVDD: A3, C11, L3, N11

*[8] GDN: B1, B12, C8, D8, F3, G2, G10, H11, M2, M4, M10, M13

*[9] PLLVDD: A9, D9

*[10] PLLGND: A10, C9

64QFP

*[11] IOVDD: 13, 30, 47, 52, 58,

*[12] COREVDD: 1, 16, 33, 48,

*[13] GND: 6, 23, 35, 54, 56,

84BGA

*[14] IOVDD: A6, A8, B1, G1, H3, H8, K7, D10,

*[15] COREVDD: A1, C9, J2, K10,

*[16] GND: A10, B3, B6, C7, D8, E2, E3, J5, J9, K1, H5, H9,

*[17] PLLVDD: C1, D2,

*[18] PLLGND: C2, C3,

*NC: A2, A3, B2, B9, B10, C10, J1, K9,

64WCSP

*[19] IOVDD: B1, E2, E3, H5, H7,

*[20] COREVDD: C2, G2, H1, F2,

*[21] GND: B7, D2, E1, G3, G6,

Table 1-1 List of ML67Q4050/ML67Q4060 Series Pin Functions (2 of 6)

Pin name	Primary function		Secondary function			Tertiary function			Setting at reset			Schmitt trigger circuit	Sink current [mA]	Pin assignment					
	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description			IPU	144 QFP	144 BGA	64 QFP	84 BGA	64 WCSP
PA0	I/O	General-purpose port A0							TCK	I	JTAG clock	○	○	3	20	A7	9	F3	D3
PA1	I/O	General-purpose port A1							TMS	I	JTAG mode setting	○	—	3	21	C6	10	F1	D4
PA2	I/O	General-purpose port A2							TDI	I	JTAG data input	○	—	3	22	D6	11	G2	C5
PA3	I/O	General-purpose port A3							TDO	O	JTAG data output	—	—	3	23	B6	12	G3	C3
PA4	I/O	General-purpose port A4							NTRST	I	JTAG reset	○	○	3	26	D5	14	H2	A2
PA5	I/O	General-purpose port A5							JTAGE	I	JTAG Enable	—	—	3	30	C4	15	H1	A1
RSTOUT_N	O	Reset output	PA6	I/O	General-purpose port A6	MCLK	O	AUDIO_CLK output				—	—	3	51	F4	22	K4	A4
PB0	I/O	General-purpose port B0	TX0	O	UART0 TX							—	—	3	96	M9	46	D9	F8
PB1	I/O	General-purpose port B1	RX0	I	UART0 RX							—	—	3	95	M8	45	E10	E5
PB2	I/O	General-purpose port B2	TX1	O	UART1 TX	EFIQ_N	I	External interrupt FIQ*Note				—	—	3	94	K8	44	E8	E6
PB3	I/O	General-purpose port B3	RX1	I	UART1 RX	EXINT1	I	External interrupt 1 *Note				—	—	3	112	L13	49	A9	H8
PB4	I/O	General-purpose port B4	SCL	I/O	I2C SCL	TXD	O	SIO TX				—	○	3	116	J11	50	B8	G8
PB5	I/O	General-purpose port B5	SDA	I/O	I2C SDA	RXD	I	SIO RX				—	○	3	121	H13	51	C8	F7
PC0	I/O	General-purpose port C0	MISO0	I/O	SPI0 MISO	DSR0	I	UART0 DSR				—	—	3	66	K3	31	J8	A7
PC1	I/O	General-purpose port C1	MOSI0	I/O	SPI0 MOSI	DTR0	O	UART0 DTR				—	—	3	60	J2	29	H7	D5
PC2	I/O	General-purpose port C2	SCK0	I/O	SPI0 SCK	RI0	I	UART0 RI				—	○	3	59	H2	28	J7	A6
PC3	I/O	General-purpose port C3	SSN0	I/O	SPI0 SSN	DCD0	I	UART0 DCD				—	○	3	58	H4	27	K6	B6
PC4	I/O	General-purpose port C4	MISO1	I/O	SPI1 MISO	DSR1	I	UART1 DSR				—	—	3	57	H3	26	H6	C6
PC5	I/O	General-purpose port C5	MOSI1	I/O	SPI1 MOSI	DTR1	O	UART1 DTR				—	—	3	56	G1	25	J6	A5
PC6	I/O	General-purpose port C6	SCK1	I/O	SPI1 SCK	RI1	I	UART1 RI				—	○	3	50	F2	21	H4	B4
PC7	I/O	General-purpose port C7	SSN1	I/O	SPI1 SSN	DCD1	I	UART1 DCD				—	○	3	49	F1	20	J4	C4

*Note: External interrupt FIQ and external interrupt 1 can be used as interrupt signals in the primary and secondary functions.

Table 1-1 List of ML67Q4050/ML67Q4060 Series Pin Functions (3 of 6)

Pin name	Primary function		Secondary function			Tertiary function			Setting at reset			IPU	Schmitt trigger circuit	Sink current [mA]	Pin assignment				
	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description				144 QFP	144 BGA	64 QFP	84 BGA	64 WCSP
PD0	I/O	General-purpose port D0	AIN0	I	Analog input 0	EXINT 2	I	External interrupt 2 *Note				—	—	3	129	F11	59	B5	G5
PD1	I/O	General-purpose port D1	AIN1	I	Analog input 1	EXINT 3	I	External interrupt 3 *Note				—	—	3	130	F10	60	C5	F5
PD2	I/O	General-purpose port D2	AIN2	I	Analog input 2							—	—	3	131	F12	61	A5	F4
PD3	I/O	General-purpose port D3	AIN3	I	Analog input 3							—	—	3	132	E12	62	B4	G4
PD4	I/O	General-purpose port D4							BS	I	Boundary scan	—	—	3	48	E2	19	K3	A3
BOOTCLK	I/O	General-purpose port D5							BOOTCLK	I	Boot clock	—	—	3	70	L1	32	K8	A8
PE0	I/O	General-purpose port E0										—	—	20	123	H10	53	B7	G7
PE1	I/O	General-purpose port E1										—	—	20	125	G12	55	A7	H6
PE2	I/O	General-purpose port E2										—	—	20	127	G11	57	C6	F6
PE3	I/O	General-purpose port E3	MCLK	O	AUDIO_CLK output				BOOT0	I	Boot select 0	—	—	3	93	L8	43	E9	E7
PE4	I/O	General-purpose port E4	SD	I/O	I2S SD							—	—	3	92	N7	42	F10	E8
PE5	I/O	General-purpose port E5	WS	I/O	I2S WS							—	O	3	43	D1	18	J3	B3
PE6	I/O	General-purpose port E6	SCK	I/O	I2S SCK							—	O	3	39	C3	17	K2	B2
PF0	I/O	General-purpose port F0	TIMER0	I/O	FTM0	CTS0	I	UART0 CTS				—	—	3	91	L7	41	F8	E4
PF1	I/O	General-purpose port F1	TIMER1	I/O	FTM1	RTS0	O	UART0 RTS				—	—	3	90	K7	40	F9	D7
PF2	I/O	General-purpose port F2	TIMER2	I/O	FTM2	CTS1	I	UART1 CTS				—	—	3	89	M7	39	G10	D8
PF3	I/O	General-purpose port F3	TIMER3	I/O	FTM3	RTS1	O	UART1 RTS				—	—	3	88	L6	38	G8	D6
PF4	I/O	General-purpose port F4	TIMER4	I/O	FTM4	EXINT 4	I	External interrupt 4 *Note				—	—	3	87	K6	37	G9	C7
PF5	I/O	General-purpose port F5	TIMER5	I/O	FTM5	EXINT 5	I	External interrupt 5 *Note				—	—	3	86	M6	36	H10	C8

*Note: External interrupts 2 to 5 can be used as interrupt signals in the primary and secondary functions.

Table 1-1 (4/6) List of pin functions of the ML67Q4050/ML67Q4060 Series that is provided below are applicable to the ML67Q4050 Series only.

Table 1-1 List of ML67Q4050/ML67Q4060 Series Pin Functions (4 of 6)

Pin name	Primary function		Secondary function			Tertiary function			Setting at reset			IPU	Schmitt trigger circuit	Sink current [mA]	Pin assignment				
	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description				144 QFP	144 BGA	64 QFP	84 BGA	64 WCSP
XA0	O	External address bus 0	PI7	I/O	General-purpose port PI7							—	—	5	24	B5	—	—	—
XA1	O	External address bus 1	PG0	I/O	General-purpose port PG0							—	—	5	114	L12	—	—	—
XA2	O	External address bus 2	PG1	I/O	General-purpose port PG1							—	—	5	115	K13	—	—	—
XA3	O	External address bus 3	PG2	I/O	General-purpose port PG2							—	—	5	117	K12	—	—	—
XA4	O	External address bus 4	PG3	I/O	General-purpose port PG3							—	—	5	118	J13	—	—	—
XA5	O	External address bus 5	PG4	I/O	General-purpose port PG4							—	—	5	119	J10	—	—	—
XA6	O	External address bus 6	PG5	I/O	General-purpose port PG5							—	—	5	120	J12	—	—	—
XA7	O	External address bus 7	PG6	I/O	General-purpose port PG6							—	—	5	133	F13	—	—	—
XA8	O	External address bus 8	PH0	I/O	General-purpose port PH0							—	—	5	134	E10	—	—	—
XA9	O	External address bus 9	PH1	I/O	General-purpose port PH1							—	—	5	135	D12	—	—	—
XA10	O	External address bus 10	PH2	I/O	General-purpose port PH2							—	—	5	136	E13	—	—	—
XA11	O	External address bus 11	PH3	I/O	General-purpose port PH3							—	—	5	138	D11	—	—	—
XA12	O	External address bus 12	PH4	I/O	General-purpose port PH4							—	—	5	139	D13	—	—	—
XA13	O	External address bus 13	PH5	I/O	General-purpose port PH5							—	—	5	140	C12	—	—	—
XA14	O	External address bus 14	PH6	I/O	General-purpose port PH6							—	—	5	142	C13	—	—	—
XA15	O	External address bus 15	PH7	I/O	General-purpose port PH7							—	—	5	144	B13	—	—	—
XA16	O	External address bus 16	PI0	I/O	General-purpose port PI0							—	—	5	1	A13	—	—	—
XA17	O	External address bus 17	PI1	I/O	General-purpose port PI1							—	—	5	2	A12	—	—	—

Pin name	Primary function		Secondary function			Tertiary function			Setting at reset			IPU	Schmitt trigger circuit	Sink current [mA]	Pin assignment				
	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description				144 QFP	144 BGA	64 QFP	84 BGA	64 WCSP
XA18	O	External address bus 18	PI2	I/O	General-purpose port PI2							—	—	5	4	A11	—	—	—
XA19	O	External address bus 19	PI3	I/O	General-purpose port PI3							—	—	5	6	B11	—	—	—
XA20	O	External address bus 20	PI4	I/O	General-purpose port PI4							—	—	5	9	B10	—	—	—
XA21	O	External address bus 21	PI5	I/O	General-purpose port PI5	DMARE Q	I	DMA request				—	—	5	12	B9	—	—	—
XA22	O	External address bus 22	PI6	I/O	General-purpose port PI6	DMACLR	O	Clear DMA request				—	—	5	19	C7	—	—	—

Table 1-1 (5/6) List of pin functions of the ML67Q4050/ML67Q4060 Series that is provided below are applicable to the ML67Q4050 Series only.

Table 1-1 List of ML67Q4050/ML67Q4060 Series Pin Functions (5 of 6)

Pin name	Primary function		Secondary function			Tertiary function			Setting at reset			IPU	Schmitt trigger circuit	Sink current [mA]	Pin assignment				
	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description				144 QFP	144 BGA	64 QFP	84 BGA	64 WCSP
XD0	I/O	External data bus 0	PJ0	I/O	General-purpose port J0							○	—	5	84	M5	—	—	—
XD1	I/O	External data bus 1	PJ1	I/O	General-purpose port J1							○	—	5	83	K5	—	—	—
XD2	I/O	External data bus 2	PJ2	I/O	General-purpose port J2							○	—	5	79	N4	—	—	—
XD3	I/O	External data bus 3	PJ3	I/O	General-purpose port J3							○	—	5	78	M3	—	—	—
XD4	I/O	External data bus 4	PJ4	I/O	General-purpose port J4							○	—	5	77	L4	—	—	—
XD5	I/O	External data bus 5	PJ5	I/O	General-purpose port J5							○	—	5	76	N3	—	—	—
XD6	I/O	External data bus 6	PJ6	I/O	General-purpose port J6							○	—	5	74	N2	—	—	—
XD7	I/O	External data bus 7	PJ7	I/O	General-purpose port J7							○	—	5	73	N1	—	—	—
XD8	I/O	External data bus 8	PK0	I/O	General-purpose port K0							○	—	5	72	M1	—	—	—
XD9	I/O	External data bus 9	PK1	I/O	General-purpose port K1							○	—	5	69	K4	—	—	—
XD10	I/O	External data bus 10	PK2	I/O	General-purpose port K2							○	—	5	68	L2	—	—	—
XD11	I/O	External data bus 11	PK3	I/O	General-purpose port K3							○	—	5	67	K1	—	—	—
XD12	I/O	External data bus 12	PK4	I/O	General-purpose port K4							○	—	5	65	J3	—	—	—
XD13	I/O	External data bus 13	PK5	I/O	General-purpose port K5							○	—	5	64	J1	—	—	—
XD14	I/O	External data bus 14	PK6	I/O	General-purpose port K6							○	—	5	62	J4	—	—	—
XD15	I/O	External data bus 15	PK7	I/O	General-purpose port K7							○	—	5	61	H1	—	—	—
XD16	I/O	External data bus 16	PL0	I/O	General-purpose port L0							○	—	5	55	G3	—	—	—
XD17	I/O	External data bus 17	PL1	I/O	General-purpose port L1							○	—	5	47	E4	—	—	—

Pin name	Primary function		Secondary function			Tertiary function			Setting at reset			IPU	Schmitt trigger circuit	Sink current [mA]	Pin assignment				
	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description				144 QFP	144 BGA	64 QFP	84 BGA	64 WCSP
XD18	I/O	External data bus 18	PL2	I/O	General-purpose port L2							○	—	5	45	D2	—	—	—
XD19	I/O	External data bus 19	PL3	I/O	General-purpose port L3							○	—	5	44	E3	—	—	—
XD20	I/O	External data bus 20	PL4	I/O	General-purpose port L4							○	—	5	42	C2	—	—	—
XD21	I/O	External data bus 21	PL5	I/O	General-purpose port L5							○	—	5	41	D3	—	—	—
XD22	I/O	External data bus 22	PL6	I/O	General-purpose port L6							○	—	5	40	C1	—	—	—
XD23	I/O	External data bus 23	PL7	I/O	General-purpose port L7							○	—	5	37	A1	—	—	—
XD24	I/O	External data bus 24	PM0	I/O	General-purpose port M0							○	—	5	36	A2	—	—	—
XD25	I/O	External data bus 25	PM1	I/O	General-purpose port M1							○	—	5	35	B2	—	—	—
XD26	I/O	External data bus 26	PM2	I/O	General-purpose port M2							○	—	5	33	D4	—	—	—
XD27	I/O	External data bus 27	PM3	I/O	General-purpose port M3							○	—	5	32	B3	—	—	—
XD28	I/O	External data bus 28	PM4	I/O	General-purpose port M4							○	—	5	31	A4	—	—	—
XD29	I/O	External data bus 29	PM5	I/O	General-purpose port M5							○	—	5	29	C5	—	—	—
XD30	I/O	External data bus 30	PM6	I/O	General-purpose port M6							○	—	5	28	A5	—	—	—
XD31	I/O	External data bus 31	PM7	I/O	General-purpose port M7							○	—	5	27	B4	—	—	—

Table 1-1 (6/6) List of pin functions of the ML67Q4050/ML67Q4060 Series that is provided below are applicable to the ML67Q4050 Series only.

Table 1-1 List of ML67Q4050/ML67Q4060 Series Pin Functions (6 of 6)

Pin name	Primary function		Secondary function			Tertiary function			Setting at reset			IPU	Schmitt trigger circuit	Sink current [mA]	Pin assignment				
	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description	Signal name	I/O	Description				144 QFP	144 BGA	64 QFP	84 BGA	64 WCSP
ROMCS_N	O	External ROM Chip Enable	PN0	I/O	General-purpose port N0							—	—	5	107	M12	—	—	—
RAMCS_N	O	External RAM Chip Enable	PN1	I/O	General-purpose port N1							—	—	5	105	K10	—	—	—
IOCS0_N	O	External IO0 Chip Enable	PN2	I/O	General-purpose port N2							—	—	5	104	M11	—	—	—
IOCS1_N	O	External IO1 Chip Enable	PN3	I/O	General-purpose port N3							—	—	5	103	N10	—	—	—
BS0_N	O	External Byte Select 0	PN4	I/O	General-purpose port N4							—	—	5	97	N8	—	—	—
BS1_N	O	External Byte Select 1	PN5	I/O	General-purpose port N5							—	—	5	109	N13	—	—	—
BS2_N	O	External Byte Select 2	PN6	I/O	General-purpose port N6							—	—	5	111	L11	—	—	—
BS3_N	O	External Byte Select 3	PN7	I/O	General-purpose port N7							—	—	5	113	K11	—	—	—
OE_N	O	External Data Output Enable	PO0	I/O	General-purpose port O0							—	—	5	108	N12	—	—	—
WR_N	O	External Write Pulse	PO1	I/O	General-purpose port O1							—	—	5	98	K9	—	—	—
EXBUSE	I/O	General-purpose port O2							EXBUSE	I	External Bus Enable ^{*Note}	—	—	3	82	N5	—	—	—
EXIROME	I/O	General-purpose port O3							EXIROME	I	External Memory Access Enable	—	—	3	100	N9	—	—	—
BOOT1	I/O	General-purpose port O4							BOOT1	I	Boot Select 1	—	—	3	102	L10	—	—	—

*Note: When setting EXBUSE to “L”, do not use EXIROME and BOOT1 as general-purpose ports.

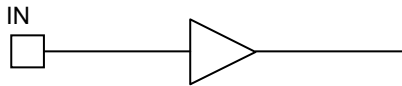
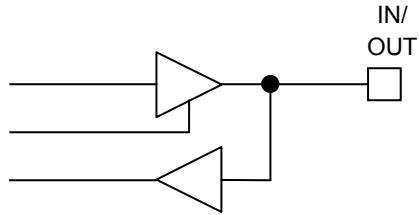
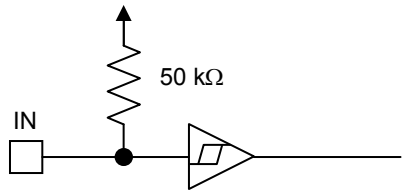
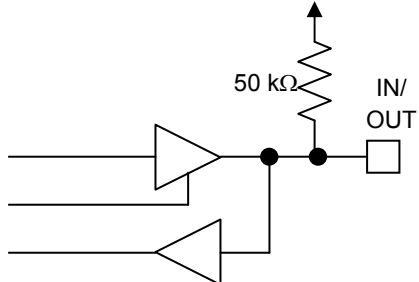
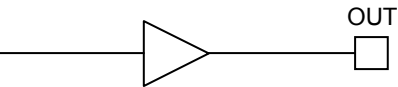
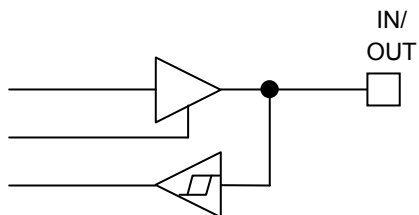
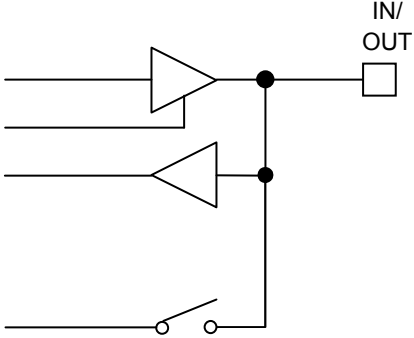
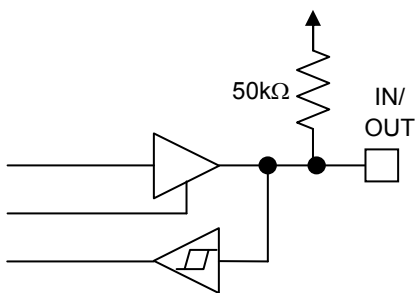
Circuit Types of Pins

The following shows simplified circuits of pins of the ML67Q4050/ML67Q4060 Series.

Table 1-2 Circuit Type of Each Pin (1 of 2)

Circuit type	Pin name
Type 1	SYSCLK_P, RTCCLK_P, TEST1, TEST2, BOOTCLK
Type 2	RESETN,
Type 3	SYSCLK_N, RTCCLK_N,
Type 4	PD0, PD1, PD2, PD3
Type 5	PA3, PA5, RSTOUT_N, PB0, PB1, PB2, PB3, PC0, PC1, PC4, PC5, PD4, PE0, PE1, PE2, PE3, PE4, PF0, PF1, PF2, PF3, PF4, PF5,
	Functions for the ML67Q4050 series. EXBUSE, EXIROME, BOOT1, XA0, XA1, XA2, XA3, XA4, XA5, XA6, XA7, XA8, XA9, XA10, XA11, XA12, XA13, XA14, XA15, XA16, XA17, XA18, XA19, XA20, XA21, XA22, ROMCS_N, RAMCS_N, IOCS0_N, IOCS1_N, BS0_N, BS1_N, BS2_N, BS3_N, OE_N, WR_N
Type 6	PA1, PA2,
	Functions for the ML67Q4050 series. XD0, XD1, XD2, XD3, XD4, XD5, XD6, XD7, XD8, XD9, XD10, XD11, XD12, XD13, XD14, XD15, XD16, XD17, XD18, XD19, XD20, XD21, XD22, XD23, XD24, XD25, XD26, XD27, XD28, XD29, XD30, XD31
Type 7	PB4, PB5, PC2, PC3, PC6, PC7, PE5, PE6
Type 8	PA0, PA4

Table 1-2 Circuit Type of Each Pin (2 of 2)

<p>Type 1</p> 	<p>Type 5</p> 
<p>Type 2</p>  <p>Schmitt trigger circuit</p>	<p>Type 6</p> 
<p>Type 3</p> 	<p>Type 7</p>  <p>Schmitt trigger circuit</p>
<p>Type 4</p>  <p>CH select</p>	<p>Type 8</p>  <p>Schmitt trigger circuit</p>

FUNCTIONAL DESCRIPTION

CPU

- 32-bit RISC CPU (ARM7TDMI)
- Little endian format
- Maximum operating frequency of 33.333 MHz
- Instruction structure: Enables mixed execution of high-density 32-bit long instructions and the subset of them, i.e., 16-bit long instructions of high object efficiency.
- General-purpose registers: 32 bits x 31 registers
- Built-in barrel shifter (operations of ALU and barrel shift can be executed by a single instruction)
- Built-in debug function (JTAG interface)
JTAG interface pin is shared with GPIO.

Internal memory

- 16KB RAM processor bus connection
- 8KB BootROM AHB connection
- Built-in Flash ROM processor bus connection of the 128KB(ML67Q4051 and ML67Q4061) or 64KB (ML67Q4050 and ML67Q4060)
- Flash rewrite count: 100 (max)

μPLAT-External memory controller (Function for the ML67Q4050 series only)

- Setting of programmable access timing for each space
- ROM (FLASH) access function
 - Supports 1-bank × 8-Mbyte ROM space
 - Supports 16-bit and 32-bit devices
 - Supports flash memories
 - Supports page access
- SRAM access function
 - 1-bank × 8-Mbyte SRAM space
 - Supports 16-bit, and 32-bit devices
 - Supports asynchronous SRAMs
- External I/O access function
 - 2-bank I/O space
 - Supports 8-bit, 16-bit, and 32-bit devices
 - Address setup, RE/WE pulse and data OFF timing can be set in one cycle units.

μPLAT-Interrupt controller/extended interrupt controller

- FIQ: 1 source (NMI pin)
- IRQ: 31 sources (40 sources for the ML67Q4050 Series)
- Seven levels of interrupt priorities can be set for each interrupt source.

μPLAT-System timer

- 16-bit auto-reload timer: × 1ch

μPLAT-SIO (UART)

- Full-duplex start-stop synchronization method
- Built-in baud rate generator

DMA controller

- × 2ch
- Multiple DMA transfer request sources can be assigned for each channel.
- Fixed mode or round robin mode can be selected for the priority order of channels.
- Cycle still mode or burst mode can be selected as the bus request method.
- Two types of DMA transfer requests are supported: software request and external request.
- Maximum number of transfers: 65,536 transfers
- Data transfer size: 8/16/32 bits
- Transfer request source: I2S I2C UART SPI
(External DMA requests are handled by the ML67Q4050 Series only.)

Watchdog timer

- 16-bit timer
- Maximum overflow time is 8.94 seconds (when operating at 30 MHz APB clock)
- Watchdog timer mode provided
- Interrupts or resets are generated according to settings.
- An “asserted” period can be set for reset signal output (RSTOUT_N).
- The WDTOVF_N pin outputs a L level at power-on reset
- Starting/stopping a watchdog timer
- Clearing a watchdog occurrence factor
- The watchdog timer cycle can be changed during watchdog timer operation.

A/D converter

- 10-bit sequential comparison type × 4ch
- Sample hold function
- Conversion time: 20 μs (Max 50ksample/s)
- Enables sequential A/D conversion (one-time/continuous) from the minimum channel to the maximum channel selected arbitrarily.
- DNL (max.) = ±6.0 LSB
- INL (max.) = ±6.0 LSB
- Zero-scale error (max.) = ±8.0 LSB
- Full-scale error (max.) = ±8.0 LSB

I2C bus controller

- Philips I2C bus specification Ver 2.1 conformed controller
- Supports multi-master mode.
- Data transfer modes
 - Standard mode (100 kHz)
 - Fast mode (400 kHz)
- 7-bit/10-bit address compatible
- Clocks are stopped to synchronize data between master and slave.
- Supports DMA transfer.

Flexible timer

- 16-bit timer × 6ch
- Operation mode
Operable in each of the modes, Auto Reload Timer (ART)/Compare Out (CMO)/Pulse Width Modulation (PWM)/Capture (CAP)

RTC

- Generates 1 second from 32.768 kHz
- Built-in 32-bit counter that counts 32 bits by 1-second clock
- 32-bit compare interrupt function

I2S transmit/receive

- Connection interface for general-purpose DACs/ADCs. Conforms to Philips I2S (the Inter-IC Sound) specification.
- 3-wire interface of word clock (WS), bit clock (SCK) and serial data (SD)
- The audio reference clock is generated from the main clock.
- Channel data length: 16/18/20/24 bits (CPU interface: 16 bits)
- Word clock length: 32/64 Fs
- Supports master/slave
- Enables the settings of 1-bit delay ON or OFF and left or right inversion.
- 256 × 16 bit FIFO shared between transmission and reception
- Supports DMA transfer.
- AUDIO_CLK output possible

GPIO

- Built-in GPIO of 8 bits × 1ch, 7 bits × 2ch, and 6 bits × 3ch
(In the ML67Q4050 Series, 8 bits × 8ch, 7 bits × 3ch, 6 bits × 3ch, and 5 bits × 1ch)
- Input or output can be specified for each bit. Every bit can be configured as interrupt input.
- Interrupt function (level/edge and positive logic/negative logic can be set, and this function is also supported even when no clock is operating.)
- Three 20 mA sink pins

UART

- Two channels of serial communication function with FIFO
- Serial communication with 16-byte FIFO
- Flow control by hardware
- DMA transfer support

SPI

- Built-in two channel of full duplex serial peripheral interface
- The master or slave mode can be selected.
- Built-in 16-byte or 16-word (16-bit) FIFO on the transmitting side and receiving side
- 8 bits (byte) or 16 bits (word) can be selected as the transfer size.
- Supports DMA transfer.
- Built-in baud rate generator

Clock

- Main clock oscillator (16 to 33.333MHz)
- RTC clock oscillator (32.768kHz clock)
- Ring oscillator

Power management

- Power saving mode
 - CPU halt mode: Stops only the CPU clock.
 - STOP mode: Stops all the clocks of the chip except RTC.
- Clock operation or stop can be set for each block.
- Variable system clock frequencies

Package

- ML67Q4060/ML67Q4061
 - 64-pin TQFP (TQFP64-P-1010-0.50-K)
 - 84-pin LFBGA (P-LFBGA84-0909-0.80) (8 pins are not connected.)
 - 64-pin WCSP (P-VFBGA64-5.09 × 4.84-0.50-W, P-VFLGA64-5.09 × 4.84-0.50-W)
- ML67Q4050
 - 144-pin LQFP (LQFP144-P-2020-0.50-ZK)
- ML67Q4051
 - 144-pin LQFP (LQFP144-P-2020-0.50-ZK)
 - 144-pin LFBGA (P-LFBGA144-1111-0.80)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage (CORE)	V_{DD_CORE}	GND = 0 V Ta = 25°C	-0.3 to +3.6	V
Digital power supply voltage (I/O)	V_{DD_IO}		-0.3 to +4.6	
Input voltage	V_I		-0.3 to $V_{DD_IO}+0.3$	
Output voltage	V_O		-0.3 to $V_{DD_IO}+0.3$	
PLL section power supply voltage (PLL)	V_{DD_PLL}		-0.3 to +3.6	
Allowable input current	I_I		-10 to +10	mA
“H” allowable input current	I_{OH}		+10	
“L” allowable input current	I_{OL}	-20		
Power dissipation	P_D	Ta = 85°C Per package	530	mW
Storage temperature	T_{STG}	144pin LQFP (LQFP144-P-2020-0.50-ZK)	-55 to +150	°C
		144pin LFBGA (P-LFBGA144-1111-0.80)	-55 to +150	
		64pin QFP (TQFP64-P-1010-0.50-K)	-55 to +150	
		84pin LFBGA (P-LFBGA84-0909-0.80)	-55 to +125	
		64pin WCSP (P-VFBGA64-5.09 x 4.84-0.50-W, P-VFLGA64-5.09 x 4.84-0.50-W)	-55 to +150	

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital power supply voltage (CORE)	V _{DD_CORE}	—	2.25	2.5	2.75	V
Digital power supply voltage (I/O; When external memory bus is not used)	V _{DD_IO}		V _{DD_CORE}	3.3	3.6	
Digital power supply voltage (I/O; When external memory bus is used)			3.0	3.3	3.6	
PLL section power supply voltage (PLL)	V _{DD_PLL}		2.25	2.5	2.75	
CPU Operating frequency	f _{OSC}	—	0.032	—	33.333	MHz
Ambient temperature	T _a	—	-40	25	85	°C

ELECTRICAL CHARACTERISTICS**DC Characteristics**(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = -40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
"H" input voltage	V _{IH}	—	2.0	—	V _{DD_IO} + 0.3	V	
"L" input voltage	V _{IL}		-0.3	—	0.8		
Schmitt trigger input threshold voltage	V _{T+}		—	—	—		V _{DD_IO} × 0.7
	V _{T-}		V _{DD_IO} × 0.2	—	—		—
Schmitt hysteresis	V _{HYS}		V _{DD_IO} × 0.1	—	—		—
"H" output voltage	V _{OH}	I _{OH} = -3 mA	2.4	—	—	V	
		I _{OH} = -5 mA					
		I _{OH} = -20 mA					
"L" output voltage	V _{OL}	I _{OL} = 3 mA	—	—	0.4		
		I _{OL} = 5 mA	—	—	0.45		
		I _{OL} = 20 mA	—	—	0.45		
Input leakage current ^{*4}	I _{IH} / I _{IL}	V _I = 0V / V _{DD_IO}	-10	—	10	uA	
Input leakage current ^{*3}		V _I = 0V Pull-up resistor 50 kΩ	—	—	200		
Output leakage current		V _O = 0V / V _{DD_IO}	-10	—	10		

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = V_{DD_CORE} to 2.75 V, Ta = -40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
"H" input voltage	V _{IH}	—	1.7	—	V _{DD_IO} +0.3	V	
"L" input voltage	V _{IL}		-0.3	—	0.7		
Schmitt trigger input threshold voltage	V _{T+}		—	—	—		V _{DD_IO} × 0.7
	V _{T-}		V _{DD_IO} × 0.2	—	—		—
Schmitt hysteresis	V _{HYS}		V _{DD_IO} × 0.1	—	—		—
"H" output voltage	V _{OH}	I _{OH} = -1 mA	2.0	—	—	V	
		I _{OH} = -5 mA					
		I _{OH} = -20 mA					
"L" output voltage	V _{OL}	I _{OL} = 1 mA	—	—	0.4		
		I _{OL} = 5 mA	—	—	0.5		
		I _{OL} = 20 mA	—	—	0.5		
Input leakage current ^{*4}	I _{IH} / I _{IL}	V _I = 0V / V _{DD_IO}	-10	—	10	uA	
Input leakage current ^{*3}		V _I = 0V Pull-up resistor 50 kΩ	—	—	150		
Output leakage current		V _O = 0V / V _{DD_IO}	-10	—	10		

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 2.75 to 3.0 V, Ta = -40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
"H" input voltage	V _{IH}	—	2.0	—	V _{DD_IO} +0.3	V	
"L" input voltage	V _{IL}		-0.3	—	0.8		
Schmitt trigger input threshold voltage	V _{T+}		—	—	—		V _{DD_IO} × 0.7
	V _{T-}		V _{DD_IO} × 0.2	—	—		—
Schmitt hysteresis	V _{HYS}		V _{DD_IO} × 0.1	—	—		—
"H" output voltage	3mA buffer ^{*2}	V _{OH}	I _{OH} = -1 mA	2.4	—	—	
	5mA buffer ^{*2}						
	20mA buffer ^{*1}						
"L" output voltage	3mA buffer ^{*2}	V _{OL}	I _{OL} = 1 mA	—	—	0.4	
	5mA buffer ^{*2}		I _{OL} = 20 mA	—	—	0.45	
	20mA buffer ^{*1}						
Input leakage current ^{*4}	I _{IH} / I _{IL}	V _I = 0V / V _{DD_IO}	-10	—	10	uA	
Input leakage current ^{*3}		V _I = 0V Pull-up resistor 50 kΩ	—	—	175		
Output leakage current		V _O = 0V / V _{DD_IO}	-10	—	10		

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = V_{DD_CORE} to 3.6V, Ta = -40 to +85°C)

Parameter	Symbol	Power Type	Condition	Min.	Typ.	Max.	Unit
Pin capacitance 1 ^{*6}	C ₁	—	—	—	5	—	pF
Pin capacitance 2 ^{*5}	C ₂	—	—	—	9	—	
Pin capacitance 3 ^{*1}	C ₃	—	—	—	18	—	
Current consumption (at STOP)	I _{DDS_CORE}	CORE	Ta = 85°C V _{DD_CORE} = 2.75V	—	—	485	uA
			Ta = 25°C V _{DD_CORE} = 2.5V	—	10.131	—	
	I _{DDS_IO} ^{*7}	IO	Ta = 85°C V _{DD_IO} = 3.6V	—	—	10	
			Ta = 25°C V _{DD_IO} = 3.3V	—	0.062	—	
	I _{DDS_PLL}	PLL	Ta = 85°C V _{DD_PLL} = 2.75V	—	—	5	
			Ta = 25°C V _{DD_PLL} = 2.5V	—	0.027	—	
Current consumption (at HALT)	I _{DDH_CORE}	CORE	ML67Q4050/51 f _{OSC} = 33.333 MHz No load	—	—	30	mA
				—	25	—	
	I _{DDH_IO}	IO		—	—	16	
				—	13.78	—	
	I _{DDH_PLL}	PLL		—	—	14	
				—	6.56	—	
	I _{DDH_CORE}	CORE	ML67Q4060/61 f _{OSC} = 33.333 MHz No load	—	—	30	
				—	25	—	
	I _{DDH_IO}	IO		—	—	16	
				—	8.49	—	
	I _{DDH_PLL}	PLL		—	—	14	
				—	6.56	—	
Current consumption (dynamic) ^{*8}	I _{DDO_CORE}	CORE	ML67Q4050/51 f _{OSC} = 33.333 MHz No load	—	—	76.00	mA
				—	49.90	—	
	I _{DDO_IO}	IO		—	—	30.00	
				—	13.78	—	
	I _{DDO_PLL}	PLL		—	—	14.00	
				—	6.56	—	
	I _{DDO_CORE}	CORE	ML67Q4060/61 f _{OSC} = 33.333 MHz No load	—	—	76.00	
				—	49.90	—	
	I _{DDO_IO}	IO		—	—	30.00	
				—	8.49	—	
	I _{DDO_PLL}	PLL		—	—	14.00	
				—	6.56	—	

Applicable pins:

*1: 20mA SINK pins

*2: Pins other than the 20mA SINK pins

*3: Pins with a 50 kΩ pull-up resistor

*4: Pins without a 50 kΩ pull-up resistor

*5: AIN pin

*6: Pin other than the AIN pin and 20mA SINK pins

*7: Input ports: V_{DD_IO} or 0V. Other ports: No load.

*8: The following lists typical operating current of each operating frequency.

REFERENCE:

The reference of the consumption current value when the MCU is operating

The following tables are reference data of consumption current (IDDO) of ML67Q4060/50 series at the time of operation. This figure changes with the circumference function to be used or its conditions of operation.

- Typical operating current of each operating frequency for ML67Q4050/51

Power Type	Condition		frequency [MHz]						
			8	12	16	20	24	28	33.333
CORE	$V_{DD_CORE} = 2.5V$	Ta = 25°C	21.80	26.19	30.59	34.98	39.38	43.78	49.90
IO	$V_{DD_IO} = 3.3V$		4.69	6.23	7.76	9.30	10.83	12.37	13.78
PLL	$V_{DD_PLL} = 2.5V$		3.29	3.64	4.00	4.50	5.15	5.80	6.56
TOTAL	—		29.78	36.06	42.35	48.78	55.36	61.94	70.23

Note: The values shown above are references. Use these values as reference when using this LSI.

- Typical operating current of each operating frequency for ML67Q4060/61

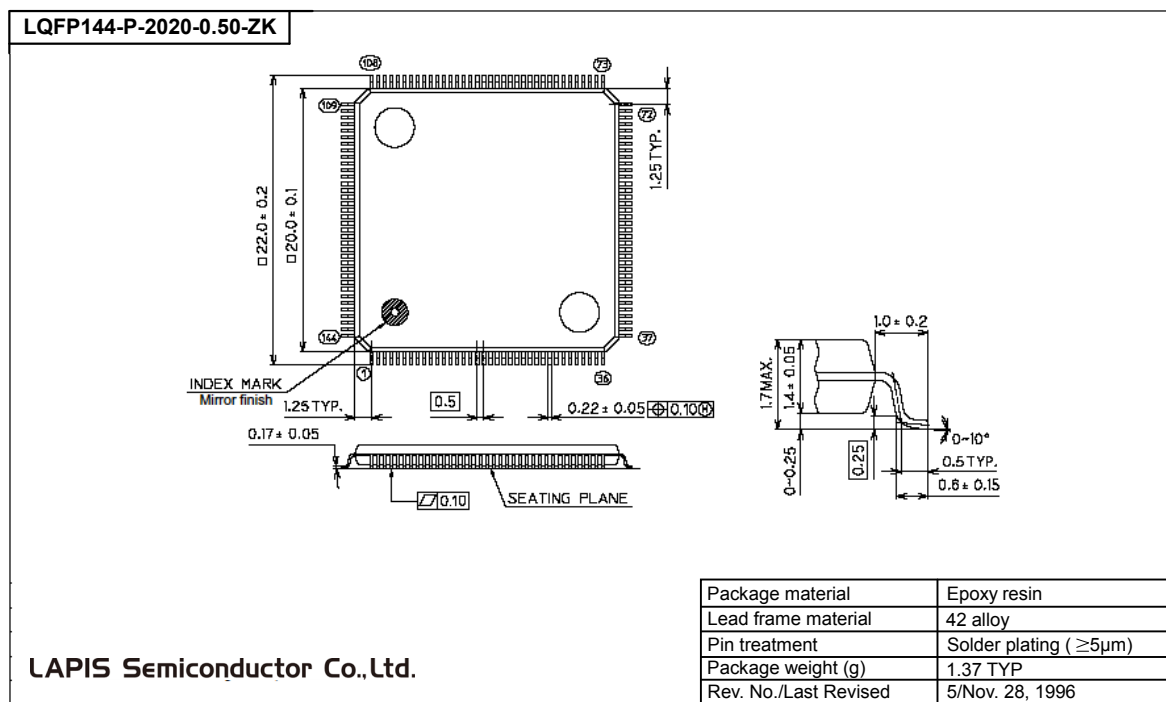
Power Type	Condition		frequency [MHz]						
			8	12	16	20	24	28	33.333
CORE	$V_{DD_CORE} = 2.5V$	Ta = 25°C	21.80	26.19	30.59	34.98	39.38	43.78	49.90
IO	$V_{DD_IO} = 3.3V$		2.89	3.84	4.78	5.73	6.67	7.62	8.49
PLL	$V_{DD_PLL} = 2.5V$		3.29	3.64	4.00	4.50	5.15	5.80	6.56
TOTAL	—		27.97	33.67	39.37	45.21	51.20	57.19	64.94

Note: The values shown above are references. Use these values as reference when using this LSI.

PACKAGE DIMENSIONS

144-Pin LQFP (LQFP144-P-2020-0.50-ZK)

(Unit: mm)

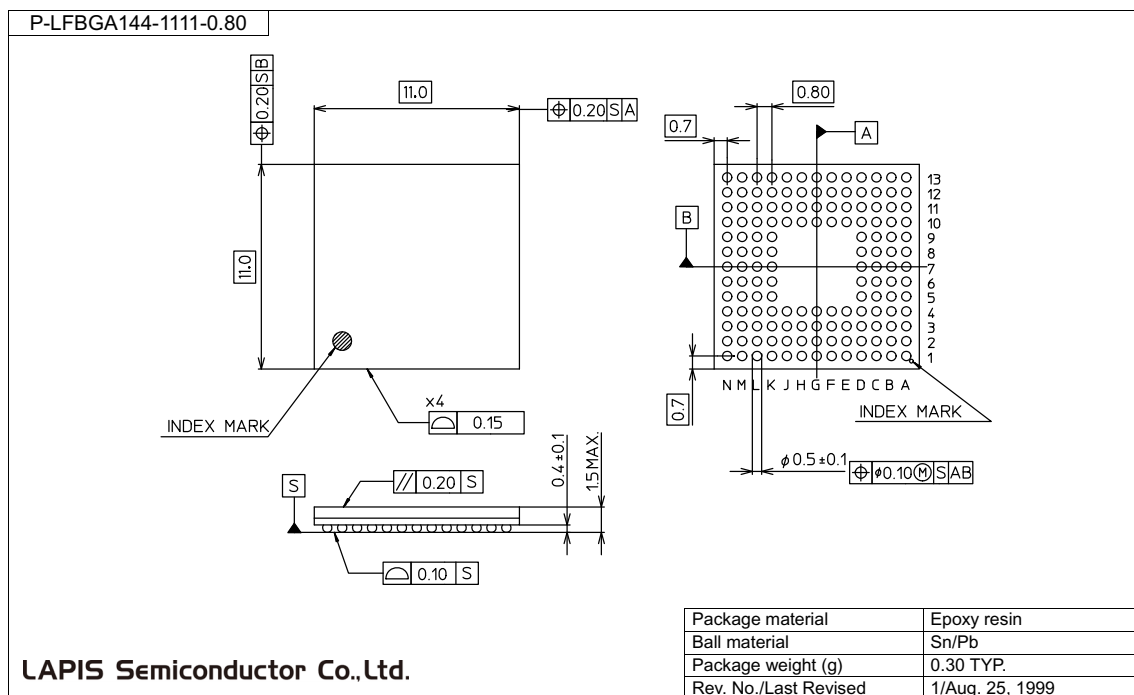


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

144-Pin LFBGA (P- LFBGA144-1111-0.80)

(Unit: mm)

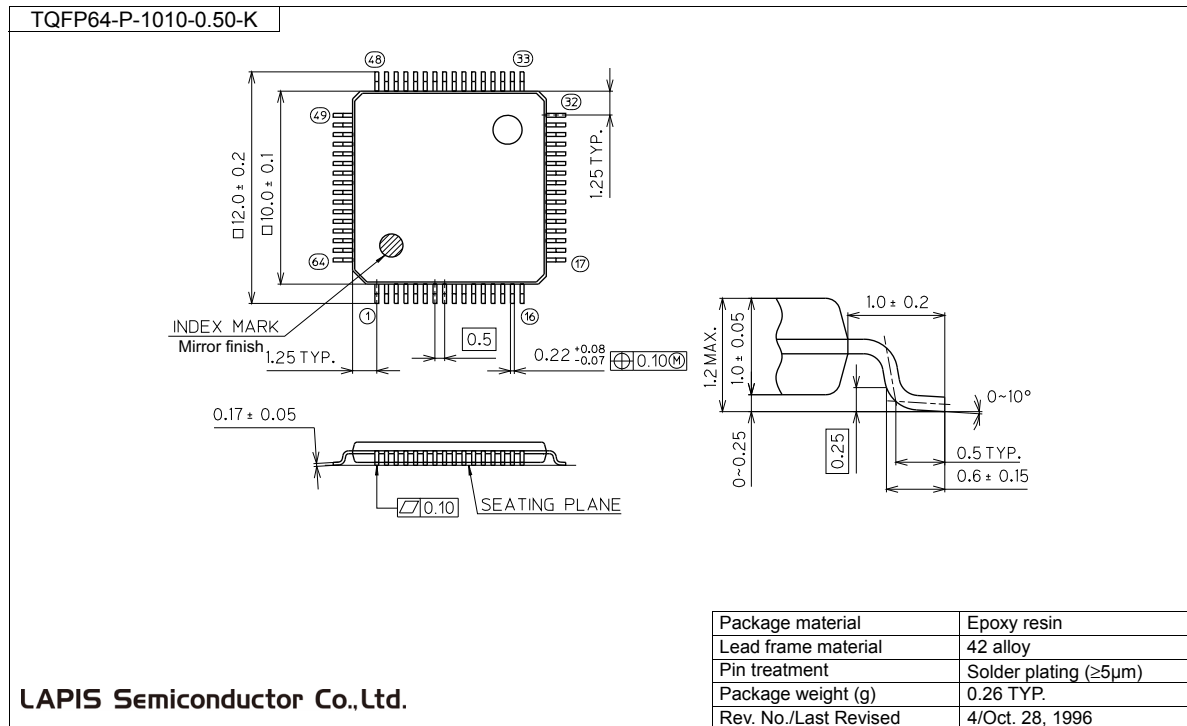


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64-Pin TQFP (TQFP64-P-1010-0.50-K)

(Unit: mm)

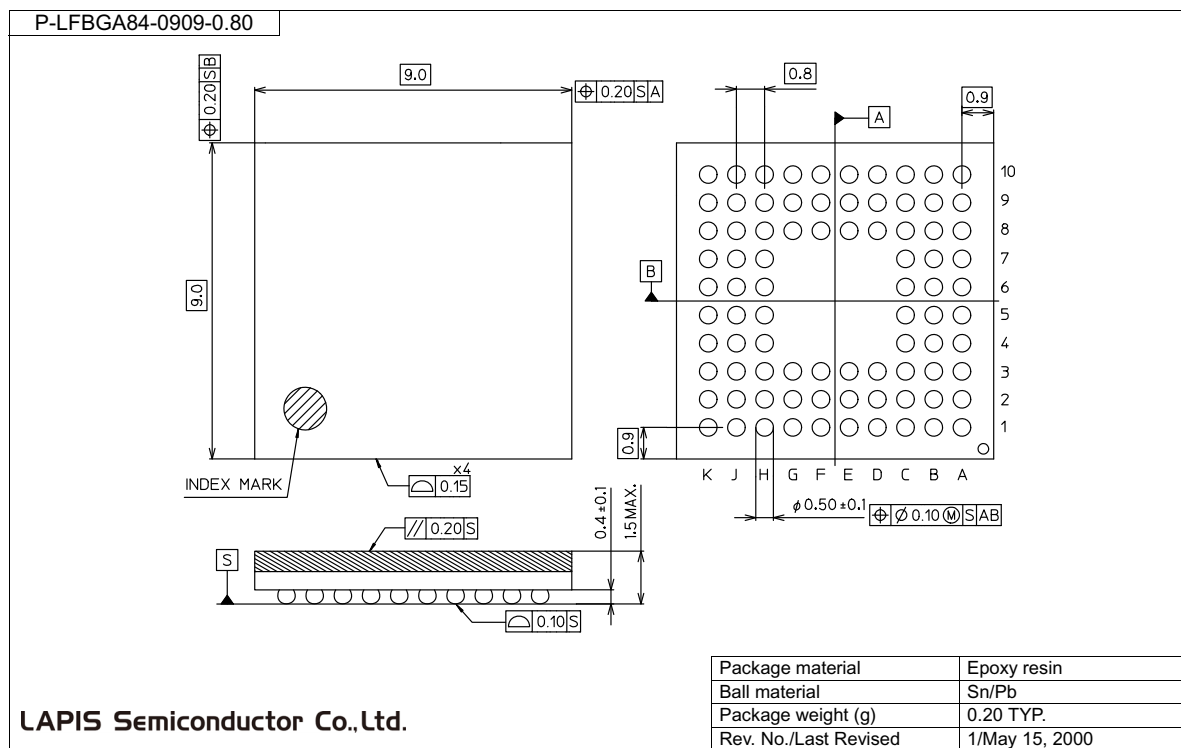


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

84-Pin LFBGA (P-LFBGA84-0909-0.80)

(Unit: mm)

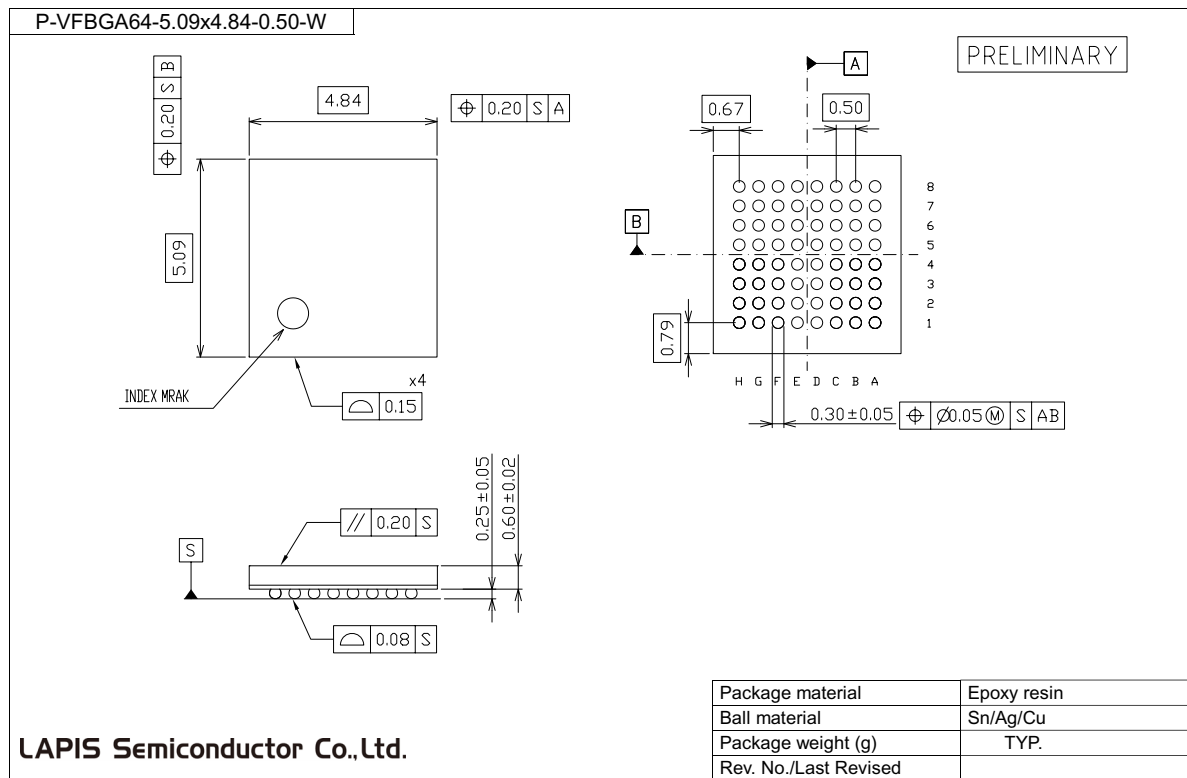


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64-Pin WCSP (P-VFBGA64-5.09 × 4.84-0.50-W)

(Unit: mm)

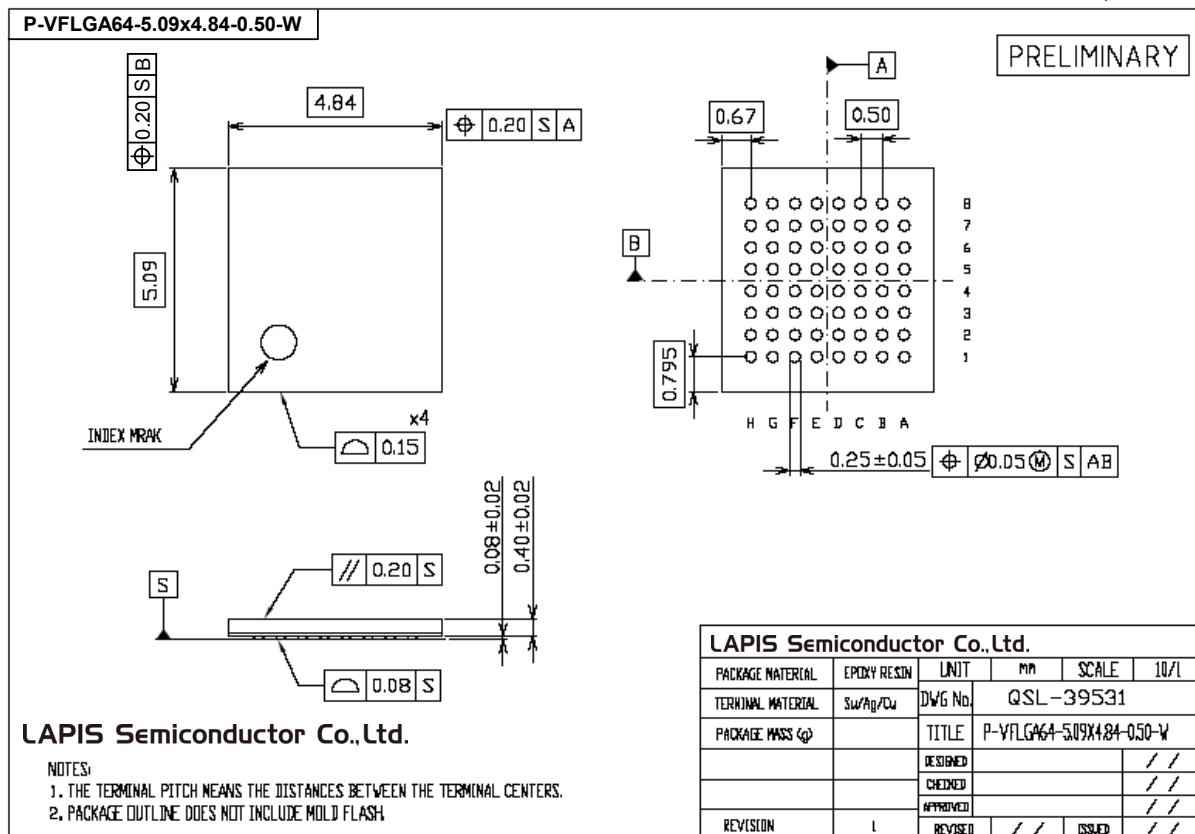


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64-Pin WCSP (P-VFLGA64-5.09 × 4.84-0.50-W)

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL67Q4060-01	Jan.21, 2008	-	-	Final edition 1

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