D I G I T R O N S E M I C O N D U C T O R S

2N681-2N692, 2N5204-2N5207 SILICON CONTROLLED RECTIFIER

Available Non-RoHS (standard) or RoHS compliant (add PBF suffix).
Available as "HR" (high reliability) screened per MIL-PRF-19500, JANTX level. Add "HR" suffix to base part number.

MAXIMUM RATINGS

Rating	Symbol	2N681-2N692	2N5204-2N5207	Unit
RMS on-state current	$I_{T(RMS)}$	25	35	A
Average on-state current	$I_{T(AV)}$	16	22	A
@ T_C	T_C	-65 to +65	-40 to +40	°C
Peak one cycle surge @ 50 Hz	I_{TSM}	145	285	A
Peak one cycle surge @ 60 Hz		150	300	A
Fusing @ 50 Hz	I^2t	103	410	A^2s
Fusing @ 60 Hz		94	375	
Gate current to trigger	I_{GT}	40	40	mA
Typical critical dv/dt exponential to V_{DRM}	dv/dt	-	100	V/µs
Critical rate of rise	di/dt	75-100	100	A/µs
Typical junction temperature	T_J	-65 to 125	-40 to 125	°C

VOLTAGE RATINGS (Applied gate voltage zero or negative)

Part Number	V_{RRM}, V_{DRM} Maximum repetitive peak reverse and off-state voltage (V)	V_{RSM} Maximum non-repetitive peak reverse voltage $t_p \leq 5$ ms (V)
	T_J = -65 to +125°C	**T_J = -65 to +125°C**
2N681	25	35
2N682	50	75
2N683	100	150
2N685	200	300
2N687	300	400
2N688	400	500
2N689	500	600
2N690	600	720
2N691	700	840
2N692	800	960
	T_J = -40 to 125°C	**T_J = -40 to 125°C**
2N5204	600	720
2N5205	800	960
2N5206	1000	1200
2N5207	1200	1440

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	2N681-2N692	2N5204-2N5207	Units	Conditions	
$I_{T(RMS)}$	Maximum RMS on-state current	25	35	A		
$I_{T(AV)}$	Maximum average on-state current	16	22	A	180° half sine wave conduction	
I_{TSM}	@ T_C =	-65 to +65	-40 to +40	°C		
	Maximum peak one cycle, non-repetitive surge current	145	285	A	50 Hz half cycle sine wave or 6 ms rectangular pulse	Following any rated load condition and with rated V_{RRM} applied following surge
		150	300		60 Hz half cycle sine wave or 5 ms rectangular pulse	
		170	340		50 Hz half cycle sine wave or 6 ms rectangular pulse	Same conditions as above except with V_{RRM} applied following surge = 0
		180	355		60 Hz half cycle sine wave or 5 ms rectangular pulse	
I^2t	Maximum I^2t capability, for fusing	103	410	A^2s	t = 10 ms	Rated V_{RRM} applied following surge, initial T_J = 125°C
		94	375		t = 8.3 ms	
I^2t	Maximum I^2t capability for individual device fusing	145	580	A^2s	t = 10 ms	V_{RRM} = 0 following surge, initial T_J = 125°C
		135	530		t = 8.3 ms	

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ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	2N681-2N692	2N5204-2N5207	Units	Conditions
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ capability for individual device fusing (1)	1450	5800	$A^2\sqrt{s}$	t = 0.1 to 10ms initial $T_J \leq 125°C$, V_{RRM} following surge = 0
V_{TM}	Maximum peak on-state voltage	2	2.3	V	T_J = 25°C, $I_{T(AV)}$ = 16A(50A peak) – 2N681 $I_{T(AV)}$ = 22A (70A) peak – 2N5204
I_H	Maximum holding current	20 @ 25°C	200 @-40°C	mA	Anode supply = 24V, initial I_T= 1.0A
BLOCKING					
dv/dt	Minimum critical rate of rise of off-state voltage	100 typical	100	V/µs	T_J = 125°C exponential to 100% rated V_{DRM}
		250 typical	250		T_J = 125°C exponential to 67% rated V_{DRM}
$I_R^{(-)}$ & $I_D^{(-)}$	Maximum reverse and off-state current	$I_{R(AV)}$ & $I_{D(AV)}$ (average values)	I_{RM} & I_{DM} (peak values)	mA	T_J = 125°C, gate open circuited
	V_{RRM} & V_{DRM} =	-	-		
	25 to 150V	6.5	-		
	200 & 250V	6.0	-		
	300V	5.0	-		
	400V	4.0	-		
	500V	3.0	-		
	600V	2.5	3.3		
	700V	2.25	-		
	800V	2.0	2.5		
	1000V	-	2.0		
	1200V	-	1.7		
SWITCHING					
t_d	Typical delay time	1	1	µs	T_C = 25°C, V_{DM} = rated V_{DRM}, I_{TM} = 10A dc resistive circuit. Gate pulse: 10 V, 40Ω source, t_p = 6µs, t_r = 0.1µs
di/dt	Maximum non-repetitive rate of rise of turned-on current V_{DM} = 25 to 600 V	100	-	A/µs	T_C = 125°C, V_{DM} = rated V_{DRM}, I_{TM} = 2 x di/dt, gate pulse: 20V, 15 Ω, t_p = 6µs, t_r = 0.1 µs maximum
	V_{DM} = 700 to 800 V	75	-		
		-	100		T_C = 125°C, V_{DM} = 600V, I_{TM} = 200A @ 400Hz max. Gate pulse: 20V, 15Ω, t_p = 6µs, t_r = 0.1µs max.
TRIGGERING					
P_{GM}	Maximum peak gate power	5	60	W	$t_p \leq$ 5ms – 2N681 $t_p \leq$ 500µs – 2N5204
$P_{G(AV)}$	Maximum average gate power	0.5	0.5	W	
I_{GM}	Maximum peak positive gate current	2	2	A	
$+V_{GM}$	Maximum peak positive gate voltage	10	-	V	
$-V_{GM}$	Maximum peak negative gate voltage	5	5	V	
I_{GT}	Maximum required DC gate current to trigger	80	80	mA	T_C = min rated value. Max. required gate trigger current is the lowest value which will trigger all units with 6V anode to cathode
		40	40		T_C = 25°C
		18.5	20		T_C = 125°C
	Typical DC gate current to trigger	30	30		T_C = 25°C, 6V anode to cathode

Note 1: I^2t for time $t_x \approx I^2\sqrt{t} \bullet \sqrt{t_x}$

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ELECTRICAL CHARACTERISTICS

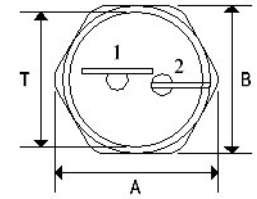
Symbol	Characteristics	2N681-2N692	2N5204-2N5207	Units	Conditions
V_{GT}	Maximum required DC gate voltage to trigger	3	3	V	T_C = -65°C. Max. required gate trigger voltage is the lowest value which will trigger all units with 6V anode to cathode
		2	2		T_C = 25°C
	Typical DC gate voltage to trigger	1.5	1.5		T_C = 25°C 6V anode to cathode
V_{GD}	Maximum DC gate voltage not to trigger	0.25	0.25	V	T_C = 125°C. Max. gate voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode

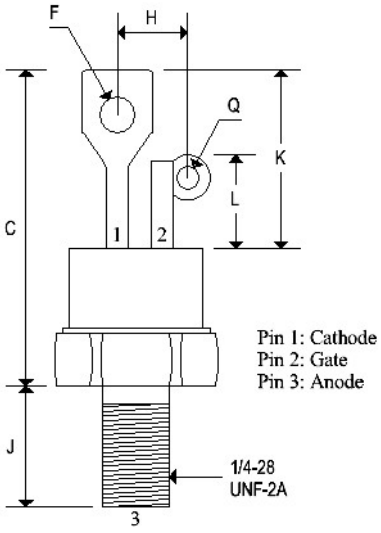
THERMAL –MECHANICAL CHARACTERISTICS

Symbol	Characteristics	2N681-2N692	2N5204-2N5207	Units	Conditions
T_J	Operating junction temperature range	-65 to 125	-40 to 125	°C	
T_{stg}	Storage temperature range	-65 to 125	-40 to 125	°C	
R_{thJC}	Maximum internal thermal resistance, junction to case	1.5	1.5	°C/W	DC operation
R_{thCS}	Thermal resistance, case to sink	0.35	0.35	°C/W	Mounting surface smooth, flat and greased

MECHANICAL CHARACTERISTICS

Case	TO-48
Marking	Alpha-numeric
Pin out	See below





	TO-48			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.604	0.614	15.340	15.600
B	0.551	0.559	14.000	14.200
C	1.050	1.190	2.670	30.230
F	0.135	0.160	3.430	4.060
H	-	0.265	-	6.730
J	0.420	0.455	10.670	11.560
K	0.620	0.670	15.750	17.020
L	0.300	0.350	7.620	8.890
Q	0.055	0.085	1.400	2.160
T	0.501	0.505	12.730	12.830

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2N681 Series

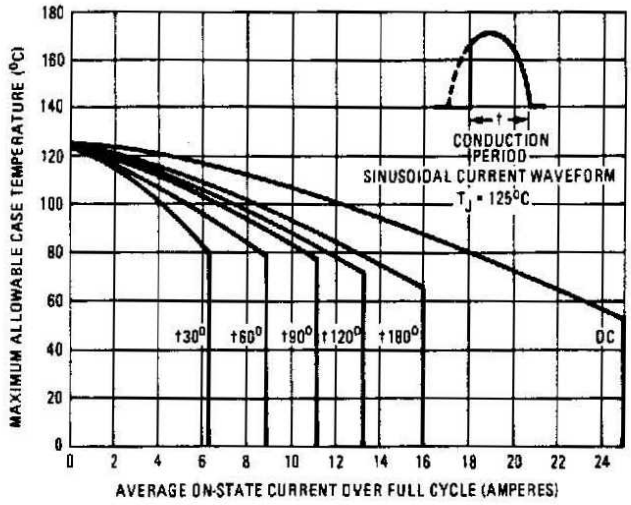

Fig. 1 – Maximum Allowable Case Temperature Vs. Average On-State Current, 2N681 Series

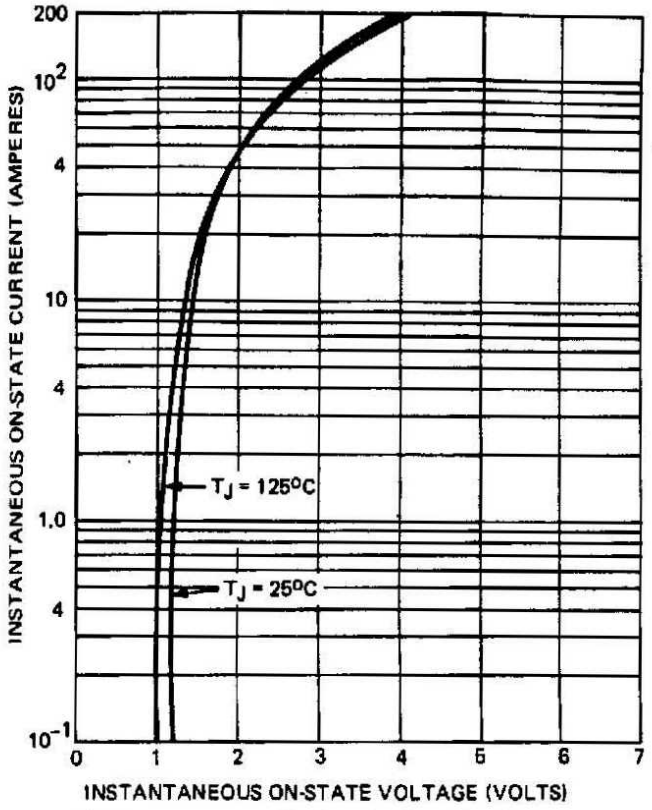

Fig. 2 – Maximum On-State Voltage Vs. Current, 2N681 Series

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2N681 Series

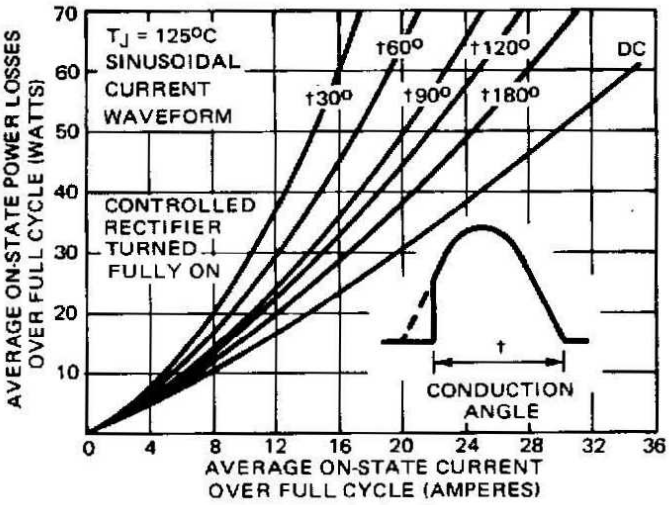

Fig. 3 – Maximum Low Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform), 2N681 Series

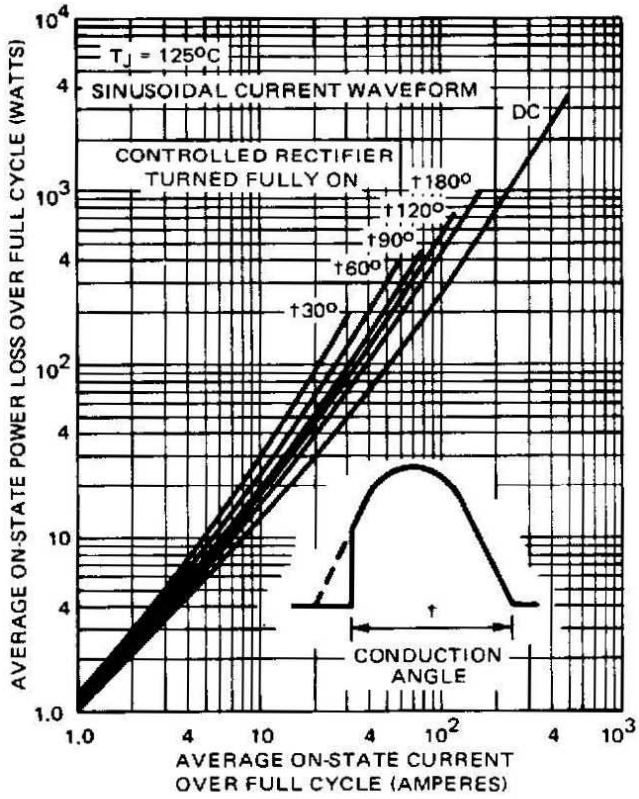

Fig. 4 – Maximum High Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform), 2N681 Series

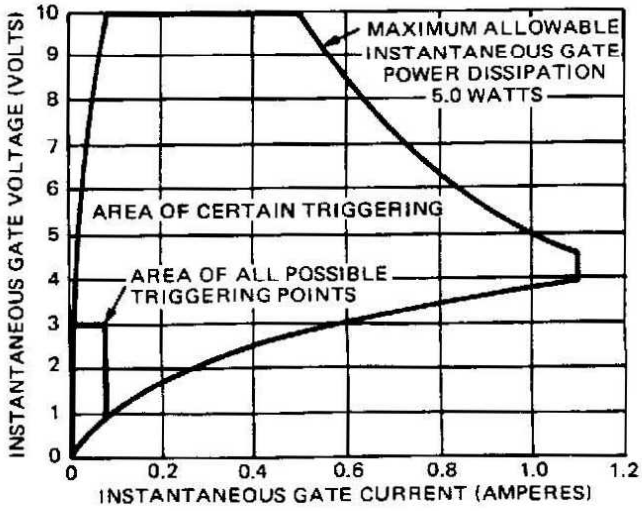

Fig. 5 – Gate Characteristics, 2N681 Series

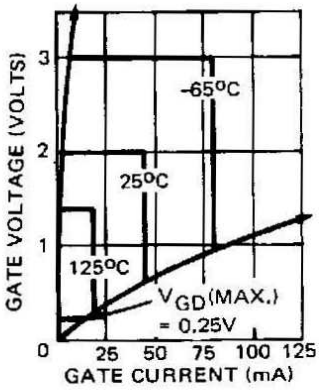

Fig. 5A – Area of All Possible Triggering Points Vs. Temperature 2N681 Series

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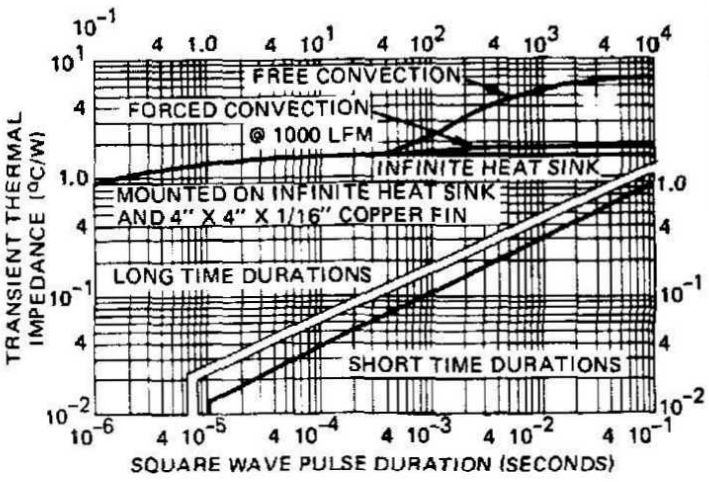

Fig. 6 – Maximum Transient Thermal Impedance, Junction to Case, Vs. Pulse Duration, 2N681 Series

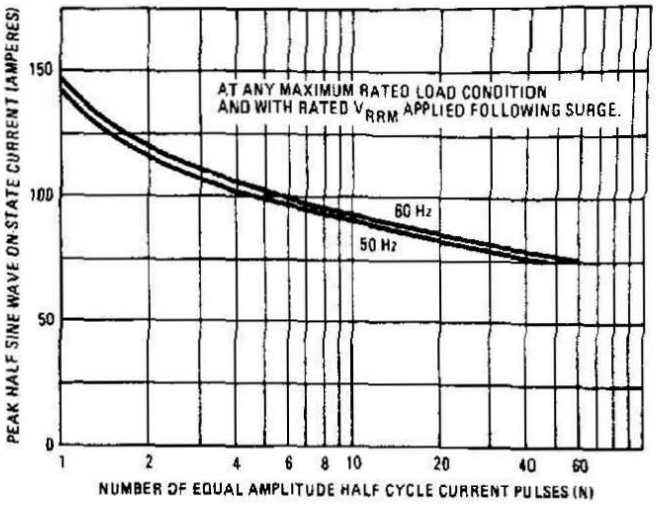

Fig. 7 – Maximum Non-Repetitive Surge Current, Vs. Number of Current Pulses, 2N681 Series

2N5204 Series

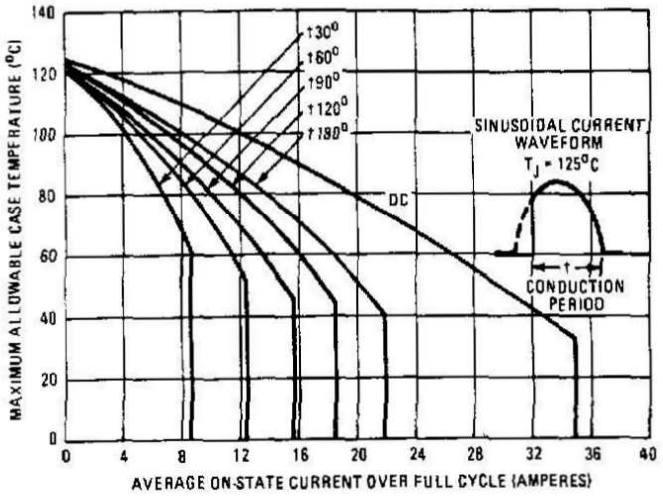

Fig. 8 – Maximum Allowable Case Temperature Vs. Average On-State Current (Sinusoidal Current Waveform), 2N5204 Series

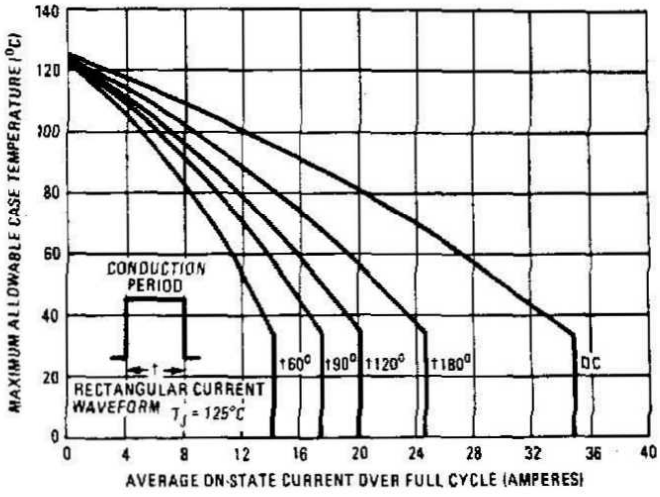

Fig. 9 – Maximum Allowable Case Temperature Vs. Average On-State Current (Rectangular Current Waveform), 2N5204 Series

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2N5204 Series

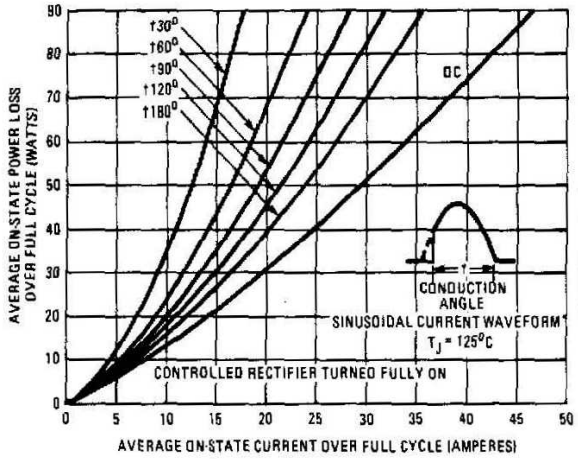

Fig. 10 – Maximum Low-Level On-State Power Loss Vs. Average On-State Current (Sinusoidal Current Waveform), 2N5204 Series

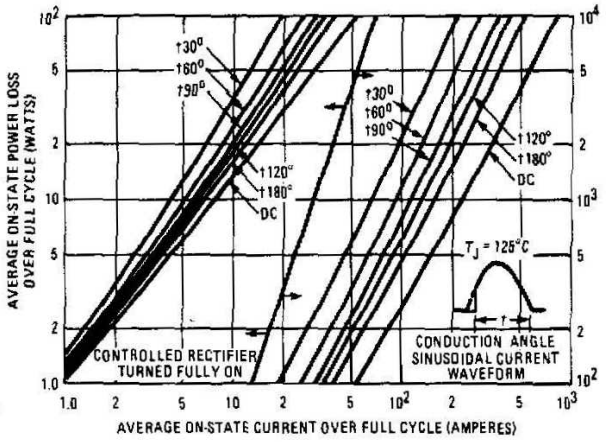

Fig. 11 – Maximum High-Level On-State Power Loss Vs. Average On-State Current (Sinusoidal Current Waveform), 2N5204 Series

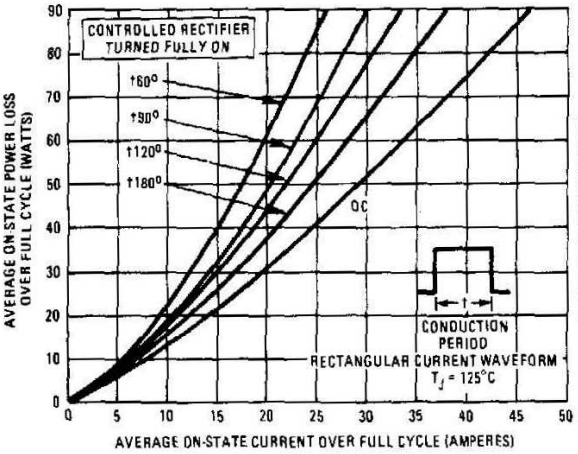

Fig. 12 – Maximum Low-Level On-State Power Loss Vs. Average On-State Current (Rectangular Current Waveform), 2N5204 Series

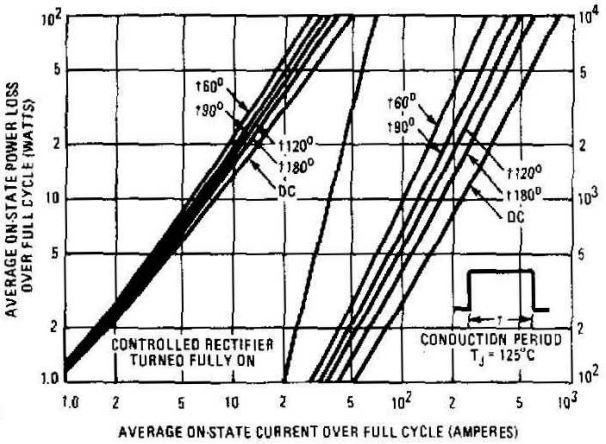

Fig. 13 – Maximum High-Level On-State Power Loss Vs. Average On-State Current (Rectangular Current Waveform), 2N5204 Series

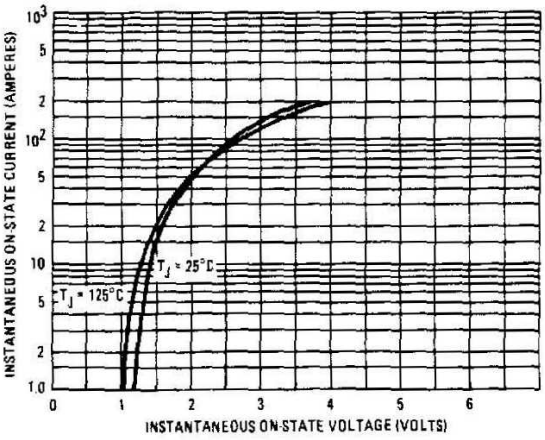

Fig. 14 – Maximum Instantaneous On-State Voltage Vs. Instantaneous On-State Current, 2N5204 Series

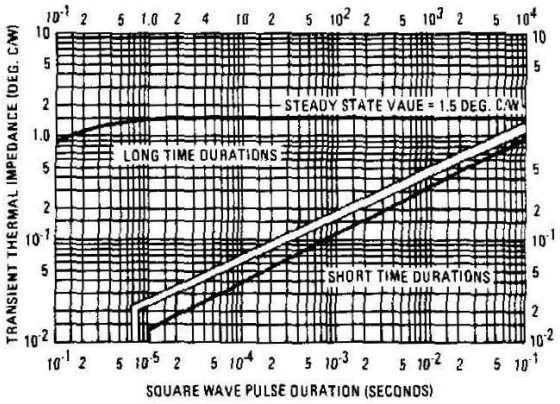

Fig. 15 – Maximum Transient Thermal Resistance, Junction to Case, Vs. Pulse Duration, 2N5204 Series

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