MP65150/MP65151
Precision 60mA-1.7A Programmable Current-Limited Power Distribution Switch

The Future of Analog IC Technology®

DESCRIPTION

MP65150/MP65151 Power Distribution Switch is designed for precision current limiting and provides up to 1.5A continuous output current. It offers programmable current limit between 60mA and 1.7A (typ) with ±10% accuracy by an external resistor. The switch includes an 88mΩ N-channel Power MOSFET and operates from 2.5V to 5.5V input voltage.

The device has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode. It will shutdown when its internal temperature reaches unsafe levels and recover once the device temperature reduces approx 10°C.

It provides built-in soft-start which controls the rise and fall times of the output voltage to limit the initial inrush current and voltage surges.

The reverse-voltage protection feature turns off the MOSFET to protect the device.

The $\overline{\text{FLAG}}$ output will report a fail mode (low level) when over current or over temperature is encountered. The $\overline{\text{FLAG}}$ will not change state when the input UVLO is triggered.

The MP65150/MP65151 is available in space saving 6-pin TQFN 2x2mm package and TSOT23-6 package.

FEATURES

- Up to 1.5A Continuous Output Current
- ±10% Current-Limit Accuracy
- Adjustable Current-Limit, 60mA~1700mA (typ)
- Fast Over-current Response 2µs (typ)
- 2.5V to 5.5V Supply Range
- 88mΩ MOSFET (TQFN Package)
- 1.5µA Maximum Standby Supply Current
- Reverse Input-Output Voltage Protection
- Built-in Soft-Start
- Thermal-Shutdown Protection
- Automatic-on after Fault Removed
- Under-Voltage Lockout
- Deglitched Fault Report
- $\overline{\text{FLAG}}$ won't Change State at Input UVLO Transition
- Bidirectional Fault Deglitch Time
- Active Low & Active High Options

APPLICATIONS

- Smart Phone and PDA
- Portable GPS Device
- Notebook PC
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

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TYPICAL APPLICATION
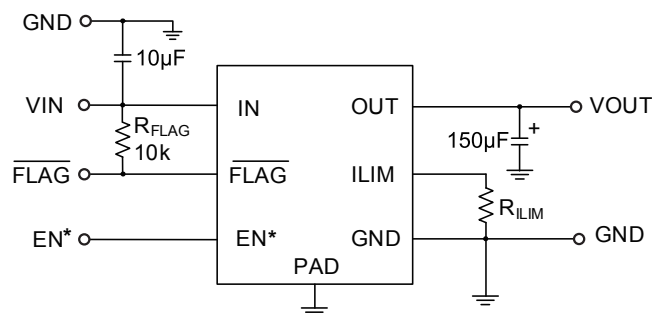
MP65151
(*EN active low for MP65150)

ORDERING INFORMATION

Part Number*	Enable	Switch	Maximum Continuous Load Current	Package	Top Marking	Free Air Temperature (T$_A$)
MP65150DGT	Active Low	Single	1.5A	TQFN6 (2x2mm)	5Y	-40°C to +85°C
MP65151DGT**	Active High			TQFN6 (2x2mm)	AJ	
MP65150DJ	Active Low	Single	1.5A	TSOT23-6	5Y	-40°C to +85°C
MP65151DJ	Active High			TSOT23-6	AAN	

*Both MP65150/1DGT and MP65150/1DJ are available now

** For Tape & Reel, add suffix –Z (e.g. MP65151DGT–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP65151DGT–LF–Z)

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
TQFN6 (2x2mm)	TSOT23-6

MP65150/MP65151
Single-Channel
(EN active low for MP65150)

ABSOLUTE MAXIMUM RATINGS [1]

IN to GND ....-0.3V to +6.5V

ILIM, EN, $\overline{FLAG}$, OUT to GND.....-0.3V to +6.5V
R$_{ILIM}$ Range (1%)....................... 12.4kΩ to 210kΩ
Continuous Power Dissipation (T$_A$ = +25°C) [2]
TQFN(2x2)-6... 1.56W
TSOT23-6 .... 0.57W
Lead Temperature....................................260°C
Storage Temperature ....-65°C to +150°C
Operating Junct. Temp (T$_J$) ......-40°C to +150°C

Thermal Resistance [3]   θ$_{JA}$ θ$_{JC}$

TQFN6 (2x2mm)…. .... 80.......16... °C/W
TSOT23-6…. .... 220.....110.. °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T$_J$(MAX), the junction-toambient thermal resistance θ$_{JA}$, and the ambient temperature T$_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P$_D$(MAX)=(T$_J$(MAX)-T$_A$)/θ$_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_A=+25°C, 2.5V≤V_{IN}≤5.5V, 12.4kΩ≤R_{ILIM}≤210kΩ, R_{FLAG}=10kΩ, unless otherwise noted.

Parameters	Symbol	Test Conditions		Min	Typ	Max	Units
IN Voltage Range	V_{IN}			2.5		5.5	V
FET On_Resistance	$R_{DS(on)}$	V_{IN}=5V, I_{OUT}=100mA -40°C≤T_A≤+85°C	TQFN2x2-6		88	135	mΩ
			TSOT23-6		100	135	
Supply Current	I_{IN_ON}	Device Enabled, V_{OUT}=float, V_{IN}=5.5V			125	145	µA
Shutdown Current	I_{IN_OFF}	Device Disabled, V_{OUT}=float, V_{IN}=5.5V				1.5	µA
Reverse Leakage Current	I_{REV}	V_{IN}=0V, V_{OUT}=5.5V			0.01	1	µA
Current Limit (See Figure 2)	I_{OS}	R_{ILIM}=13kΩ	-40°C≤T_A≤85°C, OUT connected to GND	1530	1700	1870	mA
		R_{ILIM}=20kΩ		960	1190	1360	
		R_{ILIM}=49.9kΩ		450	510	570	
		R_{ILIM}=210kΩ		105	135	166	
		ILIM Shorted to IN		45	60	85	
Short Current Response Time	T_{IOS}	V_{IN}=5V (See Figure 2)			2		µs
Under-voltage Lockout	$INUV_{VTH}$	V_{IN} Rising Edge			2.25	2.45	V
Under-voltage Hysteresis	$INUV_{HYS}$				130		mV
EN Input Logic High Voltage	VIH_{EN}			1.1			V
EN Input Logic Low Voltage	VIL_{EN}					0.66	V
EN Input Leakage Current	I_{EN}	V_{EN}=0~5.5V		-0.5		0.5	µA
$\overline{FLAG}$ Output Logic Low Voltage	V_{OL}	I_{FLAG}=1mA				180	mV
$\overline{FLAG}$ Output High Leakage Current	I_{FLAG_OFF}	V_{FLAG}=5.5V				1	µA
$\overline{FLAG}$ Deglitch Time	T_{FLAG_DEG}	Delay time for assertion or de-assertion due to over-current condition		3.5	7.5	10	ms
Reverse-Voltage Comparator Trip Point ($V_{OUT} − V_{IN}$)	V_{R_TRIP}				135		mV
Time from Reverse-Voltage to MOSFET Turn Off	T_{R_RES}	V_{IN}=5V			5		ms

ELECTRICAL CHARACTERISTICS [4] *(continued)*

T_A=+25°C, 2.5V≤V_{IN}≤5.5V, 12.4kΩ≤R_{ILIM}≤210kΩ, R_{FLAG}=10kΩ, unless otherwise noted.

Parameters	Symbol	Test Conditions		Min	Typ	Max	Units
Thermal Shutdown Threshold	T_J			155			°C
Thermal Shutdown Threshold in Current-Limit Condition	T_{J_CL}			135			°C
Thermal Shutdown Hysteresis	T_{J_HYS}				10		°C
V_{OUT} Rising Time	T_r [5]	R_{LOAD}=100Ω, C_{LOAD}=1µF	V_{IN}=5.5V		0.5	1.5	ms
			V_{IN}=2.5V		0.75		
V_{OUT} Falling Time	T_f [6]	R_{LOAD}=100Ω, C_{LOAD}=1µF	V_{IN}=5.5V	0.1		0.4	
			V_{IN}=2.5V	0.1		0.4	
Turn On Time	T_{on} [7]	R_{LOAD}=100Ω, C_{LOAD}=100µF				3	ms
Turn Off Time	T_{off} [8]					30	

Notes:
4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
5) Measured from 10% to 90% output signal.
6) Measured from 90% to 10% output signal.
7) Measured from 50% EN signal to 90% output signal.
8) Measured from 50% EN signal to 10% output signal.

PIN FUNCTIONS

| TQFN6 [9] Pin #	TSOT23 Pin #	Name	I/O	Description
1	6	OUT	O	Switch output. The V_{OUT} of the internal power FET and output terminal of the IC.
2	5	ILIM	O	External resistor used to set current-limit, recommended $12.4k\Omega \leq R_{ILIM} \leq 210k\Omega$.
3	4	$\overline{FLAG}$	O	Fault status. Logic Low when over-current, over-temperature. Open Drain.
4	3	EN	I	Enable input. Active Low: (MP65150), Active High: (MP65151).
5	2	GND		Ground. Externally connected to PAD.
6	1	IN	I	Input Voltage. Accepts 2.5V to 5.5V input.
PAD		PAD		Internally connected to GND. Used to heat-sink the part to the circuit board traces. Connect PAD to GND pin externally.

Notes:
9) The part has thermal pad on the backside and the pad is GND.
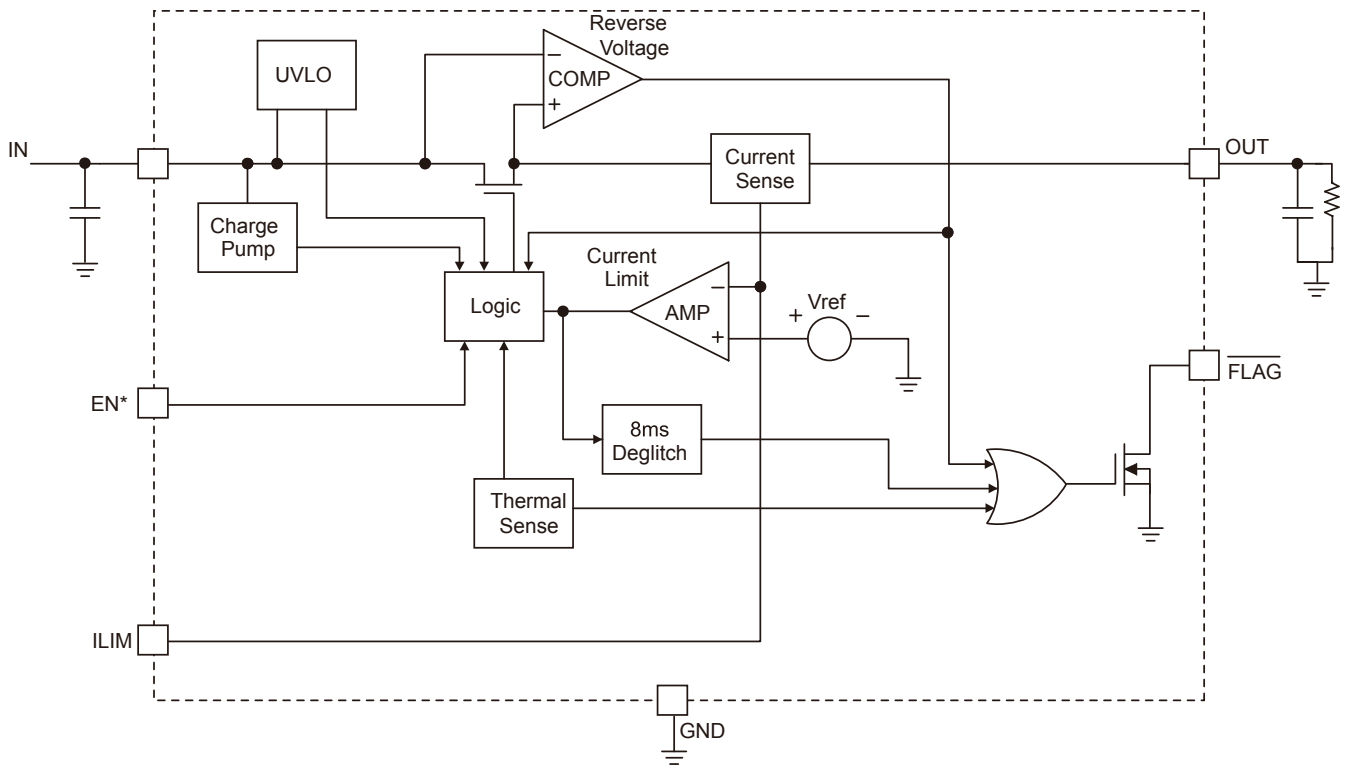
PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS
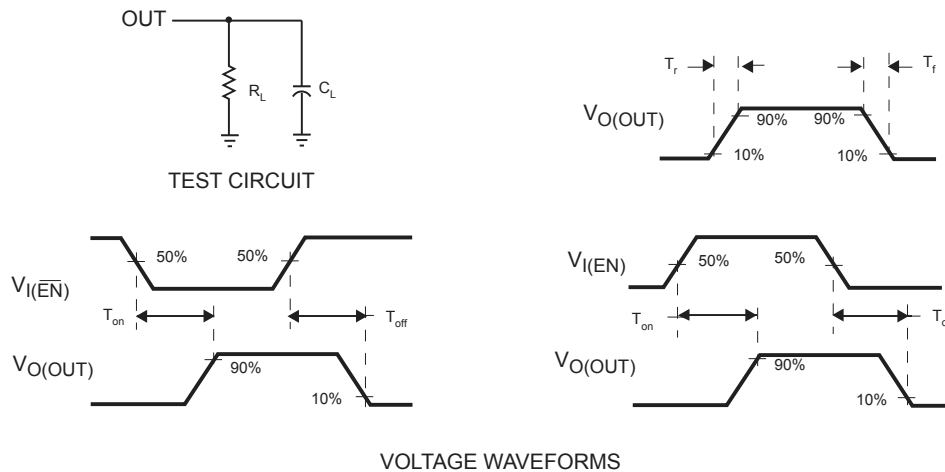
Figure 1—Definition of T_r, T_f, T_{on}, and T_{off}
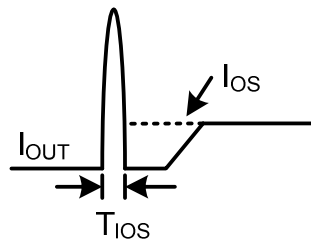
Figure 2—Short Circuit Response Time

BLOCK DIAGRAM
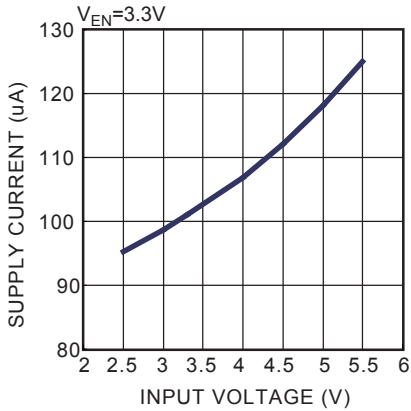

* EN is active low for MP65150

Figure 3—Function Block Diagram
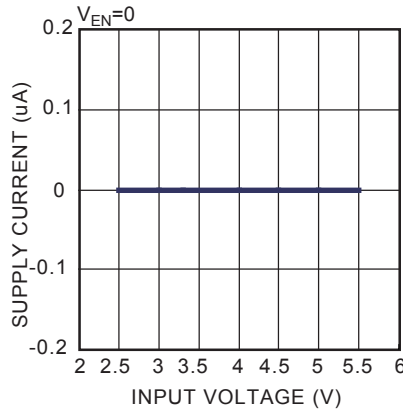
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=5V, R_{ILIM}=20kΩ, R_{FLAG}=10kΩ, C_{OUT}=100µF, T_A=+25°C, unless otherwise noted.

Supply Current, Output Enabled vs. Input Voltage

V_{EN}=3.3V

Supply Current, Output Disabled vs. Input Voltage

V_{EN}=0

Static Drain-Source On-State Resistance vs. Input Voltage

V_{EN}=3.3V, I_{OUT}=1A, TSOT Package
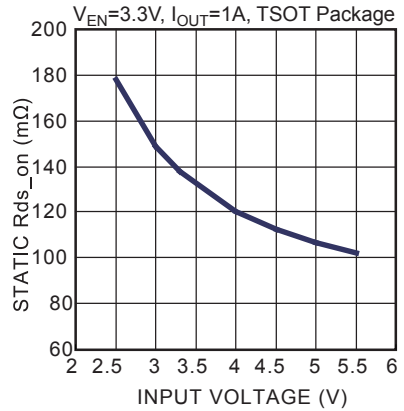
Input to Output Voltage vs. Load Current

V_{EN}=3.3V

V_{IN}=2.5V
V_{IN}=3.3V
V_{IN}=4.5V
V_{IN}=5V
V_{IN}=5.5V
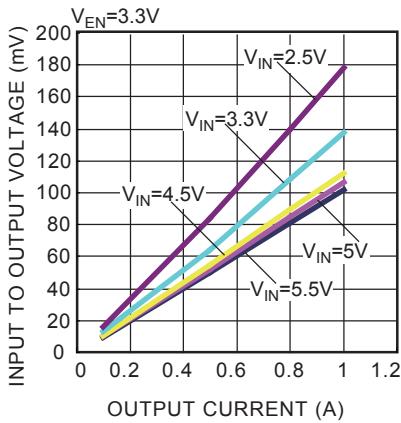
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

V_{IN}=5V, I_{OUT}=0.1A
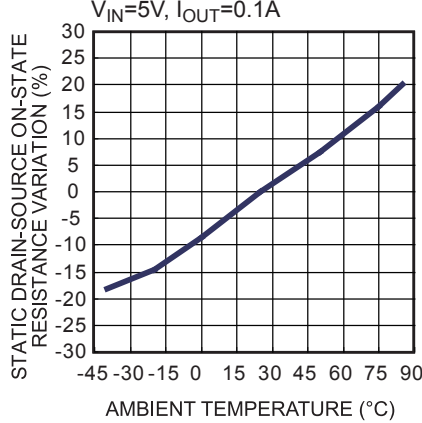
Current Limit vs. Input Voltage

V_{EN}=3.3V, R_{ILIM}=20kΩ
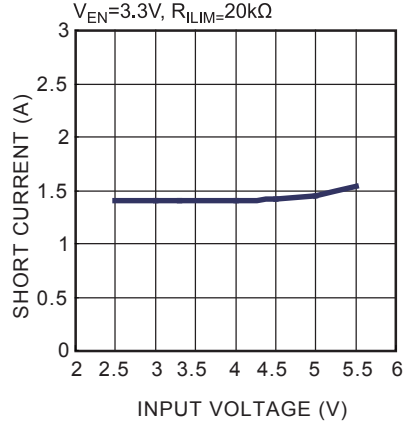
Short Circuit Response Time vs. Peak Current
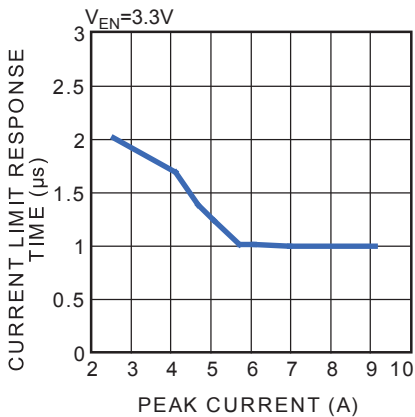
V_{EN}=3.3V

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, R_{ILIM}=20kΩ, R_{FLAG}=10kΩ, C_{OUT}=100µF, T_A=+25°C, unless otherwise noted.

Turn on Time and Rise Time
V_{IN}=5V, R_{ILIM}=20kΩ, R_{OUT}=5Ω, C_{OUT}=100µF

V_{OUT} 2V/div.
V_{EN} 5V/div.
Device Enabled
Inrush Current Limit
I_{IN} 500mA/div.
400µs/div.
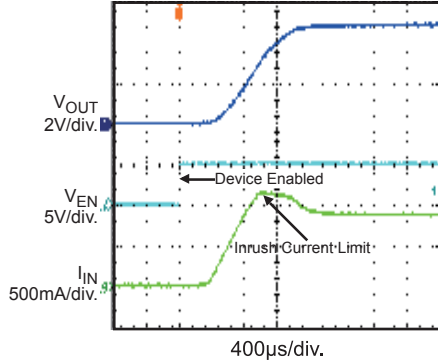
Turn off Time and Fall Time
V_{IN}=5V, R_{ILIM}=20kΩ, R_{OUT}=5Ω, C_{OUT}=100µF

V_{OUT} 2V/div.
V_{EN} 5V/div.
Device Disabled
I_{IN} 500mA/div.
400µs/div.
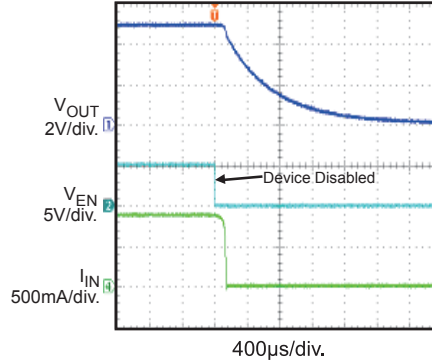
Device Enabled into Short-Circuit
V_{IN}=5V, R_{ILIM}=20kΩ, R_{OUT}=0Ω, C_{OUT}=100µF

Device Enabled
V_{EN} 2V/div.
Current Limit
I_{IN} 500mA/div.
400µs/div.
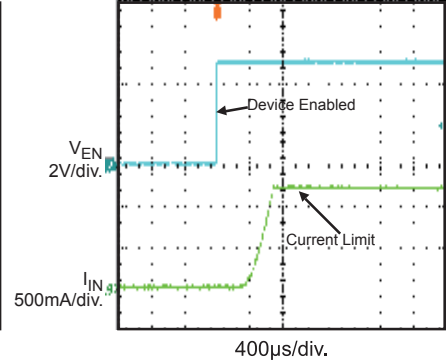
1Ω Load Connected to Enabled Device
V_{IN}=5V, R_{ILIM}=20kΩ, R_{OUT}=1Ω, C_{OUT}=100µF
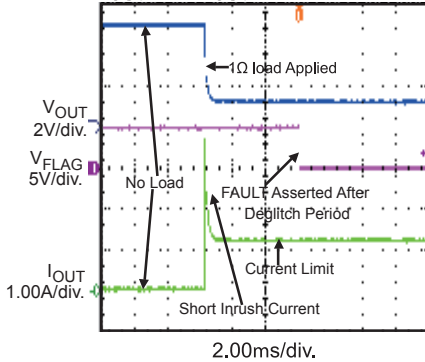
1Ω load Applied
V_{OUT} 2V/div.
V_{FLAG} 5V/div.
No Load
FAULT Asserted After Deglitch Period
I_{OUT} 1.00A/div.
Current Limit
Short Inrush Current
2.00ms/div.

Full-Load to Short-Circuit Transient Response
V_{IN}=5V, R_{ILIM}=20kΩ, R_{OUT}=5Ω, C_{OUT}=100µF

Output Short Circuit Applied
V_{OUT} 2V/div.
FAULT Asserted After Deglitch Period
5Ω Load
V_{FLAG} 5V/div.
Device Begins Thermal Cycling
I_{IN} 1.00A/div.
Device Turns Off and Re-enables into Current-Limit
4.00ms/div.
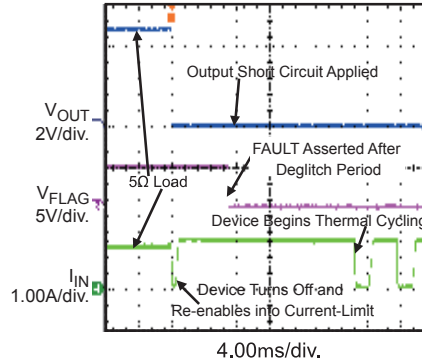
Short-Circuit to Full-Load Recovery Response
V_{IN}=5V, R_{ILIM}=20KΩ, R_{OUT}=5Ω, C_{OUT}=100µF

Output Short Circuit Removed
V_{OUT} 2V/div.
FAULT De-asserted After Deglitch Period
V_{FLAG} 5V/div.
5Ω Load
I_{IN} 1.00A/div.
Device Thermal Cycling when Short-Circuit Presents
4.00ms/div.

No-Load to Short-Circuit Transient Response
V_{IN}=5V, R_{ILIM}=20kΩ, C_{OUT}=100µF

Output Short Circuit Applied
V_{OUT} 2V/div.
FAULT Asserted After Deglitch Period
V_{FLAG} 5V/div.
No Load
Device Begins Thermal Cycling
I_{IN} 1.00A/div.
Device Enters Current-Limit
4.00ms/div.
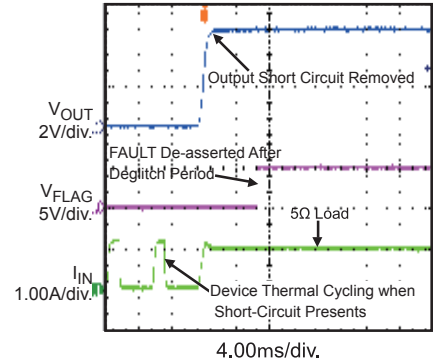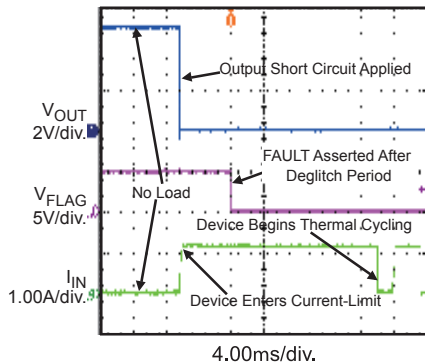
Short-Circuit to No-Load Recovery Response
V_{IN}=5V, R_{ILIM}=20kΩ, C_{OUT}=100µF

Output Short Circuit Removed
V_{OUT} 2V/div.
FAULT De-asserted After Deglitch Period
V_{FLAG} 5V/div.
I_{IN} 1.00A/div.
Device Thermal Cycling when Short-Circuit Presents
4.00ms/div.
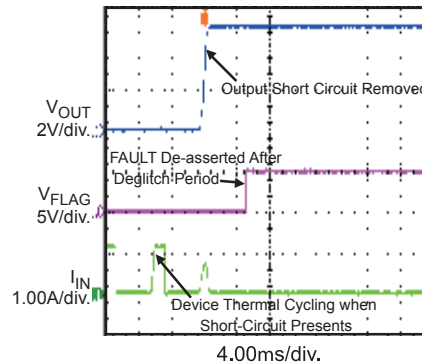
Reverse-Voltage Protection Response
V_{IN}=5V, V_{OUT}=5.5V, R_{ILIM}=20kΩ, R_{OUT}=10Ω
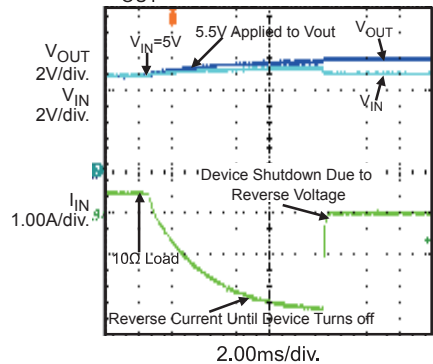
V_{IN}=5V
5.5V Applied to Vout
V_{OUT}
V_{OUT} 2V/div.
V_{IN} 2V/div.
V_{IN}
Device Shutdown Due to Reverse Voltage
I_{IN} 1.00A/div.
10Ω Load
Reverse Current Until Device Turns off
2.00ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*
V_{IN}=5V, R_{ILIM}=20kΩ, R_{FLAG}=10kΩ, C_{OUT}=100μF, T_A=+25°C, unless otherwise noted.

Reverse-Voltage Protection Recovery
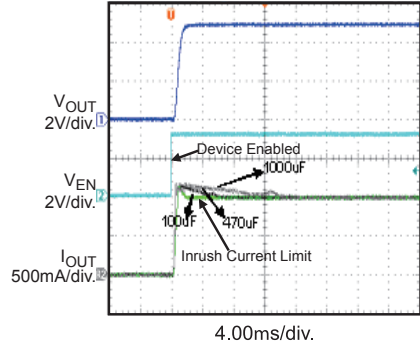V_{IN}=5V, V_{OUT}=5.5V, R_{ILIM}=20kΩ, R_{OUT}=10Ω

V_{OUT} 2V/div.
V_{IN} 2V/div.
I_{IN} 1.00A/div.

V_{OUT}=5.5V
5.5V Removed from Vout
V_{IN}=5V
Reverse-Voltage Recovery, Power Switch Re-enables
10Ω Load
Device Shutdown Due to Reverse Voltage

2.00ms/div.
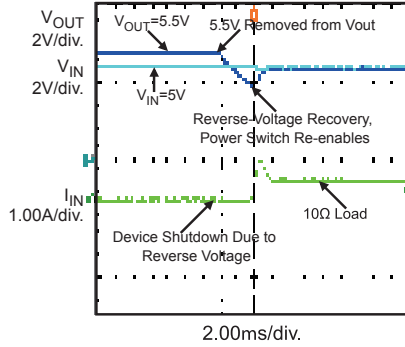
Ramped Load on Enabled Device
V_{IN}=5V, R_{ILIM}=20kΩ, C_{OUT}=100μF

V_{OUT} 2V/div.
V_{FLAG} 5V/div.
I_{OUT} 1.00A/div.

No Load
Ramp load Applied
Ramp load Removed
FAULT De-asserted After Deglitch Period
FAULT Asserted After Deglitch Period
Ramp load
Current Limit

4.00ms/div.
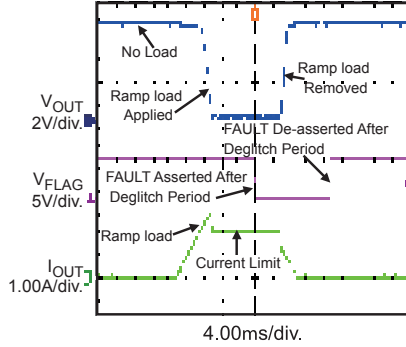
Inrush Current with Different Load Capacitance
V_{IN}=5V, R_{OUT}=5Ω, V_{EN}=3.3V, Start up by EN

V_{OUT} 2V/div.
V_{EN} 2V/div.
I_{OUT} 500mA/div.

Device Enabled
1000uF
100uF
470uF
Inrush Current Limit

4.00ms/div.

DETAILED DESCRIPTION

The MP65150/MP65151 is a precision current-limit power distribution switch which can provide up to 1.5A continuous output current. It allows the user to program the current-limit between 60mA and 1.7A (typ) with ±10% accuracy via an external resistor connected between ILIM and GND pins.

The switch includes an N-channel power MOSFET and an internal charge pump to generate the gate driver voltage which is higher than input. The charge pump can work from input as low as 2.5V.

The device has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode. It will shutdown when its internal temperature reaches unsafe levels and recover once the device temperature reduces approx 10°C.

It provides built-in soft-start which controls the rise and fall times of the output voltage to limit the initial inrush current and voltage surges.

The reverse-voltage protection feature turns off the MOSFET to protect the device.

The $\overline{FLAG}$ output will report a fail mode (low level) when over current or over temperature is encountered. The $\overline{FLAG}$ will not change state when the input UVLO is triggered.

Over Current

MP65150/MP65151 switches into to a constant-current mode when responding to over-current conditions. It ramps the output current to current limit value I_{OS} and reduces the output voltage accordingly. MP65150/MP65151 will be thermal cycles only if the over current condition stays long enough to trigger thermal protection.

Trigger over current protection for different overload conditions occurring in applications:

1) The output has been shorted or overloaded before the device is enabled or input applied. MP65150/MP65151 detects the short or overload and switches into constant-current mode immediately.

2) A short or an overload occurs after the device is enabled. The device responds to the over-current condition within time T_{IOS}. The current-sense amplifier is overdriven, so high current may flow during this period of time and the internal current-limit MOSFET is disabled momentarily before the current-limit circuit can react. Then the current-sense amplifier recovers switches into constant-current mode. Similar to the previous case, the MP65150/MP65151 will limit the current to I_{OS} until the overload condition is removed or the device entering thermal cycle.

3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The MP65150/MP65151 is capable of delivering current up to the current-limit without damaging the device.

Reverse-Voltage Protection

To prevent damage the device on the input side of MP65150/MP65151, the N-channel MOSFET will be turned off immediately whenever the output voltage exceeds the input voltage by 135mV (typ). There is an internal comparator which compares the voltage difference betweens drain and source of N-channel MOSFET. The reverse voltage protection circuit only activates when $R_{DS(on)}$ x $I_{Reverse}$>135mV, that means there must be a temporary large reverse current from output to input that can trigger the reverse-voltage protection. After the comparator is triggered, the internal driver circuit starts to discharge the gate voltage via a constant current. It needs several milliseconds to fully turn off the N-channel MOSFET.

This protection could prevent significant current sinking into the input side.

The MP65150/MP65151 exist the protection mode and enter to normal state once the reverse-voltage condition is removed. No need to recycle the input power or enable logic.

There is no reverse current flow through the switch at the condition of 0V input and 5.5V output whatever the enable is high or low.

Flag Response

The $\overline{\text{FLAG}}$ pin is an open drain configuration. When over current or over temperature is encountered, $\overline{\text{FLAG}}$ will report a fail mode (low level).

For over current, 7.5ms deglitch time-out is needed. This is used to ensure that no false fault signal is reported. This internal deglitch circuit eliminates the need for components.

For over temperature, the $\overline{\text{FLAG}}$ pin is not deglitched.

The $\overline{\text{FLAG}}$ will not change state when the input UVLO is triggered.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP65150/MP65151 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec. Built-in 130mV hysteresis prevents unwanted on/off power cycling due to input voltage drop from large current surges.

Enable

The logic pin disables the chip to reduce the supply current. Enable high activate the MP65151 while enable low activate the MP65150. The device will operate once the enable signal reaches the appropriate level. There is no hysteresis for enable pin. The input is compatible with both COMS and TTL.

Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heat the junction. The die temperature is internally monitored by two independent thermal sensing circuits until the thermal limit is reached. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current limit. The second thermal sensor turns off the power-switch when the die temperature exceeds 155°C (min) regardless of whether the switch is in current limit. Both two thermal sensors have built-in hysteresis. It will turn on the switch once it is cooled down 10°C approximately. MP65150/MP65151 continues to cycle off and on until the fault is removed.

APPLICATION INFORMATION

Power-Supply Considerations

Over 10µF capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin is recommended when the load is heavy.

A 0.01µF to 0.1µF ceramic bypassing capacitor is recommended to improve the immunity of the device to transient conditions and noise.
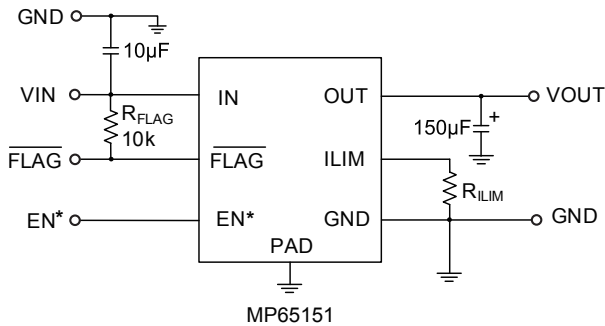
* EN is active low for MP65150

Figure 4—Application Circuit

Programming the Current-Limit

The current-limit is programmed via an external resistor from ILIM to GND. The recommended 1% resistor range of R_{ILIM} is 12.4kΩ≤R_{ILIM}≤210kΩ. The ILIM pin can be connected to IN to set the current-limit at its minimum level of 60mA (typ).

It's important to consider the tolerance of current limit when selecting a value for R_{ILIM}. Some applications require that the minimum current limit is above a certain current level, while some applications require the maximum current limit is below a certain current level.

Figure 5 can be used to calculate the current limit value for a given ILIM resistor and also can be used to select ILIM resistor for a certain current limit.

R_{ILIM} can be selected to provide a current limit that occurs 1) above a minimum load current or 2) below a maximum load current.

To determine above a minimum current limit, find the maximum desired load current on the $I_{os(min)}$ curve and choose a value of R_{ILIM} below this value. The resulting maximum current limit is the intersection of the selected value of R_{ILIM} and the $I_{os(max)}$ curve.

To determine below a maximum current limit, find the maximum desired load current on the $I_{os(max)}$ curve and choose a value of R_{ILIM} above this value. The resulting minimum current limit is the intersection of the selected value of R_{ILIM} and the $I_{os(min)}$ curve.

In theory, the result of current limit multiplied by R_{ILIM} is a constant. But the internal amplifier has offset, as a result the current limit vs $1/R_{ILIM}$ is not linear at small programming resistor range. The theoretical current limit calculation formula is given as following:

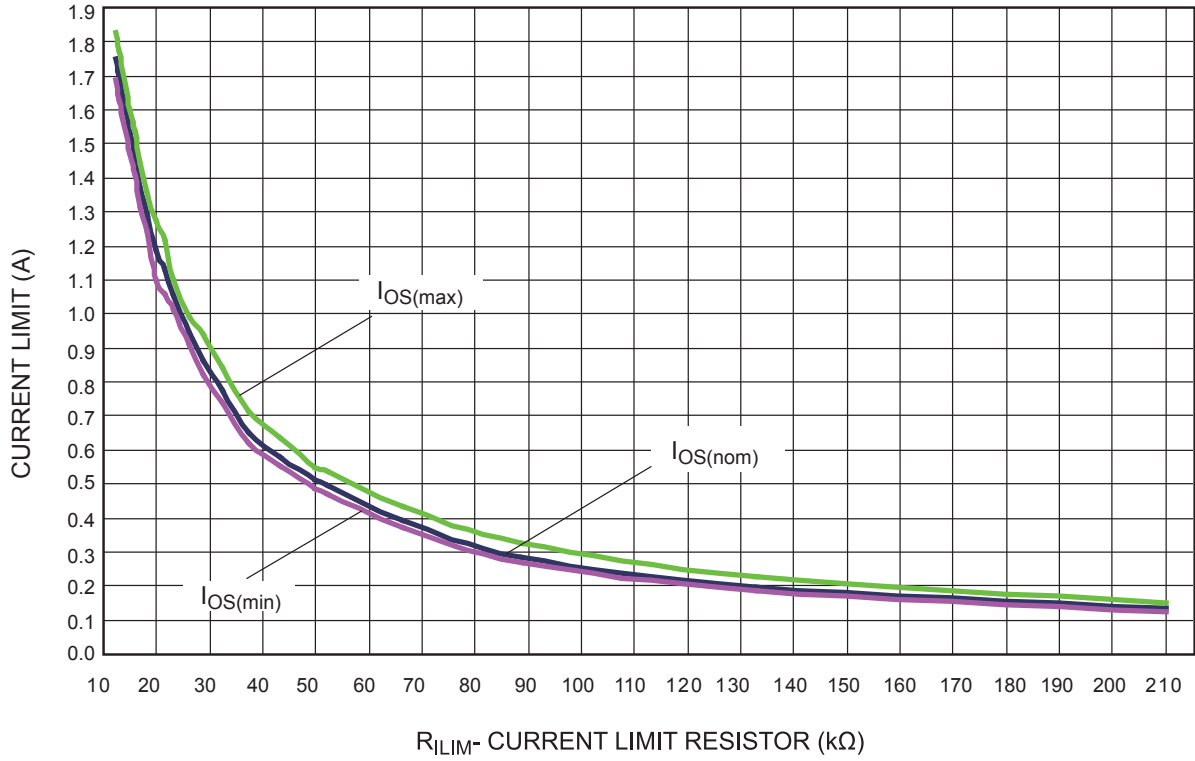$$I_{OSnom}(A) = \frac{18.818V}{R_{ILIM}^{0.9248}k\Omega}$$

$$I_{OSmin}(A) = \frac{18.489V}{R_{ILIM}^{0.9342}k\Omega}$$

$$I_{OSmax}(A) = \frac{18.229V}{R_{ILIM}^{0.8944}k\Omega}$$

Where:

$$12.4k\Omega \le R_{ILIM} \le 210k\Omega .$$

For better accuracy current limit setting, Table1 and Figure5 are highly recommended. Those curve or data are provided basing on large amount experimental test results.

Figure 5—Current-Limit vs R$_{ILIM}$

Table 1 shows the common R_{ILIM} vs. current limit data. 1% accuracy resistor is recommended for general applications. If a precision current limit is needed, it's better to use more tightly tolerance resistors, e.g. 0.5% or 0.1%. Resistor accuracy tolerance is not included in Table 1.

Table1—Common R_{ILIM} Resistor Selections

| 1% Accuracy Resistor (kΩ)	Current Limit (A)		
	IOS MIN	IOS Nom	IOS MAX
12.4	1.690	1.749	1.830
13	1.627	1.700	1.769
15	1.473	1.533	1.603
15.8	1.408	1.467	1.538
16.9	1.311	1.370	1.441
18.2	1.242	1.293	1.352
20	1.099	1.190	1.277
21.5	1.060	1.130	1.220
23.2	1.013	1.053	1.098
26.1	0.908	0.947	0.991
28.7	0.823	0.861	0.938
32.4	0.736	0.772	0.843
37.4	0.619	0.650	0.715
43.2	0.550	0.579	0.637
49.9	0.485	0.510	0.547
52.3	0.470	0.495	0.535
66.5	0.370	0.391	0.433
88.7	0.268	0.286	0.324
133	0.185	0.198	0.226
210	0.126	0.135	0.150
Short ILIM to IN	0.055	0.060	0.072

While the maximum recommended value of R_{ILIM} is 210kΩ, there is one additional configuration that allows for a lower current limit. The ILIM pin may be connected directly to IN to provide a 60 mA (typ) current limit.

Auto-Retry Function

Figure 6 shows an auto-retry circuit implanted by an external resistor and capacitor.
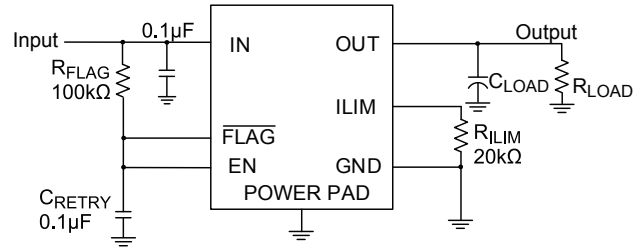
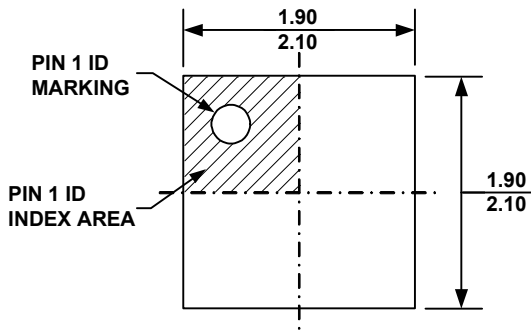**Figure 6—Auto-Retry Application**
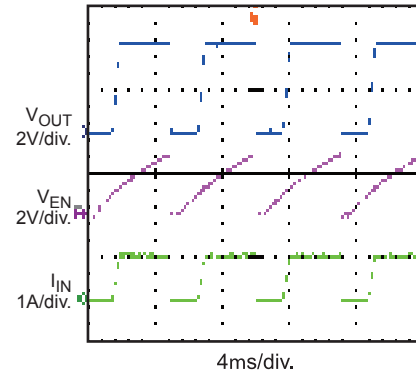
Figure 7—Auto-Retry Waveform

When over-current happens the $\overline{FLAG}$ will report a low level, EN is pulled down immediately and thus the part is shutdown.
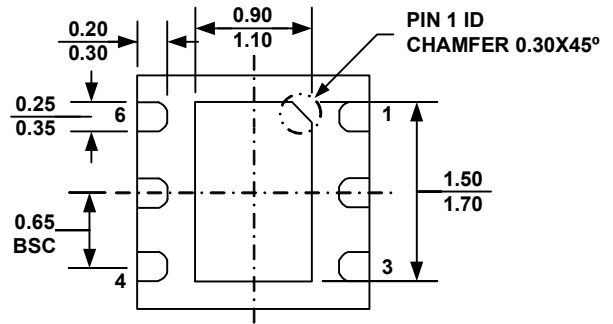
During the moment of EN shutdown, the $\overline{FLAG}$ changes to high impedance allowing C_{RETRY} to begin charging. After a time delay determined by the RC constant, the EN voltage reaches its turn-on threshold and re-enables the part. The part will continue to cycle in this manner until the fault condition is removed.
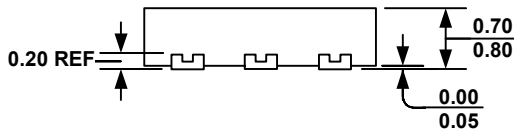
PACKAGE INFORMATION
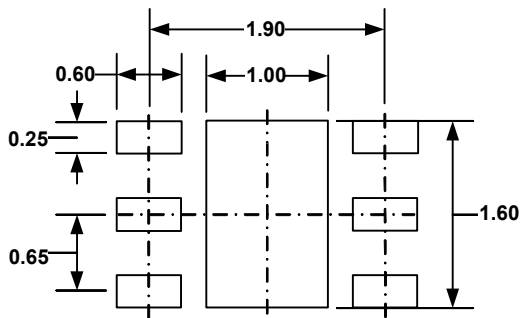
TQFN6 (2x2mm)

1.90 / 2.10

PIN 1 ID MARKING

PIN 1 ID INDEX AREA

1.90 / 2.10

TOP VIEW

0.20 / 0.30

0.90 / 1.10

PIN 1 ID CHAMFER 0.30X45º

0.25 / 0.35   6

1

0.65 BSC

1.50 / 1.70

4

3

BOTTOM VIEW

0.20 REF
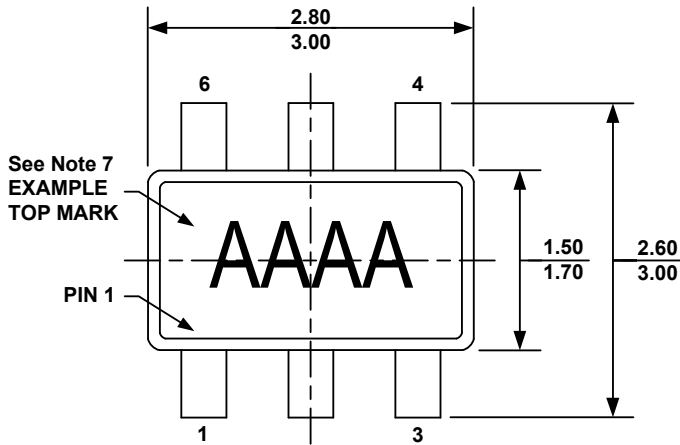
0.70 / 0.80

0.00 / 0.05

SIDE VIEW

1.90

0.60

1.00

0.25

0.65

1.60

RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
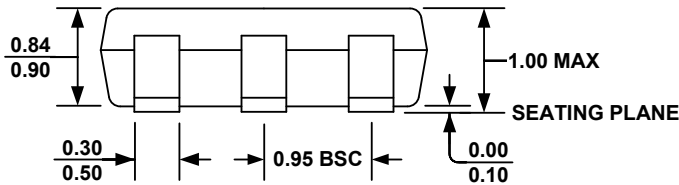4) JEDEC REFERENCE IS MO-229, VARIATION VCCC.
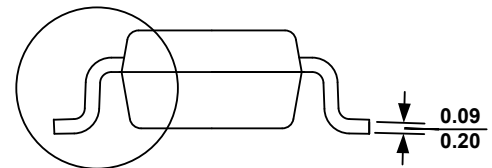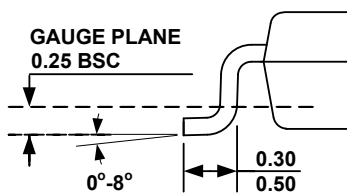5) DRAWING IS NOT TO SCALE.

TSOT23-6

2.80
3.00

6   4

See Note 7
EXAMPLE
TOP MARK

AAAA

PIN 1

1.50
1.70

2.60
3.00

1   3

TOP VIEW

0.60
TYP

0.95
BSC

1.20
TYP

2.60
TYP

RECOMMENDED LAND PATTERN

0.84
0.90

0.30
0.50

0.95 BSC

1.00 MAX

SEATING PLANE

0.00
0.10

FRONT VIEW

SEE DETAIL "A"

0.09
0.20

SIDE VIEW

GAUGE PLANE
0.25 BSC

0°-8°

0.30
0.50
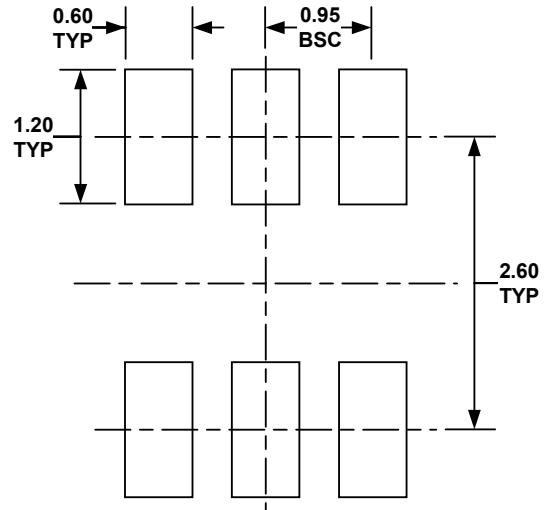
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH,
   PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH
   OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING)
   SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM
   LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)