

GENERAL DESCRIPTION

AKD5388 is an evaluation board for the digital audio 24bit 216kHz 4ch A/D converter, AK5388. The AKD5388-A includes the input circuit and also has a digital interface transmitter. Further, the AKD5388-A can achieve the interface with digital audio systems via opt-connector.

AKD5388-A is an evaluation board for AK5388, of 216kHz sampling 24bit 4ch A/D converter for professional audio. AKD5388-A has analog input buffer circuits, clock generator circuits, and digital audio interfaces. Therefore it can achieve the interface with digital audio systems via optical connector. And it can achieve the direct interface with AKEMD's D/A converter evaluation boards of via 10-line flat cable.

Ordering guide

AKD5388-A --- AK5388 Evaluation Board

FUNCTION

- DIT with optical output
- BNC connector for an external clock input

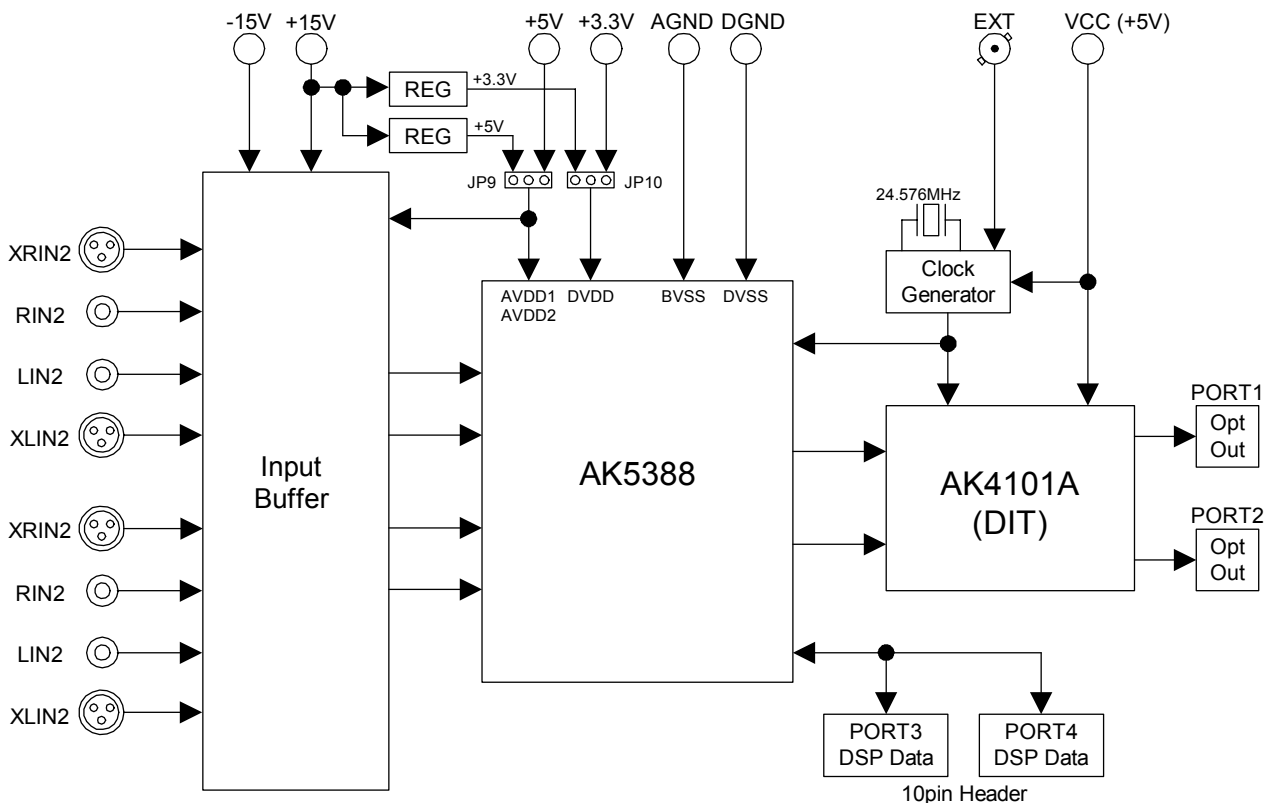


Figure 1. AKD5388-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

1) Set up the power supplies lines.

Name of connector	Color of connector	Voltage	Used for	Comment and attention	Default Setting
+15V	Red	+12~15V	Regulator T1, Regulator T2. OP-Amplifier	This connector should be connected. And this connector is used when AVDD of AK5388 is supplied from regulator T1 and DVDD of AK5388 is supplied from regulator T2. In this case, JP9 and JP10 should be REG side. When this is REG side, +5V and +3.3V connector should be open. (Default)	+15V
-15V	Blue	-12~-15V	OP-Amplifier	This connector should be connected.	-15V
+5V	Orange	+4.75~+5.25V	AVDD of AK5388, Analog input buffer circuit	This connector is used when AVDD of AK5388 is supplied from +5V connector without regulator T1. In this case, JP9 should be +5V side.	Open
+3.3V	Green	+3.0~+3.6V	DVDD of AK5388	This connector is used when DVDD of AK5388 is supplied from +3.3V connector without regulator T2. In this case, JP10 should be +3.3V side.	Open
VCC	Orange	+4.75~+5.25V	AK4101A, Logic circuit	This connector should be connected.	+5V
AGND	Black	0V	Analog ground	This connector should be connected.	0V
DGND	Black	0V	Digital ground	This connector is used when DGND is supplied besides AGND. In this case, JP15 should be open. (Default)	0V

Table 1. Power supply lines

(Note) Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.

The AK5388 and AK4101A should be reset once bringing SW3 = “L” upon power-up.

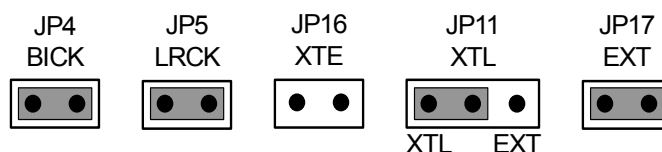
Note: When AK5388 is TDM mode, the AK4101A does not support the TDM mode. Therefore, PORT1 and PORT2 cannot be used. Also, when the sampling frequency is used by 96kHz or more, PORT1 and PORT2 cannot be used. Please use PORT3 (DSP1) and PORT4 (DSP2).

■ Evaluation mode

(1) Slave mode

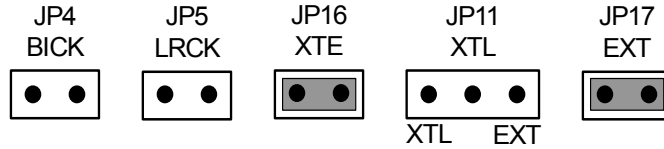
(1-1) A/D evaluation using DIT function of AK4101A

PORT1 and PORT2 are used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX197). It is possible to connect AKEMD's D/A converter evaluation boards on the digital-amplifier, which equips DIR input. Nothing should be connected to PORT3 (DSP1) and PORT4 (DSP2). In case of using external clock through a BNC connector (J9), select EXT on JP11 (MCLK) and short JP16 (XTE) and JP17 (EXT).



(1-2) Feeding all clocks from PORT3 (DSP1)

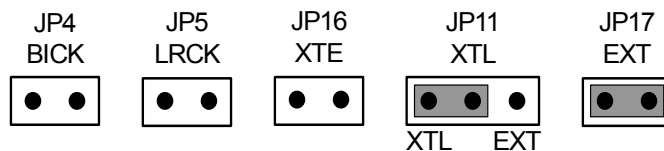
Under the following set-up, all external clocks (MCLK, BICK, LRCK) can be fed through PORT3 (DSP1). The A/D converted data is output from SDTO1/SDTO2 of PORT3 (DSP1). Also, the A/D converted data is output through optical connector (TOTX197).



(2) Master mode

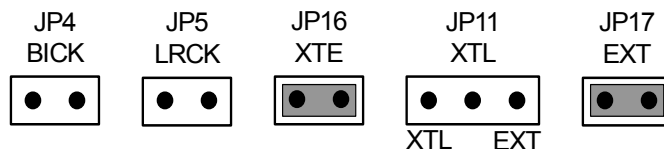
(2-1) A/D evaluation using DIT function of AK4101A

PORT1 and PORT2 are used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX197). It is possible to connect AKEMD's D/A converter evaluation boards on the digital-amplifier, which equips DIR input. Nothing should be connected to PORT3 (DSP1) and PORT4 (DSP2). In case of using external clock through a BNC connector (J9), select EXT on JP11 (MCLK) and short JP16 (XTE) and JP17 (EXT).



(2-2) Feeding all clocks from PORT3 (DSP1)

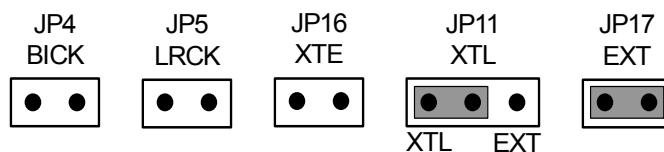
Under the following set-up, all external clocks (MCLK, BICK, LRCK) can be fed through PORT3 (DSP1). The A/D converted data is output from SDTO1/SDTO2 of PORT3 (DSP1). Also, the A/D converted data is output through optical connector (TOTX197).



(3) Cascade TDM mode

(3-1) Evaluation of cascade TDM mode that uses two AKD5388-A

PORT3 (DSP1) and PORT4 (DSP2) are used. In case of using external clock through a BNC connector (J9), select EXT on JP11 (MCLK) and short JP16 (XTE) and JP17 (EXT).



■ Default configuration of switch and jumper pins

	Name	Setting		Name	Setting
SW1-1	M SN	OFF	SW2-1	DIF	OFF
SW1-2	CKS2	ON	SW2-2	CKS1	ON
SW1-3	CKS1	OFF	SW2-3	CKS0	ON
SW1-4	CKS0	OFF			
SW1-5	TDM1	OFF			
SW1-6	TDM0	OFF			
SW1-7	MONO	OFF			
SW1-8	HPFE	OFF			

Table 2. Switch setting

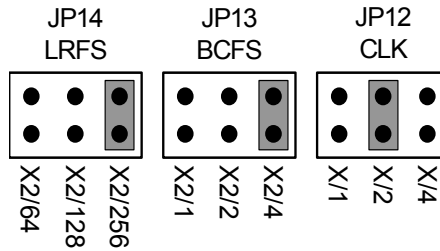
	Name	Setting		Name	Setting		Name	Setting
JP1	TEST1	Short	JP11	MCLK	XTL	JP21	RIN1-BNC	Short
JP2	TEST2	Short	JP12	CLK	X/2	JP22	LIN2-BNC	Short
JP3	TEST3	Short	JP13	BCFS	X2/4	JP23	LIN2-BNC	Short
JP4	BICK	Short	JP14	LRFS	X2/256	JP24	RIN2-BNC	Short
JP5	LRCK	Short	JP15	GND	Open	JP25	RIN2-BNC	Short
JP6	TDMIN	GND	JP16	XTE	Open			
JP7	D-SEL1	SDTO1	JP17	EXT	Short			
JP8	D-SEL2	SDTO1	JP18	LIN1-BNC	Short			
JP9	AVDD	REG	JP19	LIN1-BNC	Short			
JP10	DVDD	REG	JP20	RIN1-BNC	Short			

Table 3. Jumper pins setting

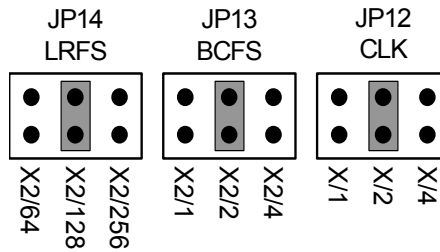
■ Other jumper pins set up

- JP6 (TDMIN) : Input data selection to TDMIN
 EXT : Select data of SDTO1 of PORT3(DSP1) or PORT4(DSP2) is input.
 In this case, either JP7 or JP8 is set to TDMIN. Separated.
 GND : 0V is input. <Default>
- JP7 (D-SEL1) : Selection to SDTO1 of PORT3
 SDTO1 : Connects with SDTO1 of AK5388. <Default>
 TDMIN: Connects with TDMIN of AK5388.
- JP8 (D-SEL2) : Selection to SDTO1 of PORT4
 SDTO1 : Connects with SDTO1 of AK5388. <Default>
 TDMIN: Connects with TDMIN of AK5388.
- JP9 (AVDD) : Select AVDD for AK5388
 +5V : Supply from +5V connector.
 REG : Supply from regulator T1. In this case, +5V connector should be open. <Default>
- JP10 (DVDD): Select DVDD for AK5388
 +3.3V : Supply from +3.3V connector.
 REG : Supply from regulator T2. In this case, +3.3V connector should be open. <Default>

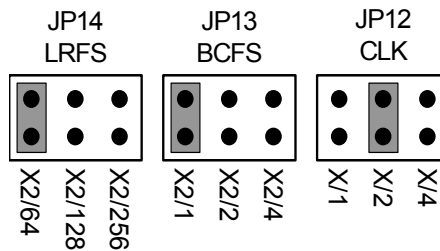
6. JP12 (CLK), JP13 (BCFS), JP14 (LRFS) : Select clock frequency
 fs=48kHz : <Default>



fs=96kHz :



fs=192kHz:



Other frequency: Please set JP12, JP13, and JP14 properly.

7. JP15 (GND) : Analog ground and Digital ground
 OPEN : Separated. <Default>
 SHORT : Common. (The connector “DGND” can be open.)
8. JP18, JP19 (LIN1-BNC) : Input terminal selection of LIN1
 OPEN : Select to XLR connector (J1).
 SHORT : Select to RCA connector (J5). <Default>
9. JP20, JP21 (RIN1-BNC) : Input terminal selection of RIN1
 OPEN : Select to XLR connector (J2).
 SHORT : Select to RCA connector (J6). <Default>
10. JP22, JP23 (LIN2-BNC) : Input terminal selection of LIN2
 OPEN : Select to XLR connector (J3).
 SHORT : Select to RCA connector (J7). <Default>
11. JP24, JP25 (RIN2-BNC) : Input terminal selection of RIN2
 OPEN : Select to XLR connector (J4).
 SHORT : Select to RCA connector (J8). <Default>

■ DIP Switch Setting

[SW1] (MODE1): Setting the evaluation mode for AK5388
ON is “H”, OFF is “L”.

No.	Name	OFF (“L”)	ON (“H”)	Default
1	M SN	Slave mode	Master mode	OFF (“L”)
2	CKS2	See Table 6		ON (“H”)
3	CKS1			OFF (“L”)
4	CKS0			OFF (“L”)
5	TDM1			See Table 7
6	TDM0	OFF (“L”)		
7	MONO	MONO mode OFF	MONO mode ON	OFF (“L”)
8	HPFE	High pass filter OFF	High pass filter ON	OFF (“L”)

Table 4. Mode setting of AK5388

[SW2] (MODE2): Setting the evaluation mode for AK5388 and AK4101A
ON is “H”, OFF is “L”.

No.	Name	OFF (“L”)	ON (“H”)	Default
1	DIF	MSB justified	I ² S Compatible	OFF (“L”)
3	CKS1	See Table 8		ON (“H”)
4	CKS0			ON (“H”)

Table 5. Mode setting of AK5388 and AK411A

M SN	CKS2	CKS1	CKS0	MCLK Frequency	
L	L	L	L	128fs (108KHz < fs ≤ 216KHz)	Default
	L	L	H	192fs (108KHz < fs ≤ 216KHz)	
	L	H	L	256fs (8KHz ≤ fs ≤ 54KHz)	
	L	H	H	256fs (54KHz < fs ≤ 108KHz)	
	H	L	L	Auto (8KHz ≤ fs ≤ 216KHz)	
	H	L	H	384fs (8KHz ≤ fs ≤ 54KHz)	
	H	H	L	512fs (8KHz < fs ≤ 54KHz)	
H	L	L	L	128fs (108KHz < fs ≤ 216KHz)	
	L	L	H	192fs (108KHz < fs ≤ 216KHz)	
	L	H	L	256fs (8KHz ≤ fs ≤ 54KHz)	
	L	H	H	256fs (54KHz < fs ≤ 108KHz)	
	H	L	L	384fs (54KHz ≤ fs ≤ 108KHz)	
	H	L	H	384fs (8KHz ≤ fs ≤ 54KHz)	
	H	H	L	512fs (8KHz < fs ≤ 54KHz)	
H	H	H	768fs (8KHz ≤ fs ≤ 54KHz)		

Table 6. MCLK Frequency Setting of AK5388

TDM1	TDM0	Mode	BICK	
L	L	Normal	48 ~ 128fs	Default
L	H	TDM256	256fs	
H	L	N/A	N/A	
H	H	TDM128	128fs	

Table 7. Mode setting of AK5388

CKS1	CKS0	MCLK	fs	
L	L	128fs	28k ~ 192kHz	
L	H	256fs	28k ~ 108kHz	
H	L	384fs	28k ~ 54kHz	
H	H	512fs	28k ~ 54kHz	Default

Table 8. MCLK Frequency Setting of AK4101A

Note: AK4101A does not support MCLK=768fs.

■ The function of the toggle SW

Upper-side is “H” and lower-side is “L”.

[SW3] (PDN): Resets of AK5388 and AK4101A. Keep “H” during normal operation.

■ Analog input buffer circuit

An analog input buffer circuit example (1st order HPF; $f_c=0.70\text{Hz}$, 2nd order LPF; $f_c=304\text{kHz}$, gain=-14.5dB) is shown in Figure 2. The analog signal is able to input through XLR or RCA connectors. (For RCA input, jumper should be short. For XLR input, jumper should be open.) The input level of this circuit is $\pm 15.4\text{Vpp}$ (AK5388: $\pm 2.9\text{Vpp}$ Typ.). When using this circuit, analog characteristics at $f_s=48\text{kHz}$ is DR=118dB, S/(N+D)=TBDdB.

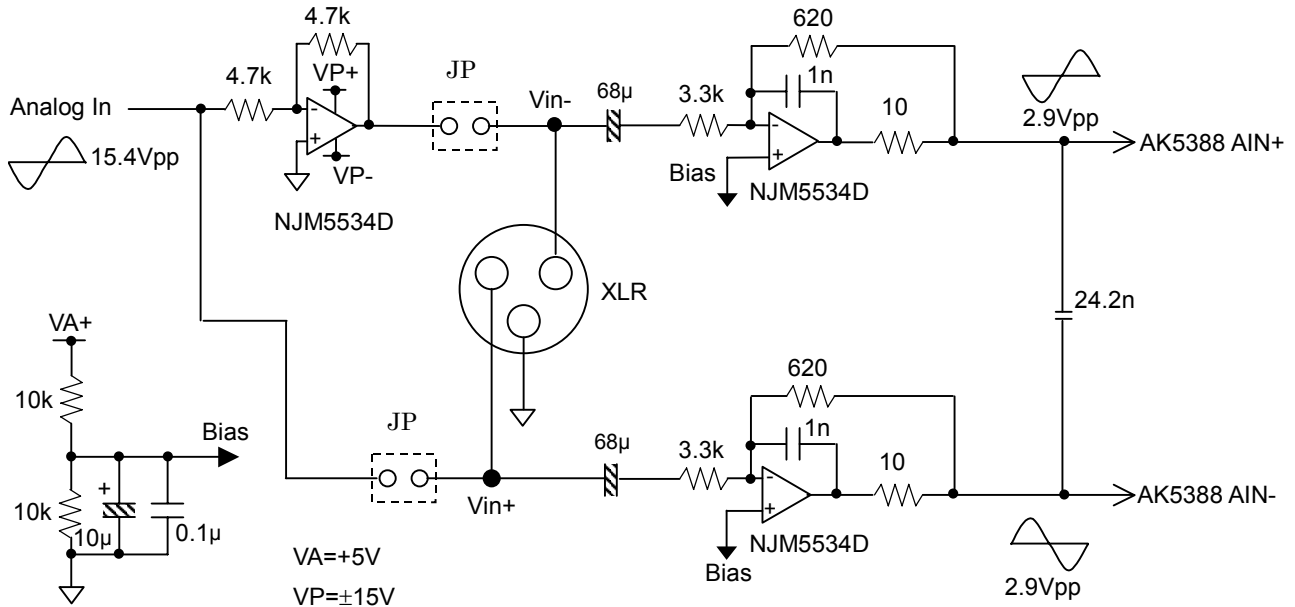


Figure 2. Analog input buffer circuits examples

F_{in}	1Hz	10Hz
Frequency Response	-1.56dB	-0.02dB

Table 9. Frequency Response of HPF

F_{in}	20kHz	40kHz	6.144MHz
Frequency Response	-0.005dB	-0.02dB	-15.6dB

Table 10. Frequency Response of LPF

* AKEMD assumes no responsibility for the trouble when using the circuit examples.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
- MCLK : 512fs (fs=48kHz), 256fs (fs=96kHz), 128fs (fs=192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : AVDD = 5.0V(REG), DVDD = 3.3V(REG)
- Interface : DSP Data (10pin Header : PSIA)
- Temperature : Room

[Measurement Results]

Parameter	Result		Unit
	L1ch / R1ch	L2ch / R2ch	
ADC Analog Input Characteristics:			
S/(N+D): Filter=none (fs=48kHz, -1dBFS, BW=20kHz)	112.3 / 110.2	110.0 / 111.0	dB
(fs=96kHz, -1dBFS, BW=40kHz)	108.8 / 107.4	107.4 / 107.9	dB
(fs=192kHz, -1dBFS, BW=40kHz)	108.8 / 107.4	107.3 / 108.3	dB
D-Range: Filter=A-weighted (fs=48kHz, -60dBFS, BW=20kHz)	120.0 / 119.9	119.9 / 120.0	dB
(fs=96kHz, -60dBFS, BW=40kHz)	119.4 / 119.5	119.5 / 119.5	dB
(fs=192kHz, -60dBFS, BW=40kHz)	119.5 / 119.7	119.6 / 119.6	dB
S/N: Filter=A-weighted (fs=48kHz, -60dBFS, BW=20kHz)	120.2 / 120.0	120.1 / 120.1	dB
(fs=96kHz, -60dBFS, BW=40kHz)	119.3 / 119.5	119.5 / 119.4	dB
(fs=192kHz, -60dBFS, BW=40kHz)	119.5 / 119.6	119.7 / 119.6	dB
S/N MONO mode: Filter=A-weighted (fs=48kHz, BW=20kHz)	123.0 / 123.0	123.1 / 123.1	dB
(fs=96kHz, BW=40kHz)	122.4 / 122.5	122.5 / 122.5	dB
(fs=192kHz, BW=40kHz)	122.6 / 122.6	122.6 / 122.6	dB

[ADC Plot: fs=48kHz]

AKM

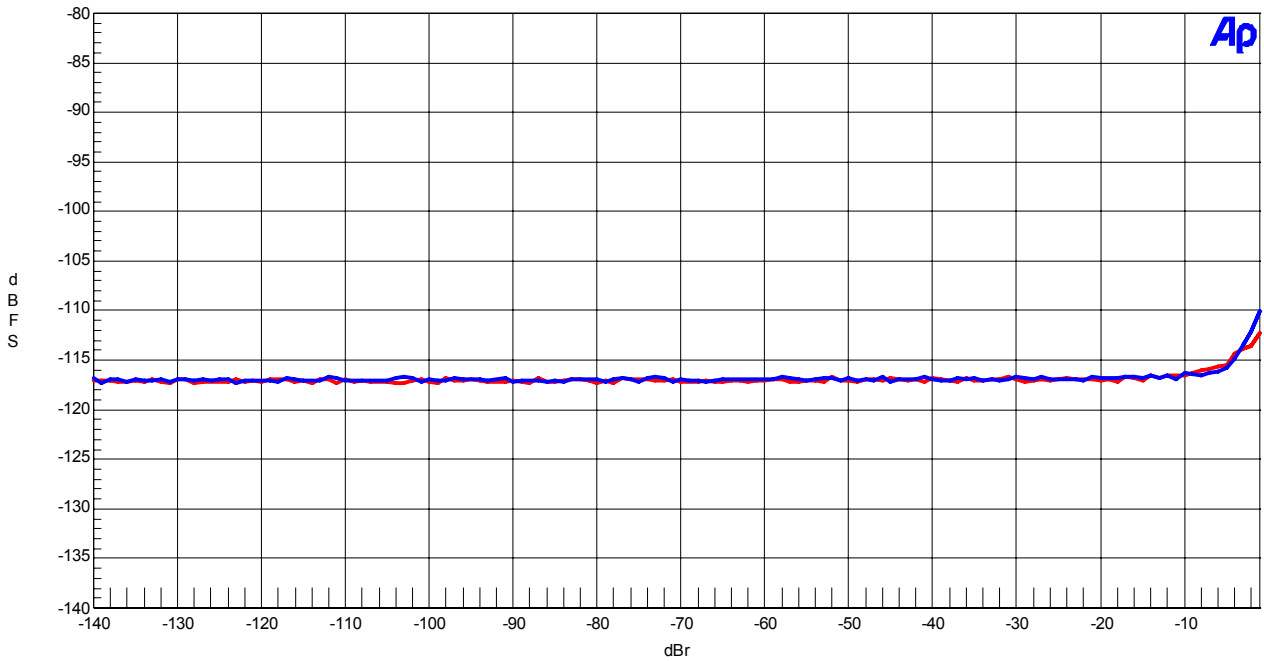
AK5388 S/(N+D) vs. Input Level
AVDD=5V, DVDD=3.3V, MCLK=512fs, fs=48kHz, fin=1kHz

Figure 3. S/(N+D) vs. Input Level

AKM

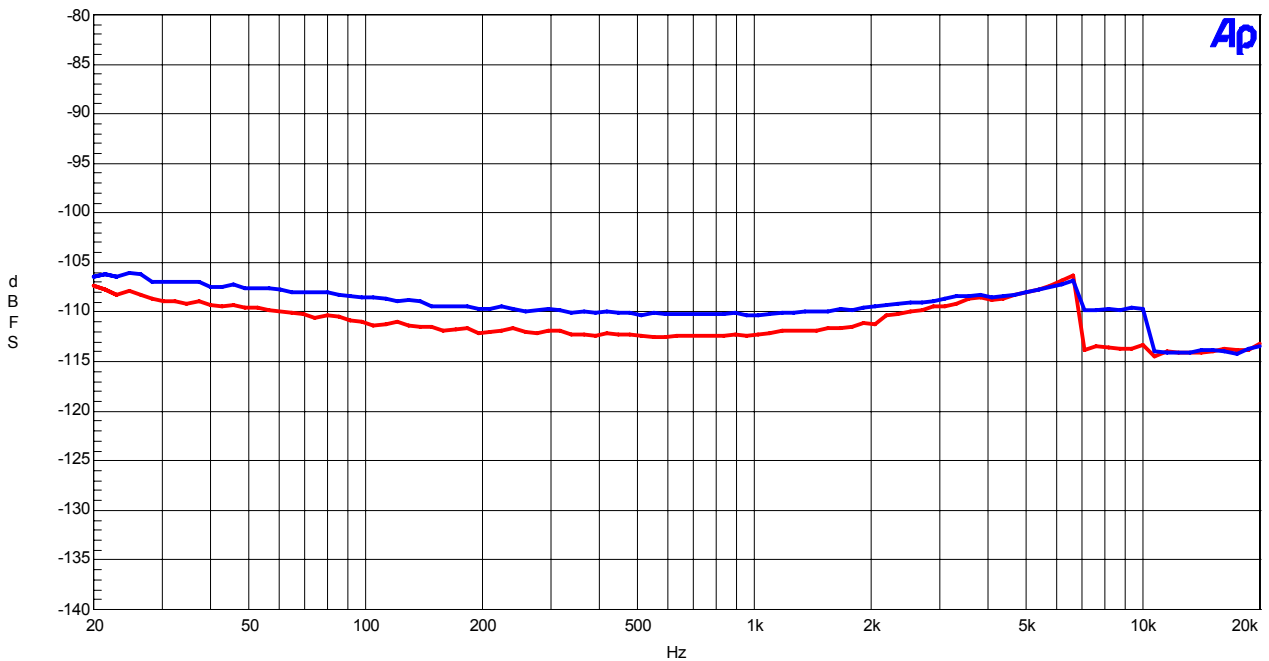
AK5388 S/(N+D) vs. Input Frequency
AVDD=5V, DVDD=3.3V, MCLK=512fs, fs=48kHz, -1dBFS Input

Figure 4. S/(N+D) vs. Input Frequency

AKM

AK5388 Linearity
 AVDD=5V, DVDD=3.3V, MCLK=512fs, fs=48kHz, fin=1kHz

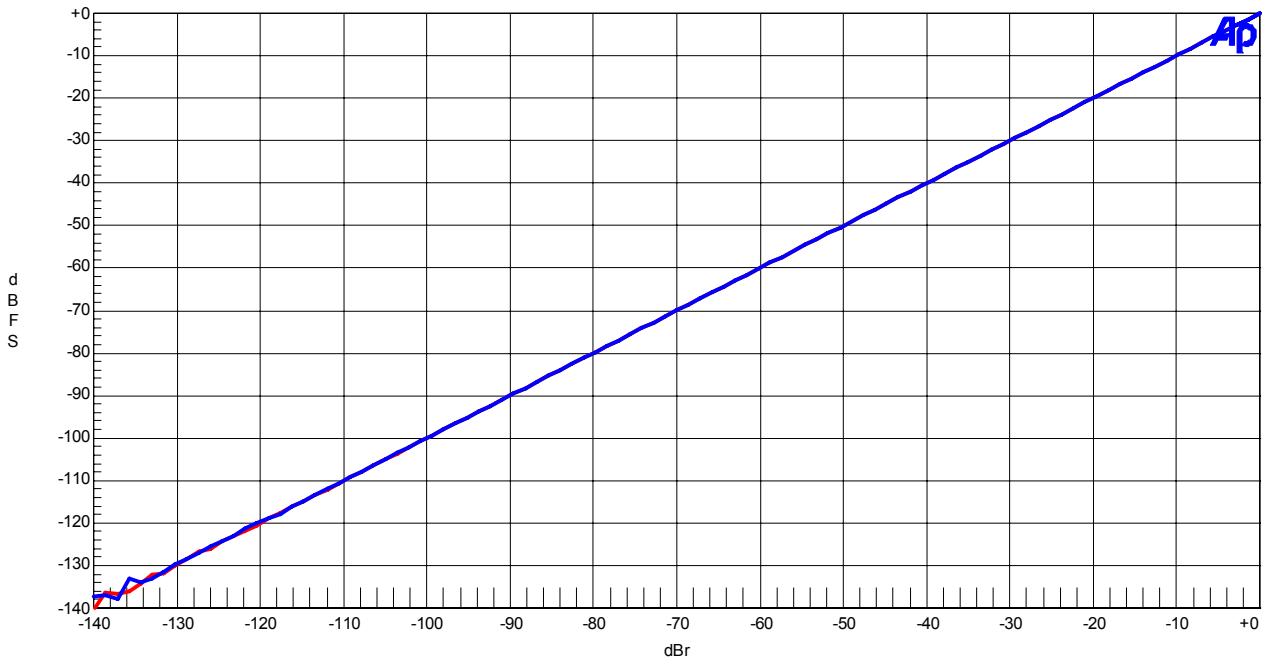


Figure 5. Linearity

AKM

AK5388 Frequency Response
 AVDD=5V, DVDD=3.3V, MCLK=512fs, fs=48kHz, -1dBFS Input

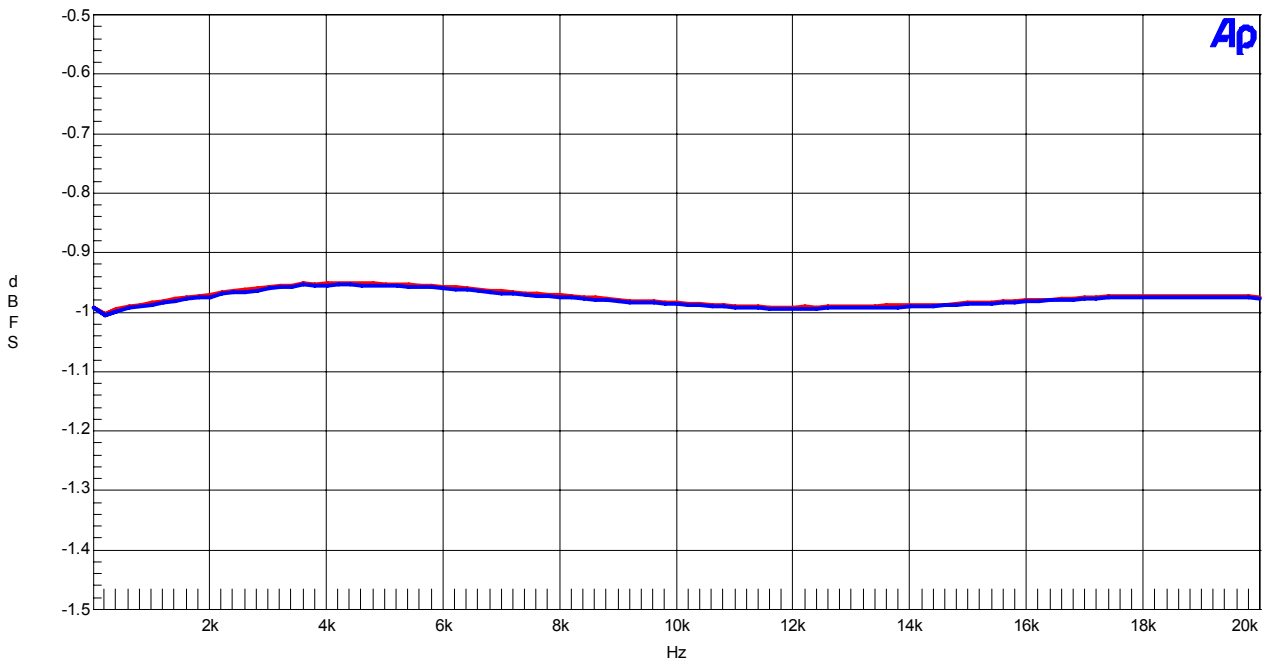


Figure 6. Frequency Response

AKM

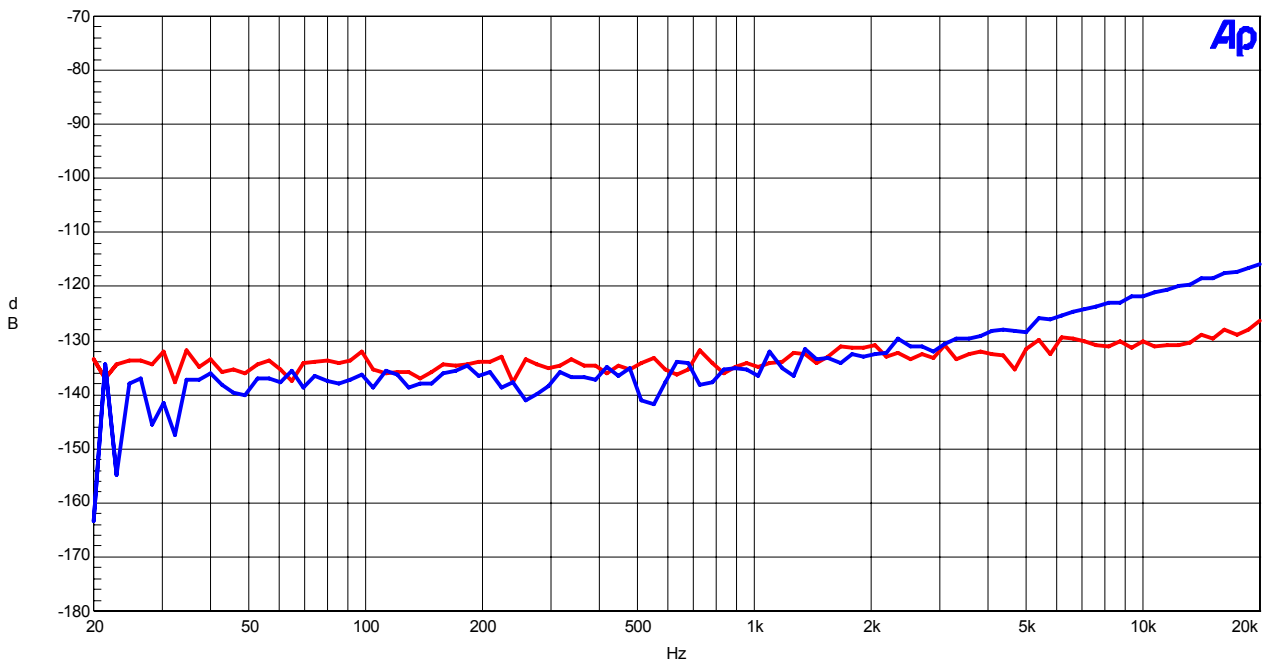
AK5388 Crosstalk (Red=Lch, Blue=Rch)
AVDD=5V, DVDD=3.3V, MCLK=512fs, fs=48kHz, -1dBFS Input

Figure 7. Crosstalk

AKM

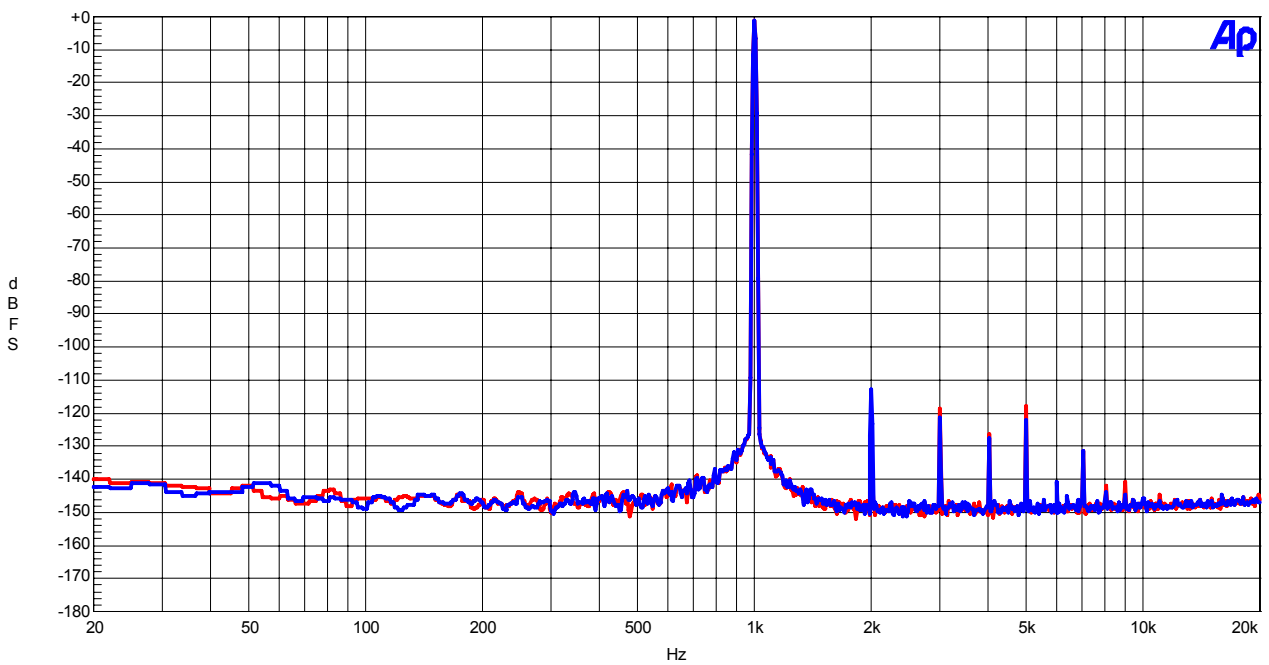
AK5388 FFT
AVDD=5V, DVDD=3.3V, MCLK=512fs, fs=48kHz, -1dBFS Input

Figure 8. FFT Plot

AKM

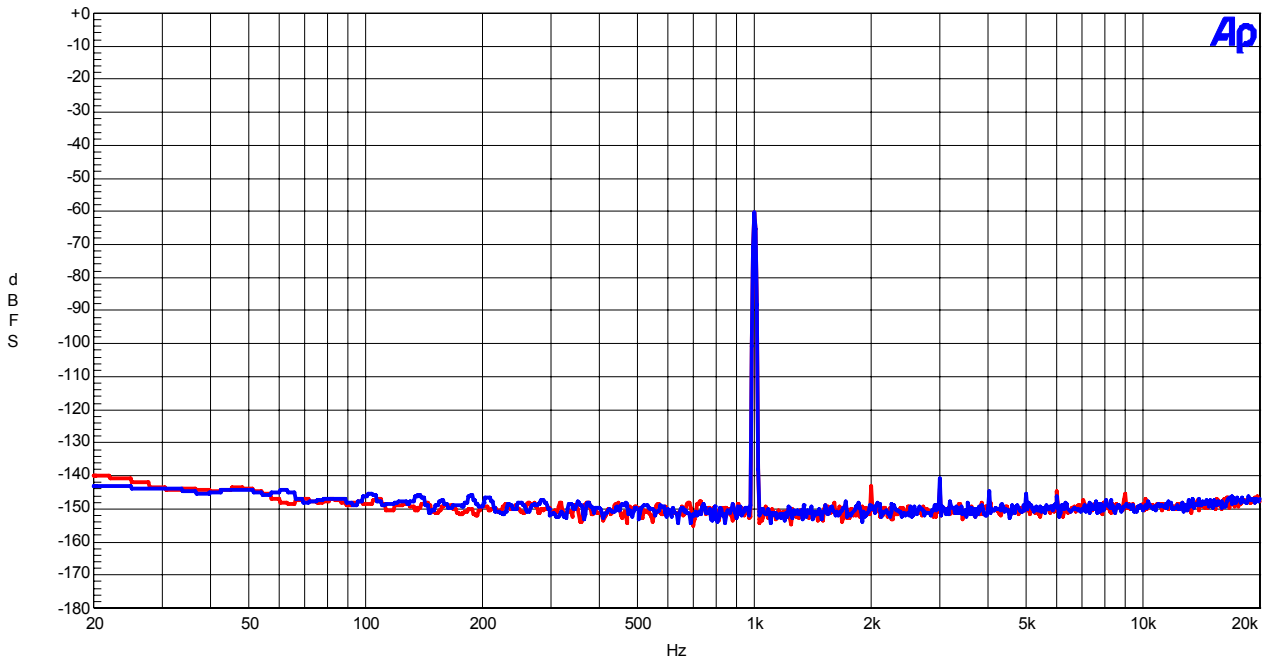
AK5388 FFT
AVDD=5V, DVDD=3.3V, MCLK=512fs, fs=48kHz, -60dBFS Input

Figure 9. FFT Plot

AKM

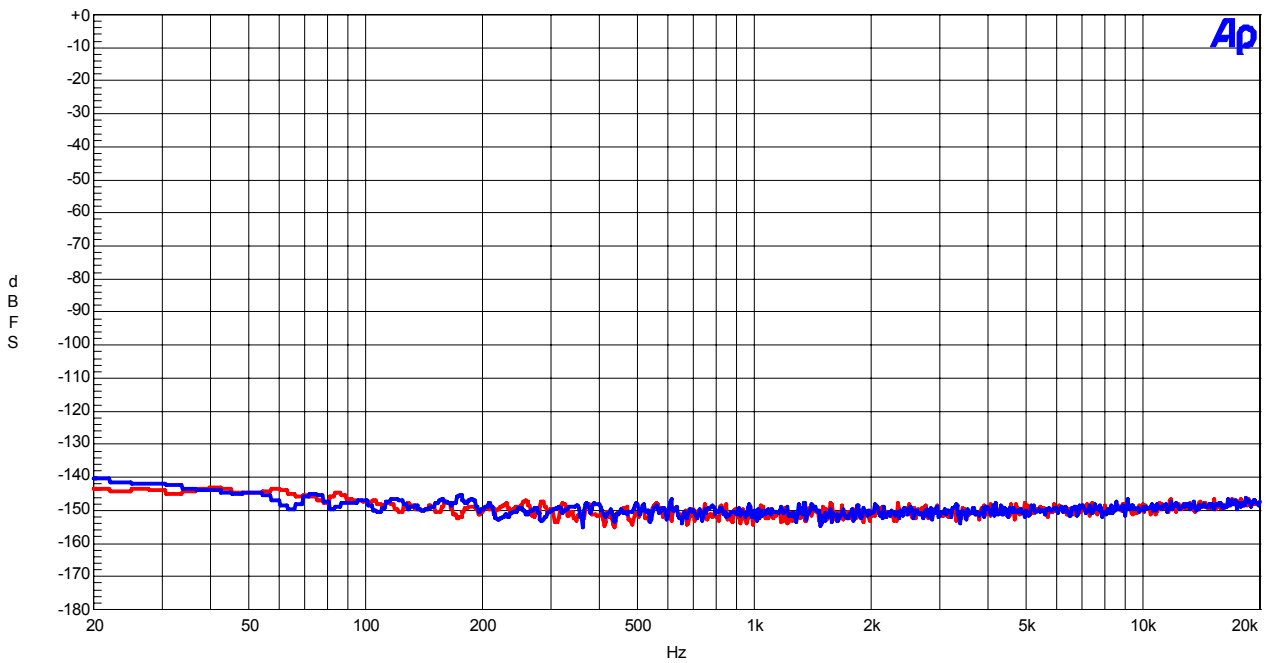
AK5388 FFT
AVDD=5V, DVDD=3.3V, MCLK=512fs, fs=48kHz, No Signal Input

Figure 10. FFT Plot

[ADC Plot: fs=96kHz]

AKM

AK5388 S/(N+D) vs. Input Level
 AVDD=5V, DVDD=3.3V, MCLK=256fs, fs=96kHz, fin=1kHz

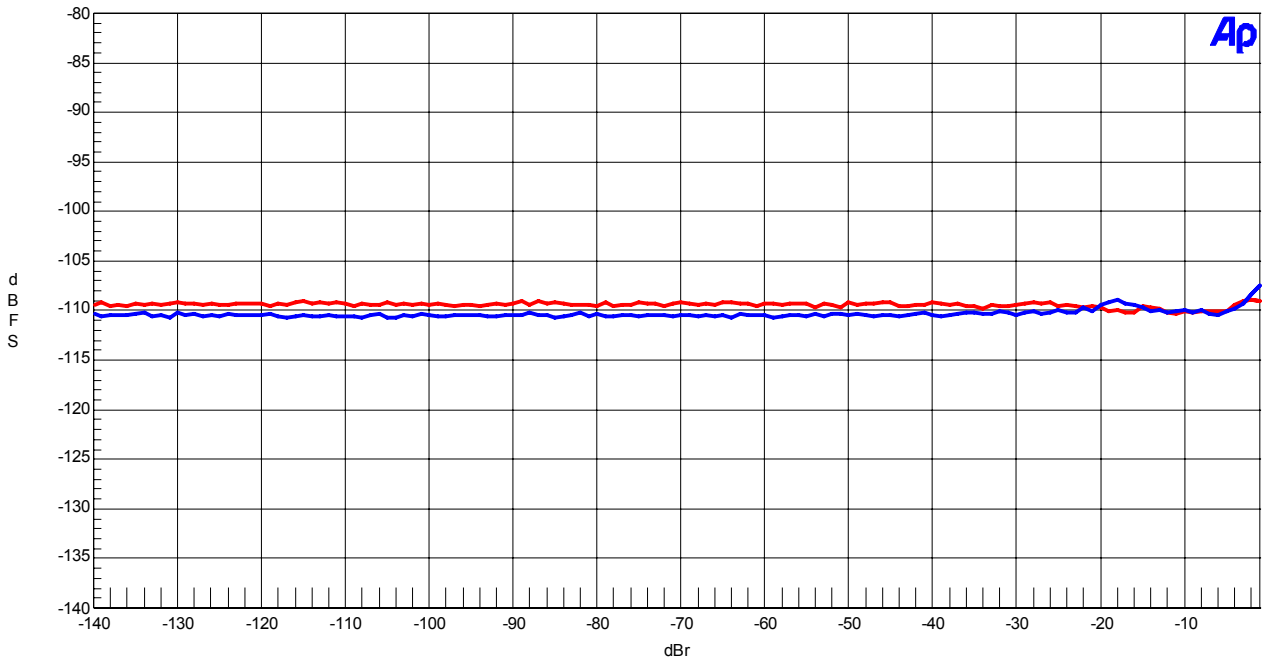


Figure 11. S/(N+D) vs. Input Level

AKM

AK5388 S/(N+D) vs. Input Frequency
 AVDD=5V, DVDD=3.3V, MCLK=256fs, fs=96kHz, -1dBFS Input

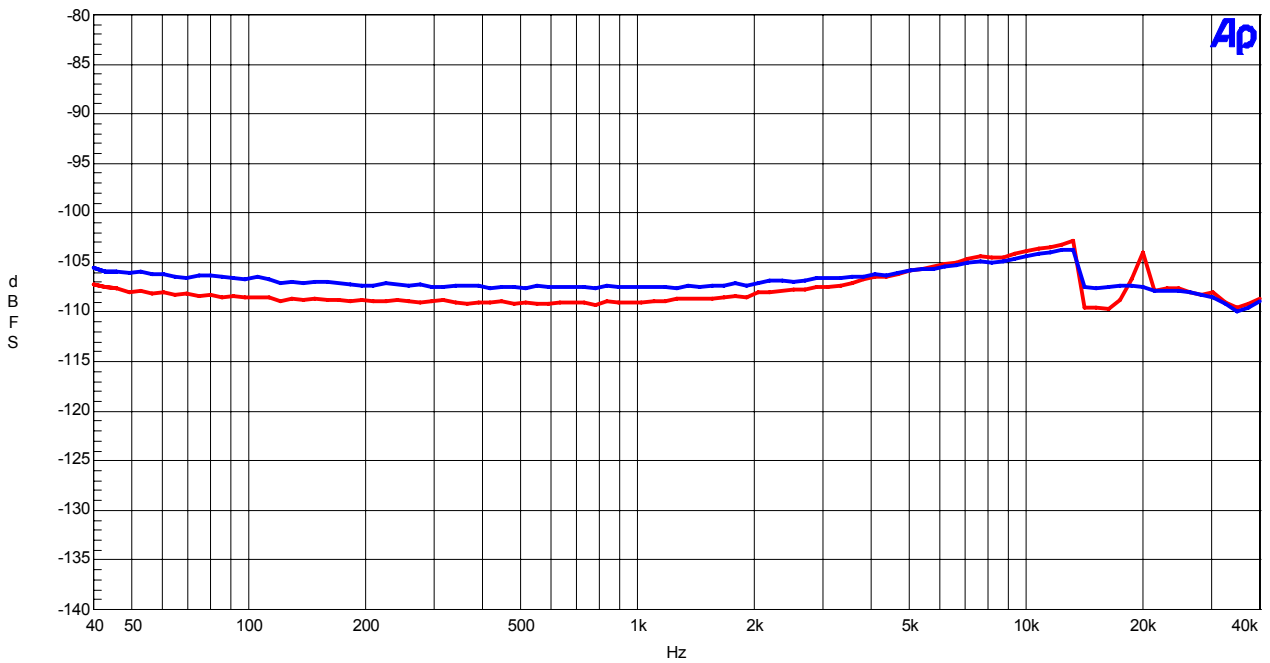


Figure 12. S/(N+D) vs. Input Frequency

AKM

AK5388 Linearity
 AVDD=5V, DVDD=3.3V, MCLK=256fs, fs=96kHz, fin=1kHz

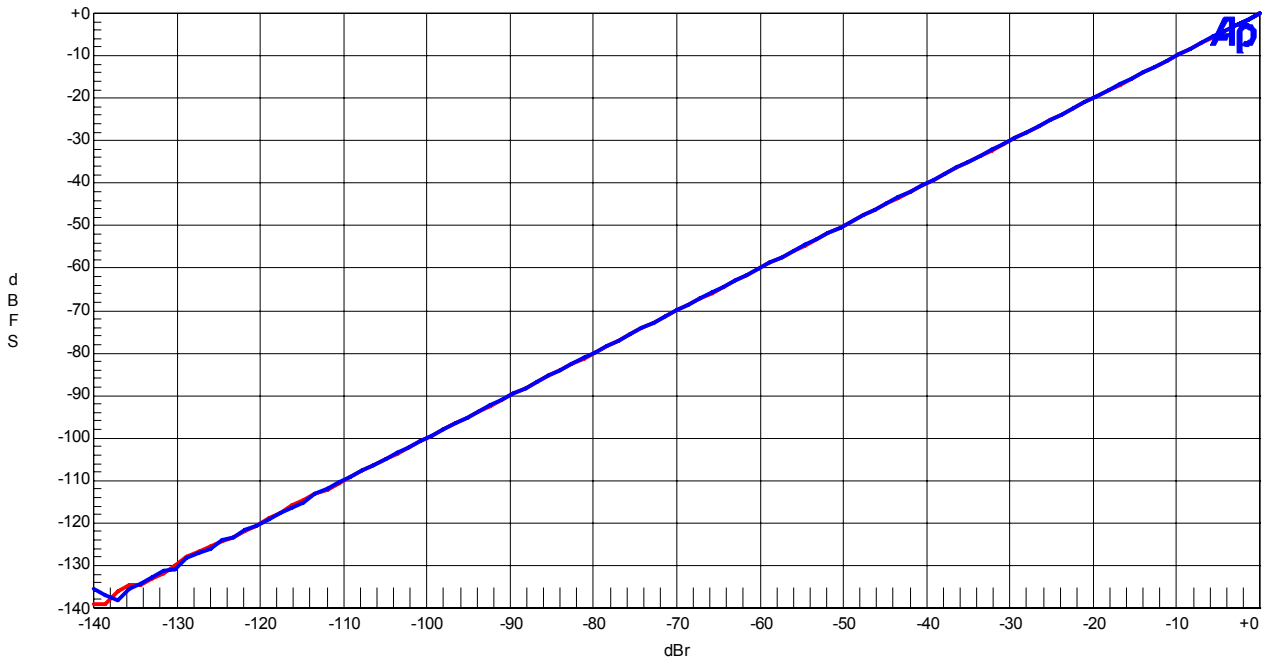


Figure 13. Linearity

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AK5388 Frequency Response
 AVDD=5V, DVDD=3.3V, MCLK=256fs, fs=96kHz, -1dBFS Input

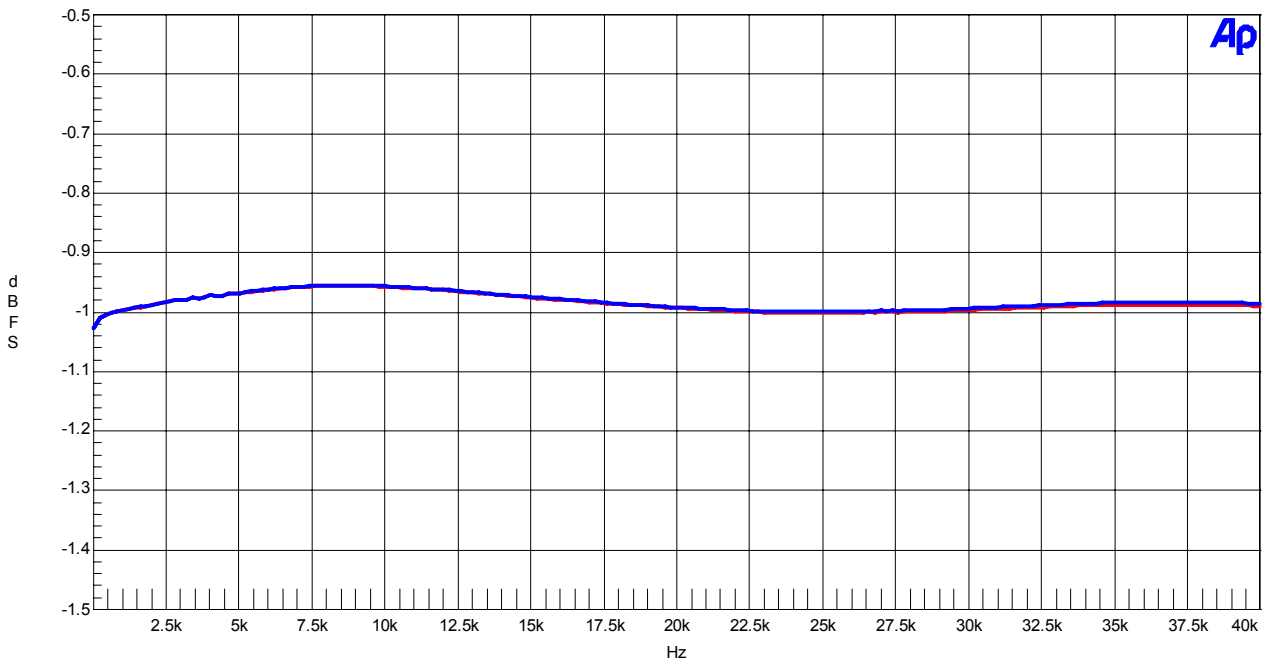


Figure 14. Frequency Response

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AK5388 Crosstalk (Red=Lch, Blue=Rch)
 AVDD=5V, DVDD=3.3V, MCLK=256fs, fs=96kHz, -1dBFS Input

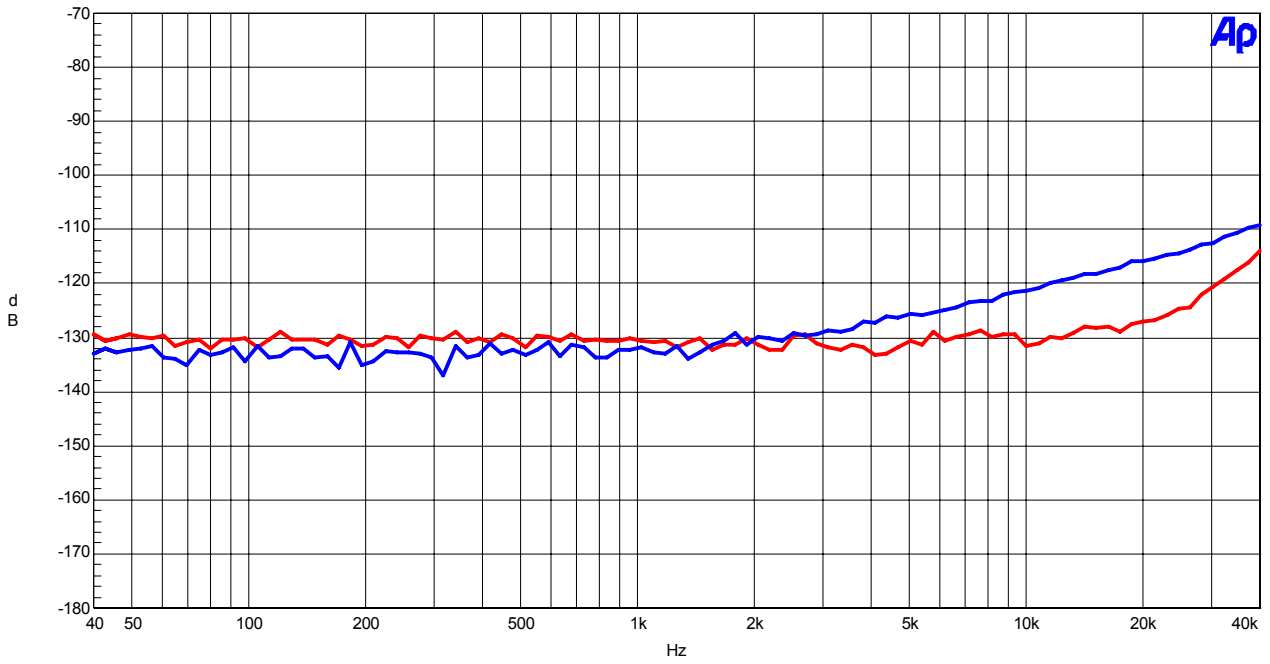


Figure 15. Crosstalk

AKM

AK5388 FFT
 AVDD=5V, DVDD=3.3V, MCLK=256fs, fs=96kHz, -1dBFS Input

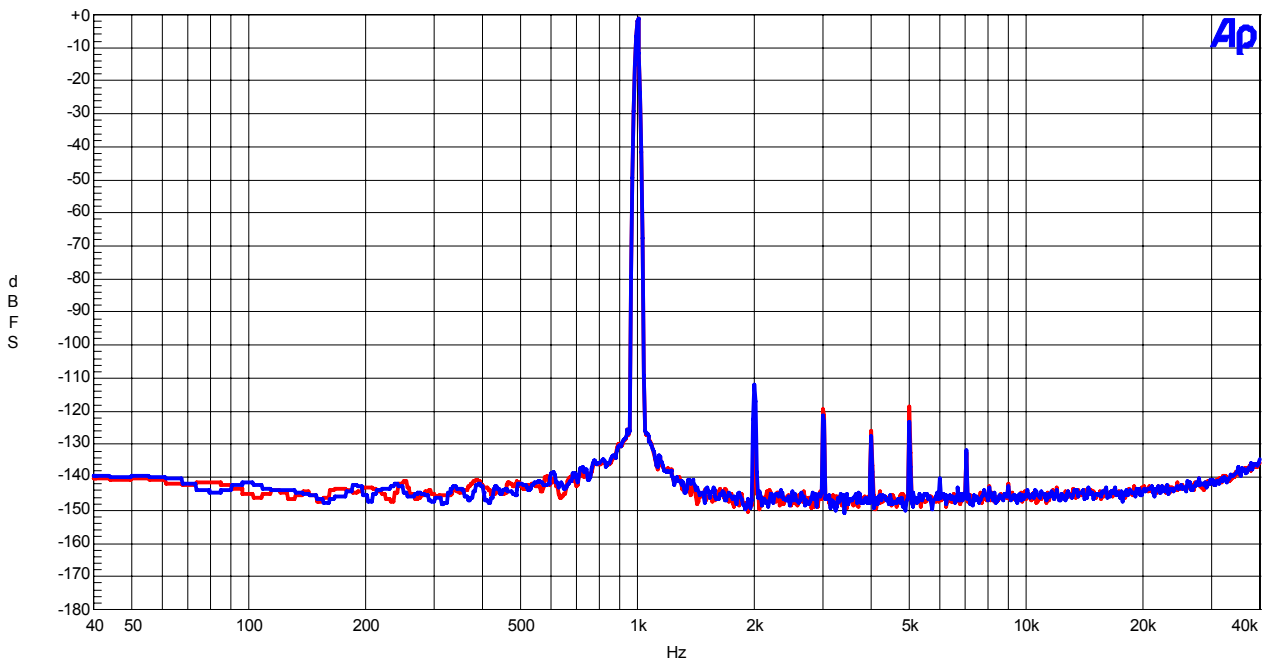


Figure 16. FFT Plot

AKM

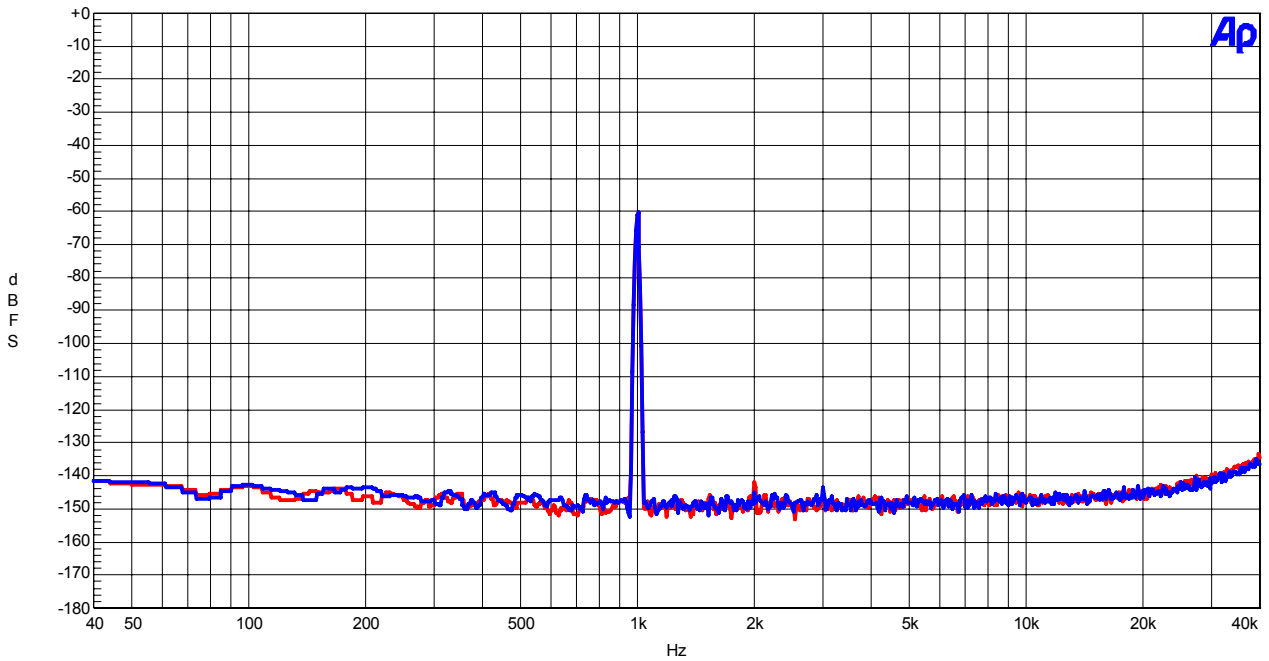
AK5388 FFT
AVDD=5V, DVDD=3.3V, MCLK=256fs, fs=96kHz, -60dBFS Input

Figure 17. FFT Plot

AKM

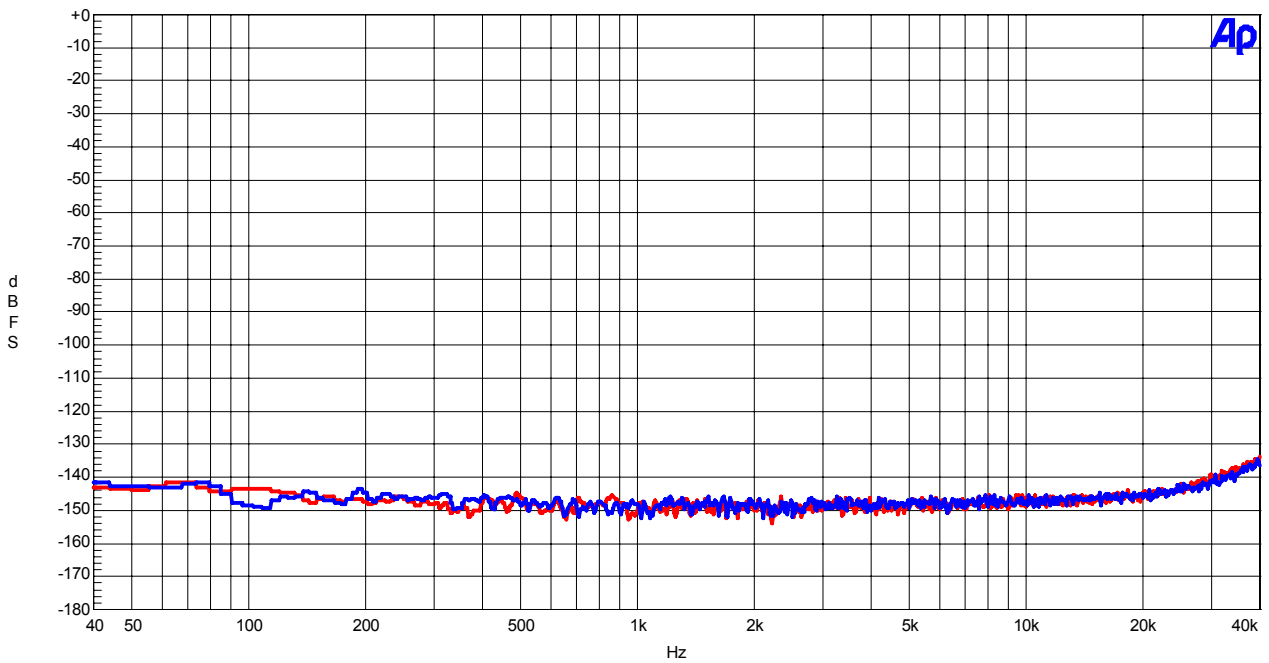
AK5388 FFT
AVDD=5V, DVDD=3.3V, MCLK=256fs, fs=96kHz, No Signal Input

Figure 18. FFT Plot

[ADC Plot: fs=192kHz]

AKM

AK5388 S/(N+D) vs. Input Level
 AVDD=5V, DVDD=3.3V, MCLK=128fs, fs=192kHz, fin=1kHz

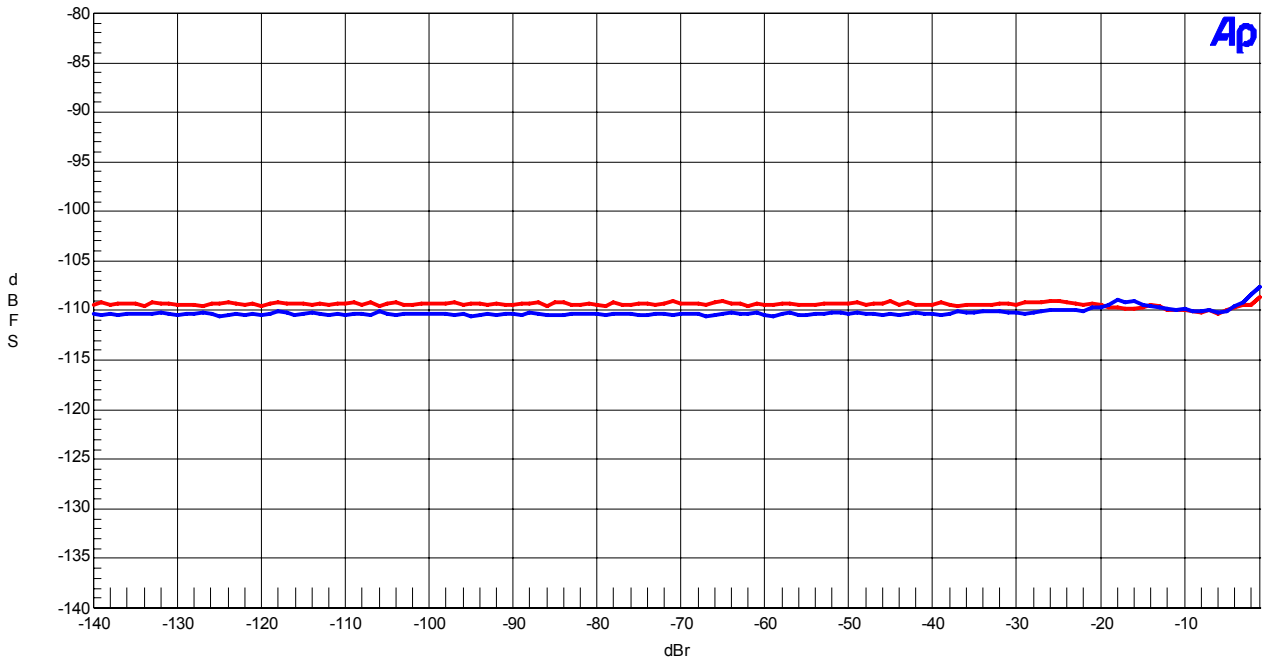


Figure 19. S/(N+D) vs. Input Level

AKM

AK5388 S/(N+D) vs. Input Frequency
 AVDD=5V, DVDD=3.3V, MCLK=128fs, fs=192kHz, -1dBFS Input

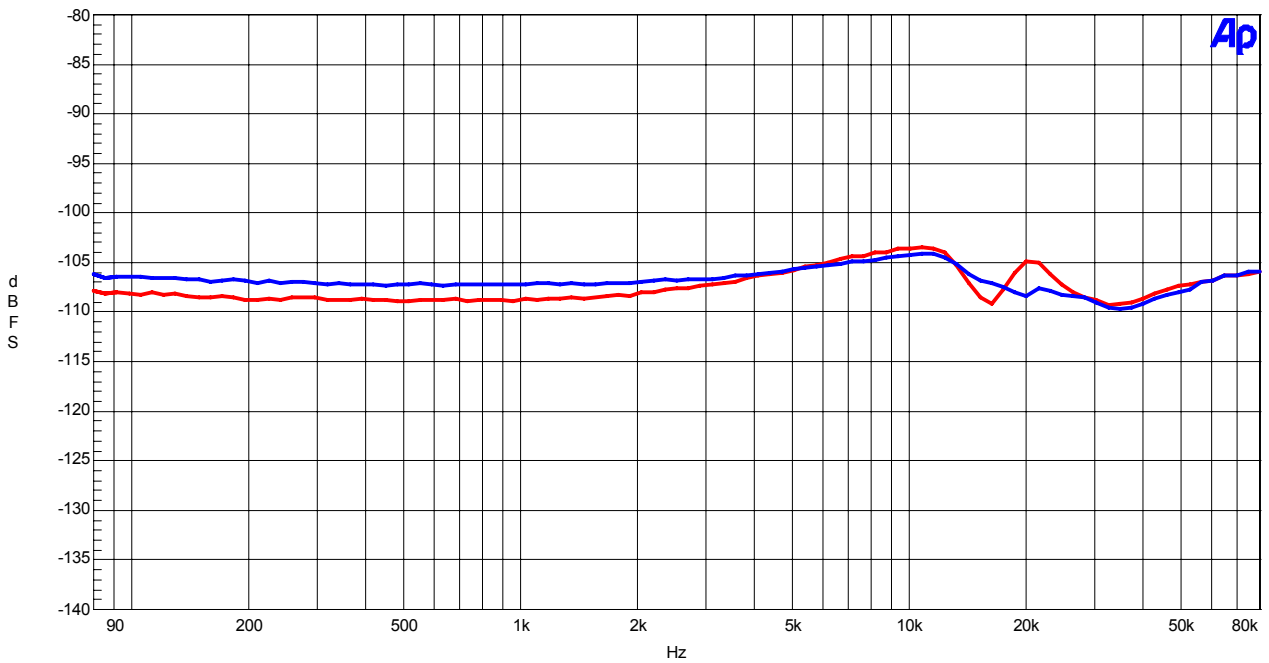


Figure 20. S/(N+D) vs. Input Frequency

AKM

AK5388 Linearity
 AVDD=5V, DVDD=3.3V, MCLK=128fs, fs=192kHz, fin=1kHz

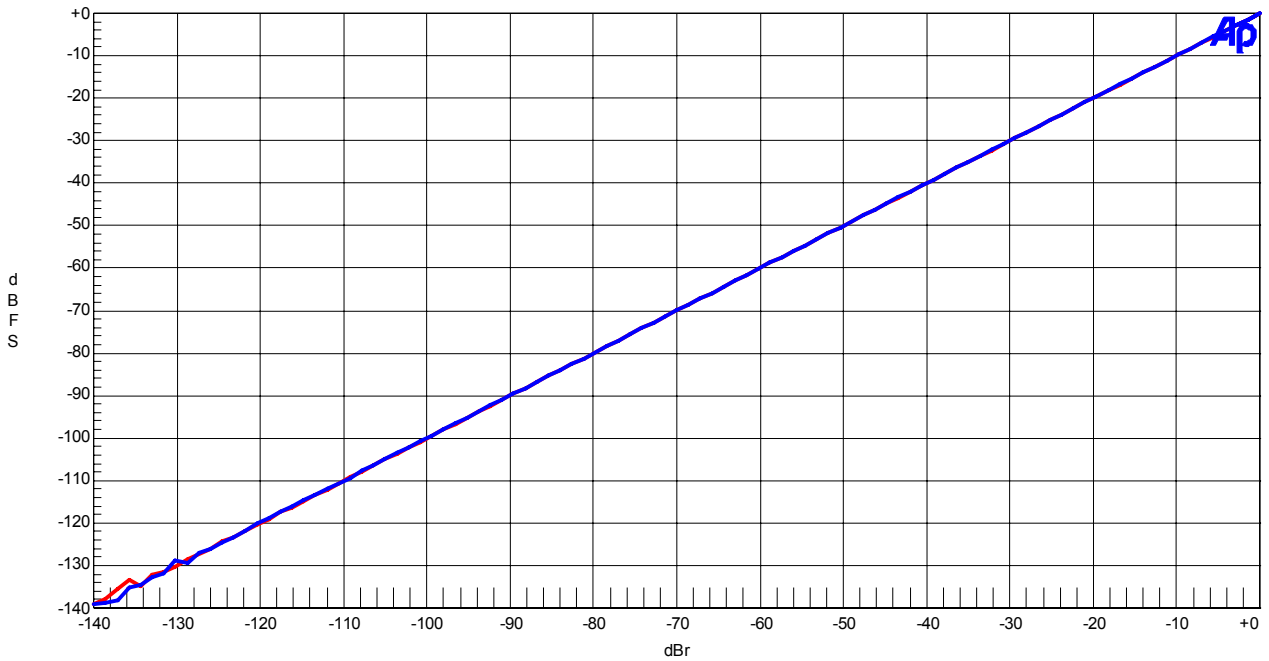


Figure 21. Linearity

AKM

AK5388 Frequency Response
 AVDD=5V, DVDD=3.3V, MCLK=128fs, fs=192kHz, -1dBFS Input

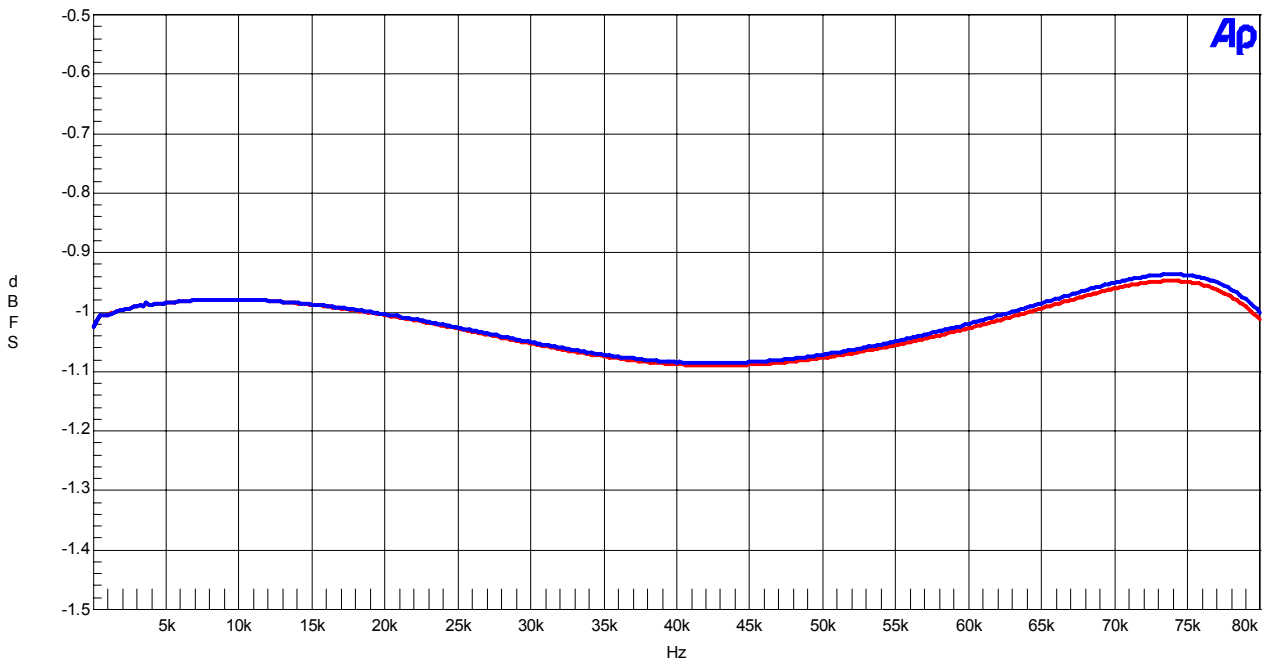


Figure 22. Frequency Response

AKM

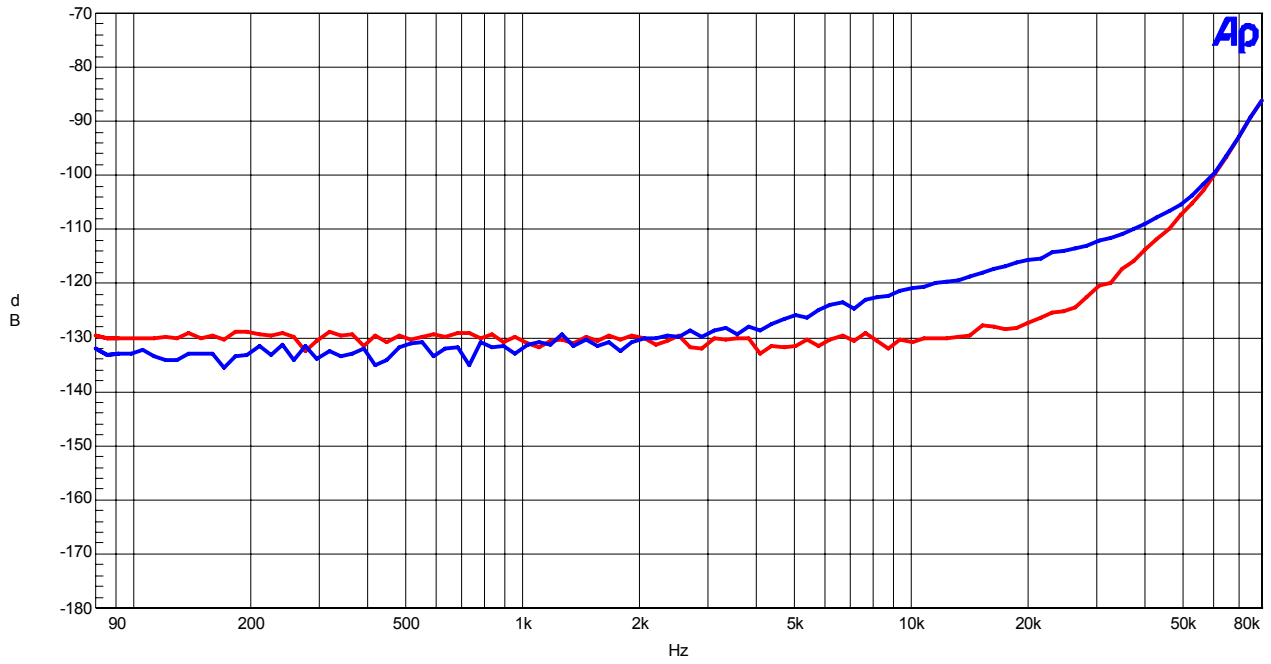
AK5388 Crosstalk (Red=Lch, Blue=Rch)
AVDD=5V, DVDD=3.3V, MCLK=128fs, fs=192kHz, -1dBFS Input

Figure 23. Crosstalk

AKM

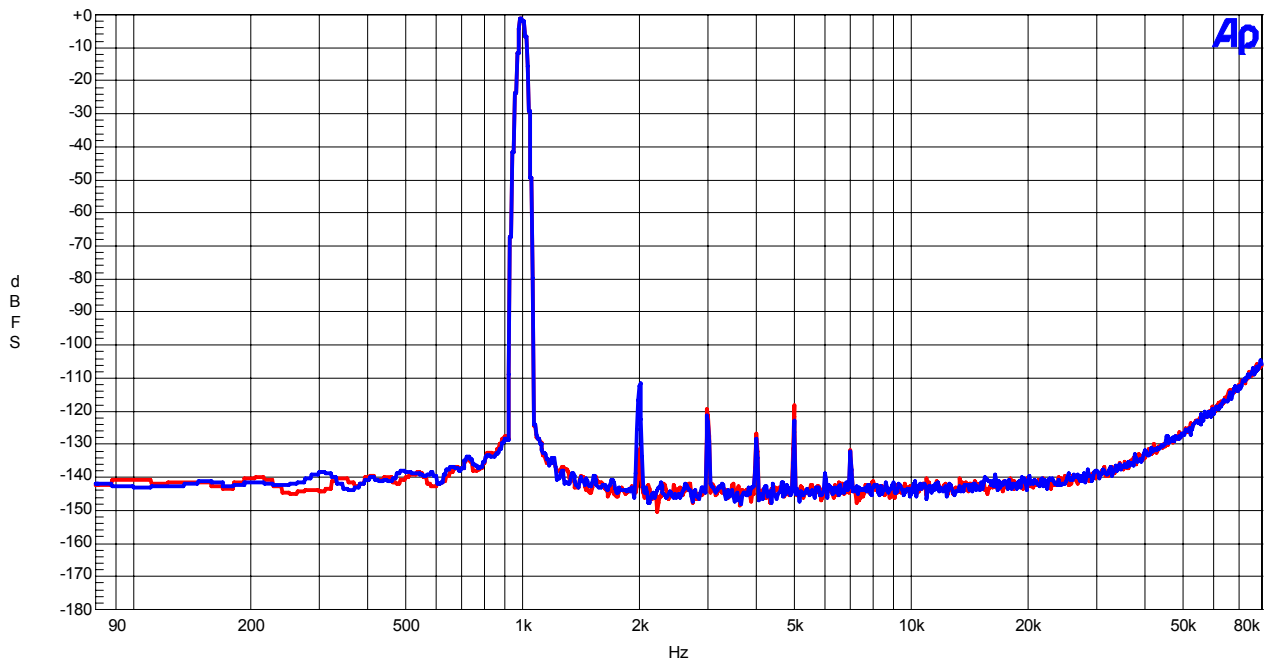
AK5388 FFT
AVDD=5V, DVDD=3.3V, MCLK=128fs, fs=192kHz, -1dBFS Input

Figure 24. FFT Plot

AKM

AK5388 FFT
 AVDD=5V, DVDD=3.3V, MCLK=128fs, fs=192kHz, -60dBFS Input

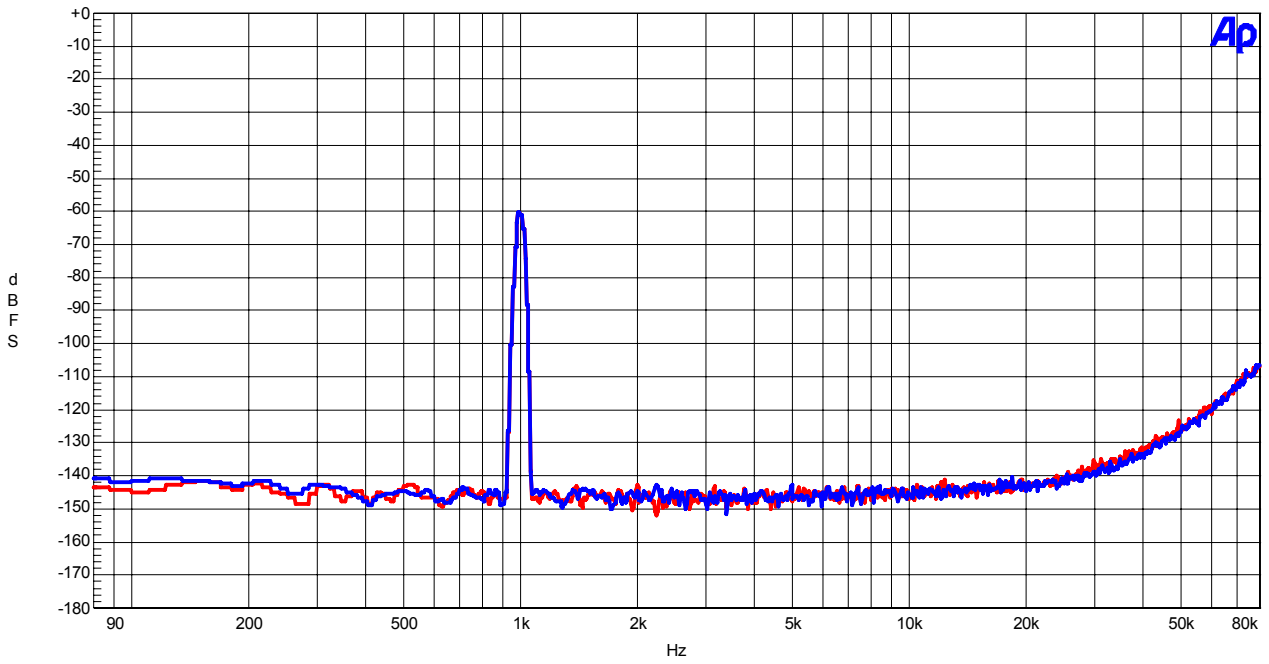


Figure 25. FFT Plot

AKM

AK5388 FFT
 AVDD=5V, DVDD=3.3V, MCLK=128fs, fs=192kHz, No Signal Input

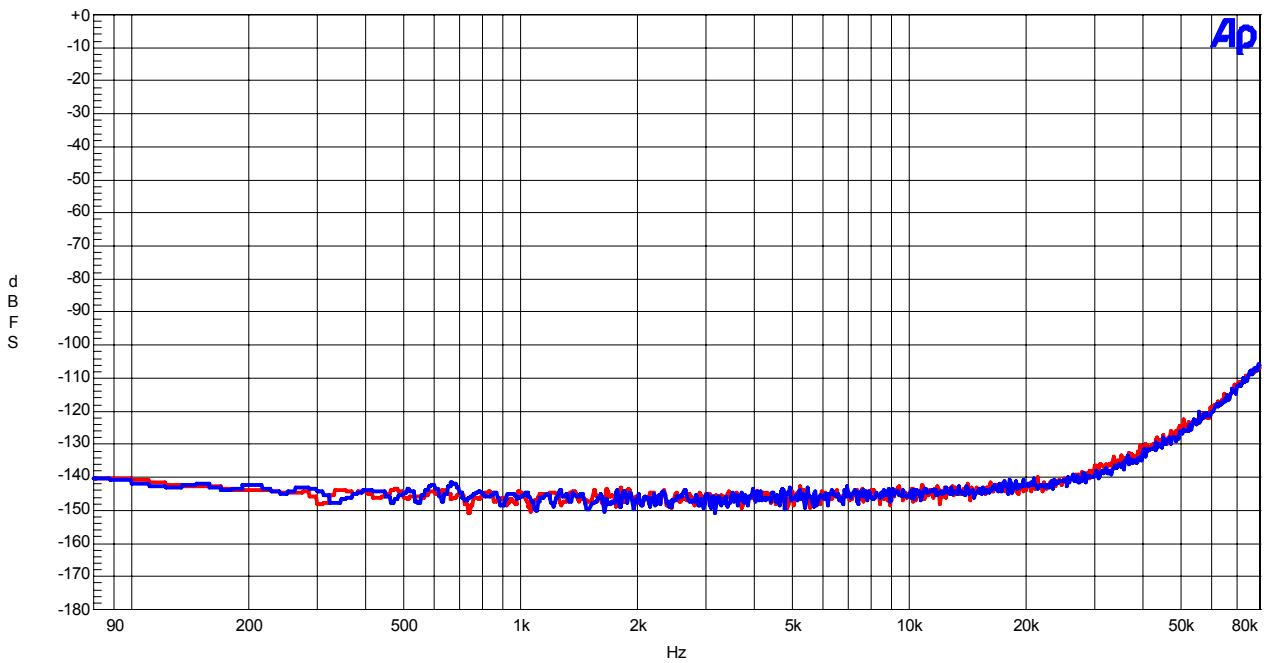


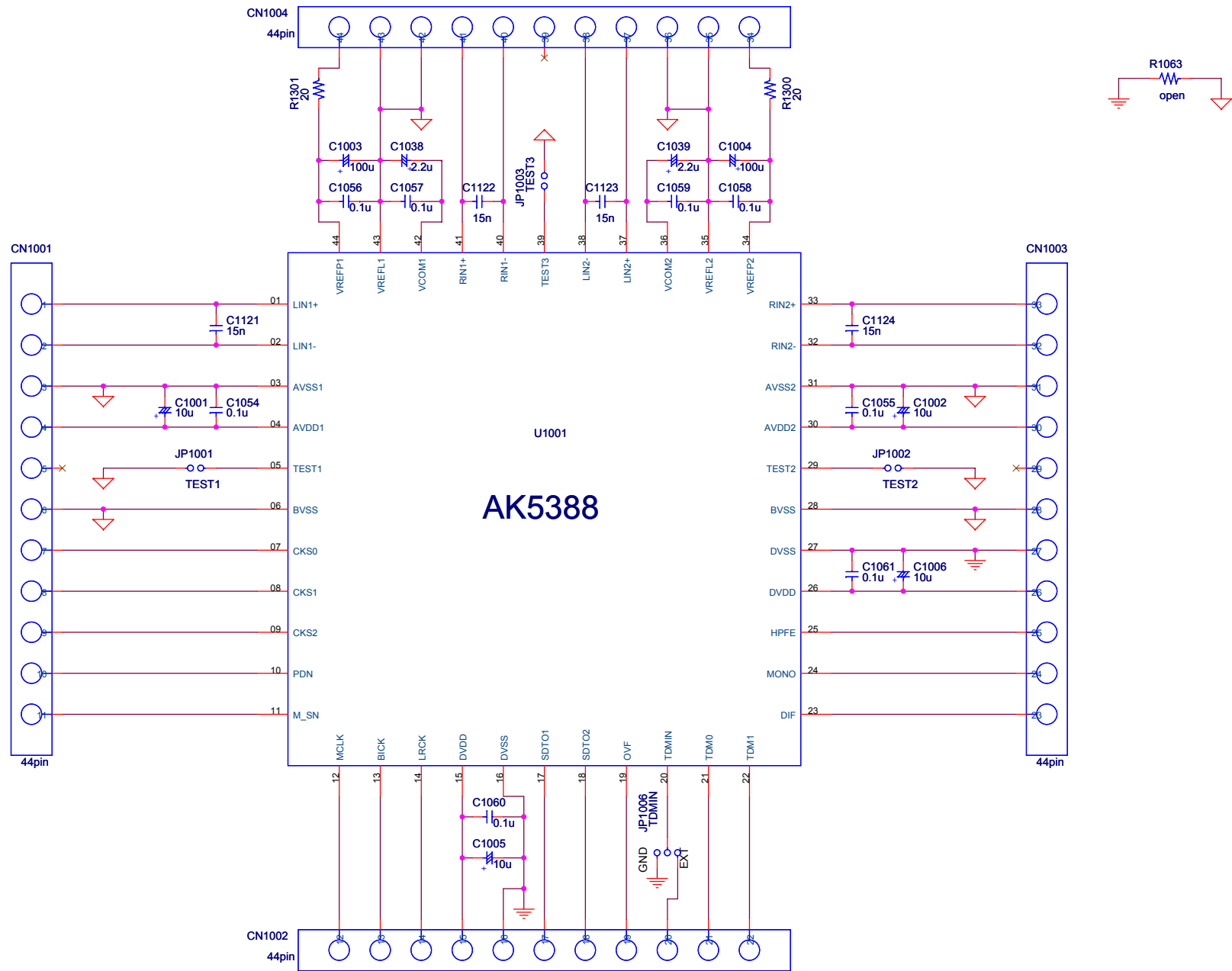
Figure 26. FFT Plot

Revision History

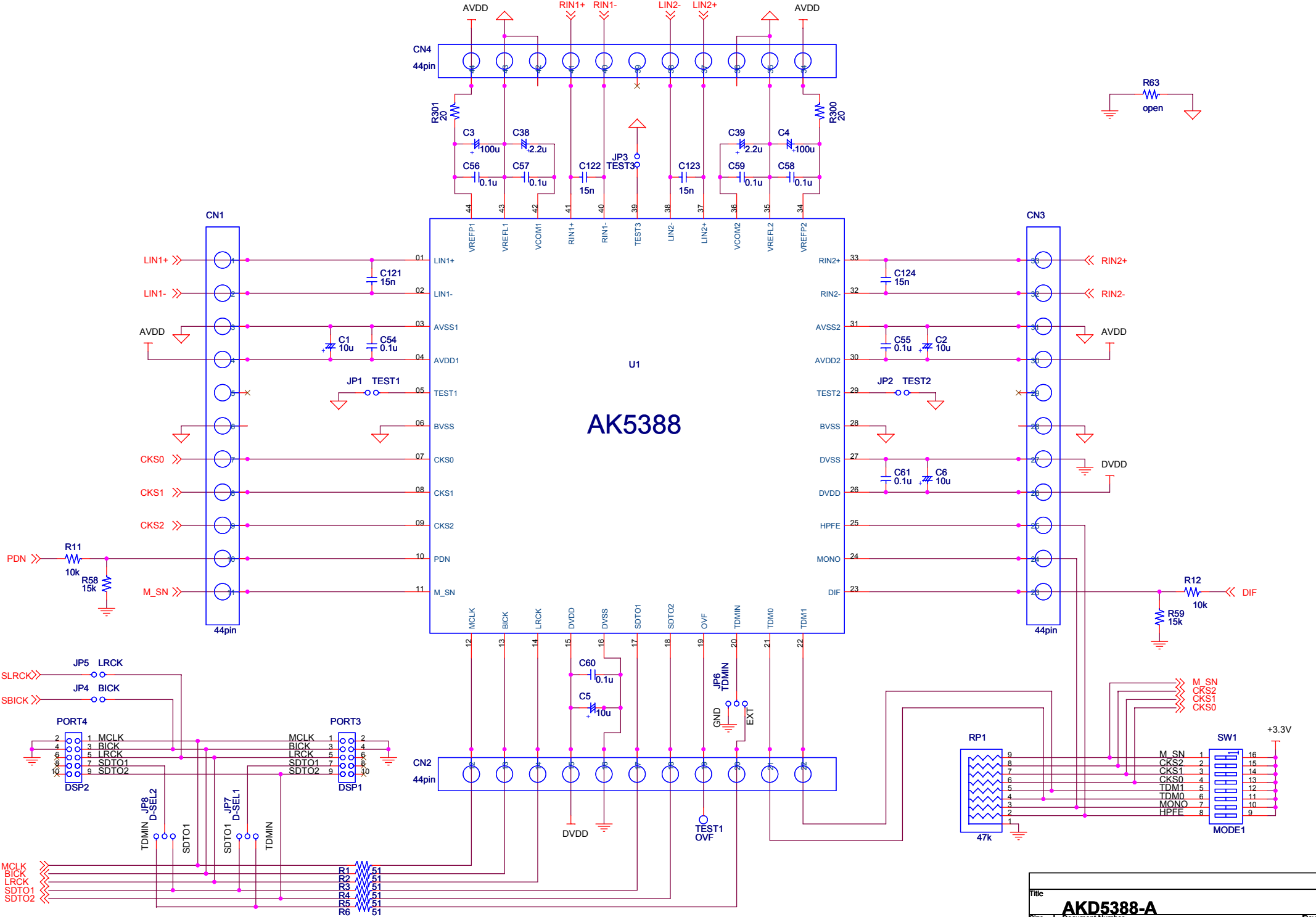
Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
07/06/27	KM090200	0	First Edition		
08/02/12	KM090201	1	Change		Device revision was changed. Rev. A -> Rev. C
			Change	8	Circuit diagram was changed. R: 91ohm -> 10ohm, OP-amp: LME49710-> NJM5534D PORT1, PORT2: TOTX197-> TOTX176
			Modification	9-21	Update of measurement results
08/07/07	KM090202	2	Change		Device revision was changed. Rev. C -> Rev. D
			Modification	9-21	Update of measurement results
08/11/04	KM090203	3	Change		Device revision was changed. Rev. D -> Rev. E
			Change		Circuit diagram was changed. R300, R301:Add 20ohm, C300, C301:Add 220pF. R1300, R1301:Add 20ohm, C1300, C1301:Add 220pF.
			Modification	9-21	Update of measurement results
09/01/05	KM090204	3	Modification	10,14, 18	Update of Plots. Figure 3, Figure 11, Figure 19
09/03/02	KM090205	4	Modification	9-21	Update of measurement results
			Change		Circuit diagram was changed. C300,C301,C1300,C1301:Deleted C121,C122,C123,C124,C1121,C1122,C1123,C1124 :24.2nF -> 15nF C3,C4,C1003,C1004: 10uF -> 100uF R15,R17,R19,R21: 10kohm -> 11kohm

IMPORTANT NOTICE

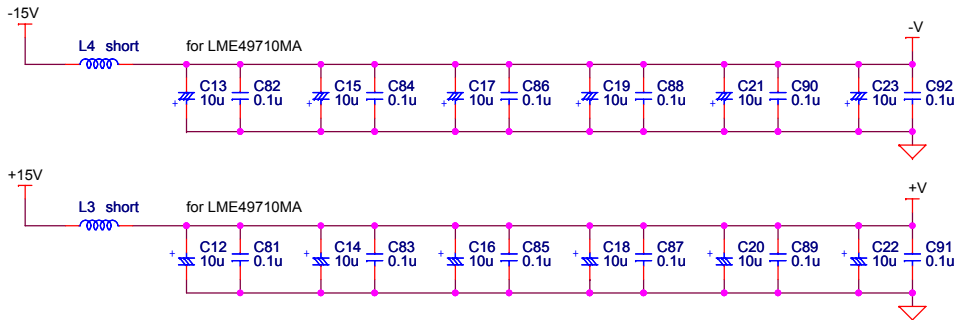
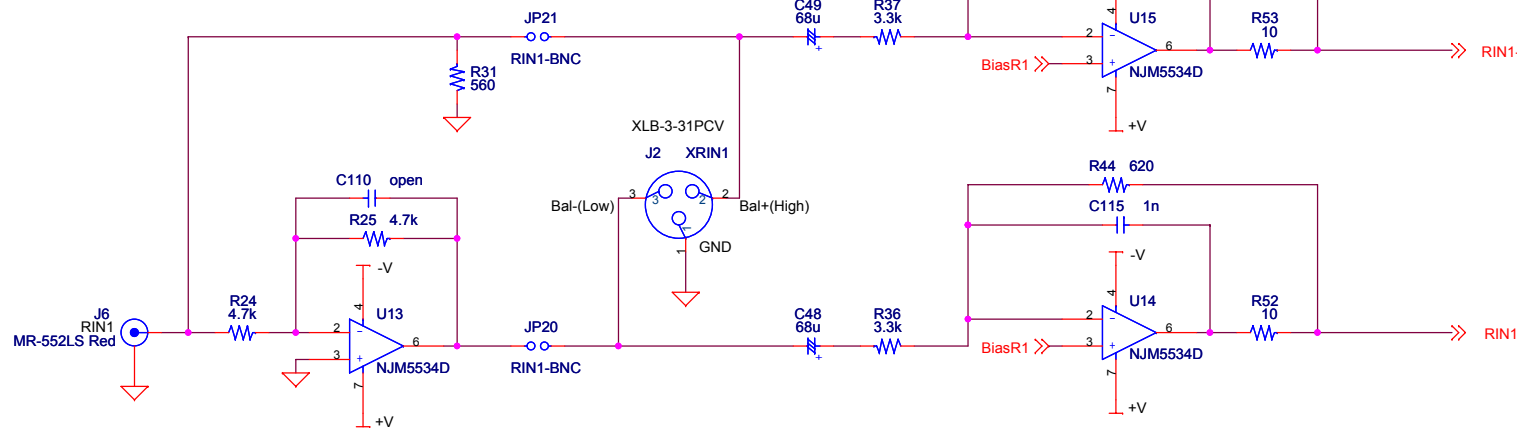
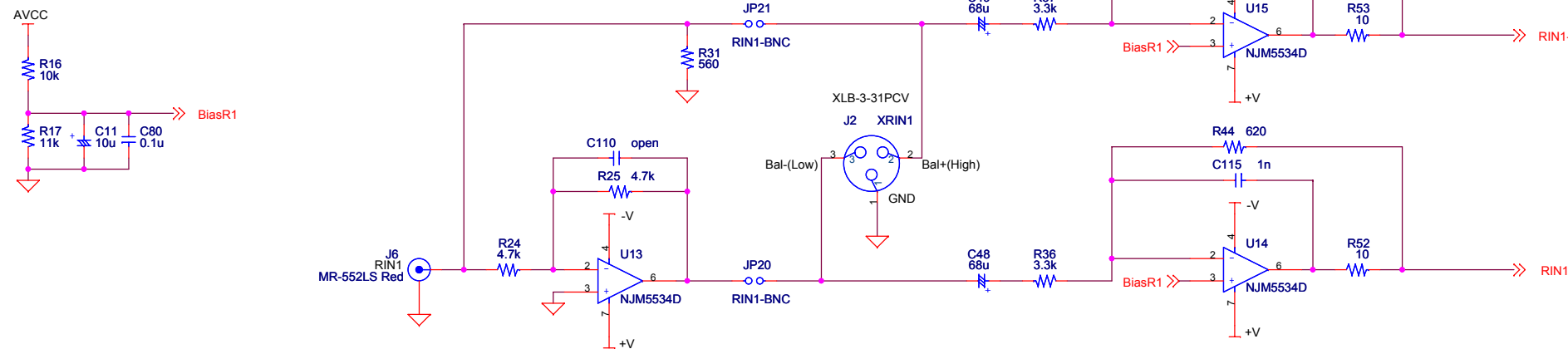
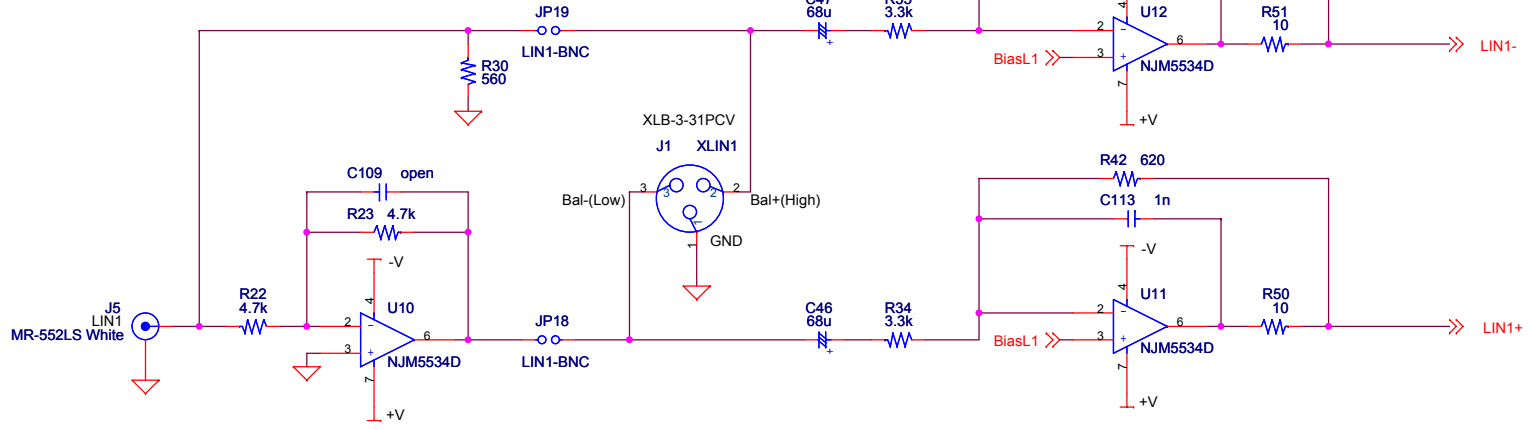
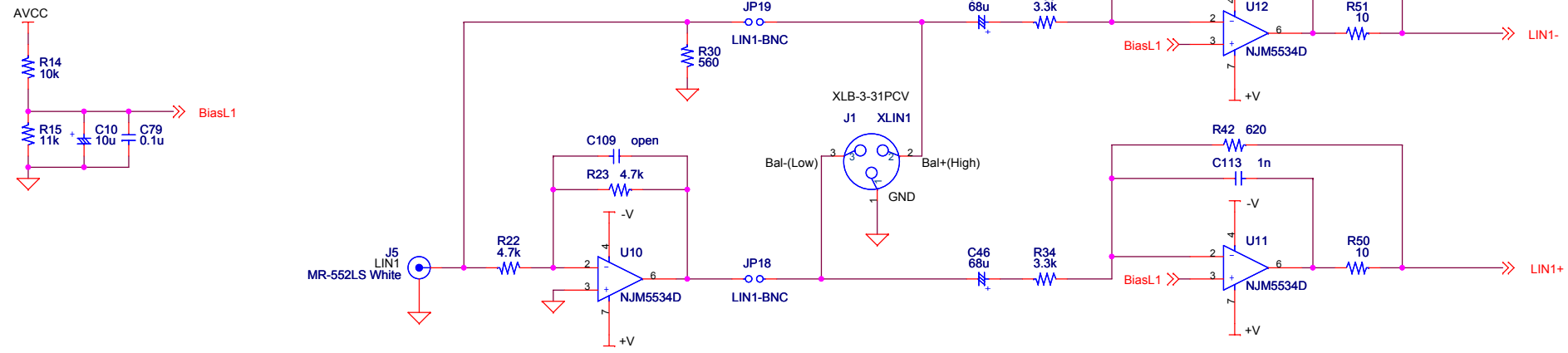
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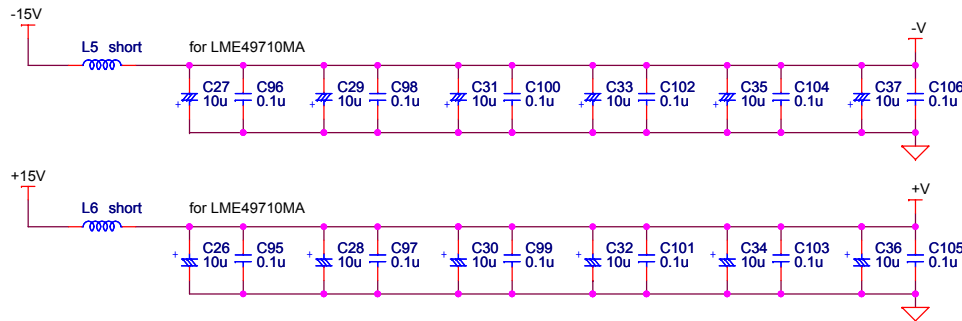
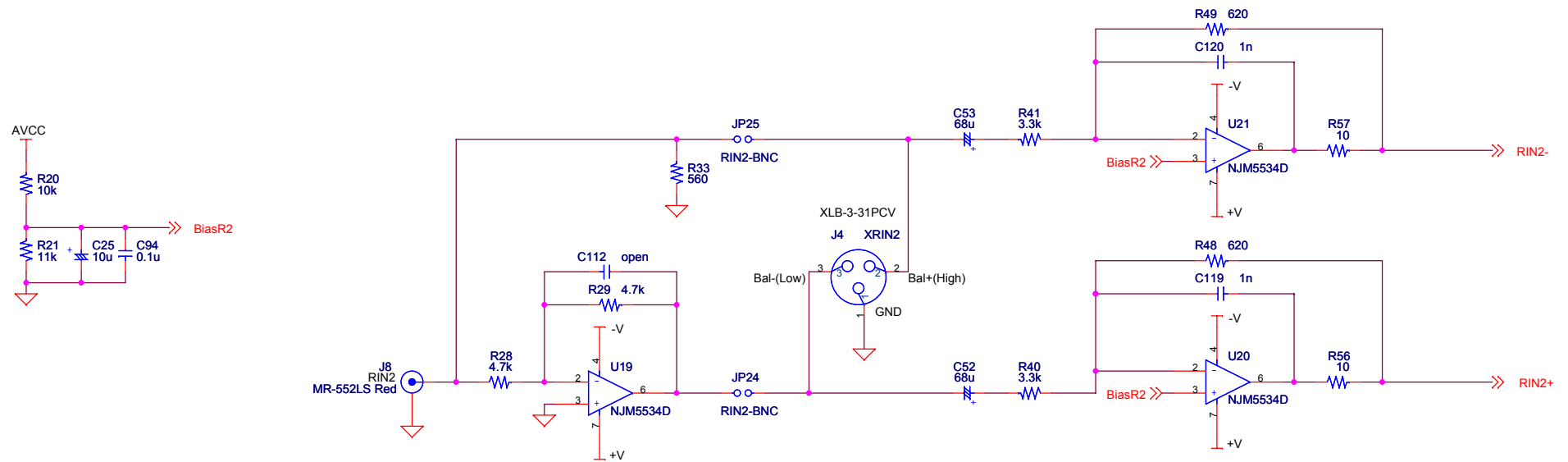
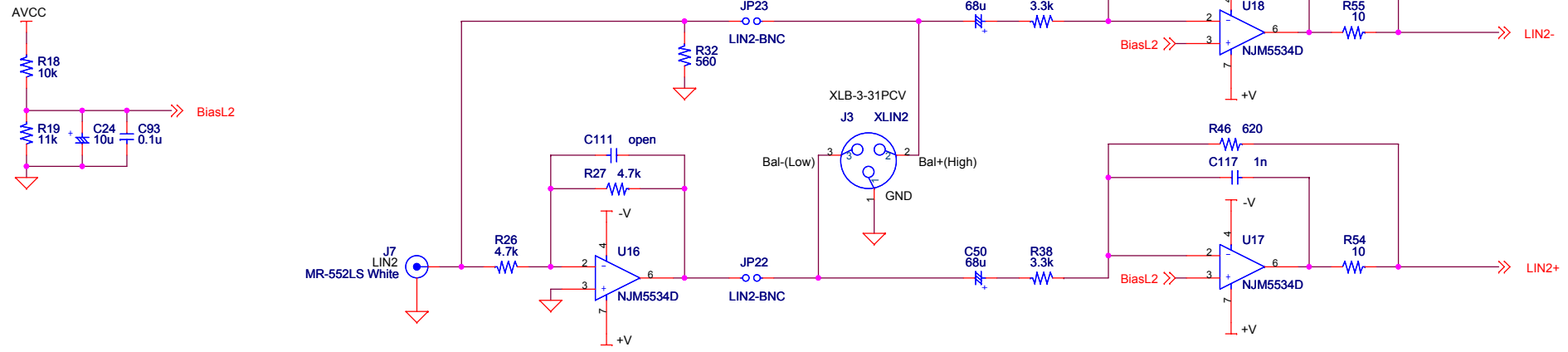
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Size	A3	Document Number	AK5388
Date:	Thursday, February 12, 2009	Sheet	1 of 1
		Rev	4



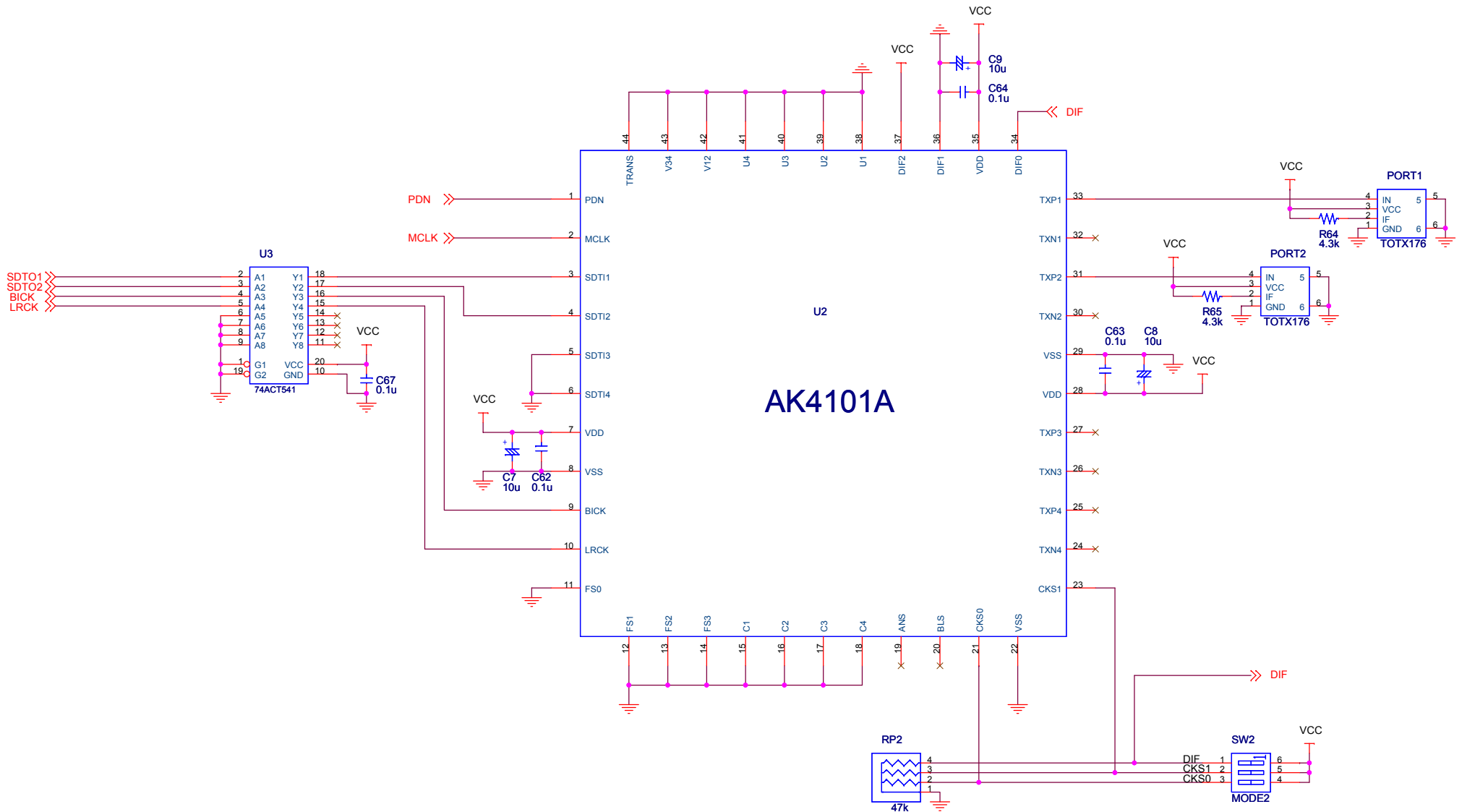
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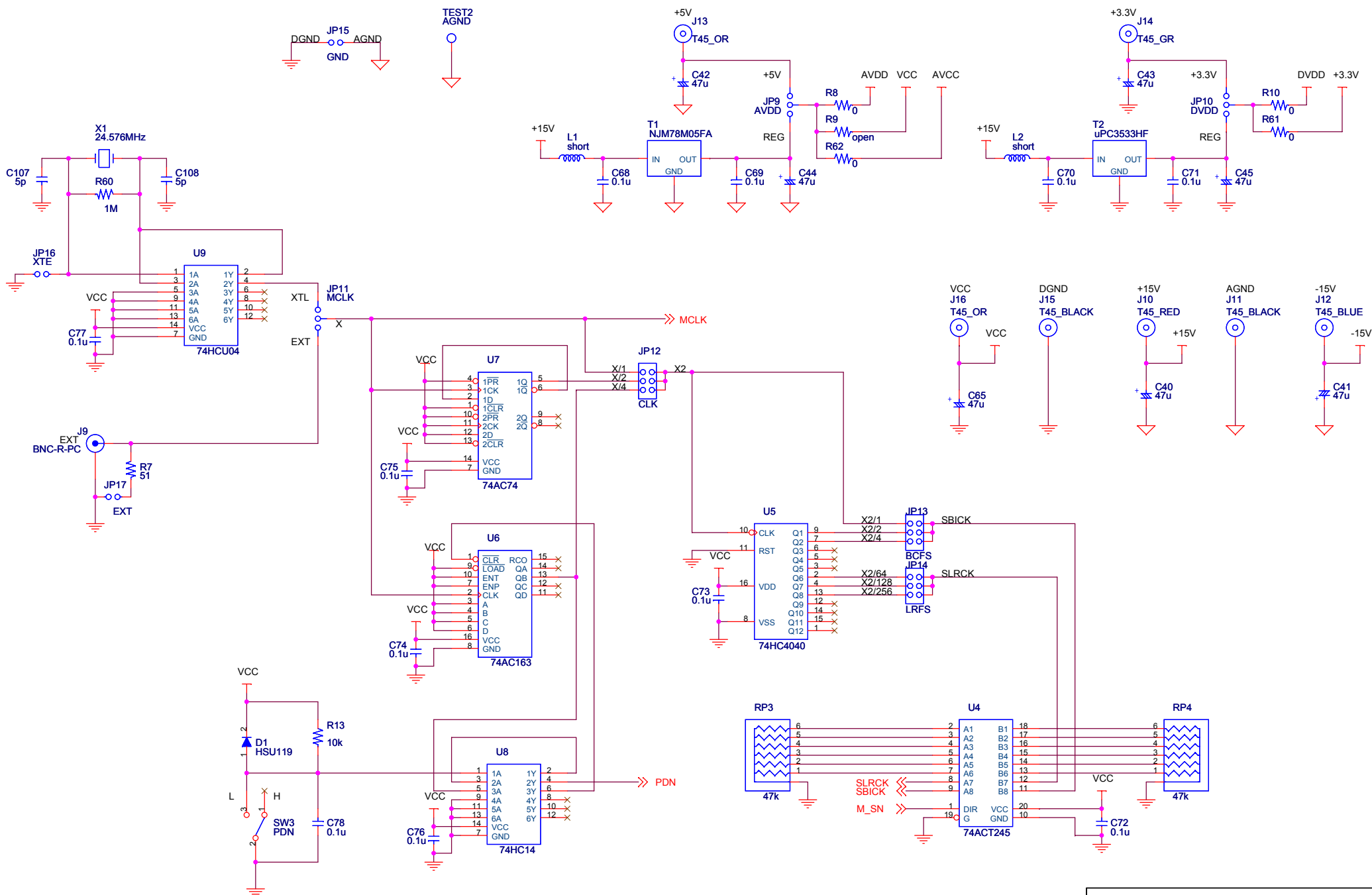
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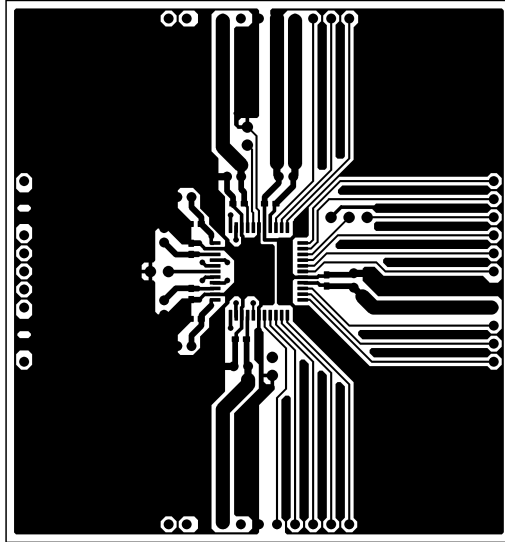


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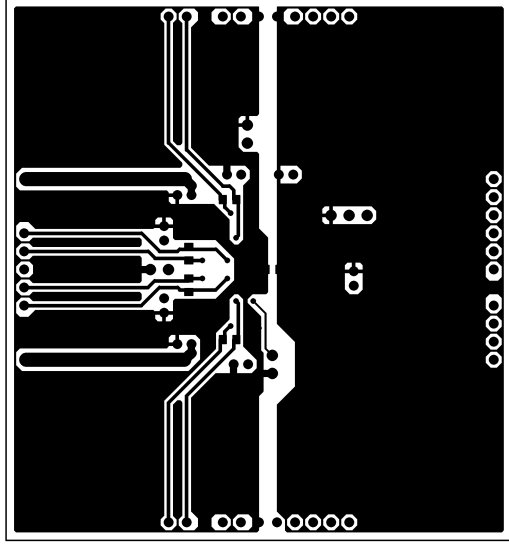


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		Rev	4

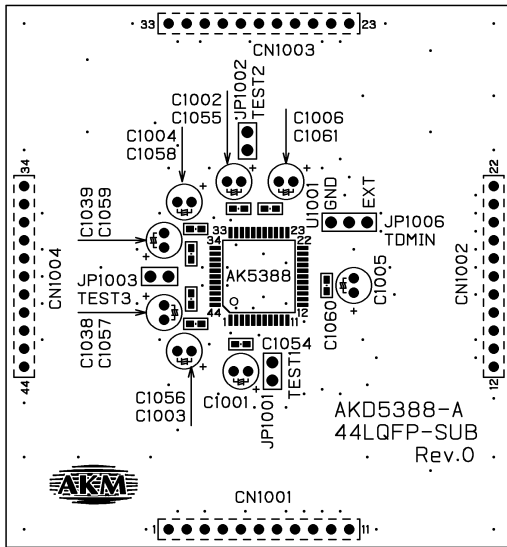




22540B L1

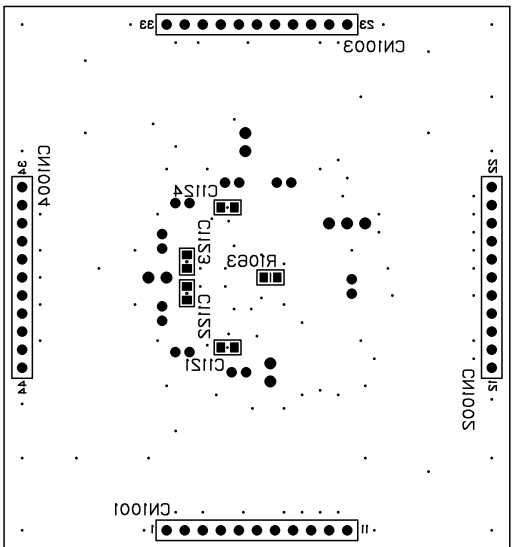


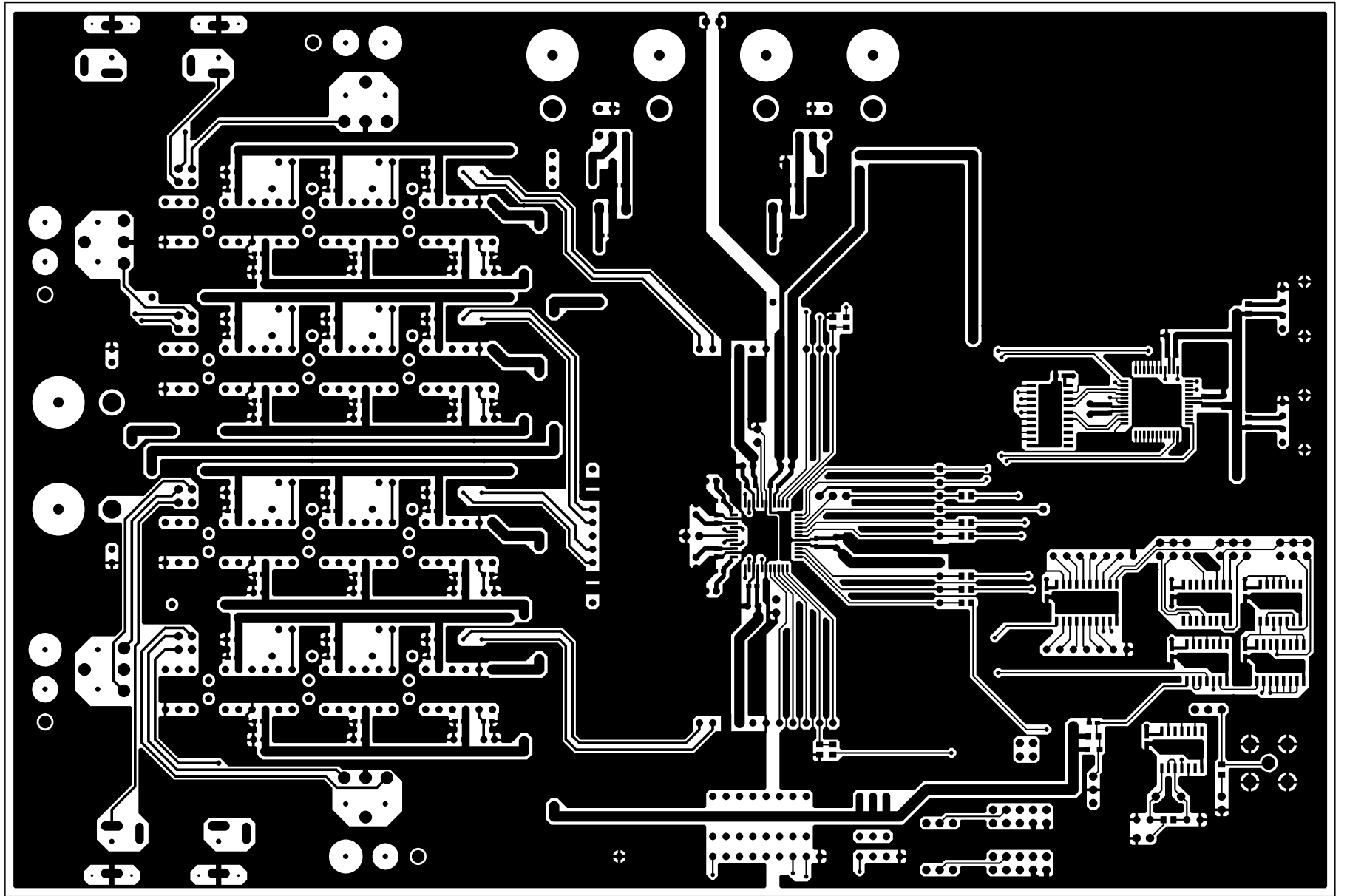
SS240B LS



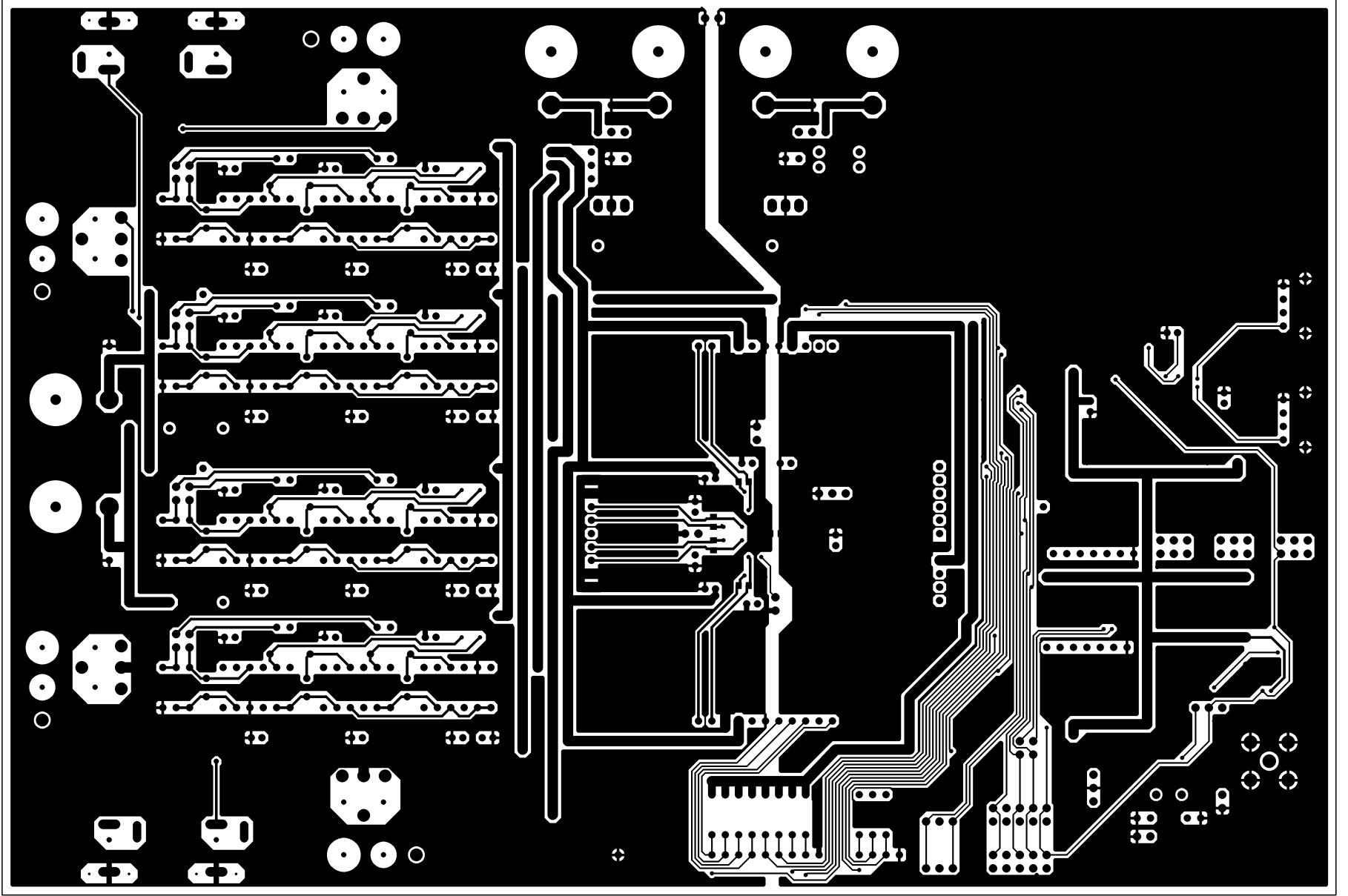
22540B L1 SR SILK

SS240B LS 2R SILK



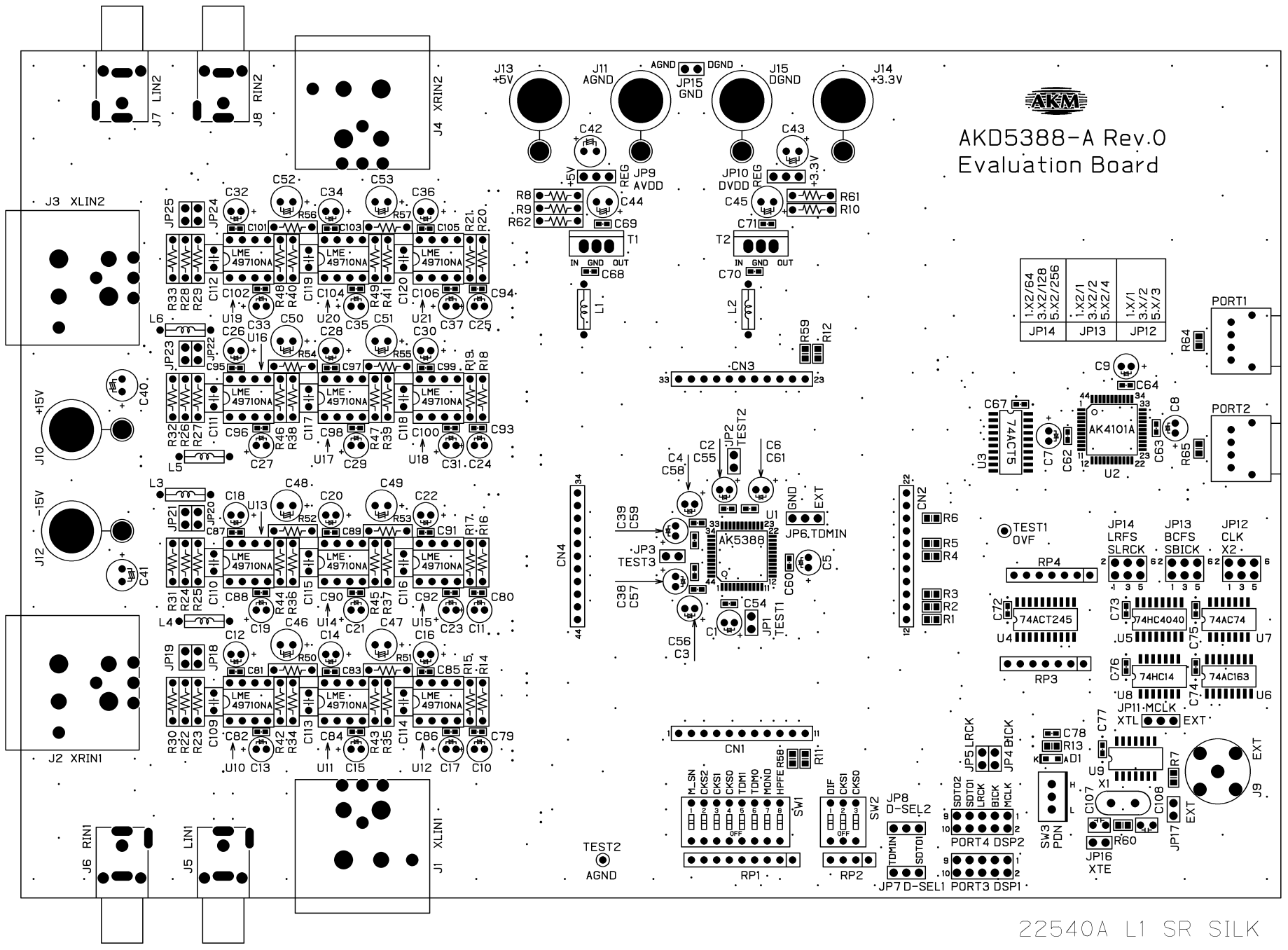


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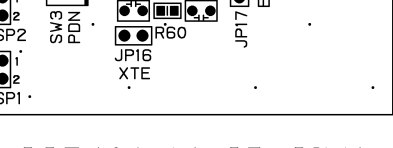
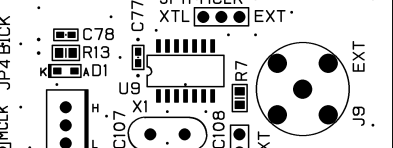
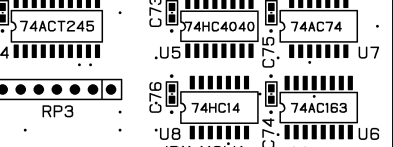
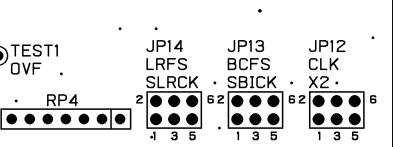
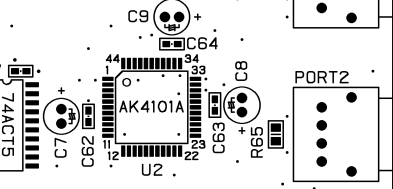




AKD5388-A Rev.0 Evaluation Board



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22540A L1 SR SILK

