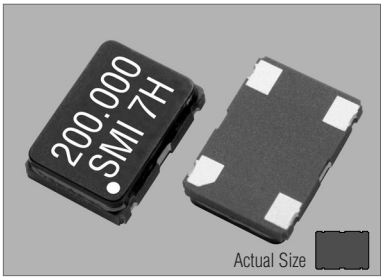
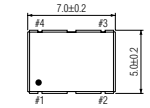
Crystal Clock Oscillators

91SMOP (+3.0V, +3.3V or +5V PROGRAMMABLE MODELS) — STANDARD SMD CLOCK OSCILLATORS

91SMOP



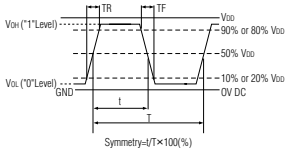
91SMOP



PIN	CONNECTION
1	"L" OPEN or "H"
2	GND
3	Z OUTPUT
4	VDD

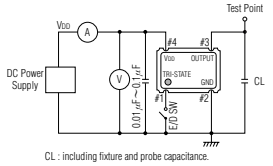
Z : high impedance

OUTPUT WAVEFORM



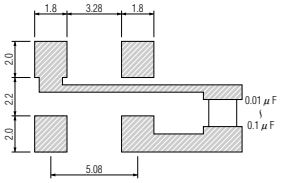
Symmetry=t/T×100(%)

TEST CIRCUIT

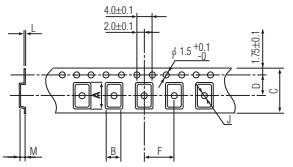


CL : including fixture and probe capacitance.

SOLDERING PATTERN



TAPE SPECIFICATIONS



A	B	C	D	F	J	L	M	Reel Dia.	Qty/Reel
7.4	5.4	16.0	7.5	8.0	1.5	0.3	1.9	180	1000pcs

STANDARD SPECIFICATIONS

using PLL technology

Item		Specifications			
Generic part number		91SMOP※1			
Frequency range		1.000 MHz to 200.000 MHz		1.000 MHz to 80.000 MHz	
Frequency stability (−20˚C to +75˚C) over all conditions		91SMOP(A) : ±100 ppm 91SMOP(B) : ±50 ppm		91SMOP(J) : ±100 ppm 91SMOP(K) : ±50 ppm	
Operating Conditions					
Operating temperature		−20˚C to +75˚C			
Input voltage (VDD)		+3.0V ±10%, +3.3V ±10% or +5V ±10%			
Tri-state control (Option1)		+3.0V & +3.3V models	SMI P/N	+3.0V & +3.3V models	SMI P/N
OE control voltage (Pin#1)/(Pin#3)		VIH : +2.2 VDD min. VIL : +0.5 VDD max.	91SMOP(3VA)OE 91SMOP(3VB)OE	VIH : +2.2 VDD min. VIL : +0.5 VDD max.	91SMOP(3VJ)OE 91SMOP(3VK)OE
OPEN→Output		+5V models	SMI P/N	+5V models	SMI P/N
VIH→Output VIL→High Impedance※2		VIH : +4.0 VDD min. VIL : +0.5 VDD max.	91SMOP(5VA)OE 91SMOP(5VB)OE	VIH : +4.0 VDD min. VIL : +0.5 VDD max.	91SMOP(5VJ)OE 91SMOP(5VK)OE
(※2) Internal crystal oscillation to continue.					
Tri-state control (Option2)		+3.0V & +3.3V models	SMI P/N	+3.0V & +3.3V models	SMI P/N
Stand-by (SB) control voltage (Pin#1)/(Pin#3)		VIH : +2.2 VDD min. VIL : +0.5 VDD max.	91SMOP(3VA)SB 91SMOP(3VB)SB	VIH : +2.2 VDD min. VIL : +0.5 VDD max.	91SMOP(3VJ)SB 91SMOP(3VK)SB
OPEN→Output		+5V models	SMI P/N	+5V models	SMI P/N
VIH→Output VIL→High Impedance※3		VIH : +4.0 VDD min. VIL : +0.5 VDD max.	91SMOP(5VA)SB 91SMOP(5VB)SB	VIH : +4.0 VDD min. VIL : +0.5 VDD max.	91SMOP(5VJ)SB 91SMOP(5VK)SB
(※3) Internal crystal oscillation to stop.					
Absolute Max. Ratings					
Supply voltage		−0.5V to +7.0V DC			
Storage temperature		−55˚C to +125˚C			
Input current (Pin#1=Open or VIH)	+3.0V ±10%	30 mA max.		20 mA max.	
	+3.0V ±10%	30 mA max.		20 mA max.	
	+5V ±10%	50 mA max.		30 mA max.	
Stand−by current※3(option)		50 μA max. (VDD = +3.0V & Pin #1=VIL)			
Output (−20˚C to +75˚C)					
Symmetry		45% to 55% at 50%VDD level (1.00MHz to 80.00MHz) 40% to 60% at 50%VDD level (80.00MHz to 200.00MHz)			
Rise and fall times		5 ns max. (20%VDD to 80%VDD level)			
"0" level		VOL : 10%VDD max. (1.00MHz to 130.00MHz) VOL : 20%VDD max. (130.00MHz to 200.00MHz)			
"1" level		VOH : 90%VDD min. (1.00MHz to 130.00MHz) VOH : 80%VDD min. (130.00MHz to 200.00MHz)			
Load		15 pF max. (CMOS)		50 pF max. (CMOS)	
Disable delay time		100 ns max.			
Enable delay time		150 ns max.(OE models) 10 ms max.(Stand-by models)			
Startup time		10 ms max.			
Jitter (pSp-p)		100, 200, 250 max. (depending on frequencies)			
Aging (non operating)		±5 ppm max. at +25˚C ±3˚C for first year			
Reflow condition		+250˚C ±10˚C for 10 seconds +170˚C ±10˚C for 1 to 2 minutes (preheating)			

PACKAGE DATA

Item \ Package	91SMOP
Lid	Ceramic
Base	Ceramic
Sealing	Glass
Terminal	Tungsten (metalized)
Terminal plating	Gold / Nickel (surface) / (under)
RoHS	Compliant

(※1) Final exact part number to be determined with frequency, frequency stability, operating temperature and input voltage. e.g. 91SMOP(3.3VA)SB 200.000 MHz.
(※2) Internal crystal oscillation to continue(Pin #1=VIL).
(※3) Internal crystal oscillation to be halted(Pin #1=VIL).