4096x4 Diagnostic Registered PROM
Asynchronous Enable

53D1641
63D1641

Patent Pend.

Features/Benefits

- **Asynchronous output enable**
- **Provides system diagnostic testing for system controllability and observability**
- **Shadow register eliminates shifting hazards**
- **Edge-triggered "D" registers simplifies system timing**
- **Casadable for wide control words used in microprogramming**
- **24-pin SKINNYDIP® saves space**
- 24-mA output drive capability
- **Replaces embedded diagnostic code**

Applications

- **Microprogram control store with built-in system diagnostic testing**
- **Serial character generator**
- **Serial code converter**
- **Parallel in/serial out memory**
- **Cost-effective board testing**

Description

The 53/63D1641 is a 4Kx4 PROM with registered three-state outputs and a shadow register for diagnostic capabilities.

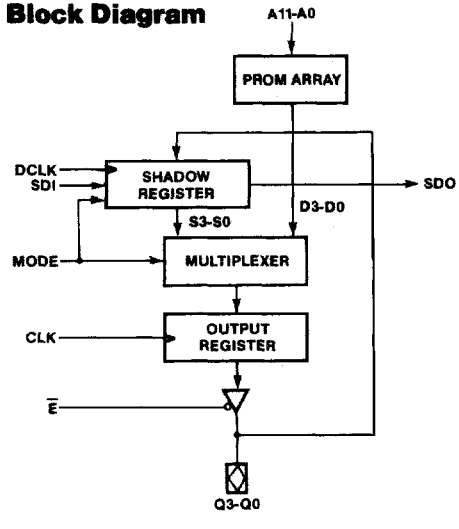
Ordering Information

MEMORY		TEMP.	PACKAGE		PART NO.
SIZE	ORG.		PINS	TYPE	
16K	4096x4	Mil	24 (28)	NS,JS,W, (NL),(L)	53D1641
		Com			63D1641

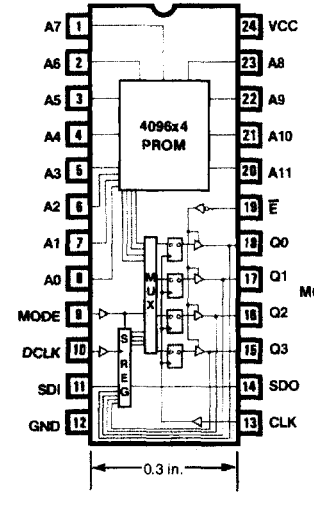
Flat-pack — contact the factory

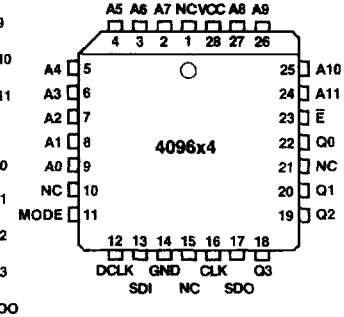
Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register, is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independent of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

Block Diagram



Pin Configurations





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Monolithic Memories

Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	↑	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.

† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

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Definition of Signals

MODE — The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI — The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO — The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK — The CLOCK pin loads the output register on the rising edge of CLK.

DCLK — The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 — Qn represents the data outputs of the output register. During a shadow register load with outputs enabled these pins are the internal data inputs to the shadow register. With the outputs three-stated these pins are external data inputs to the shadow register.

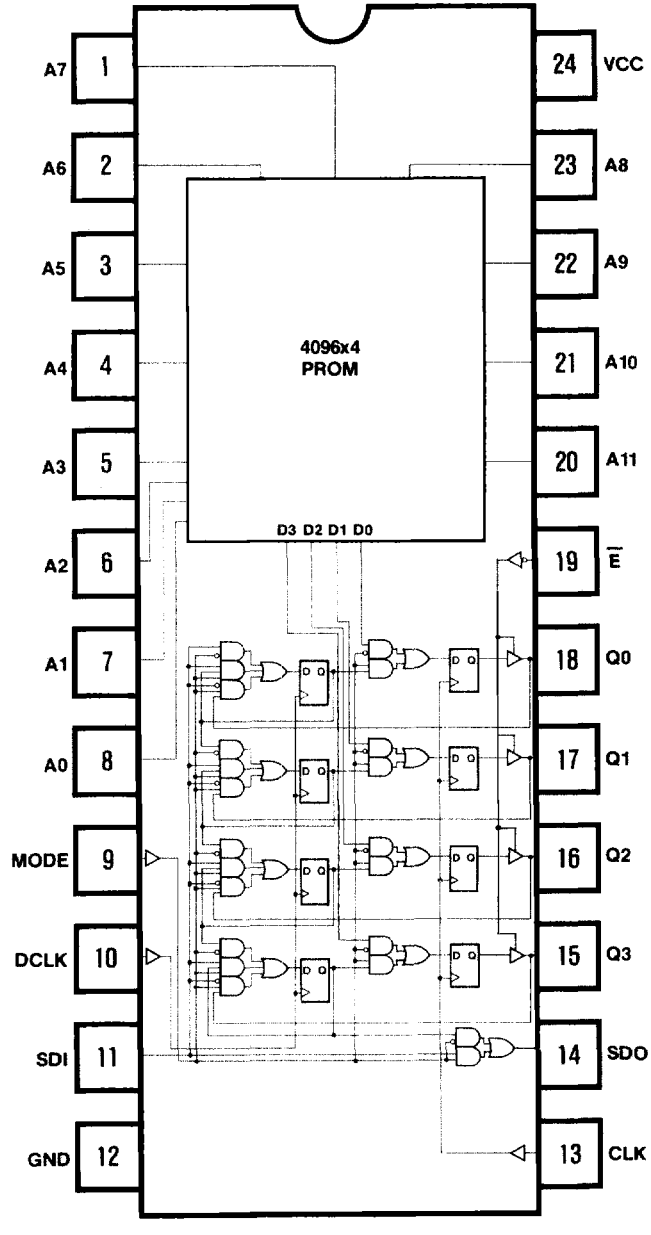
S3-S0 — Sn represents the internal shadow register outputs.

A11-A0 — An represents the address inputs to the PROM array.

$\overline{E}$ — The Output Enable pin operates independent of CLK. When $\overline{E}$ is LOW the outputs are enabled. When $\overline{E}$ is HIGH, the outputs are in the high impedance state.

Logic Diagram

4096x4 Diagnostic PROM with Asynchronous Enable



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input Current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	-55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	25		40	25		ns
t_h	Hold time for CLK	0	-15		0	-15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	-5		0	-5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL I_{OL} = 16 mA			0.5	V
			COM I_{OL} = 24 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = -2 mA	2.4			V
			COM I_{OH} = -3.2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	μA
I_{OZH}			V_O = 2.4 V			40	
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL; all outputs open			140	190	mA

† Typical at 5.0 V V_{CC} and 25°C T_A.

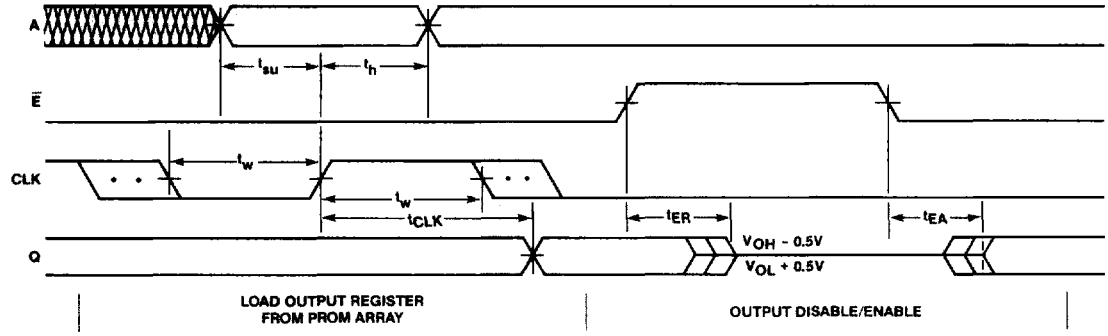
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

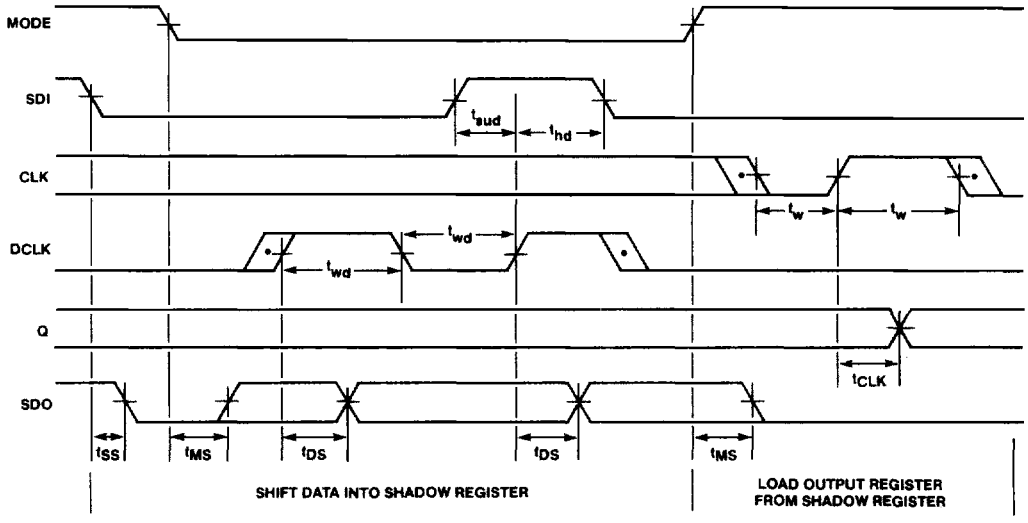
SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		11	25		11	20	ns
t_{ER}	Disable time		16	30		16	25	ns
t_{EA}	Enable time		16	30		16	25	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		17	35		17	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

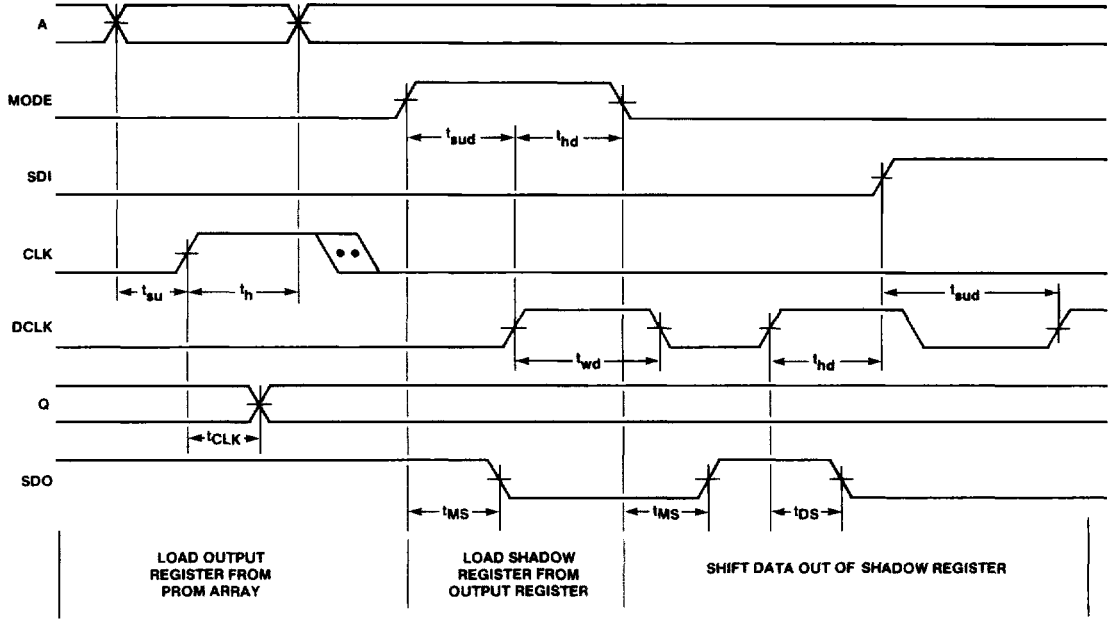
Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)

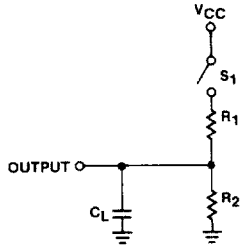


SYSTEM CONTROL



SYSTEM OBSERVATION

Switching Test Load



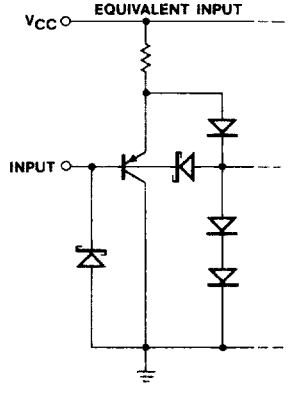
Definition of Timing Diagram

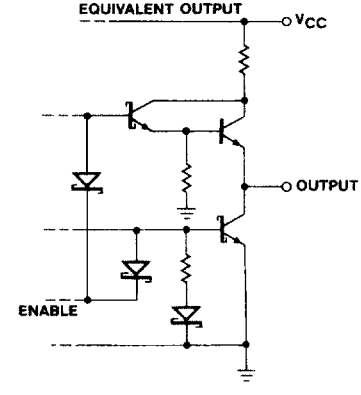
WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

NOTES. 1. For commercial operating range R_1 = 200Ω, R_2 = 390Ω.
For military operating range R_1 = 300Ω, R_2 = 600Ω.

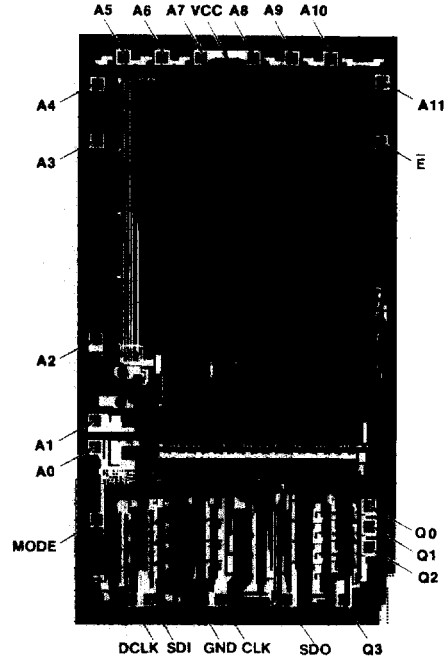
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
4. Input access measured at the 1.5 V level.
5. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
6. t_{EA} is measured at the 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.
t_{ER} is measured with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.

Schematic of Inputs and Outputs





Die Configuration



Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltage must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

MANUFACTURER	PROGRAMMER TYPE	PROGRAMMING MODULE	SOCKET CONFIGURATION
Data I/O	Unipack Rev-V07 Unipack2 Rev-V05	Family Code B2	Pinout Code 80