8-Channel High Voltage Analog Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options		
			18-pin Ceramic Side-brazed DIP*	18-pin Plastic DIP	Die in waffle pack
+70V	-70V	110V P-P	HV1214C	HV1214P	HV1214X
+80V	-80V	130V P-P	HV1216C	HV1216P	HV1216X

* Consult factory for Cerdip and Ceramic LCC availability.

Features

- HVCMOS® Technology
- Up to 130V peak to peak switching capability
- Output On-resistance typically 40 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- 45 dB typical output off isolation at 5 MHz
- CMOS logic circuitry for low power and excellent noise immunity
- On-chip shift register, latch, and clear logic circuitry

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

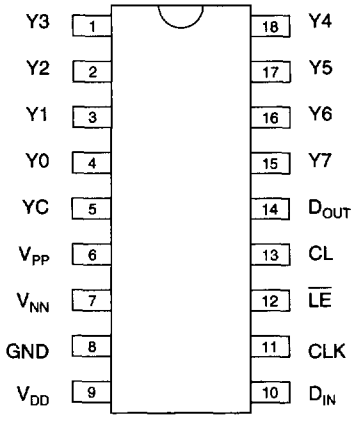
Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} positive high voltage supply	-0.5V to +90V†
V_{NN} negative high voltage supply	+0.5V to -90V†
Logic input voltages	-0.5 to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

† For HV1216

Pin Configuration



top view

18-pin DIP

Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V, and V_{DD} = 15V unless otherwise noted)*

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{ONS}		40		40	50		60	ohms	I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		35		25	35		45	ohms	I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		55		45	55		65	ohms	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		40		25	40		50	ohms	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance Matching	ΔR_{ONS}		30		10	30		30	%	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch Off Leakage Per Switch	I_{SOL}		50		0.5	50		150	µA	V_{SIG} = V_{PP} -10V thru 10KΩ with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	µA	
Pos. HV Supply Current	I_{PPQ}				0.8	1.6			mA	1 SWS ON, I_{SW} = 5mA
Neg. HV Supply Current	I_{NNQ}				-0.8	-1.6			mA	V_{SIG} = 0V
Pos. HV Supply Current	I_{PPQ}				0.6	1.2			mA	V_{PP} = +50V, V_{NN} = -50V
Neg. HV Supply Current	I_{NNQ}				-0.6	-1.2			mA	1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	V_{SIG} ≤ 0.1% Duty Cycle, f = 10KHz
Logic Supply Average Current	I_{DD}				4	6			mA	f_{CLK} = 3 MHz
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	V_{OUT} = V_{DD} -0.7V
Data Out Sink Current	I_{SINK}	0.7		0.8	0.9		0.7		mA	V_{OUT} = 0.7V
Logic Supply Quiesent Current	I_{DDQ}				10	500			µA	

AC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Set Up Time Before $\overline{LE}$ Rises	t_{SD}			260					ns	
Time Width of $\overline{LE}$	t_{WLE}			300					ns	
Clock Delay Time Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5.0		2.5	5.0		5.0	µs	R_L = 10KΩ
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	R_L = 10KΩ
Time Width of CL	t_{WCL}			150					ns	
Off Isolation	KO			-35	-45				dB	f = 5MHz
Clock Frequency	f_{CLK}					3.0			MHz	50% Duty Cycle f_{DATA} = $f_{CLK}/2$
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data from Clock	t_h			5.0					ns	
Switch Crosstalk	K_{CR}				-45				dB	Signal Freq = 5MHz

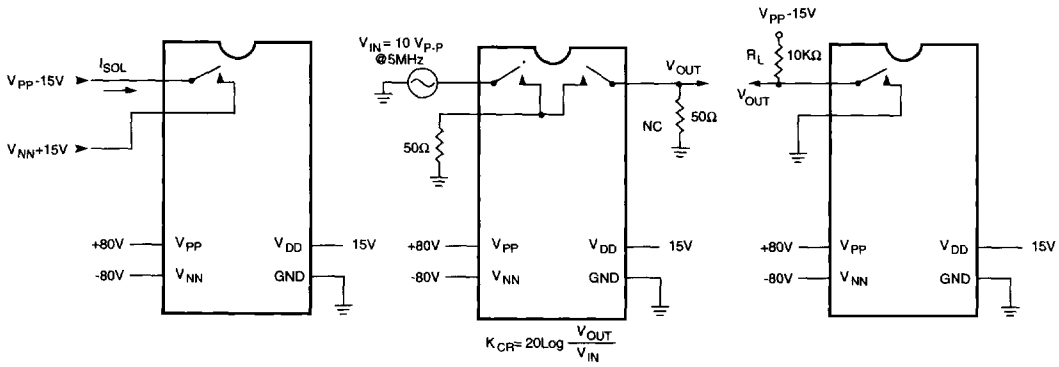
* For HV1216. For HV1214; V_{PP} = +70V, V_{NN} = -70V, and V_{DD} = 15V .

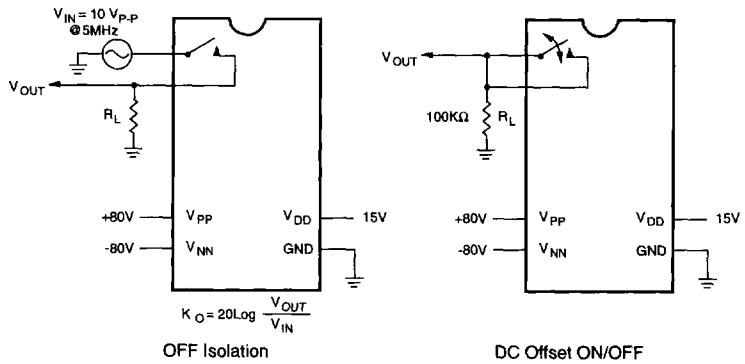
Operating Conditions

Symbol	Parameter	Device		Value
		HV1214	HV1216	
V_{DD}	Logic power supply voltage	X	X	+10V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70V
			X	+50.0V to +80V
V_{NN}	Negative high voltage supply	X		-50V to -70V
			X	-50V to -80V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

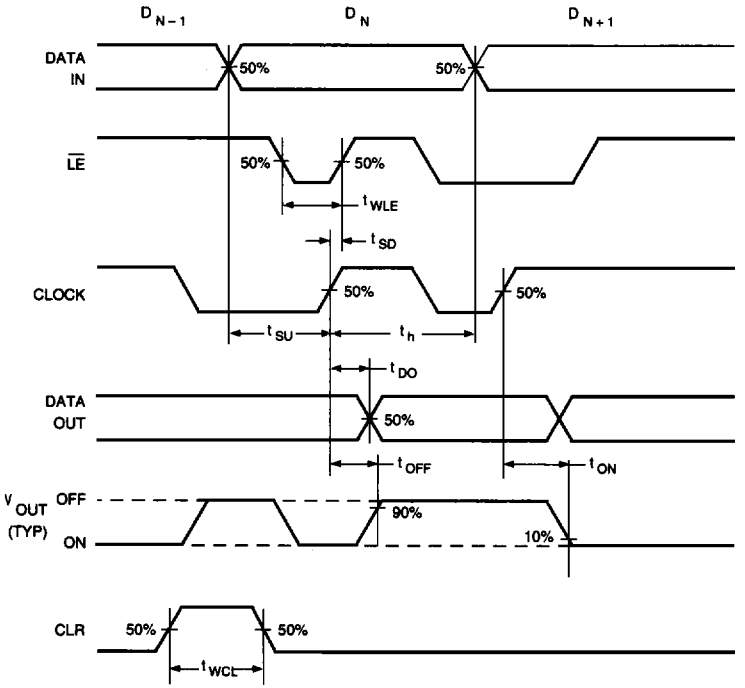
Note:
1. Power up/down sequence is arbitrary except GND must be powered-up first and powered - down last.
2. V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.

Test Circuits

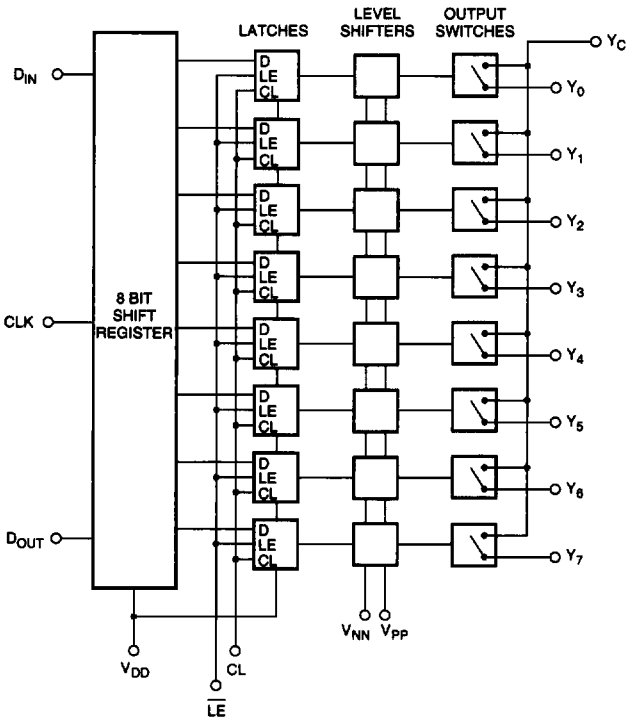




Logic Timing Waveform



Logic Diagram



Truth Table

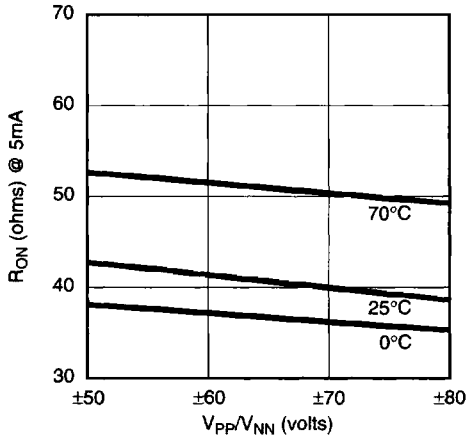
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	$\overline{LE}$	CL	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							

Notes:

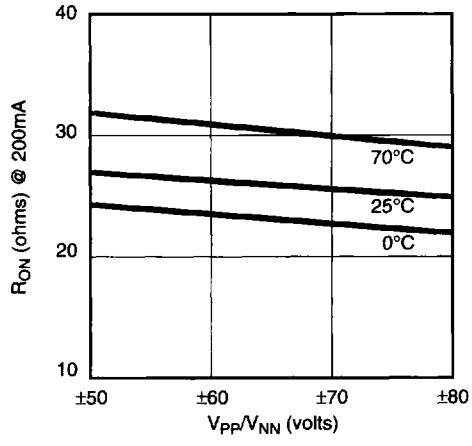
1. The eight switches operate independently, but connect to a common Z line.
2. Serial data is clocked in on the L→H transition of CLK.
3. The clear input overrides all other inputs.
4. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the shift register data flows through the latch.
5. D_{OUT} is high when switch 7 is on.
6. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.

Typical Performance Curves

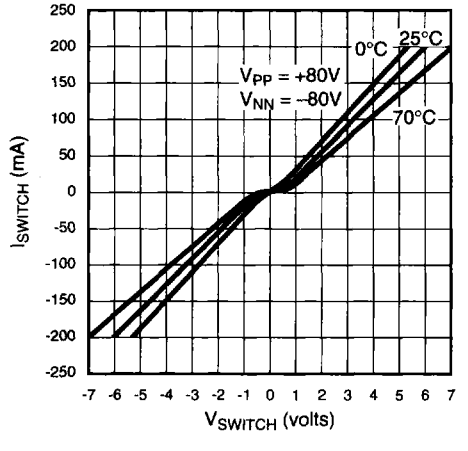
R_{ON} vs. V_{PP}/V_{NN}



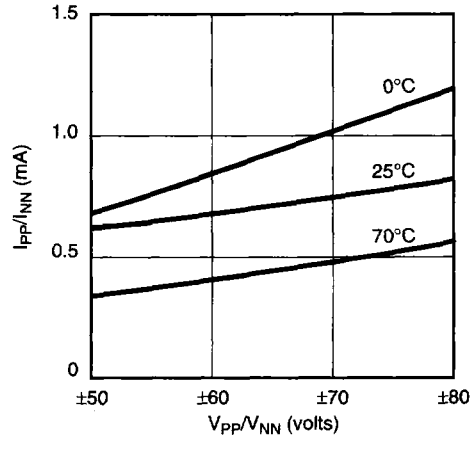
R_{ON} vs. V_{PP}/V_{NN}



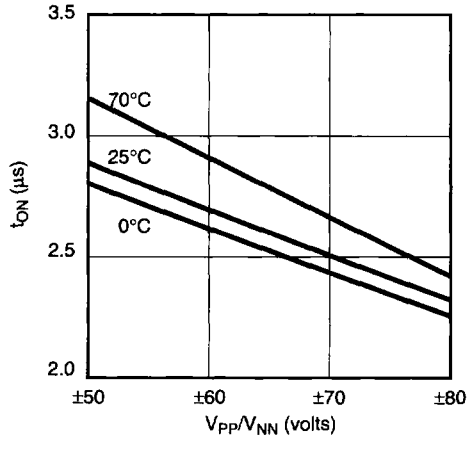
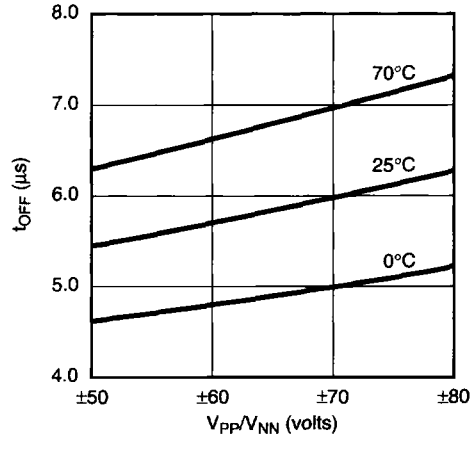
Switch Current vs. Switch Voltage



I_{PP}/I_{NN} vs. V_{PP}/V_{NN} (1 Switch ON)



t_{ON} vs. V_{PP}/V_{NN}



t_{OFF} vs. V_{PP}/V_{NN}