QL3100 / QL3100R
100,000 Usable PLD Gate pASIC®3 FPGA
Combining High Performance *and* High Density

ADVANCED DATA

pASIC 3 HIGHLIGHTS

... 100,000 usable PLD gates, 363 I/O pins

16,128 bit RAM Option

QL3100 Block Diagram

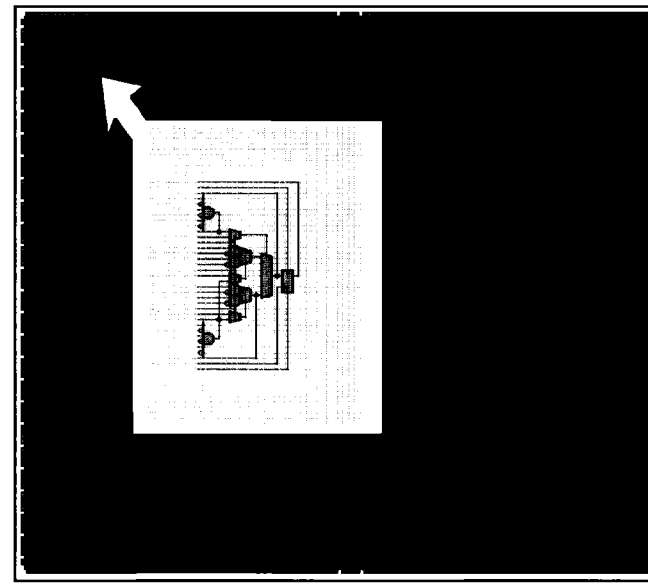
2,688 Logic Cells

High Performance and High Density
-100,000 Usable PLD Gates with 363 I/Os
-16-bit counter speeds over 225 MHz, data path speeds over 275 MHz
-0.35µm four-layer metal non-volatile CMOS process for smallest die sizes

Easy to Use / Fast Development Cycles
-100% routable with 100% utilization and complete pin-out stability
-Variable-grain logic cells provide high performance and 100% utilization
-Comprehensive design tools include high quality Verilog/VHDL synthesis

High Speed Embedded SRAM Available in "R" Versions
-28 dual-port RAM modules, organized in user-configurable 576-bit blocks
-5ns access times, each port independently accessible
-Fast and efficient for FIFO, RAM, and ROM functions

Advanced I/O Capabilities
-Interfaces with both 3.3 volt and 5.0 volt devices
-PCI compliant with 3.3V and 5.0V buses for -1/-2/-3 speed grades
-Full JTAG boundary scan
-Registered I/O cells with individually controlled clocks and output enables



QUICKLOGIC

PRODUCT SUMMARY

The QL3100 is a 100,000 usable PLD gate member of the pASIC 3 family of FPGAs. pASIC 3 FPGAs are fabricated on a 0.35µm four-layer metal process using QuickLogic's patented ViaLink technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The QL3100 contains 2,688 logic cells. With a maximum of 363 I/Os, the QL3100 is available in 208-pin PQFP, 256-pin PBGA, and 456-pin PBGA packages. The QL3100R also includes 28 dual port RAM modules, each with 576 bits, for a total of 16,128 RAM bits.

Software support for the complete pASIC 3 family, including the QL3100, is available through three basic packages. The turnkey Quick*Works*® package provides the most complete FPGA software solution from design entry to logic synthesis, to place and route, to simulation. The Quick*Chip*™ and Quick*Tools*™ packages provide a solution for designers who use Cadence, Exemplar, Mentor, Synopsys, Synplicity, Viewlogic, Veribest, or other third-party tools for design entry, synthesis, or simulation.

FEATURES

Total of 363 I/O Pins

- 355 bidirectional input/output pins, PCI-compliant for 5.0 volt and 3.3 volt buses for -1/-2/-3 speed grades
- 8 high-drive input/distributed network pins

Four Low-Skew (less than 0.5ns) Distributed Networks

- Two array clock/control networks available to the logic cell flip-flop clock, set and reset inputs - each driven by an input-only pin
- Two global clock/control networks available to the logic cell F1, clock, set and reset inputs and the input and I/O register clock, reset and enable inputs as well as the output enable control - each driven by an input-only or I/O pin, or any logic cell output or I/O cell feedback

High Performance

- Input + logic cell + output total delays under 6 ns
- Data path speeds exceeding 275 MHz
- Counter speeds over 225 MHz