UT54ACS164245S

Radiation-Hardened
Schmitt CMOS 16-bit Bidirectional MultiPurpose Transceiver
Advanced Datasheet

UTMC
MICROELECTRONIC
SYSTEMS
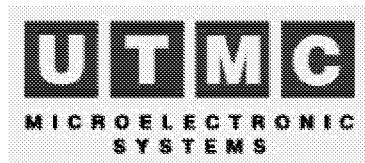
August 19, 1998

FEATURES

- Voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus
- Cold sparing
  - 3MΩ minimum input impedance power-off
- 0.6μm Commercial RadHard™ CMOS
  - Total dose: 100K rads(Si)
  - Single Event Latchup immune
- High speed, low power consumption
- Schmitt trigger inputs to filter noisy signals
- Available QML Q or V processes
- Standard Microcircuit Drawing 5962-98580
- Flexible package
  - 48-lead flatpack, 25 mil pitch (.390 x .640)

DESCRIPTION

The 16-bit wide UT54ACS164245S MultiPurpose transceiver is built using UTMC's Commercial RadHard™ epitaxial CMOS technology and is ideal for space applications. This high speed, low power UT54ACS164245S transceiver is designed to perform multiple functions including: asynchronous two-way communication, signal buffering, voltage translation, and cold sparing. With V_{DD} equal to zero volts, the UT54ACS164245S outputs and inputs present a minimum impedance of 3MΩ making it ideal for "cold spare" applications. Balanced outputs and low "on" output impedance make the UT54ACS164245S well suited for driving high capacitance loads and low impedance backplanes. The UT54ACS164245S enables system designers to interface 3.3 volt CMOS compatible components with 5 volt CMOS components. For voltage translation, the A port interfaces with the 3.3 volt bus; the B port interfaces with the 5 volt bus. The direction control (DIRx) controls the direction of data flow. The output enable ($\overline{OEx}$) overrides the direction control and disables both ports. These signals can be driven from either port A or B. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver.

LOGIC SYMBOL
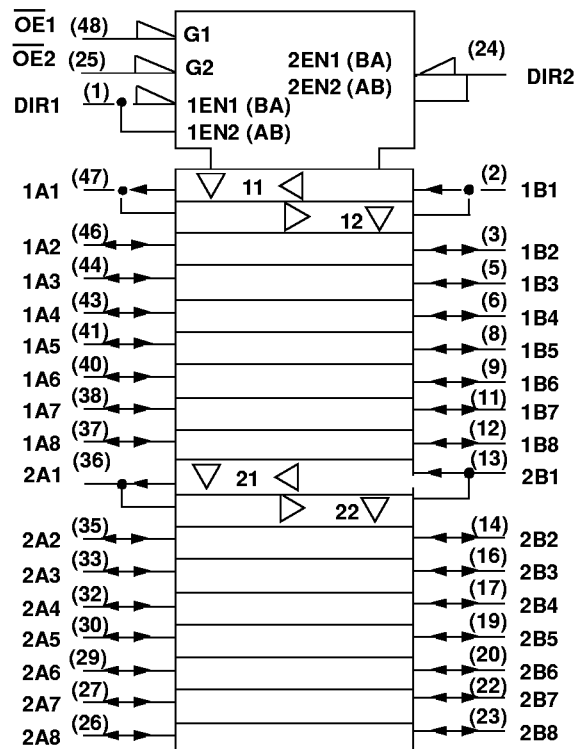
PIN DESCRIPTION

Pin Names	Description
$\overline{OEx}$	Output Enable Input (Active Low)
DIRx	Direction Control Inputs
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)

FUNCTION TABLE

ENABLE $\overline{OEx}$	DIRECTION DIRx	OPERATION
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Isolation

PINOUTS

48-Lead Flatpack
Top View

Pin			Pin
DIR1	1	48	$\overline{OE1}$
1B1	2	47	1A1
1B2	3	46	1A2
V_{SS}	4	45	V_{SS}
1B3	5	44	1A3
1B4	6	43	1A4
VDD1	7	42	VDD2
1B5	8	41	1A5
1B6	9	40	1A6
V_{SS}	10	39	V_{SS}
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
V_{SS}	15	34	V_{SS}
2B3	16	33	2A3
2B4	17	32	2A4
VDD1	18	31	VDD2
2B5	19	30	2A5
2B6	20	29	2A6
V_{SS}	21	28	V_{SS}
2B7	22	27	2A7
2B8	23	26	2A8
DIR2	24	25	$\overline{OE2}$

POWER TABLE

Port B	Port A	OPERATION
5 Volts	3.3 Volts	Voltage Translator
5 Volts	5 Volts	Non Translating
3.3 Volts	3.3 Volts	Non Translating

Control signals DIRx and $\overline{OEx}$ are 5 volt tolerant inputs. When V_{DD2} is at 3.3 volts, either 3.3 or 5 volt CMOS logic levels can be applied to all control inputs. For proper operation connect power to all V_{DD} and ground all V_{SS} pins (i.e., no floating V_{DD} or V_{SS} input pins). To minimize power consumption, when either V_{DD1} or V_{DD2} equal to 5 volts, input voltage on inputs other than DIRx and $\overline{OEx}$ should exceed 3.15 volts. Tie unused inputs to V_{SS}.

LOGIC DIAGRAM

3
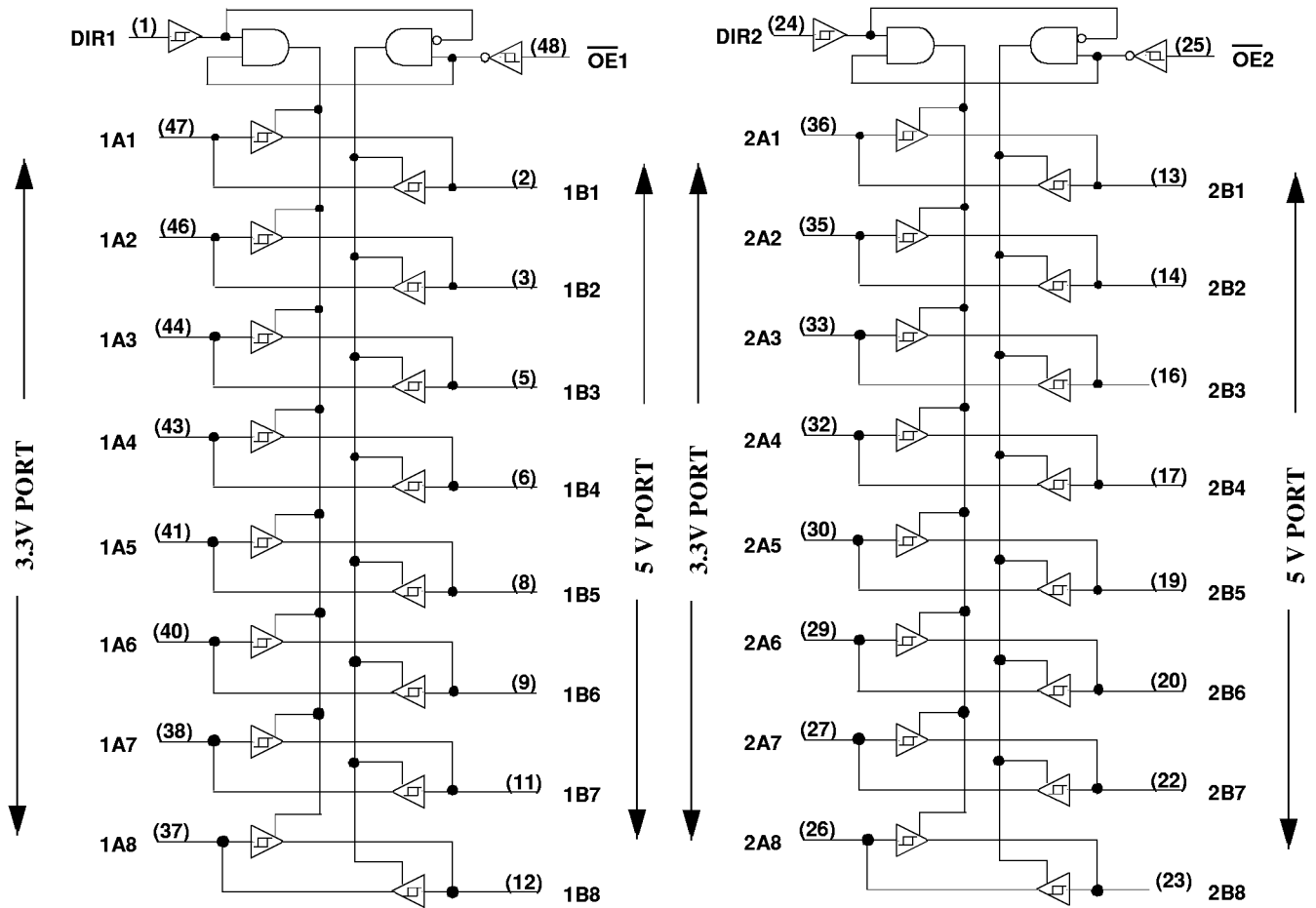
RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rads(Si)
SEL Latchup	>120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
$V_{I/O}$	Voltage any pin	-.3 to V_{DD1} +.3	V
V_{DD1}	Supply voltage	-0.3 to 6.0	V
V_{DD2}	Supply voltage	-0.3 to 6.0	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DUAL SUPPLY OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD1}	Supply voltage	4.5 to 5.5	V
V_{DD2}	Supply voltage	3.0 to 3.6	V
V_{IN}	Input voltage any pin	0 to V_{DD1}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS [1]

(-55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_T+	Schmitt Trigger, positive going threshold[2]			$.7V_{DD}$	V
V_T-	Schmitt Trigger, negative going threshold[2]		$.3V_{DD}$		V
V_{H1}	Schmitt Trigger range of hysteresis[11]	V_{DD} from 4.5 to 5.5	0.6		V
V_{H2}	Schmitt Trigger range of hysteresis	V_{DD} from 3.0 to 3.6	0.4		V
I_{IN} (on)	Input "on" leakage current[3]	V_{DD} from 3.0 to 5.5 $V_{IN} = V_{DD}$ or V_{SS}	-1	1	µA
I_{IN} (off)	Input "off" leakage current[4]	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	µA
V_{OL1}	Low-level output voltage[5]	I_{OL}= 8mA I_{OL}= 100µA[11] V_{DD} from 4.5 to 5.5		0.4 0.2	V
V_{OL2}	Low-level output voltage[5]	I_{OL}= 8mA[11] I_{OL}= 100µA[11] V_{DD} from 3.0 to 3.6		0.5 0.2	V
V_{OH1}	High-level output voltage[5]	I_{OH}= -8mA I_{OH}= -100µA[11] V_{DD} from 4.5 to 5.5	V_{DD} - 0.7 V_{DD} - 0.2		V
V_{OH2}	High-level output voltage[5]	I_{OH}= -8mA[11] I_{OH}= -100µA[11] V_{DD} from 3.0 to 3.6	V_{DD} - 0.9 V_{DD} - 0.2		V
I_{OZ} (on)	Three-state "on" output leakage current[3]	V_{DD} from 3.0 to 5.5 $V_{IN} = V_{DD}$ or V_{SS}	-1	1	µA
I_{OZ} (off)	Three-state "off" output leakage current[4]	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	µA
I_{OS1}	Short-circuit output current [6,7]	$V_O = V_{DD}$ or V_{SS} V_{DD} from 4.5 to 5.5	-200	200	mA
I_{OS2}	Short-circuit output current [6,7]	$V_O = V_{DD}$ or V_{SS} V_{DD} from 3.0 to 3.6	-100	100	mA

P_{total1}	Power dissipation [6, 8, 9]	$C_L = 50pF$ V_{DD} from 4.5 to 5.5		2.0	mW/MHz
P_{total2}	Power dissipation [6, 8, 9]	$C_L = 50pF$ V_{DD} from 3.0 to 3.6		1.5	mW/MHz
I_{DDQ}	Quiescent Supply Current Pre-Rad @ 25°C Pre-Rad -55°C to +125°C Post-Rad -55°C to +125°C	$V_{IN} = V_{DD}$ or V_{SS} V_{DD} from 3.0 to 5.5		10 100 200	µA
C_{IN}	Input capacitance [10]	$f = 1MHz$ @ 0V V_{DD} from 3.0 to 5.5		15	pF
C_{OUT}	Output capacitance[10]	$f = 1MHz$ @ 0V V_{DD} from 3.0 to 5.5		15	pF

Notes:
1. All specifications valid for radiation dose ≤ 1E5 rads(Si) per MIL-STD-883, Method 1019.
2. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%$, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
3. "On" is defined as powered on.
4. "Off" is defined as powered off.
5. Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
6. Guaranteed by characterization.
7. Not more than one output may be shorted at a time for maximum duration of one second.
8. Power does not include power contribution of any CMOS output sink current.
9. Power dissipation specified per switching output.
10. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
11. Guranteed; tested 100% at worst case V_{DD}/current, otherwise tested on a sample of pins per device.

AC ELECTRICAL CHARACTERISTICS[1] (Port B = 5 Volt, Port A = 3.3 Volt)

(V_{DD1} = 5V $\pm$10%; V_{DD2} = 3.0V to 3.6V, -55°C < T_C < +125°C)

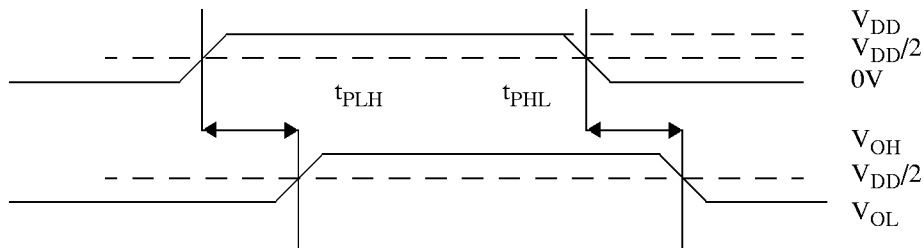| SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay Data to Bus	1	20	ns
t_{PHL}	Propagation delay Data to Bus	1	20	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus	1	18	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus	1	18	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	20	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	20	ns
t_{PZL}[2]	Output enable time DIRx to Bus	1	18	ns
t_{PZH}[2]	Output enable time DIRx to Bus	1	18	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance	1	20	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance	1	20	ns

Notes:
1. All specifications valid for radiation dose $\leq$ 1E5 rads(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. OEx to bus times are tested.

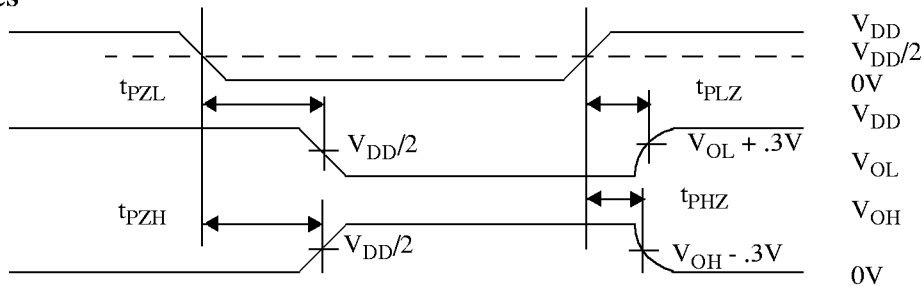### Propagation Delay

Same Phase Input
Transition

Output

Enable Disable Times

Control Input

Output Normally
Low
Output Normally
High

AC ELECTRICAL CHARACTERISTICS[1] (Port A = Port B, 5 Volt Operation)

(V_{DD1} = 5V $\pm$10%; V_{DD2} = 5.0V $\pm$10%, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay Data to Bus	1	15	ns
t_{PHL}	Propagation delay Data to Bus	1	15	ns
t_{PZL}	Output enable time $\overline{OE}$x to Bus	1	12	ns
t_{PZH}	Output enable time $\overline{OE}$x to Bus	1	12	ns
t_{PLZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	15	ns
t_{PHZ}	Output disable time $\overline{OE}$x to Bus high impedance	1	15	ns
$t_{PZL}{}^2$	Output enable time DIRx to Bus	1	12	ns
$t_{PZH}{}^2$	Output enable time DIRx to Bus	1	12	ns
$t_{PLZ}{}^2$	Output disable time DIRx to Bus high impedance	1	15	ns
$t_{PHZ}{}^2$	Output disable time DIRx to Bus high impedance	1	15	ns

Notes:
1. All specifications valid for radiation dose ≤ 1E5 rads(Si) per MIL-STD-883, Method 1019.
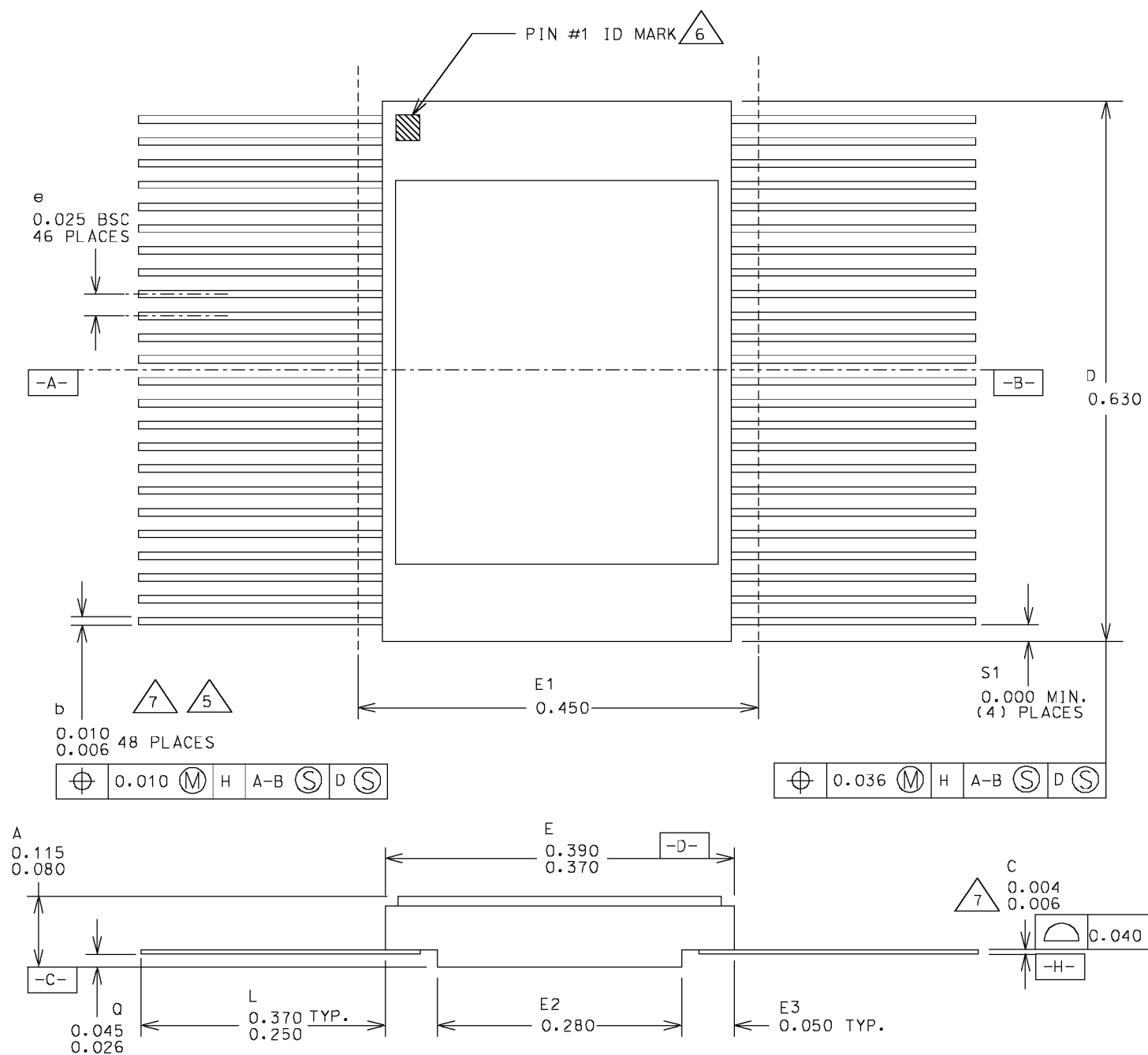2. DIRx to bus times are guaranteed by design, but not tested. OEx to bus times are tested

AC ELECTRICAL CHARACTERISTICS[1] (Port A = Port B, 3.3 Volt Operation)
(V_{DD1} = 3.0V to 3.6V; V_{DD2} = 3.0V to 3.6V, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay Data to Bus	1	20	ns
t_{PHL}	Propagation delay Data to Bus	1	20	ns
t_{PZL}	Output enable time $\overline{OE}x$ to Bus	1	18	ns
t_{PZH}	Output enable time $\overline{OE}x$ to Bus	1	18	ns
t_{PLZ}	Output disable time $\overline{OE}x$ to Bus high impedance	1	20	ns
t_{PHZ}	Output disable time $\overline{OE}x$ to Bus high impedance	1	20	ns
t_{PZL}[2]	Output enable time DIRx to Bus	1	18	ns
t_{PZH}[2]	Output enable time DIRx to Bus	1	18	ns
t_{PLZ}[2]	Output disable time DIRx to Bus high impedance	1	20	ns
t_{PHZ}[2]	Output disable time DIRx to Bus high impedance	1	20	ns

Notes:
1. All specifications valid for radiation dose ≤ 1E5 rads(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. OEx to bus times are tested.

PACKAGE

PIN #1 ID MARK △6

e
0.025 BSC
46 PLACES

-A-

-B-

D
0.630

E1
0.450

S1
0.000 MIN.
(4) PLACES

b
0.010
0.006 48 PLACES

△7 △5

| ⊕ | 0.010 Ⓜ | H | A-B Ⓢ | D Ⓢ |

| ⊕ | 0.036 Ⓜ | H | A-B Ⓢ | D Ⓢ |

A
0.115
0.080

E
0.390
0.370 -D-

C
△7 0.004
0.006

⌒ | 0.040

-H-

-C-

Q
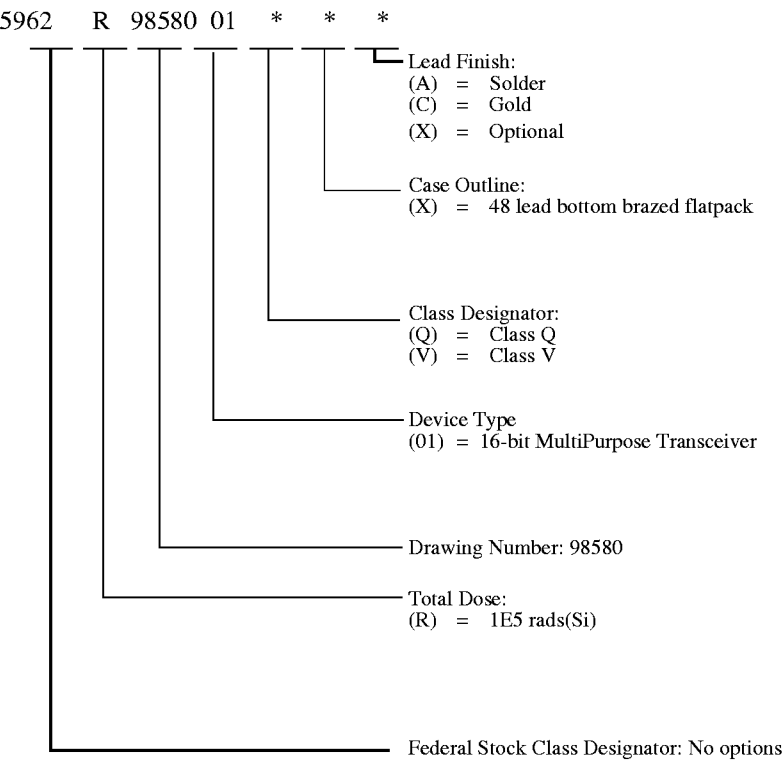0.045
0.026

L
0.370 TYP.
0.250

E2
0.280

E3
0.050 TYP.

1. All exposed metalized areas are gold plated.
2. The lid is electrically connected to VSS.
3. Lead finish is in accordance with MIL-PRF-38535.
4. Package dimensions are similar to MIL-STD-1835 variation F-19.
△5 Lead position and coplanarity are not measured.
△6 ID mark symbol is a vendor option.
△7 With solder, increase maximum by 0.003.
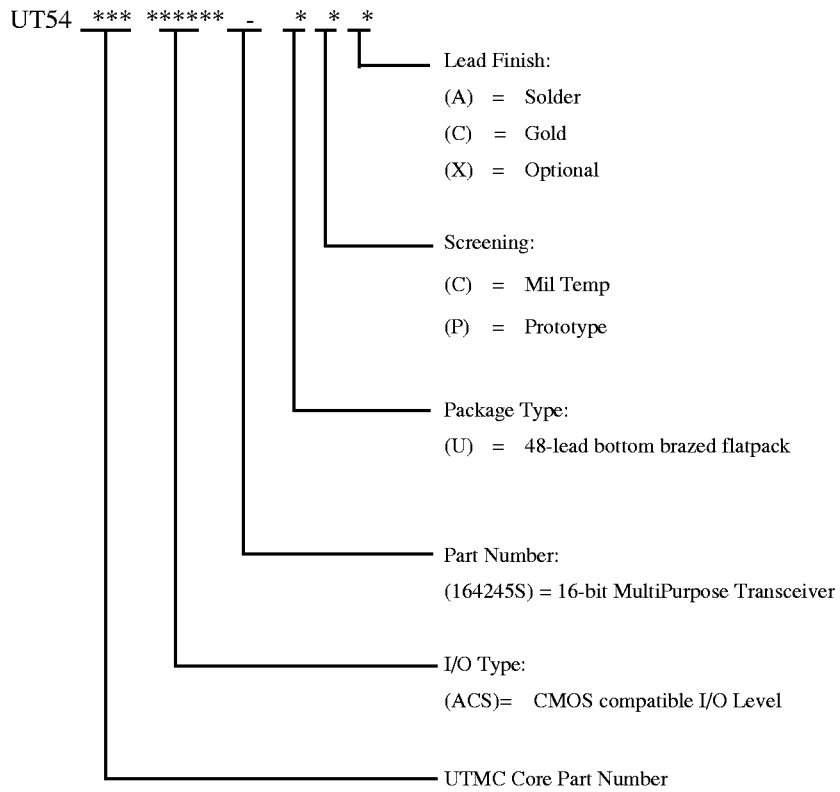
Figure 1. 48-Lead Flatpack

ORDERING INFORMATION

UT54ACS164245S: SMD

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5962   R  98580 01  *   *   *
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Lead Finish:
(A) = Solder
(C) = Gold
(X) = Optional

Case Outline:
(X) = 48 lead bottom brazed flatpack

Class Designator:
(Q) = Class Q
(V) = Class V

Device Type
(01) = 16-bit MultiPurpose Transceiver

Drawing Number: 98580

Total Dose:
(R) = 1E5 rads(Si)

Federal Stock Class Designator: No options

Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part number will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

UT54ACS164245

UT54 *** ****** - * * *

Lead Finish:

(A) = Solder

(C) = Gold

(X) = Optional

Screening:

(C) = Mil Temp

(P) = Prototype

Package Type:

(U) = 48-lead bottom brazed flatpack

Part Number:

(164245S) = 16-bit MultiPurpose Transceiver

I/O Type:

(ACS)= CMOS compatible I/O Level

UTMC Core Part Number

Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part number will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested -55C, room temp, and 125C. Radiation neither tested nor guaranteed.
4. Prototype flow per UTMC Manufacturing Flows Document Tested at 25C only. Lead finish is gold only.

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