# Multi-Purpose Flash Plus + SRAM ComboMemory

## SST32HF162C / SST32HF164C / SST32HF324C

***Preliminary Specifications***

## FEATURES:

- **ComboMemories organized as:**
  - SST32HF162C: 1M x16 Flash + 128K x16 SRAM
  - SST32HF164C: 1M x16 Flash + 256K x16 SRAM
  - SST32HF324C: 2M x16 Flash + 256K x16 SRAM
- **Single 2.7-3.3V Read and Write Operations**
- **Concurrent Operation**
  - Read from or Write to SRAM while Erase/Program Flash
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 15 mA (typical) for Flash or SRAM Read
  - Standby Current:
    - SST32HFx1C: 12 µA (typical)
- **Flexible Erase Capability**
  - Uniform 2 KWord sectors
  - Uniform 32 KWord size blocks
- **Erase-Suspend/Erase-Resume Capabilities**
- **Fast Read Access Times:**
  - Flash: 70 ns
  - SRAM: 70 ns
- **Latched Address and Data for Flash**
- **Flash Fast Erase and Word-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 40 ms (typical)
  - Word-Program Time: 7 µs (typical)
- **Flash Automatic Erase and Program Timing**
  - Internal $V_{PP}$ Generation
- **Flash End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Package Available**
  - 48-ball LBGA (10mm x 12mm x 1.4mm)

## PRODUCT DESCRIPTION

The SST32HF16xC/324C ComboMemory devices integrate a CMOS flash memory bank with a CMOS SRAM memory bank in a Multi-Chip Package (MCP), manufactured with SST's proprietary, high performance SuperFlash technology.

Featuring high performance Word-Program, the flash memory bank provides a maximum Word-Program time of 7 µsec. To protect against inadvertent flash write, the SST32HF16xC/324C devices contain on-chip hardware and software data protection schemes. The SST32HF16xC/324C devices offer a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST32HF16xC/324C devices consist of two independent memory banks with respective bank enable signals. The Flash and SRAM memory banks are superimposed in the same memory address space. Both memory banks share common address lines, data lines, WE# and OE#. The memory bank selection is done by memory bank enable signals. The SRAM bank enable signal, BES# selects the SRAM bank. The flash memory bank enable signal, BEF# selects the flash memory bank. The WE# signal has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The SDP command sequence protects the data stored in the flash memory bank from accidental alteration.

The SST32HF16xC/324C provide the added functionality of being able to simultaneously read from or write to the SRAM bank while erasing or programming in the flash memory bank. The SRAM memory bank can be read or written while the flash memory bank performs Sector-Erase, Bank-Erase, or Word-Program concurrently. All flash memory Erase and Program operations will automatically latch the input address and data signals and complete the operation in background without further input stimulus requirement. Once the internally controlled Erase or Program cycle in the flash bank has commenced, the SRAM bank can be accessed for Read or Write.

The SST32HF16xC/324C devices are suited for applications that use both flash memory and SRAM memory to store code or data. For systems requiring low power and small form factor, the SST32HF16xC/324C devices significantly improve performance and reliability while lowering power consumption when compared with multiple chip solutions. The SST32HF16xC/324C inherently use less energy during Erase and Program operations than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since, for any given voltage range, SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies.

SuperFlash technology provides fixed Erase and Program times independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

## Device Operation

The ComboMemory uses BES# and BEF# to control operation of either the SRAM or the flash memory bank. When BES# is low, the SRAM Bank is activated for Read and Write operation. When BEF# is low the flash bank is activated for Read, Program or Erase operation. BES# and BEF# cannot be at low level at the same time. **If BES# and BEF# are both asserted to low level bus contention will result and the device may suffer permanent damage.** All address, data, and control lines are shared by SRAM Bank and flash bank which minimizes power consumption and loading. The device goes into standby when both bank enables are high.

## Concurrent Read/Write Operation

The SST32HF16xC/324C provide the unique benefit of being able to read from or write to SRAM, while simultaneously erasing or programming the flash. This allows data alteration code to be executed from SRAM, while altering the data in flash. See Figure 21 for a flowchart. The following table lists all valid states.

**CONCURRENT READ/WRITE STATE TABLE**

| Flash | SRAM |
|---|---|
| Program/Erase | Read |
| Program/Erase | Write |

The device will ignore all SDP commands when an Erase or Program operation is in progress. Note that Product Identification commands use SDP; therefore, these commands will also be ignored while an Erase or Program operation is in progress.

## Flash Read Operation

The Read operation of the SST32HF16xC/324C devices is controlled by BEF# and OE#. Both have to be low, with WE# high, for the system to obtain data from the outputs. BEF# is used for flash memory bank selection. When BEF# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to Figure 5 for further details.

## Flash Word-Program Operation

The flash memory bank of the SST32HF16xC/324C devices is programmed on a word-by-word basis. Before Program operations, the memory must be erased first. The Program operation consists of three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load word address and word data. During the Word-Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs last. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed, within 10 µs. See Figures 6 and 7 for WE# and BEF# controlled Program operation timing diagrams and Figure 17 for flowcharts. During the Program operation, the only valid flash Read operations are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any SDP commands loaded during the internal Program operation will be ignored.

## Flash Sector/Block-Erase Operation

The Flash Sector/Block-Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST32HF16xC/324C offer both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 2 KWord. The Block-Erase mode is based on uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The address lines $A_{MS}$-$A_{11}$ are used to determine the sector address. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The address lines $A_{MS}$-$A_{15}$ are used to determine the block address. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figures 11 and 12 for timing waveforms. Any commands issued during the Sector- or Block-Erase operation are ignored.

## Erase-Suspend/Erase-Resume Commands

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read from any memory location, or program data into any sector/block that is not suspended for an Erase operation. The operation is executed by issuing one byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode typically within 20 µs after the Erase-Suspend command had been issued. Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output $DQ_2$ toggling and $DQ_6$ at "1". While in Erase-Suspend mode, a Word-Program operation is allowed except for the sector or block selected for Erase-Suspend.

To resume Sector-Erase or Block-Erase operation which has been suspended the system must issue Erase Resume command. The operation is executed by issuing one byte command sequence with Erase Resume command (30H) at any address in the last Byte sequence.

## Flash Chip-Erase Operation

The SST32HF16xC/324C provide a Chip-Erase operation, which allows the user to erase the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or BEF#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 5 for the command sequence, Figure 9 for timing diagram, and Figure 20 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

## Write Operation Status Detection

The SST32HF16xC/324C provide two software means to detect the completion of a write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling ($DQ_7$) and Toggle Bit ($DQ_6$). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either $DQ_7$ or $DQ_6$. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

## Flash Data# Polling ($DQ_7$)

When the SST32HF16xC/324C flash memory banks are in the internal Program operation, any attempt to read $DQ_7$ will produce the complement of the true data. Once the Program operation is completed, $DQ_7$ will produce true data. Note that even though $DQ_7$ may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read $DQ_7$ will produce a '0'. Once the internal Erase operation is completed, $DQ_7$ will produce a '1'. The Data# Polling is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operation. For Sector- or Block-Erase, the Data# Polling is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 8 for Data# Polling timing diagram and Figure 18 for a flowchart.

## Toggle Bits (DQ6 and DQ2)

During the internal Program or Erase operation, any consecutive attempts to read $DQ_6$ will produce alternating "1"s and "0"s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the $DQ_6$ bit will stop toggling. The device is then ready for the next operation. For Sector-, Block-, or Chip-Erase, the toggle bit ($DQ_6$) is valid after the rising edge of sixth WE# (or BEF#) pulse. $DQ_6$ will be set to "1" if a Read operation is attempted on an Erase-Suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, $DQ_6$ will toggle.

An additional Toggle Bit is available on $DQ_2$, which can be used in conjunction with $DQ_6$ to check whether a particular sector is being actively erased or erase-suspended. Table 1 shows detailed status bits information. The Toggle Bit ($DQ_2$) is valid after the rising edge of the last WE# (or BEF#) pulse of Write operation. See Figure 9 for Toggle Bit timing diagram and Figure 18 for a flowchart.

**TABLE 1: WRITE OPERATION STATUS**

| Status | | $DQ_7$ | $DQ_6$ | $DQ_2$ |
|---|---|---|---|---|
| Normal Operation | Standard Program | $DQ_7$# | Toggle | No Toggle |
| | Standard Erase | 0 | Toggle | Toggle |
| Erase-Suspend Mode | Read from Erase-Suspended Sector/Block | 1 | 1 | Toggle |
| | Read from Non- Erase-Suspended Sector/Block | Data | Data | Data |
| | Program | $DQ_7$# | Toggle | N/A |

T1.0 1267

**Note:** $DQ_7$ and $DQ_2$ require a valid address when reading status information.

## Flash Memory Data Protection

The SST32HF16xC/324C flash memory bank provides both hardware and software features to protect nonvolatile data from inadvertent writes.

## Flash Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

$V_{DD}$ Power Up/Down Detection: The Write operation is inhibited when $V_{DD}$ is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the flash Write operation. This prevents inadvertent writes during power-up or power-down.

## Flash Software Data Protection (SDP)

The SST32HF16xC/324C provide the JEDEC approved software data protection scheme for all flash memory bank data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. The SST32HF16xC/324C devices are shipped with the software data protection permanently enabled. See Table 5 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode, within $T_{RC}$. The contents of $DQ_{15}$-$DQ_8$ can be $V_{IL}$ or $V_{IH}$, but no other value, during any SDP command sequence.

## SRAM Read

The SRAM Read operation of the SST32HF16xC/324C is controlled by OE# and BES#, both have to be low with WE# high for the system to obtain data from the outputs. BES# is used for SRAM bank selection. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram, Figure 2, for further details.

## SRAM Write

The SRAM Write operation of the SST32HF16xC/324C is controlled by WE# and BES#; both have to be low for the system to write to the SRAM. During the Word-Write operation, the addresses and data are referenced to the rising edge of either BES# or WE#, whichever occurs first. The Write time is measured from the last falling edge of BES# or WE# to the first rising edge of BES# or WE#. Refer to the Write cycle timing diagrams, Figures 3 and 4, for further details.

## Product Identification

The Product Identification mode identifies the devices as the SST32HF16xC/324C and manufacturer as SST. **This mode may be accessed by software operations only. The hardware device ID Read operation, which is typically used by programmers, cannot be used on this device because of the shared lines between flash and SRAM in the multi-chip package. Therefore, application of high voltage to pin $A_9$ may damage this device.** Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Tables 4 and 5 for software operation, Figure 13 for the software ID entry and read timing diagram and Figure 19 for the ID entry command sequence flowchart.

**TABLE 2: PRODUCT IDENTIFICATION**

| | Address | Data |
|---|---|---|
| Manufacturer's ID | 0000H | BFH |
| Device ID | | |
| SST32HF162C | 0001H | 234BH |
| SST32HF164C | 0001H | 234BH |
| SST32HF324C | 0001H | 235BH |

T2.0 1267

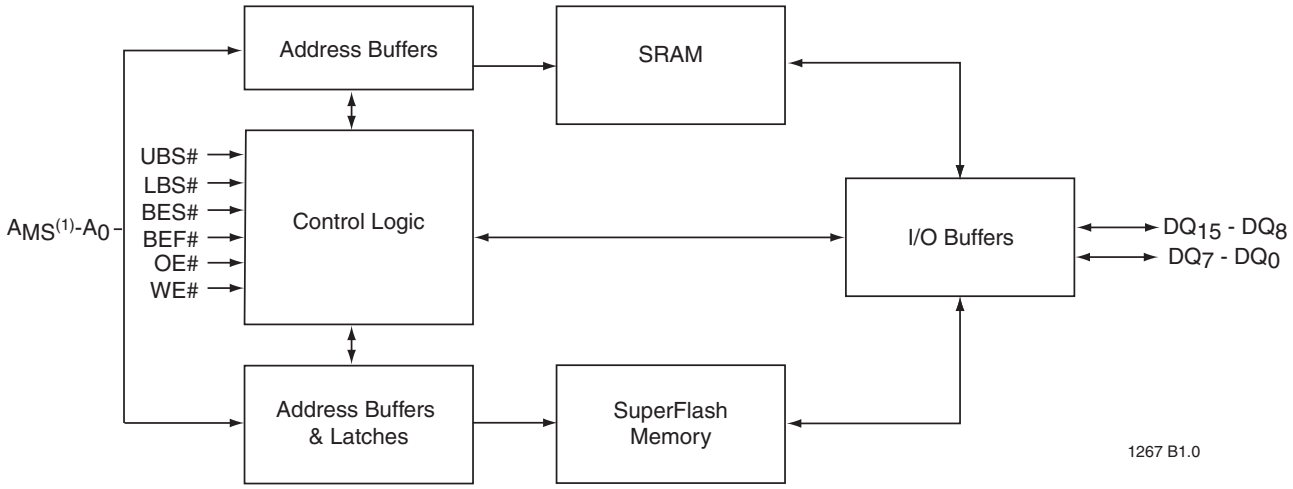
## Product Identification Mode Exit/Reset

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. This command may also be used to reset the device to Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g. not read correctly. See Table 5 for software command codes, Figure 14 for timing waveform and Figure 19 for a flowchart.

## Design Considerations

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between $V_{DD}$ and $V_{SS}$, e.g., less than 1 cm away from the $V_{DD}$ pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from $V_{DD}$ to $V_{SS}$ should be placed within 1 cm of the $V_{DD}$ pin.

**FUNCTIONAL BLOCK DIAGRAM**



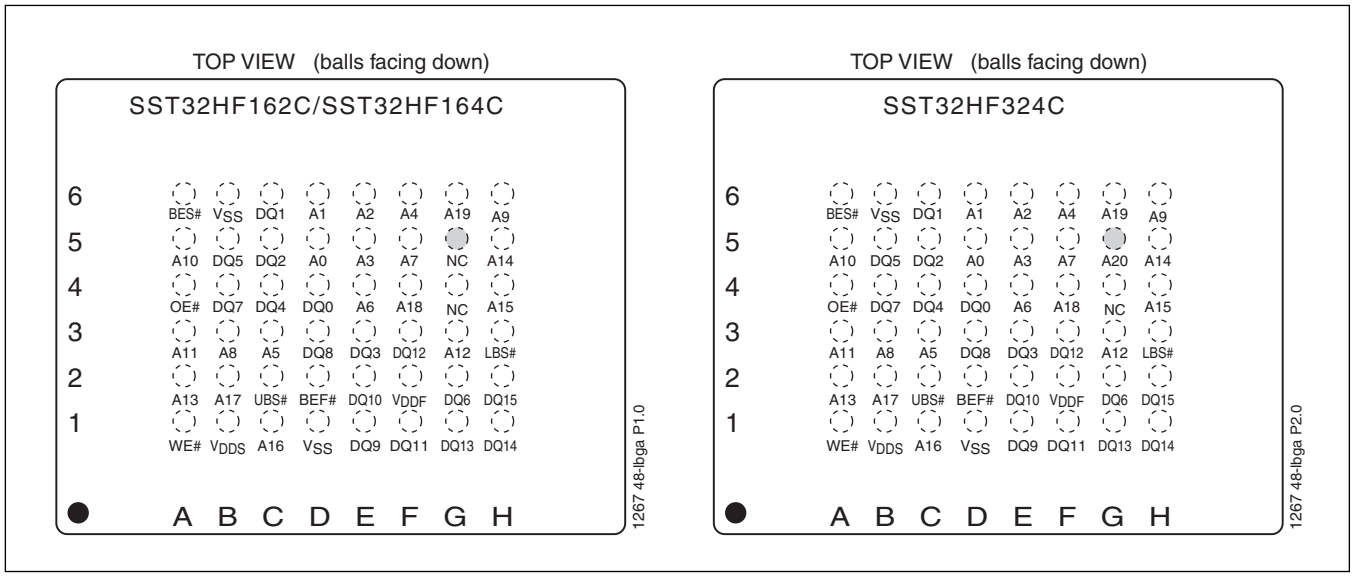



**FIGURE 1: PIN ASSIGNMENTS FOR 48-BALL LBGA (10MM X 12MM)**

**TABLE 3: PIN DESCRIPTION**

| Symbol | Pin Name | Functions |
|---|---|---|
| $A_{MS}$[1]-$A_0$ | Address Inputs | To provide flash addresses: $A_{19}$-$A_0$ for 16M and $A_{20}$-$A_0$ for 32M<br>SRAM addresses: $A_{16}$-$A_0$ for 2M and $A_{17}$-$A_0$ for 4M |
| $DQ_{15}$-$DQ_0$ | Data Input/output | To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE# or BES# and BEF# are high. |
| BES# | SRAM Memory Bank Enable | To activate the SRAM memory bank when BES# is low. |
| BEF# | Flash Memory Bank Enable | To activate the flash memory bank when BEF# is low. |
| OE# | Output Enable | To gate the data output buffers. |
| WE# | Write Enable | To control the Write operations. |
| $V_{DDF}$ | Power Supply (Flash) | 2.7-3.3V Power Supply to flash only. |
| $V_{DDS}$ | Power Supply (SRAM) | 2.7-3.3V Power Supply to SRAM only |
| $V_{SS}$ | Ground | |
| UBS# | Upper Byte Control (SRAM) | To enable $DQ_{15}$-$DQ_8$ |
| LBS# | Lower Byte Control (SRAM) | To enable $DQ_7$-$DQ_0$ |
| NC | No Connection | Unconnected Pins |

T3.0 1267

1. $A_{MS}$=Most significant address

**TABLE 4: OPERATION MODES SELECTION**

| Mode | BES#[1] | BEF#[1] | OE# | WE# | UBS# | LBS# | $DQ_{15}$ to $DQ_8$ | $DQ_7$ to $DQ_0$ | Address |
|---|---|---|---|---|---|---|---|---|---|
| Not Allowed | $V_{IL}$ | $V_{IL}$ | X[2] | X | X | X | X | X | X |
| Flash | | | | | | | | | |
| Read | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | $D_{OUT}$ | $D_{OUT}$ | $A_{IN}$ |
| Program | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | $D_{IN}$ | $D_{IN}$ | $A_{IN}$ |
| Erase | X | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | X | X | Sector or Block address, XXH for Chip-Erase |
| SRAM | | | | | | | | | |
| Read | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $D_{OUT}$ | $D_{OUT}$ | $A_{IN}$ |
| | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | High Z | $A_{IN}$ |
| | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | High Z | $D_{OUT}$ | $A_{IN}$ |
| Write | $V_{IL}$ | $V_{IH}$ | X | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $D_{IN}$ | $D_{IN}$ | $A_{IN}$ |
| | $V_{IL}$ | $V_{IH}$ | X | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{IN}$ | High Z | $A_{IN}$ |
| | $V_{IL}$ | $V_{IH}$ | X | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | High Z | $D_{IN}$ | $A_{IN}$ |
| Standby | $V_{IHC}$ | $V_{IHC}$ | X | X | X | X | High Z | High Z | X |
| Flash Write Inhibit | X | X | $V_{IL}$ | X | X | X | High Z / $D_{OUT}$ | High Z / $D_{OUT}$ | X |
| | X | X | X | $V_{IH}$ | X | X | High Z / $D_{OUT}$ | High Z / $D_{OUT}$ | X |
| | X | $V_{IH}$ | X | X | X | X | High Z / $D_{OUT}$ | High Z / $D_{OUT}$ | X |
| Output Disable | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | X | High Z | High Z | X |
| | $V_{IL}$ | $V_{IH}$ | X | X | $V_{IH}$ | $V_{IH}$ | High Z | High Z | X |
| | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | X | X | High Z | High Z | X |
| Product Identification | | | | | | | | | |
| Software Mode | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | Manufacturer's ID (00BFH) Device ID[3] | | $A_{19}$-$A_1$=$V_{IL}$, $A_0$=$V_{IH}$ (See Table 4) |

T4.0 1267

1. Do not apply BES#=$V_{IL}$ and BEF#=$V_{IL}$ at the same time
2. X can be $V_{IL}$ or $V_{IH}$, but no other value.
3. With $A_{MS}$-$A_1$ = 0; SST Manufacturer's ID = 00BFH, is read with $A_0$=0,
   SST32HF16xC Device ID = 234BH, is read with $A_0$=1,
   SST32HF324C Device ID = 235BH, is read with $A_0$=1

**TABLE 5: SOFTWARE COMMAND SEQUENCE**

| Command Sequence | 1st Bus Write Cycle | | 2nd Bus Write Cycle | | 3rd Bus Write Cycle | | 4th Bus Write Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Addr[1] | Data[2] | Addr[1] | Data[2] | Addr[1] | Data[2] | Addr[1] | Data[2] | Addr[1] | Data[2] | Addr[1] | Data[2] |
| Word-Program | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | WA[3] | Data | | | | |
| Sector-Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | $SA_X$[4] | 30H |
| Block-Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | $BA_X$[4] | 50H |
| Chip-Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| Erase-Suspend | XXXXH | B0H | | | | | | | | | | |
| Erase-Resume | XXXXH | 30H | | | | | | | | | | |
| Software ID Entry[5,6] | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | | | | | | |
| Software ID Exit[7] /Sec ID Exit | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | | | | | | |
| Software ID Exit[7] /Sec ID Exit | XXH | F0H | | | | | | | | | | |

T5.0 1267

1. Address format $A_{14}$-$A_0$ (Hex).
   Addresses $A_{15}$-$A_{19}$ can be $V_{IL}$ or $V_{IH}$, but no other value, for Command sequence for SST32HF16xC,
   Addresses $A_{15}$-$A_{20}$ can be $V_{IL}$ or $V_{IH}$, but no other value, for Command sequence for SST32HF324C.
2. $DQ_{15}$-$DQ_8$ can be $V_{IL}$ or $V_{IH}$, but no other value, for Command sequence
3. WA = Program Word address
4. $SA_X$ for Sector-Erase; uses $A_{MS}$-$A_{11}$ address lines
   $BA_X$, for Block-Erase; uses $A_{MS}$-$A_{15}$ address lines
   $A_{MS}$ = Most significant address
   $A_{MS}$ = $A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C.
5. The device does not remain in Software Product ID Mode if powered down.
6. With $A_{MS}$-$A_1$ =0; SST Manufacturer ID = 00BFH, is read with $A_0$ = 0,
   SST32HF16xC Device ID = 234BH, is read with $A_0$ = 1,
   SST32HF324C Device ID = 235BH, is read with $A_0$ = 1,
   $A_{MS}$ = Most significant address
   $A_{MS}$ = $A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C.
7. Both Software ID Exit operations are equivalent

Preliminary Specifications

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature . . . . . -20°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to $V_{DD}$[1]+0.3V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -1.0V to $V_{DD}$[1]+1.0V
Package Power Dissipation Capability (Ta = 25°C) . . . . . 1.0W
Output Short Circuit Current[2] . . . . . 50 mA

1. $V_{DD} = V_{DDF}$ and $V_{DDS}$
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

**OPERATING RANGE**

| Range | Ambient Temp | $V_{DD}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 2.7-3.3V |
| Extended | -20°C to +85°C | 2.7-3.3V |

**AC CONDITIONS OF TEST**

| | |
|---|---|
| Input Rise/Fall Time | 5 ns |
| Output Load | $C_L$ = 30 pF |
| See Figures 15 and 16 | |

**TABLE 6: DC OPERATING CHARACTERISTICS ($V_{DD}$ = $V_{DDF}$ AND $V_{DDS}$ = 2.7-3.3V)**

| Symbol | Parameter | Limits | | | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | Units | |
| $I_{DD}$ | Active $V_{DD}$ Current | | | | Address input = $V_{ILT}/V_{IHT}$, at f=5 MHz, $V_{DD}=V_{DD}$ Max, all DQs open |
| | Read | | | | OE#=$V_{IL}$, WE#=$V_{IH}$ |
| | Flash | | 18 | mA | BEF#=$V_{IL}$, BES#=$V_{IH}$ |
| | SRAM | | 30 | mA | BEF#=$V_{IH}$, BES#=$V_{IL}$ |
| | Concurrent Operation | | 40 | mA | BEF#=$V_{IH}$, BES#=$V_{IL}$ |
| | Write[1] | | | | WE#=$V_{IL}$ |
| | Flash | | 35 | mA | BEF#=$V_{IL}$, BES#=$V_{IH}$, OE#=$V_{IH}$ |
| | SRAM | | 30 | mA | BEF#=$V_{IH}$, BES#=$V_{IL}$ |
| $I_{SB}$ | Standby $V_{DD}$ Current | | 30 | µA | $V_{DD}$ = $V_{DD}$ Max, BEF#=BES#=$V_{IHC}$ |
| $I_{LI}$ | Input Leakage Current | | 1 | µA | $V_{IN}$=GND to $V_{DD}$, $V_{DD}=V_{DD}$ Max |
| $I_{LO}$ | Output Leakage Current | | 10 | µA | $V_{OUT}$=GND to $V_{DD}$, $V_{DD}=V_{DD}$ Max |
| $V_{IL}$ | Input Low Voltage | | 0.8 | V | $V_{DD}=V_{DD}$ Min |
| $V_{ILC}$ | Input Low Voltage (CMOS) | | 0.3 | V | $V_{DD}=V_{DD}$ Max |
| $V_{IH}$ | Input High Voltage | 0.7 $V_{DD}$ | | V | $V_{DD}=V_{DD}$ Max |
| $V_{IHC}$ | Input High Voltage (CMOS) | $V_{DD}$-0.3 | | V | $V_{DD}=V_{DD}$ Max |
| $V_{OLF}$ | Flash Output Low Voltage | | 0.2 | V | $I_{OL}$=100 µA, $V_{DD}=V_{DD}$ Min |
| $V_{OHF}$ | Flash Output High Voltage | $V_{DD}$-0.2 | | V | $I_{OH}$=-100 µA, $V_{DD}=V_{DD}$ Min |
| $V_{OLS}$ | SRAM Output Low Voltage | | 0.4 | V | IOL =1 mA, $V_{DD}=V_{DD}$ Min |
| $V_{OHS}$ | SRAM Output High Voltage | 2.2 | | V | IOH =-500 µA, $V_{DD}=V_{DD}$ Min |

T6.0 1267

1. $I_{DD}$ active while Erase or Program is in progress.

**TABLE 7: RECOMMENDED SYSTEM POWER-UP TIMINGS**

| Symbol | Parameter | Minimum | Units |
|---|---|---|---|
| $T_{PU-READ}$[1] | Power-up to Read Operation | 100 | µs |
| $T_{PU-WRITE}$[1] | Power-up to Program/Erase Operation | 100 | µs |

T7.0 1267

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 8: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)**

| Parameter | Description | Test Condition | Maximum |
|---|---|---|---|
| $C_{I/O}$[1] | I/O Pin Capacitance | $V_{I/O}$ = 0V | 12 pF |
| $C_{IN}$[1] | Input Capacitance | $V_{IN}$ = 0V | 12 pF |

T8.0 1267

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 9: FLASH RELIABILITY CHARACTERISTICS**

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|---|---|---|---|---|
| $N_{END}$[1] | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| $T_{DR}$[1] | Data Retention | 100 | Years | JEDEC Standard A103 |
| $I_{LTH}$[1] | Latch Up | 100 + $I_{DD}$ | mA | JEDEC Standard 78 |

T9.0 1267

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

## AC CHARACTERISTICS

**TABLE 10: SRAM READ CYCLE TIMING PARAMETERS**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{RCS}$ | Read Cycle Time | 70 | | ns |
| $T_{AAS}$ | Address Access Time | | 70 | ns |
| $T_{BES}$ | Bank Enable Access Time | | 70 | ns |
| $T_{OES}$ | Output Enable Access Time | | 35 | ns |
| $T_{BYES}$ | UBS#, LBS# Access Time | | 70 | ns |
| $T_{BLZS}$[1] | BES# to Active Output | 0 | | ns |
| $T_{OLZS}$[1] | Output Enable to Active Output | 0 | | ns |
| $T_{BYLZS}$[1] | UBS#, LBS# to Active Output | 0 | | ns |
| $T_{BHZS}$[1] | BES# to High-Z Output | | 25 | ns |
| $T_{OHZS}$[1] | Output Disable to High-Z Output | 0 | 25 | ns |
| $T_{BYHZS}$[1] | UBS#, LBS# to High-Z Output | | 35 | ns |
| $T_{OHS}$ | Output Hold from Address Change | 10 | | ns |

T10.0 1267

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 11: SRAM WRITE CYCLE TIMING PARAMETERS**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{WCS}$ | Write Cycle Time | 70 | | ns |
| $T_{BWS}$ | Bank Enable to End-of-Write | 60 | | ns |
| $T_{AWS}$ | Address Valid to End-of-Write | 60 | | ns |
| $T_{ASTS}$ | Address Set-up Time | 0 | | ns |
| $T_{WPS}$ | Write Pulse Width | 60 | | ns |
| $T_{WRS}$ | Write Recovery Time | 0 | | ns |
| $T_{BYWS}$ | UBS#, LBS# to End-of-Write | 60 | | ns |
| $T_{ODWS}$ | Output Disable from WE# Low | | 30 | ns |
| $T_{OEWS}$ | Output Enable from WE# High | 0 | | ns |
| $T_{DSS}$ | Data Set-up Time | 30 | | ns |
| $T_{DHS}$ | Data Hold from Write Time | 0 | | ns |

T11.0 1267

**TABLE 12: FLASH READ CYCLE TIMING PARAMETERS $V_{DD}$ = 2.7-3.6V**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{RC}$ | Read Cycle Time | 70 | | ns |
| $T_{CE}$ | Chip Enable Access Time | | 70 | ns |
| $T_{AA}$ | Address Access Time | | 70 | ns |
| $T_{OE}$ | Output Enable Access Time | | 35 | ns |
| $T_{CLZ}$[1] | BEF# Low to Active Output | 0 | | ns |
| $T_{OLZ}$[1] | OE# Low to Active Output | 0 | | ns |
| $T_{CHZ}$[1] | BEF# High to High-Z Output | | 20 | ns |
| $T_{OHZ}$[1] | OE# High to High-Z Output | | 20 | ns |
| $T_{OH}$[1] | Output Hold from Address Change | 0 | | ns |

T12.0 1267

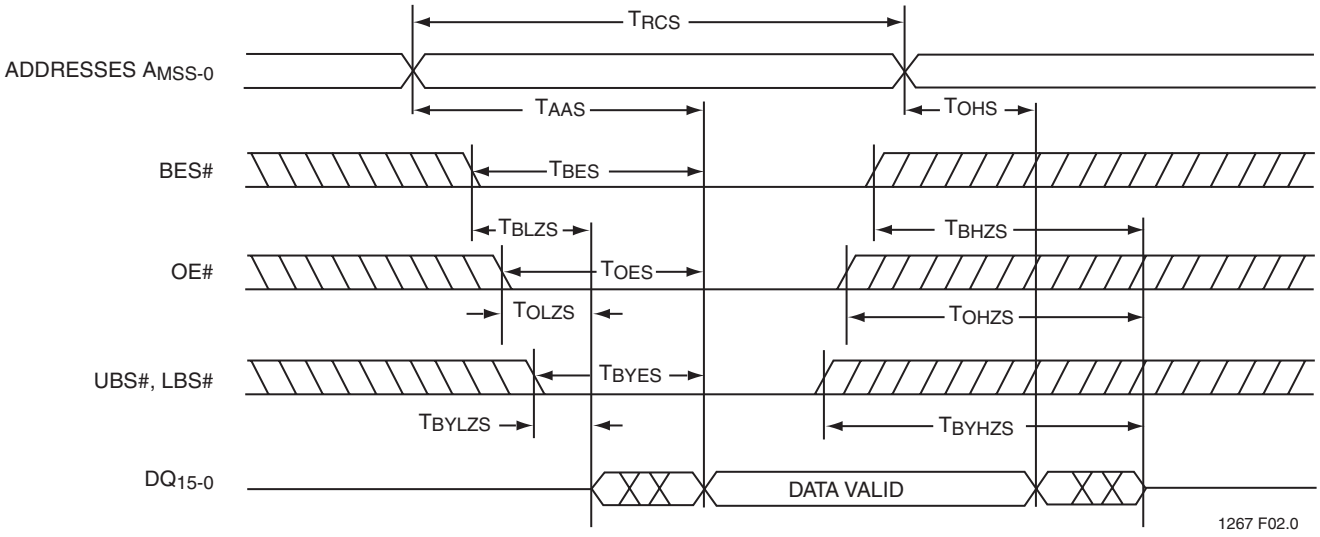
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 13: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{BP}$ | Word-Program Time | | 10 | µs |
| $T_{AS}$ | Address Setup Time | 0 | | ns |
| $T_{AH}$ | Address Hold Time | 30 | | ns |
| $T_{CS}$ | WE# and BEF# Setup Time | 0 | | ns |
| $T_{CH}$ | WE# and BEF# Hold Time | 0 | | ns |
| $T_{OES}$ | OE# High Setup Time | 0 | | ns |
| $T_{OEH}$ | OE# High Hold Time | 10 | | ns |
| $T_{CP}$ | BEF# Pulse Width | 40 | | ns |
| $T_{WP}$ | WE# Pulse Width | 40 | | ns |
| $T_{WPH}$[1] | WE# Pulse Width High | 30 | | ns |
| $T_{CPH}$[1] | BEF# Pulse Width High | 30 | | ns |
| $T_{DS}$ | Data Setup Time | 30 | | ns |
| $T_{DH}$[1] | Data Hold Time | 0 | | ns |
| $T_{IDA}$[1] | Software ID Access and Exit Time | | 150 | ns |
| $T_{SE}$ | Sector-Erase | | 25 | ms |
| $T_{BE}$ | Block-Erase | | 25 | ms |
| $T_{SCE}$ | Chip-Erase | | 50 | ms |

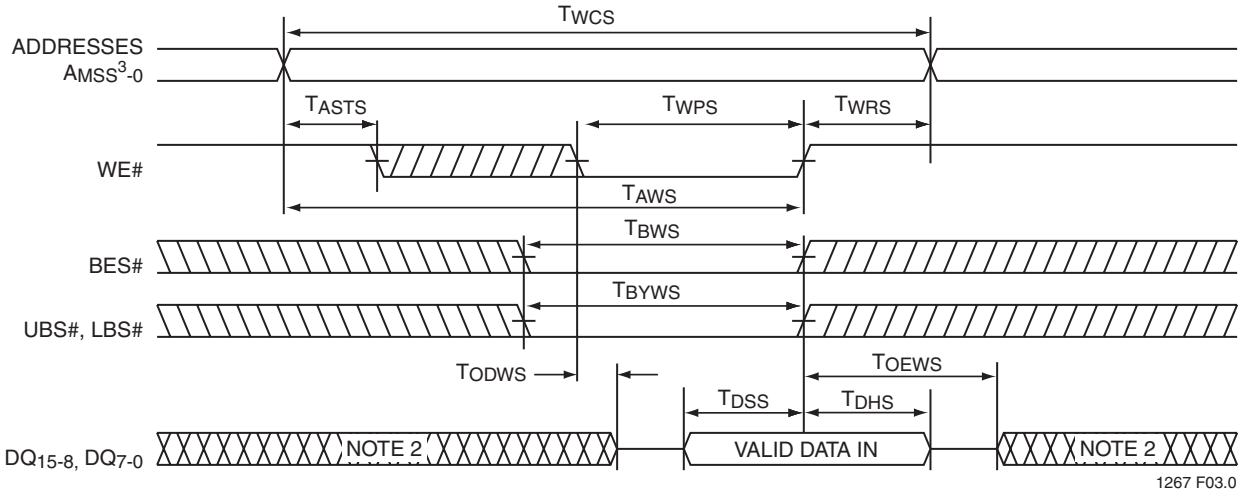
T13.0 1267

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



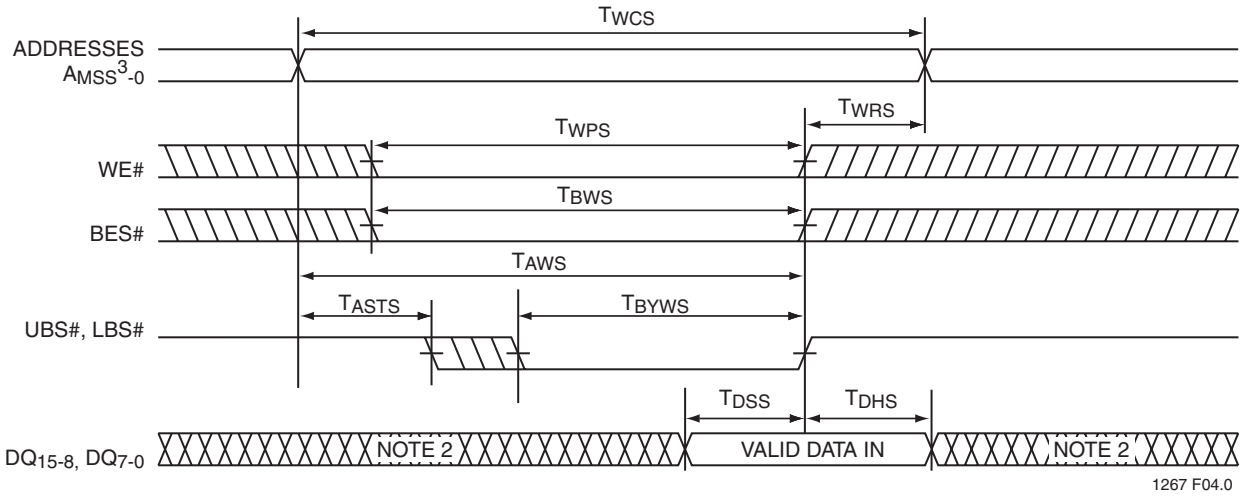

**Note:** $A_{MSS}$ = Most Significant SRAM Address
$A_{MSS}$ = $A_{16}$ for SST32HF162C and $A_{17}$ for SST32HF164C or SST32HF324C

**FIGURE 2: SRAM READ CYCLE TIMING DIAGRAM**



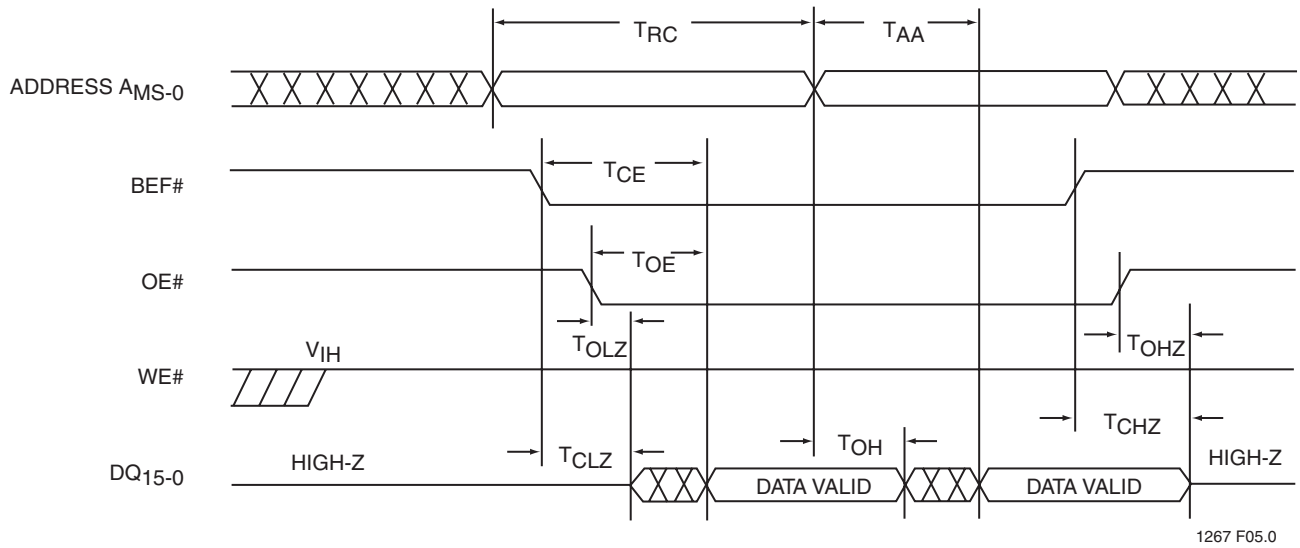

**Note:** 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. If BES# goes Low coincident with or after WE# goes Low, the output will remain at high impedance.
If BES# goes High coincident with or before WE# goes High, the output will remain at high impedance.
Because $D_{IN}$ signals may be in the output state at this time, input signals of reverse polarity must not be applied.
3. $A_{MSS}$ = Most Significant SRAM Address
$A_{MSS}$ = $A_{16}$ for SST32HF162C and $A_{17}$ for SST32HF164C or SST32HF324C

**FIGURE 3: SRAM WRITE CYCLE TIMING DIAGRAM (WE# CONTROLLED)[1]**



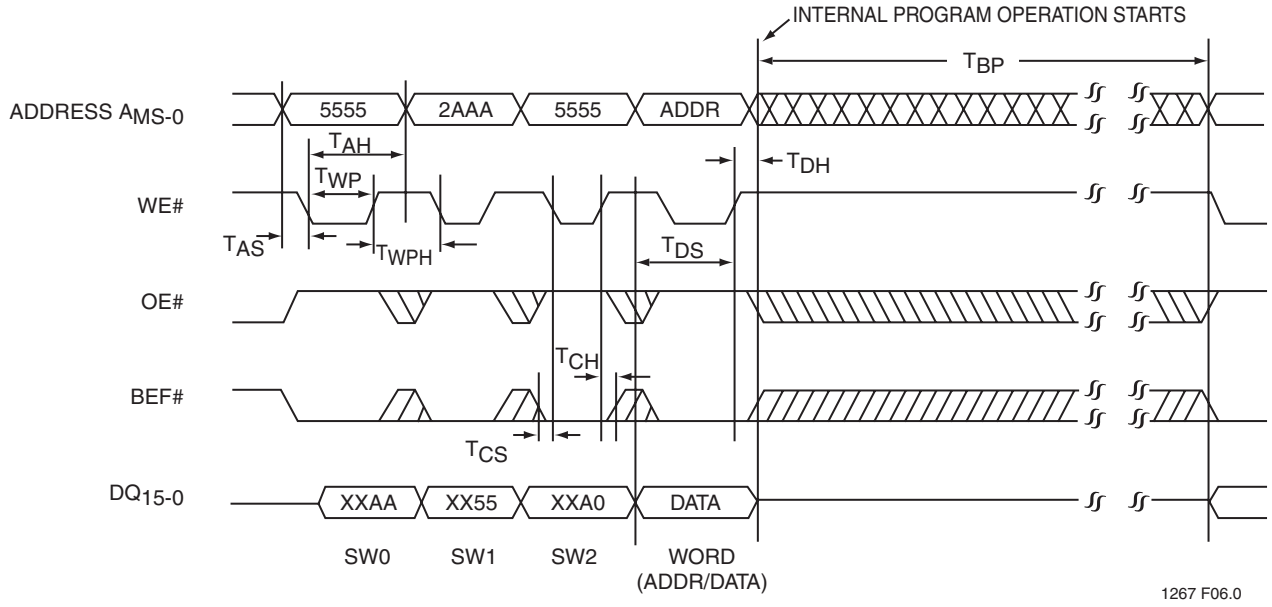

**Note:** 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. Because $D_{IN}$ signals may be in the output state at this time, input signals of reverse polarity must not be applied.
3. $A_{MSS}$ = Most Significant SRAM Address
$A_{MSS} = A_{16}$ for SST32HF162C and $A_{17}$ for SST32HF164C or SST32HF324C

**FIGURE 4: SRAM WRITE CYCLE TIMING DIAGRAM (UBS#, LBS# CONTROLLED)[1]**



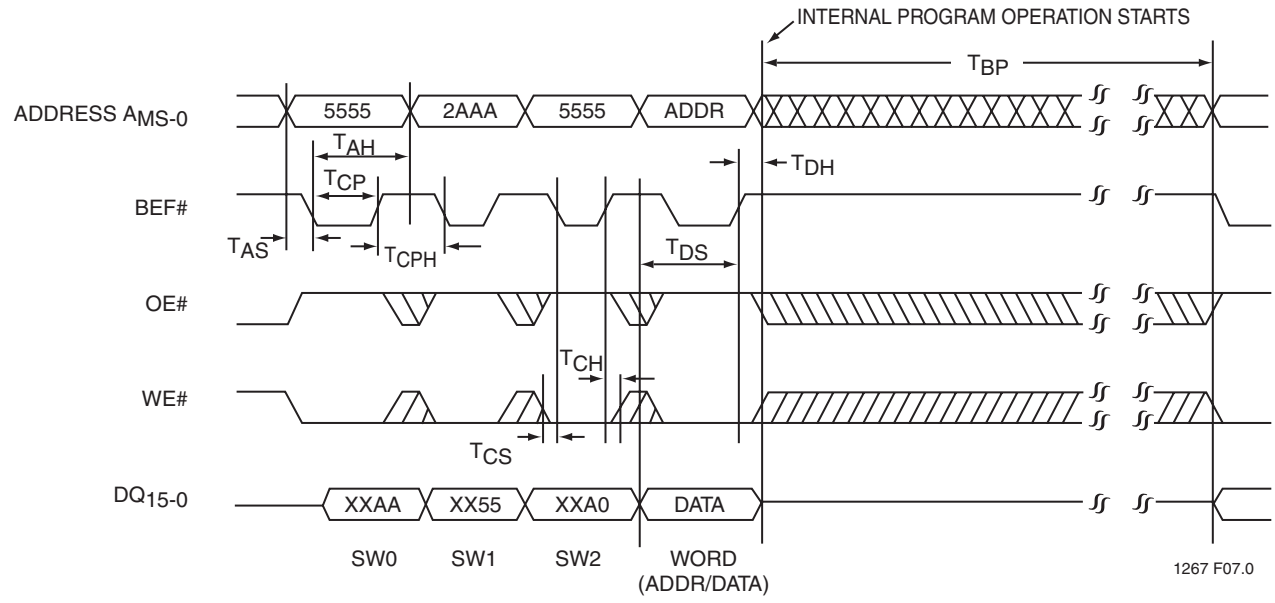

**Note:** $A_{MSF}$ = Most Significant Flash Address
$A_{MSF} = A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C

**FIGURE 5: FLASH READ CYCLE TIMING DIAGRAM**



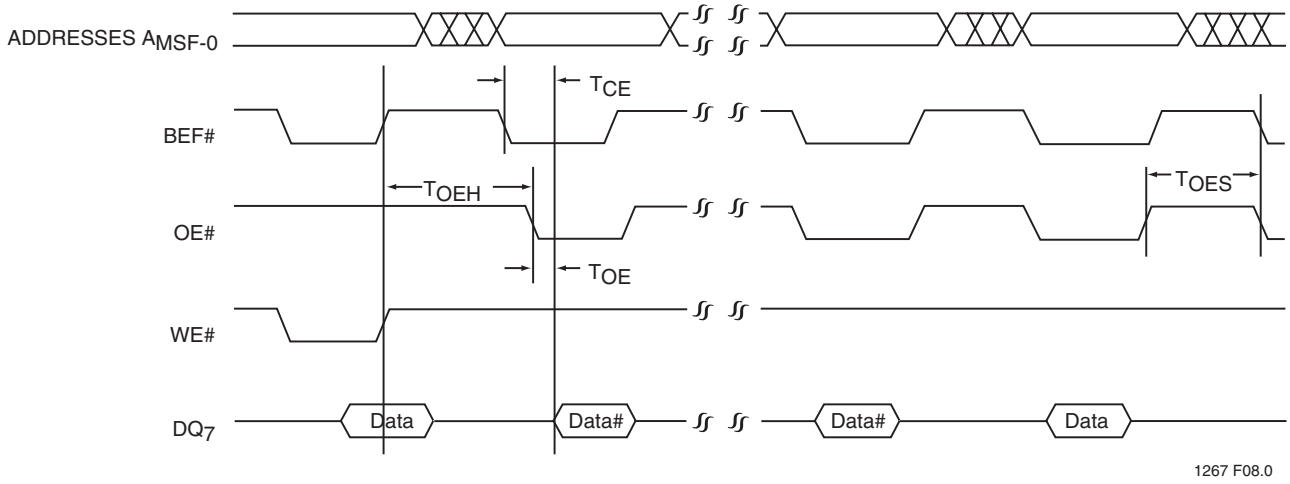

**Note:** $A_{MSF}$ = Most Significant Flash Address
$A_{MSF} = A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C
X can be $V_{IL}$ or $V_{IH}$, but no other value

**FIGURE 6: FLASH WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM**



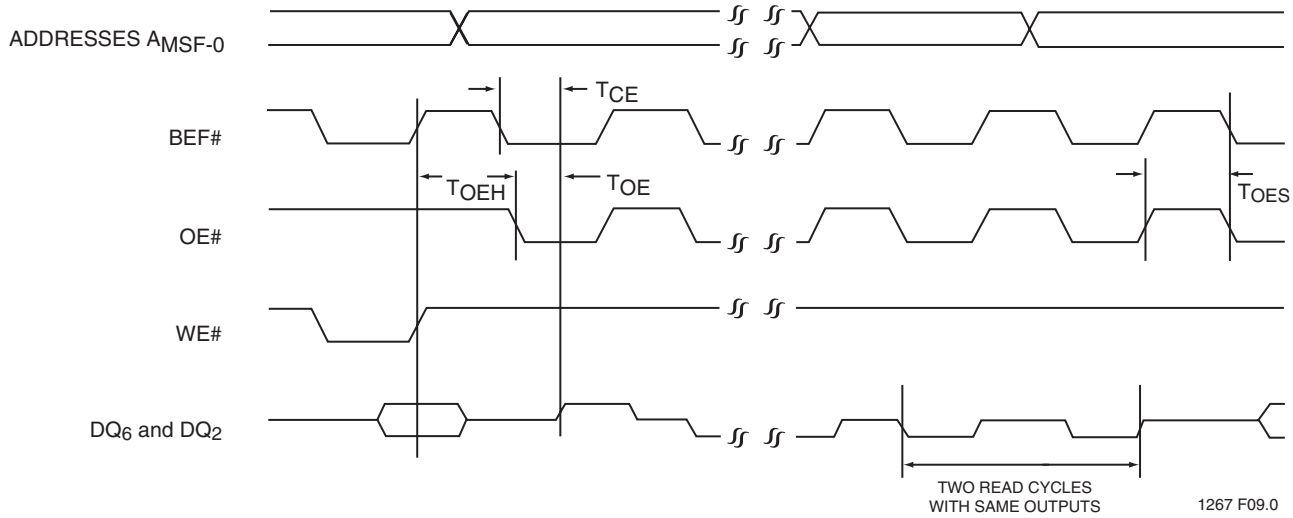

**Note:** $A_{MSF}$ = Most Significant Flash Address
$A_{MSF} = A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C
X can be $V_{IL}$ or $V_{IH}$, but no other value

**FIGURE 7: BEF# CONTROLLED FLASH PROGRAM CYCLE TIMING DIAGRAM**



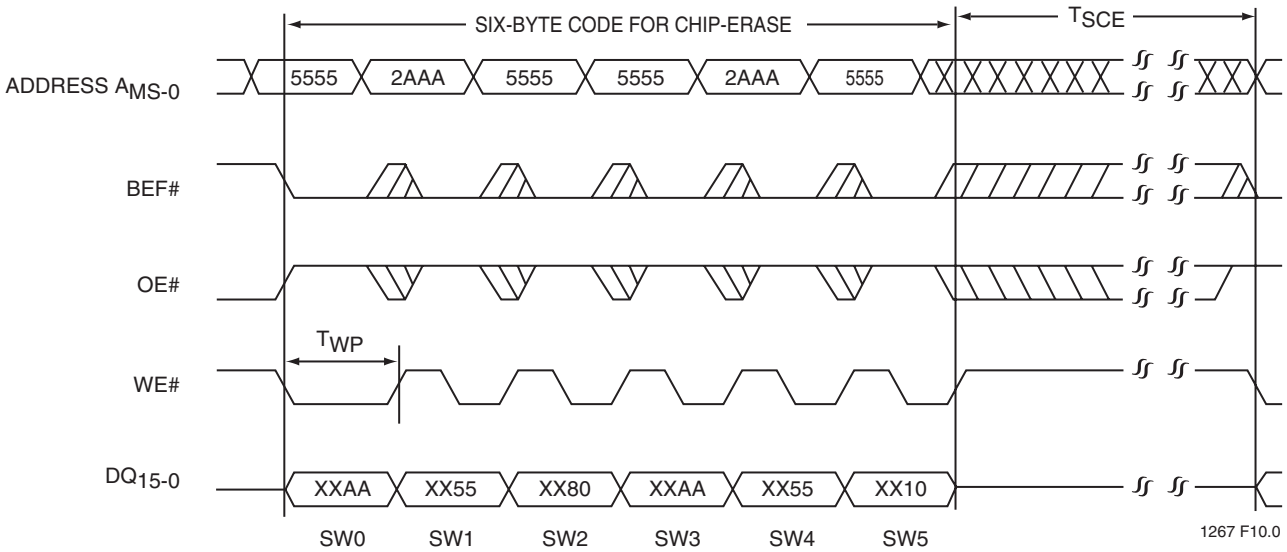

**Note:** $A_{MSF}$ = Most Significant Flash Address
$A_{MSF} = A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C

**FIGURE 8: FLASH DATA# POLLING TIMING DIAGRAM**



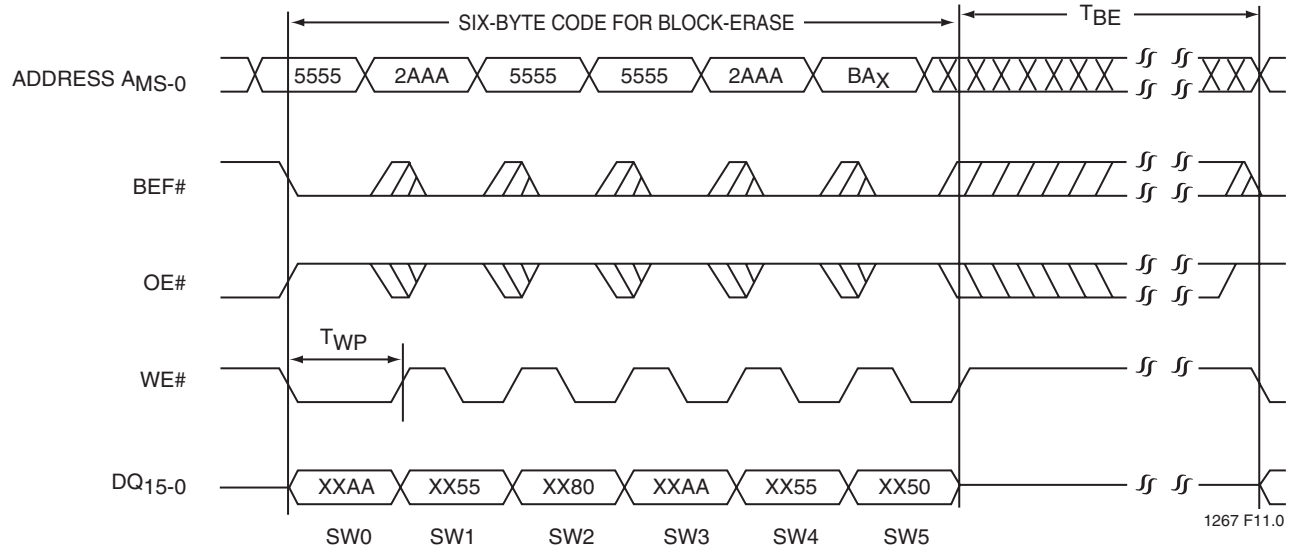

**Note:** $A_{MSF}$ = Most Significant Flash Address
$A_{MSF} = A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C

**FIGURE 9: FLASH TOGGLE BIT TIMING DIAGRAM**



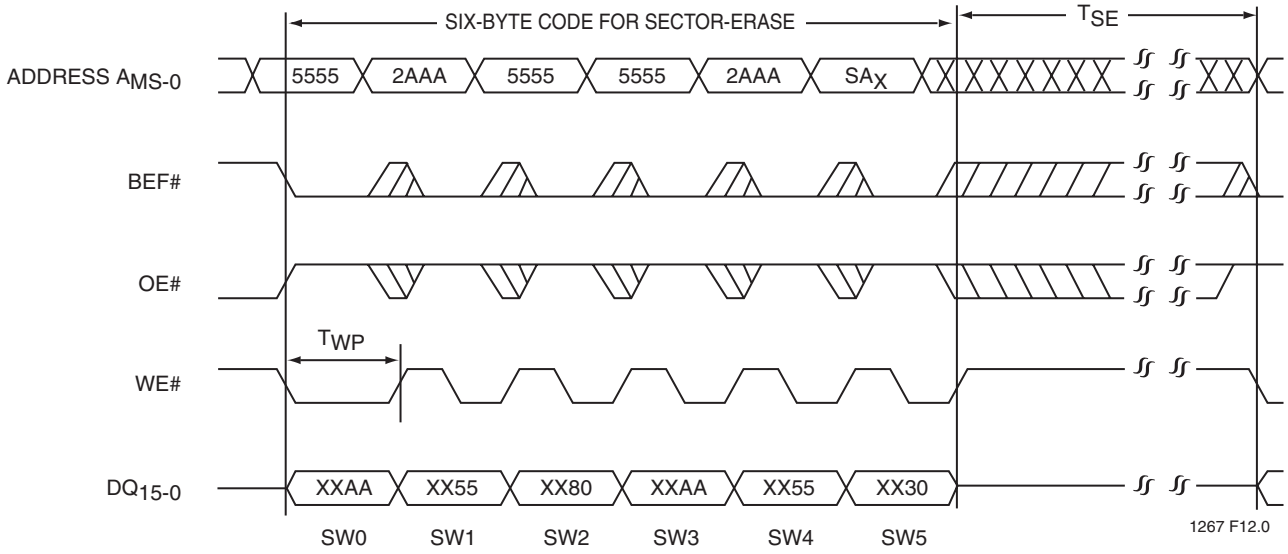

**Note:** This device also supports BEF# controlled Chip-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 13)
$A_{MSF}$ = Most Significant Flash Address
$A_{MSF}$ = $A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C
X can be $V_{IL}$ or $V_{IH,}$ but no other value.

**FIGURE 10: WE# CONTROLLED FLASH CHIP-ERASE TIMING DIAGRAM**



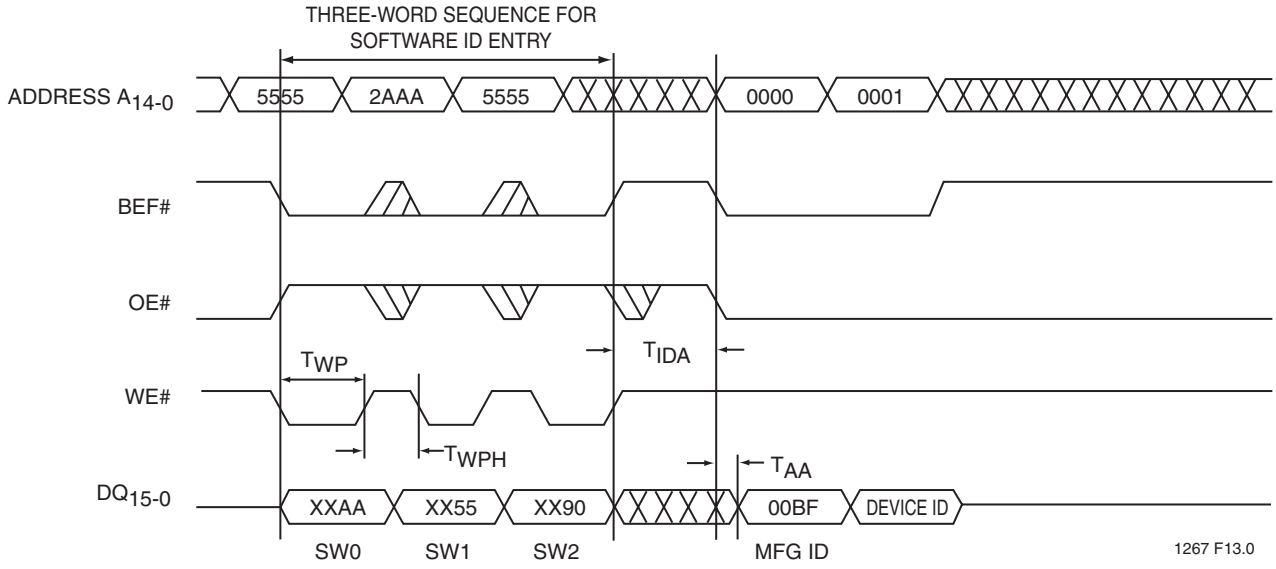

**Note:** $A_{MSF}$ = Most Significant Flash Address
$A_{MSF}$ = $A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C
This device also supports BEF# controlled Block-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 13.)
$BA_X$ = Block Address
X can be $V_{IL}$ or $V_{IH,}$ but no other value.

**FIGURE 11: WE# CONTROLLED FLASH BLOCK-ERASE TIMING DIAGRAM**



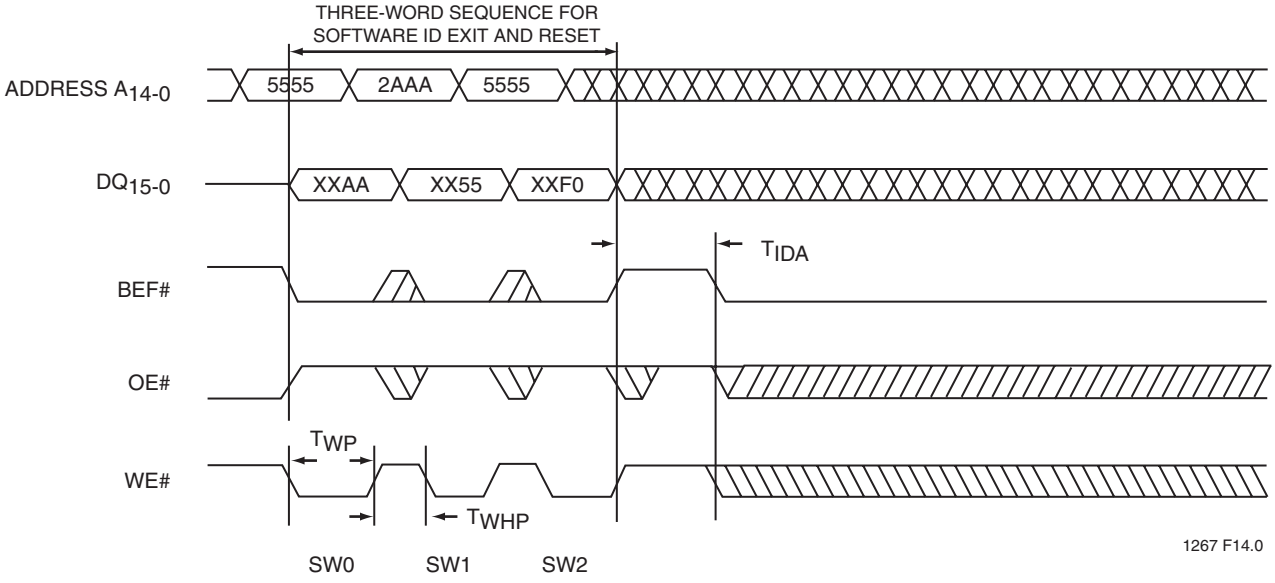

**Note:** $A_{MSF}$ = Most Significant Flash Address
$A_{MSF} = A_{19}$ for SST32HF16xC and $A_{20}$ for SST32HF324C
This device also supports BEF# controlled Sector-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 13.)
$SA_X$ = Sector Address
X can be $V_{IL}$ or $V_{IH}$, but no other value.

**FIGURE 12: WE# CONTROLLED FLASH SECTOR-ERASE TIMING DIAGRAM**



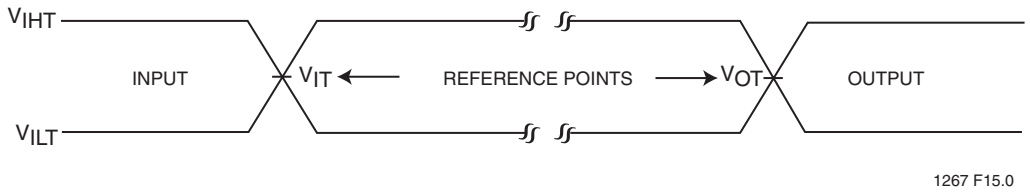

**Note:** X can be $V_{IL}$ or $V_{IH,}$ but no other value.
Device ID - See Table 2 on page 5

**FIGURE 13: SOFTWARE ID ENTRY AND READ**




**Note:** X can be $V_{IL}$ or $V_{IH,}$ but no other value.

**FIGURE 14: SOFTWARE ID EXIT AND RESET**




AC test inputs are driven at $V_{IHT}$ (0.9 $V_{DD}$) for a logic "1" and $V_{ILT}$ (0.1 $V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are $V_{IT}$ (0.5 $V_{DD}$) and $V_{OT}$ (0.5 $V_{DD}$). Input rise and fall times (10% ↔ 90%) are <5 ns.

**Note:** $V_{IT}$ - $V_{INPUT}$ Test
$V_{OT}$ - $V_{OUTPUT}$ Test
$V_{IHT}$ - $V_{INPUT}$ HIGH Test
$V_{ILT}$ - $V_{INPUT}$ LOW Test

**FIGURE 15: AC INPUT/OUTPUT REFERENCE WAVEFORMS**

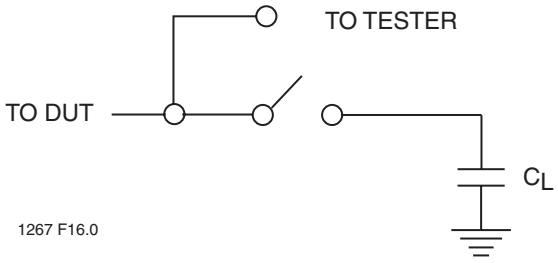



**FIGURE 16: A TEST LOAD EXAMPLE**

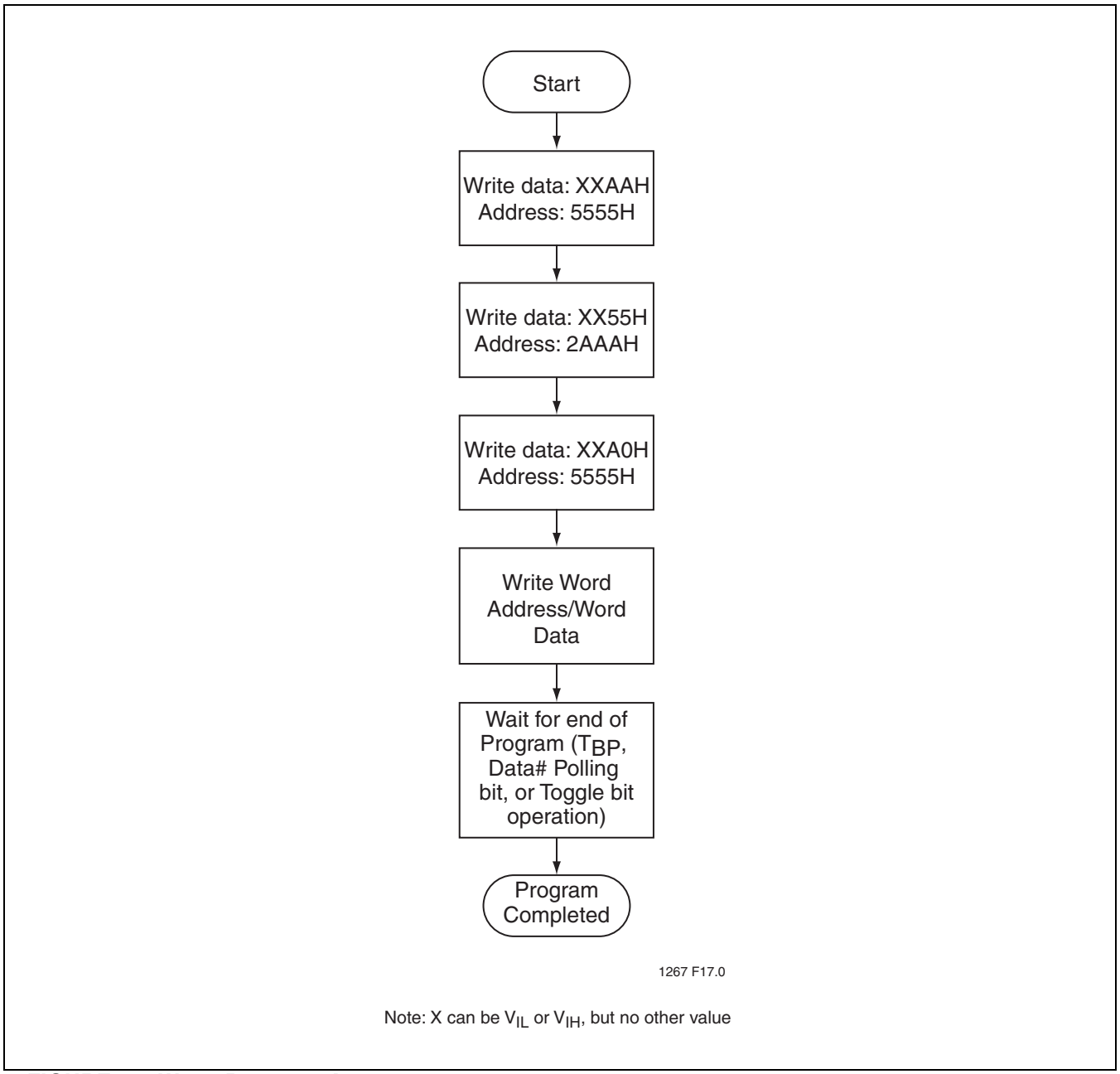



**FIGURE 17: WORD-PROGRAM ALGORITHM**

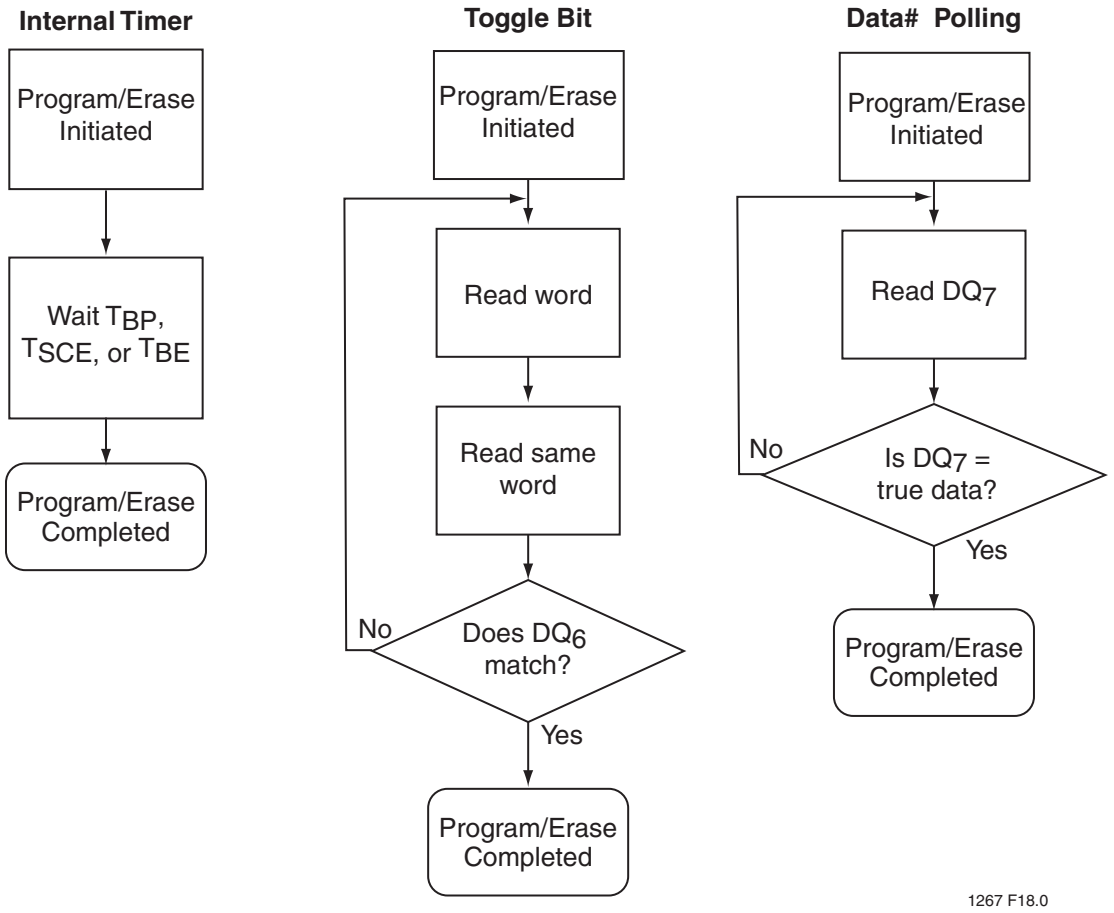



**FIGURE 18: WAIT OPTIONS**

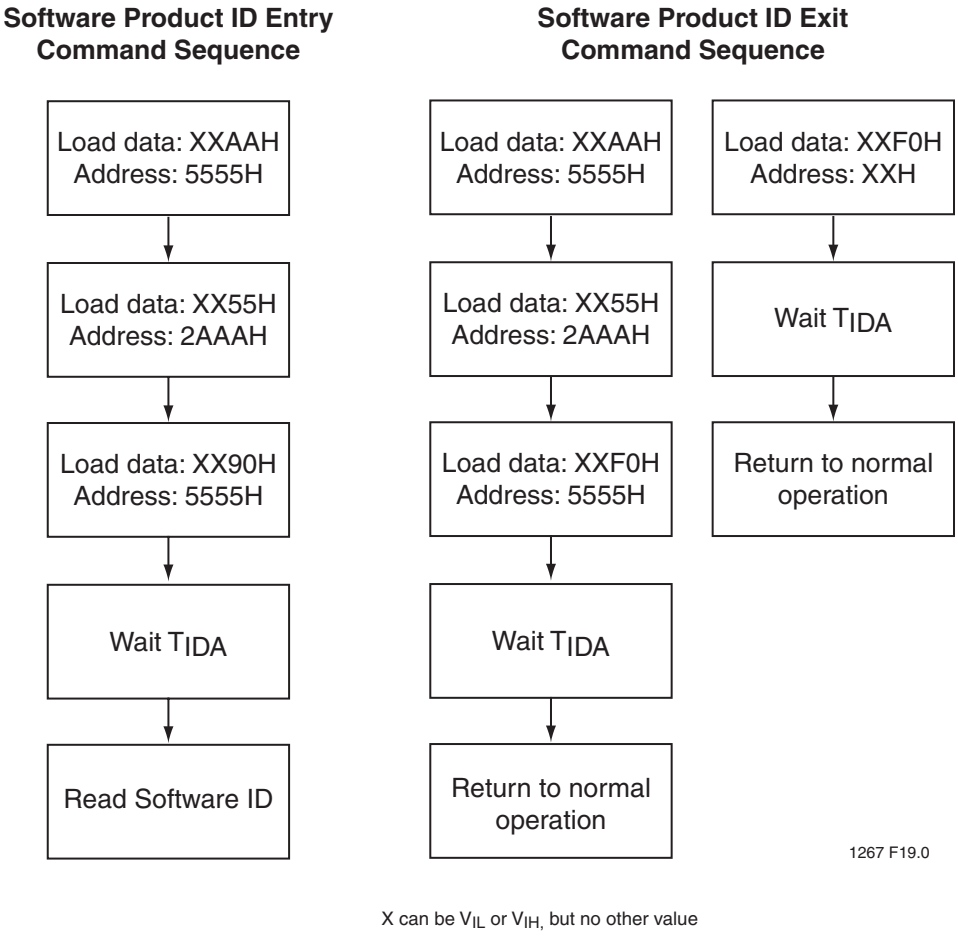
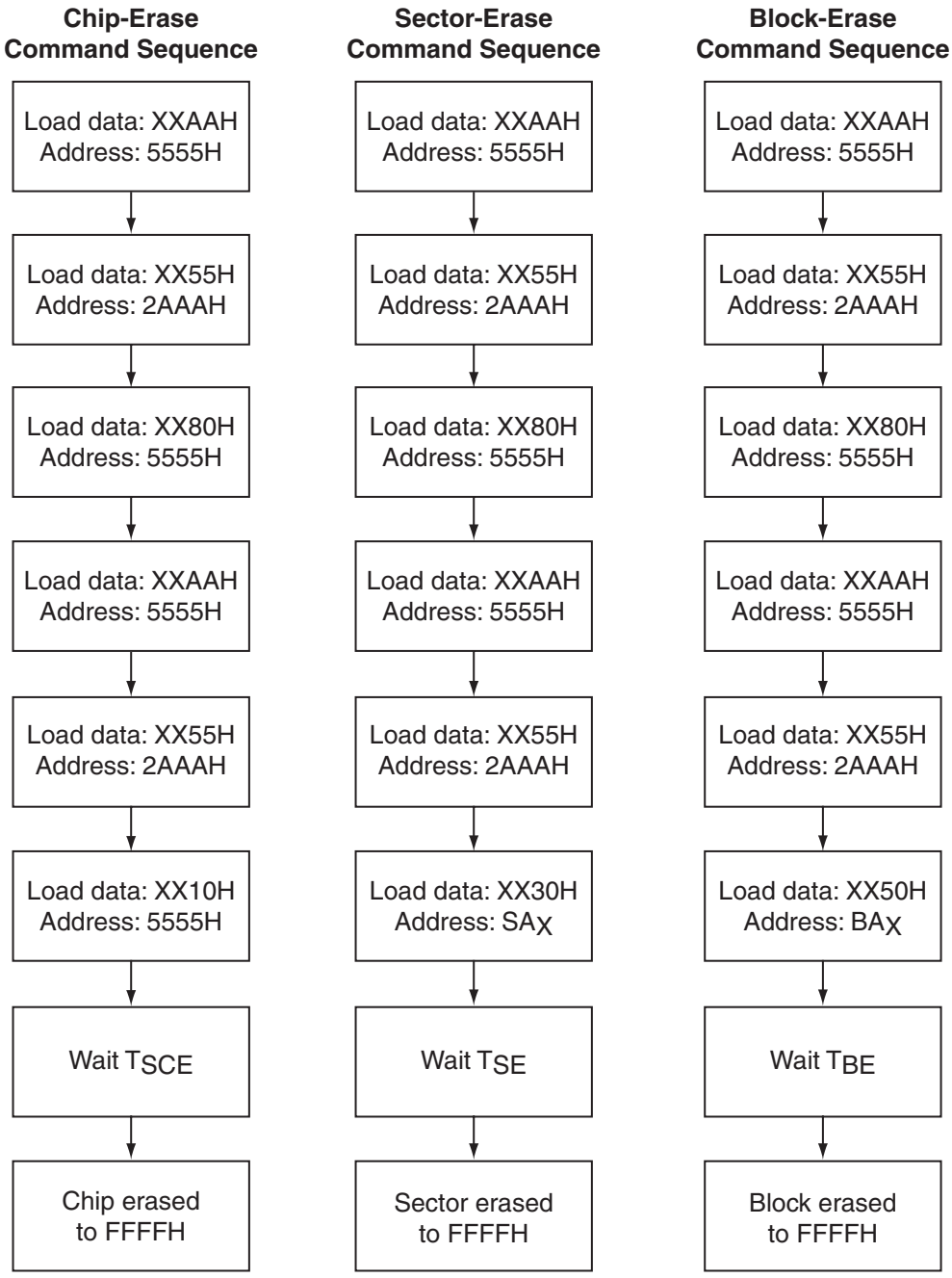



**FIGURE 19: SOFTWARE PRODUCT COMMAND FLOWCHARTS**




Note: X can be $V_{IL}$ or $V_{IH}$, but no other value.

**FIGURE 20: ERASE COMMAND SEQUENCE**

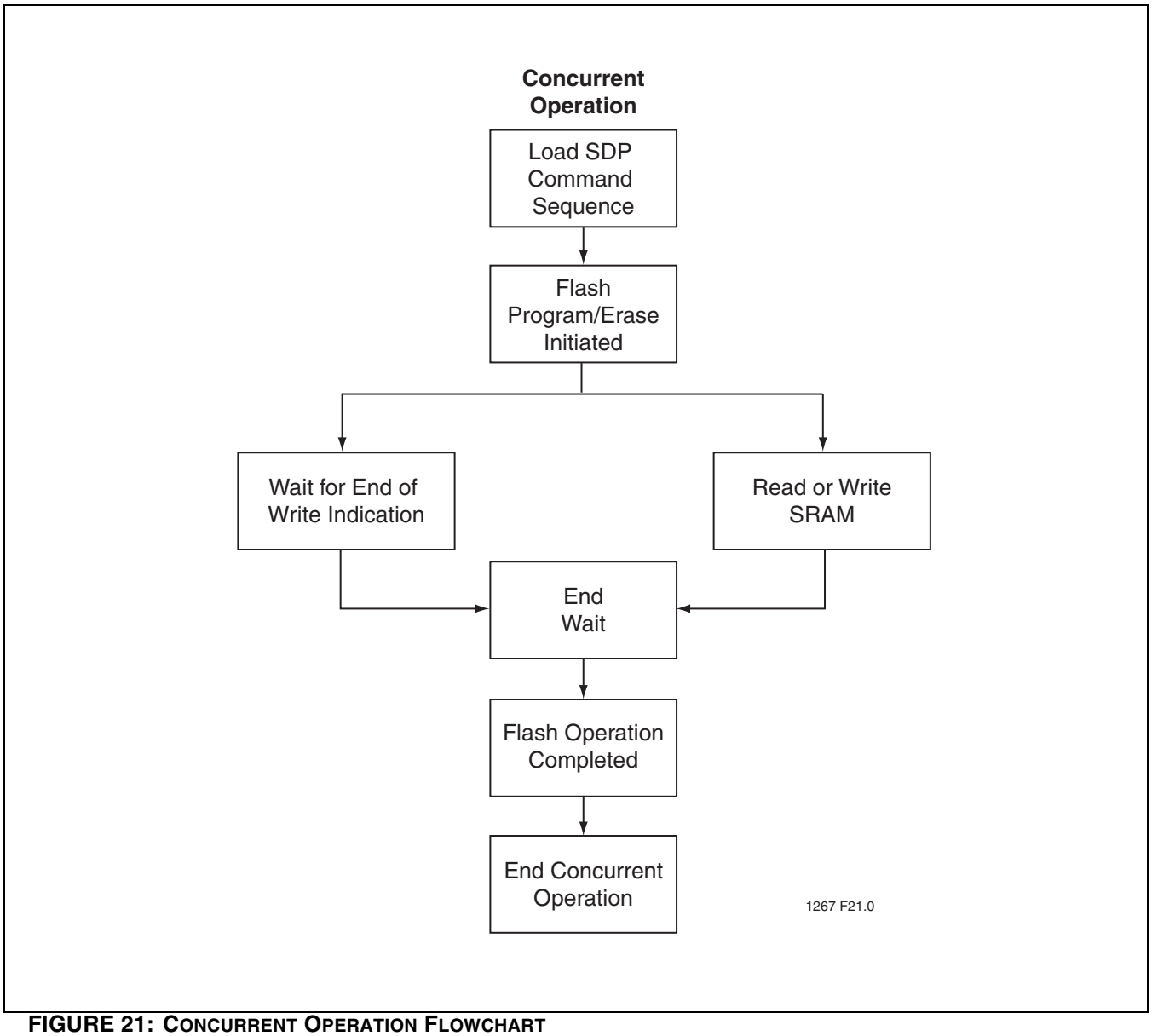
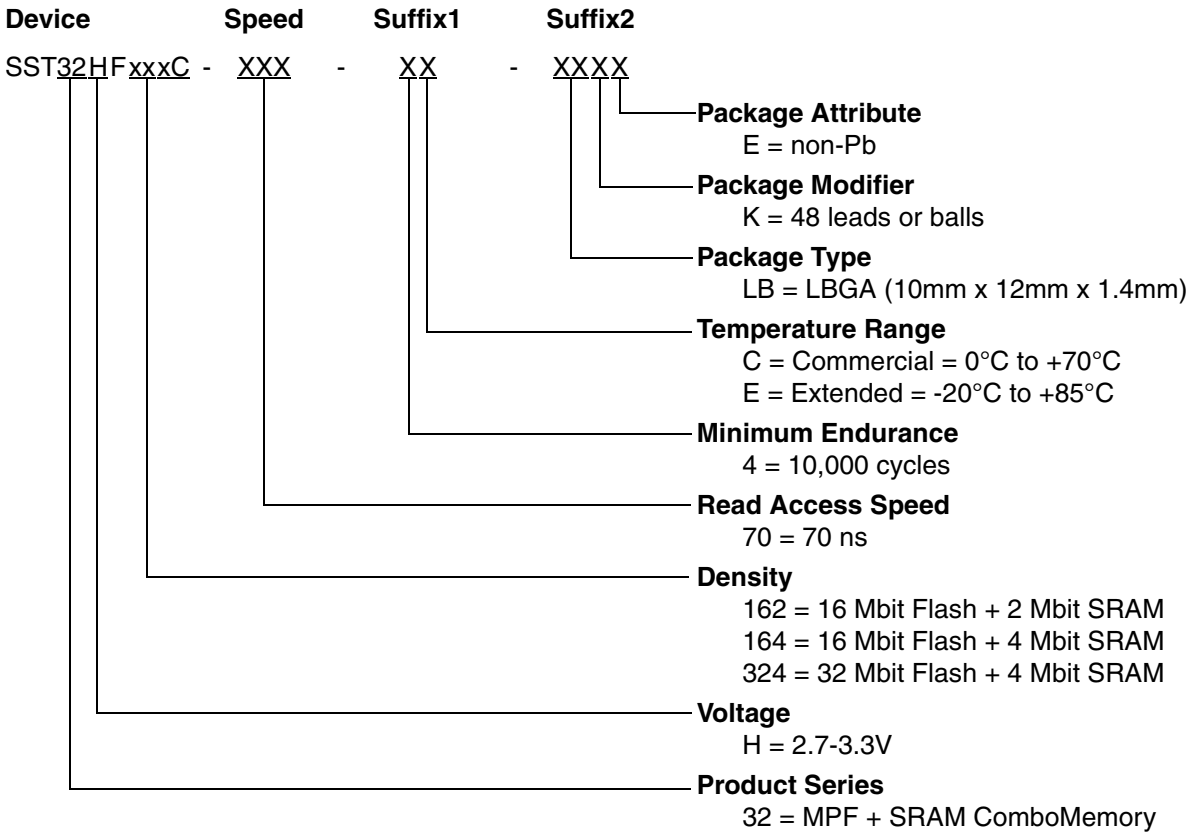



**FIGURE 21: CONCURRENT OPERATION FLOWCHART**

## PRODUCT ORDERING INFORMATION




**Valid combinations for SST32HF162C**

SST32HF162C-70-4C-LBK
SST32HF162C-70-4C-LBKE

SST32HF162C-70-4E-LBK
SST32HF162C-70-4E-LBKE

**Valid combinations for SST32HF164C**

SST32HF164C-70-4C-LBK
SST32HF164C-70-4C-LBKE

SST32HF164C-70-4E-LBK
SST32HF164C-70-4E-LBKE

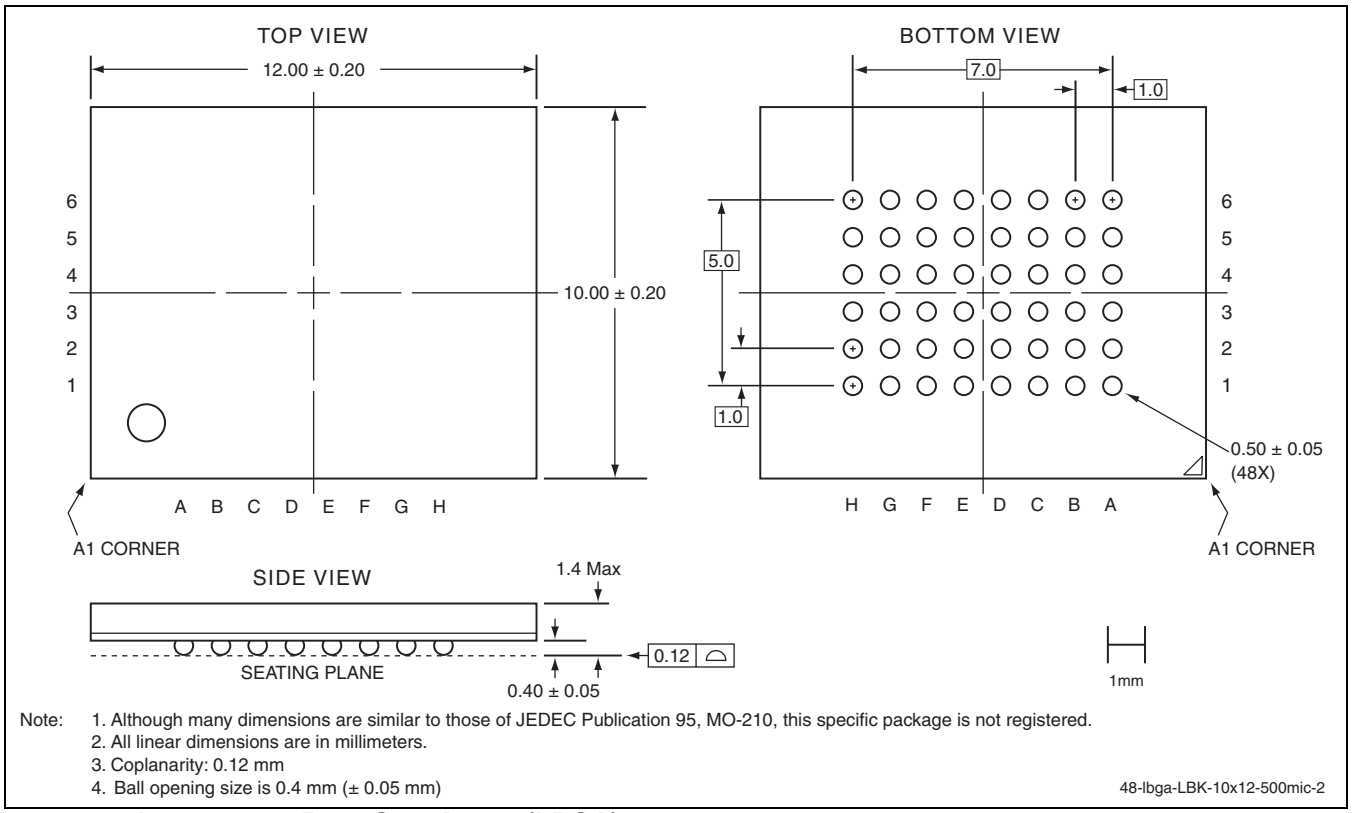
**Valid combinations for SST32HF324C**

SST32HF324C-70-4C-LBK
SST32HF324C-70-4C-LBKE

SST32HF324C-70-4E-LBK
SST32HF324C-70-4E-LBKE

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

## PACKAGING DIAGRAMS




Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.4 mm (± 0.05 mm)

48-lbga-LBK-10x12-500mic-2

**48-BALL LOW-PROFILE BALL GRID ARRAY (LBGA) 10MM X 12MM**
**SST PACKAGE CODE: LBK**

**TABLE 14: REVISION HISTORY**

| Number | Description | Date |
|---|---|---|
| 00 | • Initial Release | Jul 2004 |