

## Description

The  $\mu$ PB8282 and  $\mu$ PB8283 are 8-bit latches with three-state output buffers. The  $\mu$ PB8282 is non-inverting and the  $\mu$ PB8283 inverts the input data. These devices are ideal for demultiplexing the address/data buses on the 8085A/8086 microprocessors. The  $\mu$ PB8282/83 are fabricated using NEC's Schottky bipolar process.

## Features

- ☐ Support  $\mu$ PB8080, 8085A, 8048, 8086 family systems
- ☐ Transparent during active strobe
- ☐ Fully parallel 8-bit data register and buffer
- ☐ High output drive capability (32 mA) for driving the system data bus
- ☐ Three-state outputs

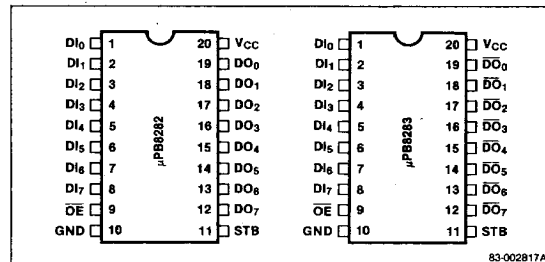
## Ordering Information

Part Number	Package Type	Output Drive Capability
$\mu$ PB8282C	20-pin plastic DIP	32 mA
$\mu$ PB8283C	20-pin plastic DIP	32 mA

## Pin Identification

No.	Symbol	Function
1-8	DI <sub>0</sub> -DI <sub>7</sub>	Data in
9	$\overline{OE}$	Output enable
10	GND	Ground
11	STB	Strobe
12-19	( $\mu$ PB8282) DO <sub>7</sub> -DO <sub>0</sub> ( $\mu$ PB8283) $\overline{DO}$ <sub>7</sub> - $\overline{DO}$ <sub>0</sub>	Data out
20	V <sub>CC</sub>	Power supply

## Pin Configurations



## Pin Functions

### $\overline{OE}$ (Output Enable)

This active low input control signal enables the contents of the data latches onto the data output pins (B<sub>0</sub>-B<sub>7</sub>). When  $\overline{OE}$  goes high, the output buffers become high impedance.

### STB (Strobe)

This input control pulse strobes data at input A<sub>0</sub>-A<sub>7</sub> into the data latches. Data is latched at STB's high to low transition. When active high, STB admits input data.

### DI<sub>0</sub>-DI<sub>7</sub> (Data In)

When data that satisfies the STB strobe setup time requirements is input to these pins, it is latched into the data latches.

### DO<sub>0</sub>-DO<sub>7</sub> ( $\mu$ PB8282) (Data Out) $\overline{DO}$ <sub>0</sub>- $\overline{DO}$ <sub>7</sub> ( $\mu$ PB8283)

When  $\overline{OE}$  is active (low), it outputs data to the DO<sub>0</sub>-DO<sub>7</sub> pins. When  $\overline{OE}$  is inactive high, DO<sub>0</sub>-DO<sub>7</sub> are high impedance. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

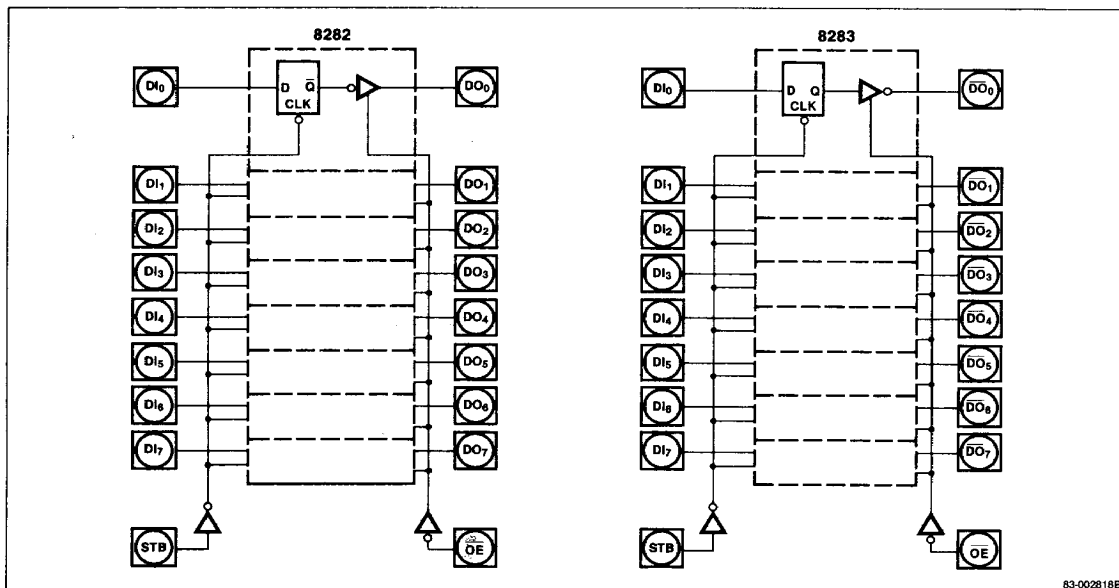
### GND (Ground)

This is the ground.

### V<sub>CC</sub> (Power Supply)

This is the +5 V power supply.

## Block Diagrams



## Functional Description

The μPB8282/83 are 8-bit latches with three-state output buffers. Data on the inputs is latched into the data latches on a high-to-low transition of the STB line. When STB is high, the latches appear transparent. The  $\overline{OE}$  input enables the latched data to be transferred to the output pins. When  $\overline{OE}$  is high, the outputs are put in the three-state condition.  $\overline{OE}$  will not cause transients to appear on the data outputs.

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$

Operating temperature	$0^\circ\text{C}$ to $+70^\circ\text{C}$
Storage temperature	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
All output and supply voltages	$-0.5$ to $+7$ V
All input voltages	$-1.0$ V to $5.5$ V

**Comment:** Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +5\text{ V} \pm 10\%$

Parameter	Symbol	Limits		Unit	Test Conditions
		Min	Max		
Input clamp voltage	$V_C$		-1	V	$I_C = -5\text{ mA}$
Power supply current	$I_{CC}$		160	mA	
Forward input current	$I_F$		-0.2	mA	$V_F = 0.45\text{ V}$
Reverse input current	$I_R$		50	$\mu\text{A}$	$V_R = 5.25\text{ V}$
Output low voltage	$V_{OL}$		0.45	V	$I_{OL} = 32\text{ mA}$
Output high voltage	$V_{OH}$	2.4		V	$I_{OH} = -5\text{ mA}$
Output off current	$I_{OFF}$		$\pm 50$	$\mu\text{A}$	$V_{OFF} = 0.45$ to $5.25\text{ V}$
Input low voltage	$V_{IL}$		0.8	V	$V_{CC} = 5.0\text{ V}$ (1)
Input high voltage	$V_{IH}$	2.0		V	$V_{CC} = 5.0\text{ V}$ (1)
Input capacitance	$C_{IN}$		12	pF	$V_{BIAS} = 2.5\text{ V}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , $F = 1\text{ MHz}$

### Note:

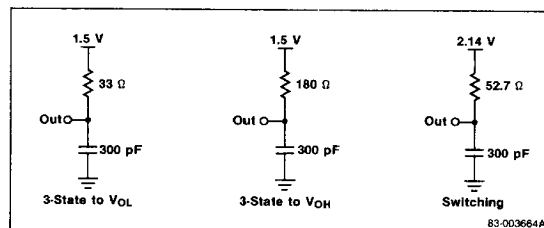
(1) Output loading  $I_{OL} = 32\text{ mA}$ ,  $I_{OH} = -5\text{ mA}$ ,  $C_L = 300\text{ pF}$

## AC Characteristics

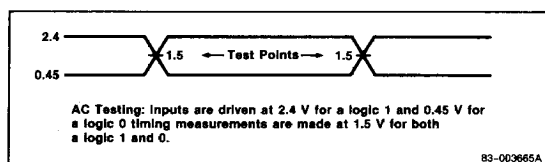
$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$   
 $I_{OL} = 32\text{ mA}$ ,  $I_{OH} = -5\text{ mA}$ ,  $C_L = 300\text{ pF}$

Parameter	Symbol	Limits		Unit
		Min	Max	
Input to output delay	$t_{IVOV}$			
— Inverting		5	22	ns
— Non-inverting		5	30	ns
STB to output delay	$t_{SHOV}$			
— Inverting		10	40	ns
— Non-inverting		10	45	ns
Output disable time	$t_{EHOZ}$	5	22	ns
Output enable time	$t_{ELOV}$	10	30	ns
Input to STB setup time	$t_{IVSL}$	0		ns
Input to STB hold time	$t_{SLIX}$	25		ns
STB high time	$t_{SHSL}$	15		ns
Input, output rise time	$t_{ILIH}$ , $t_{OLOH}$		20	ns
Input, output fall time	$t_{IHIL}$ , $t_{OHOL}$		12	ns

## Load Circuits



## AC Test Points



## Timing Waveform

