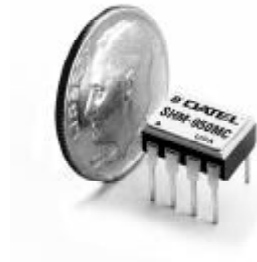


FEATURES

- 18-Bit accuracy
- Small 8-pin DIP package
- 800ns max. acquisition time to $\pm 0.001\%$
- 200ns max. sample-to-hold settling time to $\pm 0.001\%$
- 16MHz small signal bandwidth
- 90dB feedthrough attenuation
- ± 25 picoseconds aperture uncertainty
- 415mW maximum power dissipation



GENERAL DESCRIPTION

DATEL's SHM-950 is a high-speed, highly accurate sample/hold designed for precision, high-speed analog signal processing applications. The SHM-950 features excellent dynamic specifications including a maximum acquisition time of only 800 nanoseconds for a 10V step to $\pm 0.001\%$.

Sample-to-hold settling time, to $\pm 0.001\%$ accuracy, is 200 nanoseconds maximum with an aperture uncertainty of ± 25 picoseconds.

The SHM-950 is a complete sample/hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, a FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+5V SUPPLY
2	S/ \bar{H} CONTROL
3	ANALOG INPUT
4	ANALOG RETURN
5	-15V SUPPLY
6	ANALOG OUTPUT
7	+15V SUPPLY
8	POWER GROUND

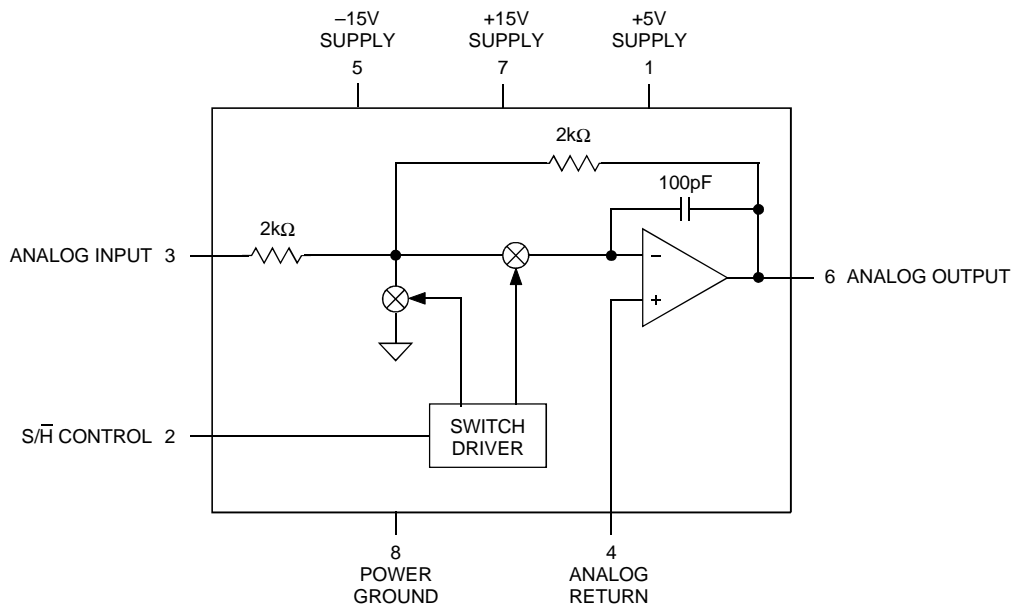


Figure 1. SHM-950 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

±15V Supply Voltage	±18V
+5V Supply Voltage	-0.5V to +7V
Analog Input	±18V
Digital Input	-0.5V to +5.5V
Output Current	±65 mA

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range with ±15V and +5V supplies unless otherwise specified.)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range				
±15V Nominal Supplies	±10	±11.5	—	Volts
±12V Nominal Supplies	±7	±8.5	—	Volts
Input Impedance	1.75	2	—	kΩ
Output Current	—	—	±40	mA
Output Impedance	—	0.1	—	Ω
Capacitive Load	100	250	—	pF
DIGITAL INPUT				
Input Logic Levels				
Logic 1	+2.0	—	+5.0	Volts
Logic 0	0	—	+0.8	Volts
Loading				
Logic 1	—	—	+5	μA
Logic 0	—	—	-5	μA
TRANSFER CHARACTERISTICS				
Gain	—	-1	—	V/V
Gain Error, +25°C	—	±0.05	±0.5	%
Linearity Error ①	—	±0.001	±0.005	%FS
Sample Mode Offset, +25°C	—	±2	±7	mV
Sample-to-Hold Offset (Pedestal), +25°C ②	—	±2.5	±25	mV
Gain Drift	—	±0.5	±15	ppm/°C
Sample Mode Offset Drift ①	—	±3	±15	ppm of FSR/°C
Sample-to-Hold Off. (Pedestal) Drift	—	±5	±20	ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time				
10V to ±0.001%FS (±0.1mV)				
+25°C	—	160	800	ns
-55 to +125°C	—	—	900	ns
10V to ±0.1%FS (±10 mV)				
+25°C	—	100	400	ns
-55 to +125°C	—	—	450	ns
10V to ±1%FS (±100 mV)	—	200	—	ns
1V to ±1%FS (±10 mV)	—	200	—	ns
Sample-to-Hold Settling Time				
10V to ±0.01%FS (±1 mV)	—	100	150	ns
10V to ±0.1%FS (±10 mV)	—	100	120	ns
Sample-to-Hold Transient	—	100	—	mVp-p
Aperture Delay Time	—	10	15	ns
Aperture Uncertainty (Jitter)	—	±25	±50	ps
Output Slew Rate	±40	60	—	V/μs
Output Droop				
+25°C	—	±0.5	±15	μV/μs
0 to +70°C	—	±15	±30	μV/μs
-55 to +125°C	—	±1.2	±2.4	mV/μs
Feedthrough Rejection	—	-84	-78	dB

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Voltage Range				
+15V Supply	+11.5	+15.0	+15.5	Volts
-15V Supply	-11.5	-15.0	-15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Power Supply Rejection Ratio	—	±0.5	±1	mV/V
Quiescent Current Drain				
+15V Supply	—	+8	+13.5	mA
-15V Supply	—	-8	-13.5	mA
+5V Supply	—	+1	+1.5	mA
Power Consumption	—	365	415	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
SHM-950MC	0 to +70°C			
SHM-950MM	-55 to +125°C			
Storage Temperature Range				
-65 to +150°C				
Thermal Impedance				
θ _{jc}	15°C/W			
θ _{ca}	35°C/W			
Package Type	8-pin ceramic DIP			

Footnotes:

① Full Scale (FS) = 10V. Full Scale Range (FSR) = 20V.

② Sample-to-hold offset error (pedestal) is constant regardless of input/output level.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
SHM-950MC	0 to +70°C
SHM-950MM	-55 to +125°C
For availability of high-reliability versions of the SHM-950, contact DATEL.	

TECHNICAL NOTES

- All ground pins should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder ground pins directly to it. Take care to ensure that no ground potentials can exist between ground pins.
- External 0.1μF to 1μF tantalum bypass capacitors are required in critical applications.
- A logic 1 on S/H puts the unit in the sample mode. A logic 0 puts the unit in hold mode.
- The maximum capacitive load to avoid oscillation is typically 250pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50pF. Greater load capacitances will affect both acquisition and settling time.
- Gain and offset adjusting can be accomplished using the external circuitry shown in Figure 2. Adjust offset with a 0V input. Adjust gain with a ±FS input. Adjust so that the output in the hold mode matches the input.

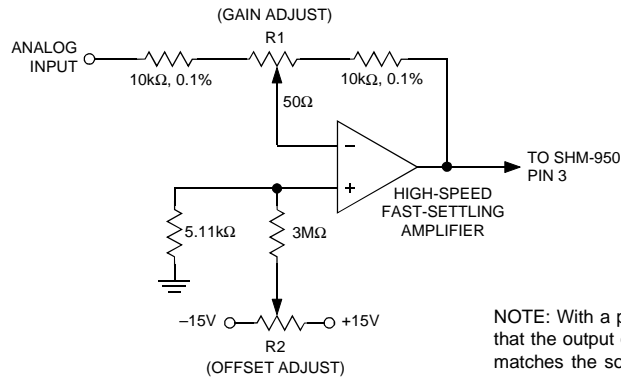


Figure 2. Offset and Gain Adjustments

MECHANICAL DIMENSIONS
INCHES (mm)

