

NCS2003, NCV2003

Low Voltage, Rail-to-Rail Output Operational Amplifier

The NCS2003/NCV2003 is a low voltage operational amplifier with rail-to-rail output drive capability. The 1.8 V operation allows high performance operation in low voltage, low power applications.

Additional features include no output phase reversal with overdriven inputs, a low input offset voltage of 0.5 mV, ultra low input bias current of 1 pA, and a unity gain bandwidth of 5 MHz at 1.8 V. The tiny NCS2003 is the ideal solution for small portable electronic applications and is available in the space saving SOT23-5 and SOT-553 packages. The NCV2003 is available in SOT23-5 and is AEC-Q100 Qualified and PPAP Capable.

Features

- 7 MHz Unity Gain Bandwidth at 5 V
- 5 MHz Unity Gain Bandwidth at 1.8 V
- Rail-to-Rail Output
- No Output Phase Reversal for Over-Driven Input Signals
- Low Offset Voltage – 500 μ V typical
- Low Input Bias Current – 1 pA typical
- Space saving SOT23-5 and SOT553-5 Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Cellular Telephones
- Current Shunt Monitors for battery monitoring
- Pulse Oximetry Signal Conditioning
- Blood Pressure Monitor Conditioning and Filtering
- Hard Drive Sensor Buffer

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.



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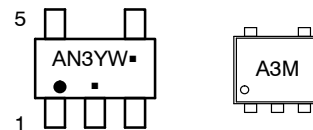


SOT23-5
CASE 483-02
(NCS/NCV2003)



SOT553, 5 LEAD
CASE 463B
(NCS2003)

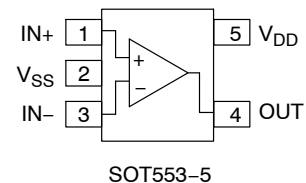
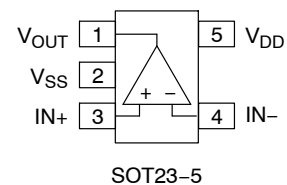
MARKING DIAGRAMS



AN3 = NCS/NCV2003SN2T1G
A3 = NCS2003XV53T2G
Y = Year
W = Work Week
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NCS2003, NCV2003

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature, unless otherwise stated

Parameter	Symbol	Limit	Unit
Supply Voltage ($V_{DD} - V_{SS}$)	V_S	7	V

INPUT AND OUTPUT PINS

Input Voltage (Note 1)	V_{IN}	$V_{SS} - 300 \text{ mV}$ to 7.0 V	V
Input Current	I_{IN}	10	mA
Output Short Circuit Current (Note 2)	I_{OSC}	100	mA

TEMPERATURE

Storage Temperature	T_{STG}	-65 to 150	°C
Junction Temperature	T_J	150	°C

ESD RATINGS

Human Body Model	HBM	2000	V
Machine Model	MM	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Neither input should exceed the range of $V_{SS} - 300 \text{ mV}$ to 7.0 V
- Indefinite duration; however, maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded.

THERMAL INFORMATION (Note 3)

Thermal Metric	Symbol	Limit	Unit
Junction to Ambient – SOT23-5	θ_{JA}	235	°C/W
Junction to Ambient – SOT553-5	θ_{JA}	250	°C/W

- As mounted on an 80 x 80 x 1.5 mm FR4 PCB with 650 mm² and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines.

OPERATING CONDITIONS

Parameter	Symbol	Limit	Unit
Operating Supply Voltage	V_S	1.7 to 5.5	V
Specified Operating Range	NCS2003 NCV2003 T_A	-40 to +85 -40 to +125	°C

NCS2003, NCV2003

ELECTRICAL CHARACTERISTICS: $V_S = +1.8\text{ V}$

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted. **Boldface** limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (NCS2003), $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (NCV2003). Guaranteed by design and/or characterization.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
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INPUT CHARACTERISTICS

Offset Voltage	V_{OS}			0.5	4.0	mV
					5.0	
Offset Voltage Drift	$\Delta V/\Delta T$			2.0		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_{IB}			1		pA
Input Offset Current	I_{OS}			1		pA
Differential Input Resistance	R_{IN}			>1		$\text{T}\Omega$
Differential Input Capacitance	C_{IN}			1.2		pF
Input Common Mode Range	V_{ICR}	Inferred from CMRR	V_{SS}		$V_{DD} - 0.6$	V
Common Mode Rejection Ratio	CMRR	$V_{IN} = 0\text{ V to }V_{DD} - 0.6\text{ V}$	70	80		dB
		$V_{IN} = 0.2\text{ V to }V_{DD} - 0.6\text{ V}$	65			

OUTPUT CHARACTERISTICS

Output Voltage High	V_{OH}	$V_{ID} = +0.5\text{ V, }R_L = 10\text{ k}\Omega$	1.75	1.798		V
			1.75			
		$V_{ID} = +0.5\text{ V, }R_L = 2\text{ k}\Omega$	1.7	1.78		
			1.7			
Output Voltage Low	V_{OL}	$V_{ID} = -0.5\text{ V, }R_L = 10\text{ k}\Omega$		7.0	50	mV
					50	
		$V_{ID} = -0.5\text{ V, }R_L = 2\text{ k}\Omega$		20	100	
					100	
Short Circuit Current	I_{SC}	$V_{ID} = +0.5\text{ V, }V_O = V_{SS}, \text{ Sourcing}$	5.0	8.0		mA
		$V_{ID} = -0.5\text{ V, }V_O = V_{DD}, \text{ Sinking}$	10	14		

NOISE PERFORMANCE

Voltage Noise Density	e_N	$f = 1\text{ kHz}$		20		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_N	$f = 1\text{ kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$

DYNAMIC PERFORMANCE

Open Loop Voltage Gain	A_{VOL}	$R_L = 10\text{ k}\Omega$	80	92		dB
			75			
		$R_L = 2\text{ k}\Omega$		92		dB
			70			
Gain Bandwidth Product	GBWP			5		MHz
Gain Margin	A_M	$R_L = 10\text{ k}\Omega, C_L = 5\text{ pF}$		12		dB
Phase Margin	ψ_M	$R_L = 10\text{ k}\Omega, C_L = 5\text{ pF}$		53		$^\circ$
Slew Rate	SR	Positive Slope, $R_L = 2\text{ k}, A_V = +1$		6		$\text{V}/\mu\text{s}$
		Negative Slope, $R_L = 2\text{ k}, A_V = +1$		9		$\text{V}/\mu\text{s}$
Total Harmonic Distortion + Noise	THD+N	$V_O = 1\text{ Vpp, }R_L = 2\text{ k}\Omega, A_V = +1, 1\text{ kHz}$		0.015		%
		$V_O = 1\text{ Vpp, }R_L = 2\text{ k}\Omega, A_V = +1, 10\text{ kHz}$		0.025		%

POWER SUPPLY

Power Supply Rejection Ratio	PSRR		72	80		dB
			65			
Quiescent Current	I_{CC}	No Load		230	560	μA
					1	mA

NCS2003, NCV2003

ELECTRICAL CHARACTERISTICS: $V_S = +5.0\text{ V}$

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted. **Boldface** limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (NCS2003), $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (NCV2003). Guaranteed by design and/or characterization.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
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INPUT CHARACTERISTICS

Offset Voltage	V_{OS}			0.5	4.0	mV
					5.0	
Offset Voltage Drift	$\Delta V/\Delta T$			2.0		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_{IB}			1		pA
Input Offset Current	I_{OS}			1		pA
Differential Input Resistance	R_{IN}			>1		$\text{T}\Omega$
Differential Input Capacitance	C_{IN}			1.2		pF
Input Common Mode Range	V_{ICR}	Inferred from CMRR	V_{SS}		$V_{DD} - 0.6$	V
Common Mode Rejection Ratio	CMRR	$V_{IN} = 0\text{ V to }V_{DD} - 0.6\text{ V}$	65	70		dB
		$V_{IN} = 0.2\text{ V to }V_{DD} - 0.6\text{ V}$	63			

OUTPUT CHARACTERISTICS

Output Voltage High	V_{OH}	$V_{ID} = +0.5\text{ V, }R_L = 10\text{ k}\Omega$	4.95	4.99		V
			4.95			
		$V_{ID} = +0.5\text{ V, }R_L = 2\text{ k}\Omega$	4.9	4.97		
			4.9			
Output Voltage Low	V_{OL}	$V_{ID} = -0.5\text{ V, }R_L = 10\text{ k}\Omega$		8.0	50	mV
					50	
		$V_{ID} = -0.5\text{ V, }R_L = 2\text{ k}\Omega$		24	100	
					100	
Short Circuit Current	I_{SC}	$V_{ID} = +0.5\text{ V, }V_O = V_{SS}, \text{ Sourcing}$	40	76		mA
		$V_{ID} = -0.5\text{ V, }V_O = V_{DD}, \text{ Sinking}$	50	96		

NOISE PERFORMANCE

Voltage Noise Density	e_N	$f = 1\text{ kHz}$		20		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_N	$f = 1\text{ kHz}$		0.2		$\text{pA}/\sqrt{\text{Hz}}$

DYNAMIC PERFORMANCE

Open Loop Voltage Gain	A_{VOL}	$R_L = 10\text{ k}\Omega$	86	92		dB
			78			
		$R_L = 2\text{ k}\Omega$	83	92		dB
			78			
Gain Bandwidth Product	GBWP			7.0		MHz
Total Harmonic Distortion + Noise	THD+N	$V_O = 4\text{Vpp, }R_L = 2\text{ k}\Omega, A_V = +1, 1\text{ kHz}$		0.005		%
		$V_O = 4\text{Vpp, }R_L = 2\text{ k}\Omega, A_V = +1, 10\text{ kHz}$		0.01		%
Gain Margin	A_M	$R_L = 10\text{ k}\Omega, C_L = 5\text{ pF}$		9		dB
Phase Margin	ψ_M	$R_L = 10\text{ k}\Omega, C_L = 5\text{ pF}$		64		$^\circ$
Slew Rate	SR	Positive Slope, $R_L = 2\text{ k}, A_V = +1$		7		$\text{V}/\mu\text{s}$
		Negative Slope, $R_L = 2\text{ k}, A_V = +1$		14		$\text{V}/\mu\text{s}$

POWER SUPPLY

Power Supply Rejection Ratio	PSRR		72	80		dB
			65			
Quiescent Current	I_{CC}	No Load		300	660	μA
					1	mA

TYPICAL CHARACTERISTICS

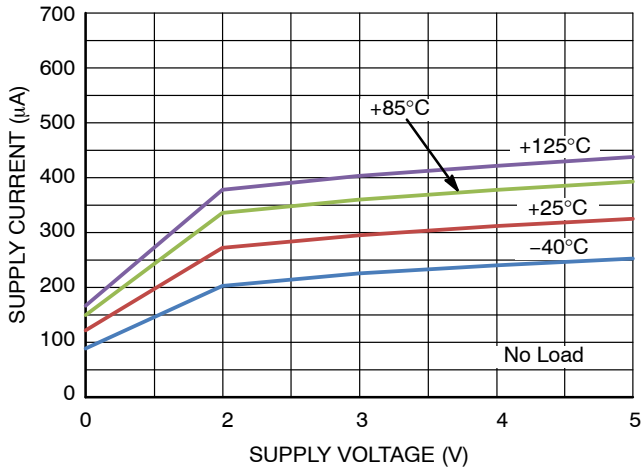


Figure 1. Quiescent Supply Current vs. Supply Voltage

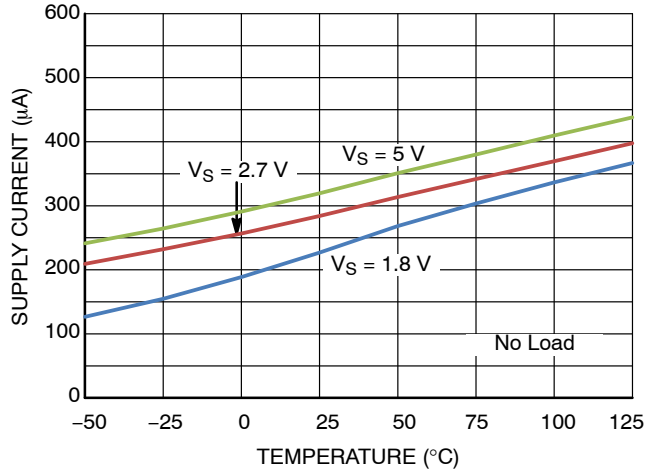


Figure 2. Quiescent Supply Current vs. Temperature

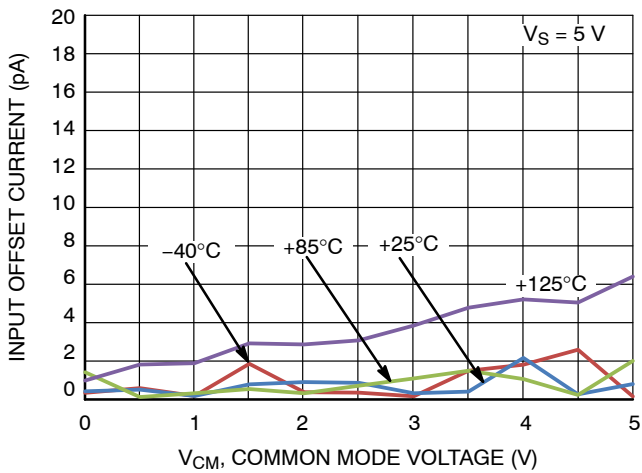


Figure 3. Input Offset Current vs. V_{CM}

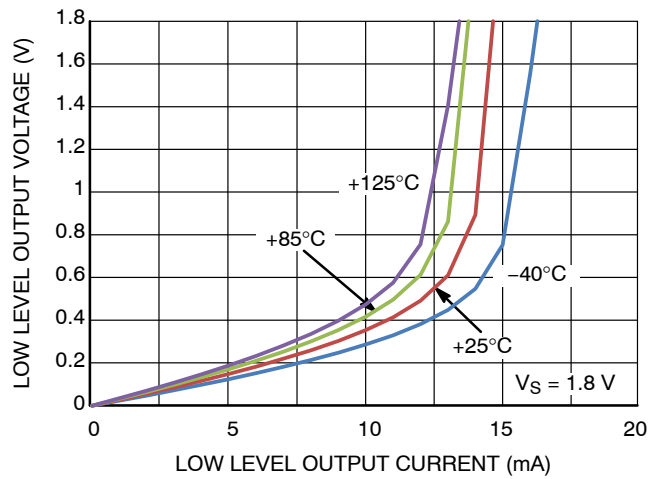


Figure 4. Low Level Output Voltage vs. Output Current @ $V_S = 1.8 V$

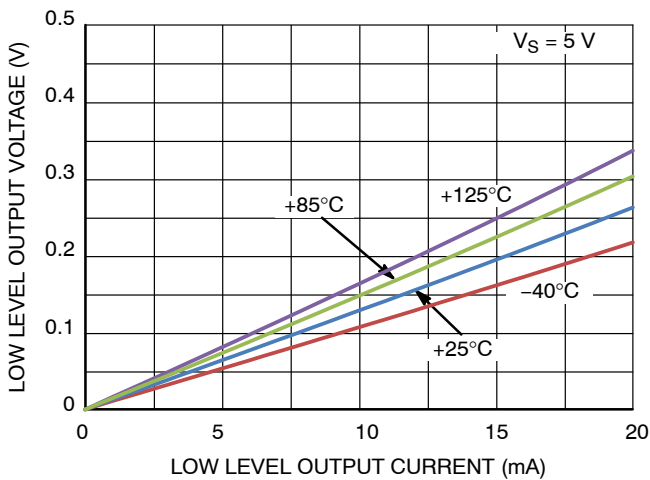


Figure 5. Low Level Output Voltage vs. Output Current @ $V_S = 5 V$

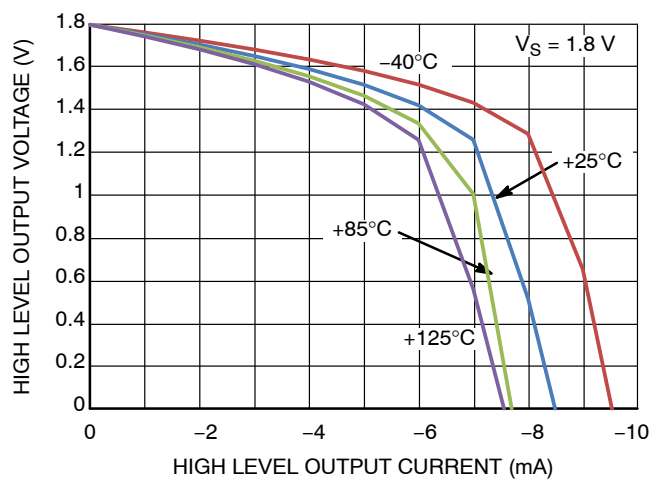


Figure 6. High Level Output Voltage vs. Output Current @ $V_S = 1.8 V$

TYPICAL CHARACTERISTICS

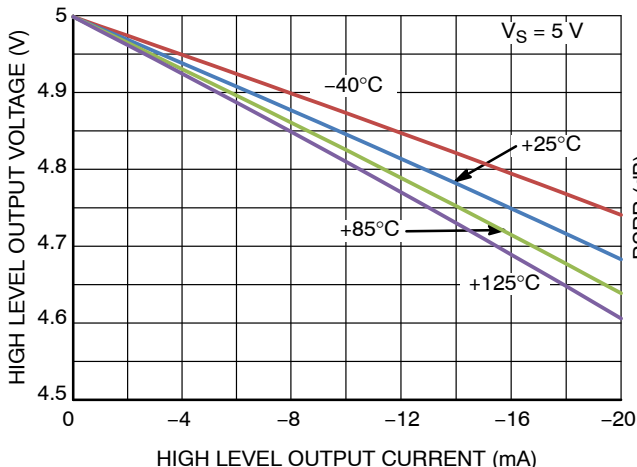


Figure 7. High Level Output Voltage vs. Output Current @ $V_S = 5\text{ V}$

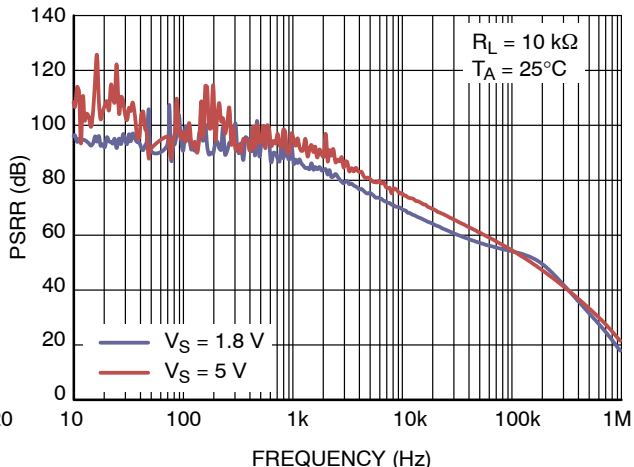


Figure 8. PSRR vs. Frequency

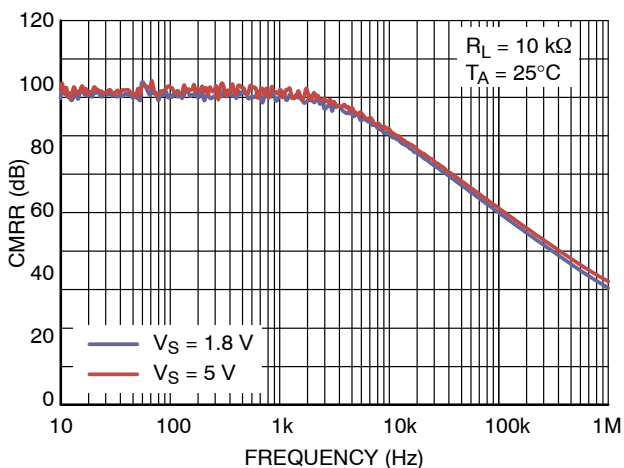


Figure 9. CMRR vs. Frequency

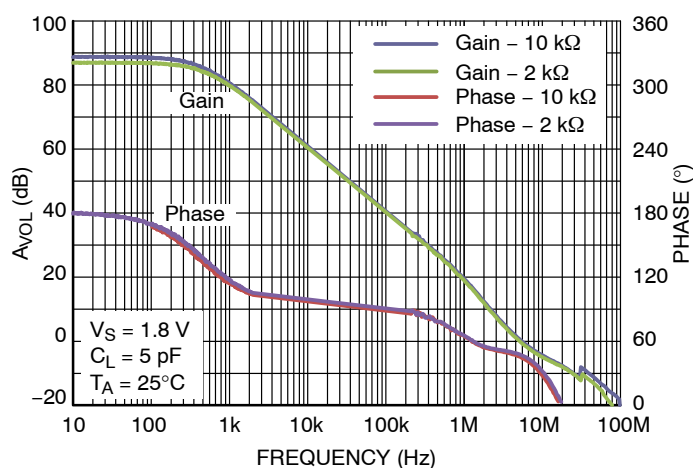


Figure 10. Open Loop Gain and Phase vs. Frequency @ $V_S = 1.8\text{ V}$

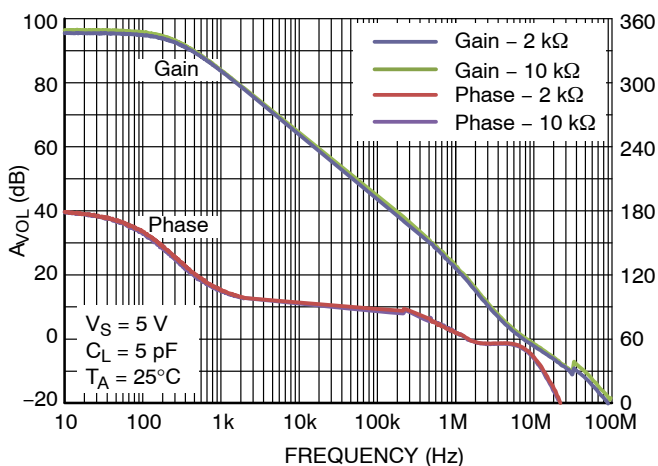


Figure 11. Open Loop Gain and Phase vs. Frequency @ $V_S = 5\text{ V}$

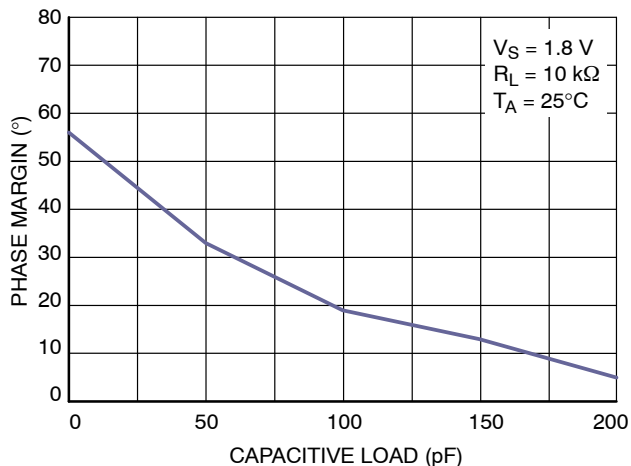


Figure 12. Phase Margin vs. Capacitive Load

TYPICAL CHARACTERISTICS

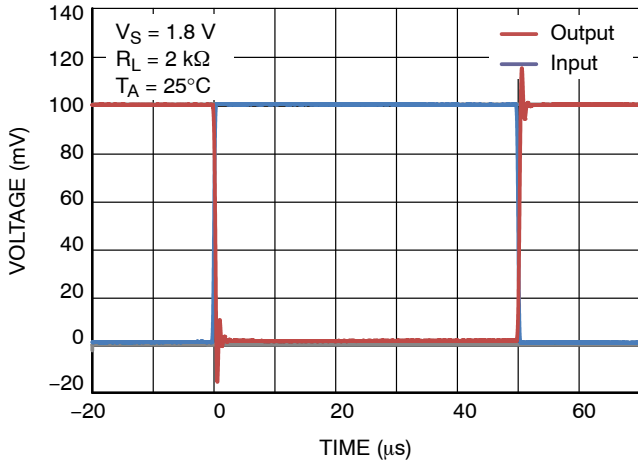


Figure 13. Inverting Small Signal Transient Response

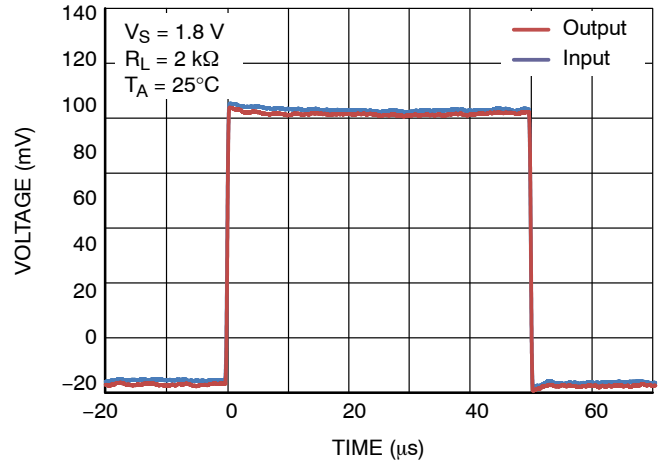


Figure 14. Non-Inverting Small Signal Transient Response

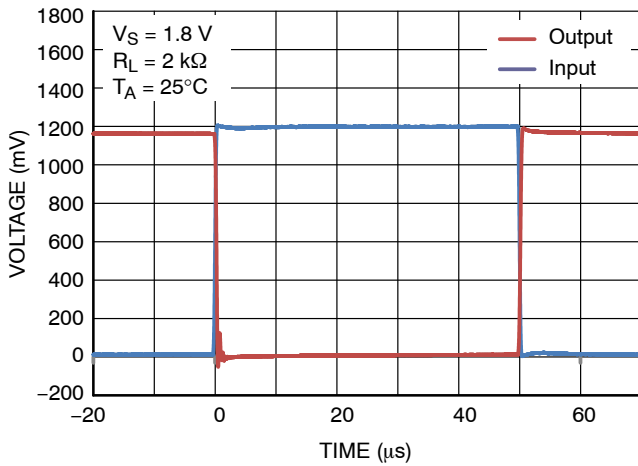


Figure 15. Inverting Large Signal Transient Response

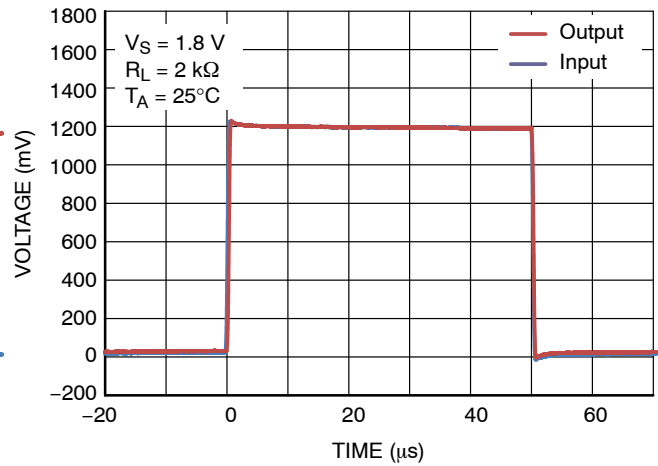


Figure 16. Non-Inverting Large Signal Transient Response

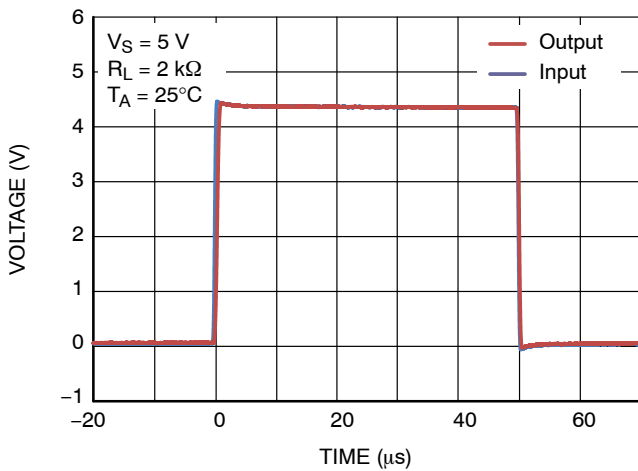


Figure 17. Non-Inverting Large Signal Transient Response

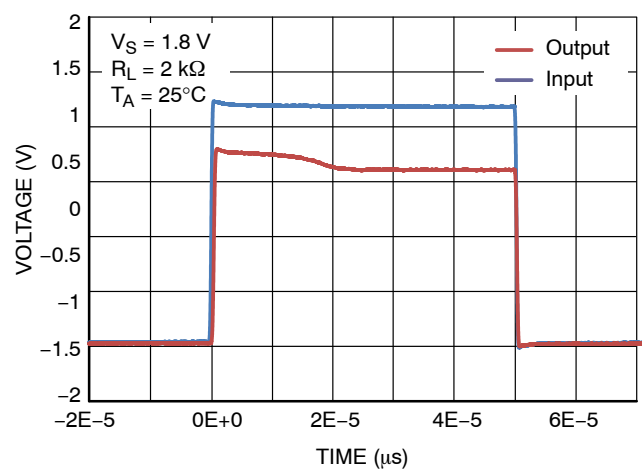


Figure 18. Output Overload Recovery

TYPICAL CHARACTERISTICS

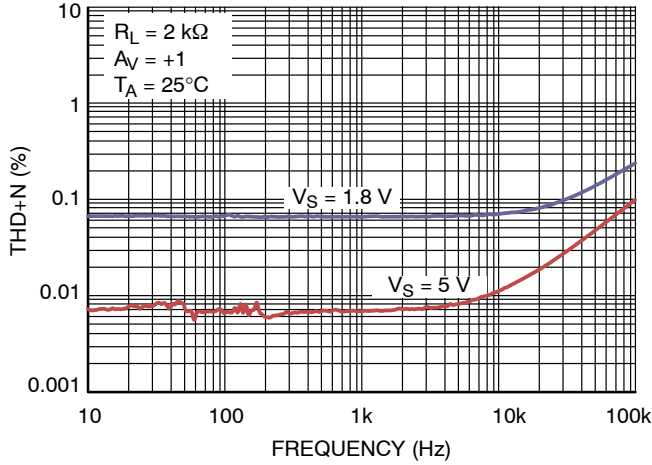


Figure 19. THD+N vs. Frequency

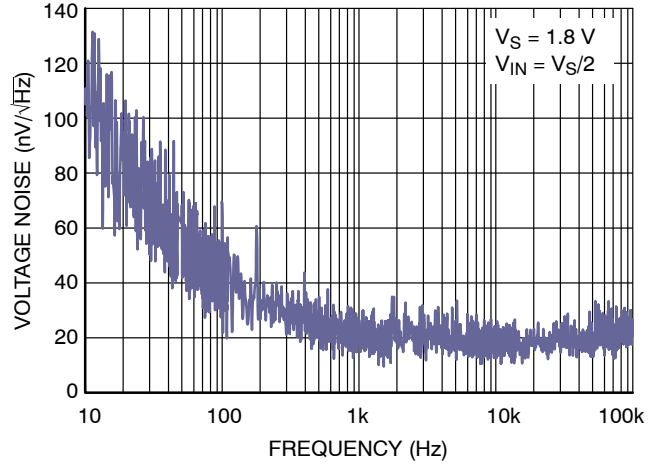


Figure 20. Input Voltage Noise vs. Frequency

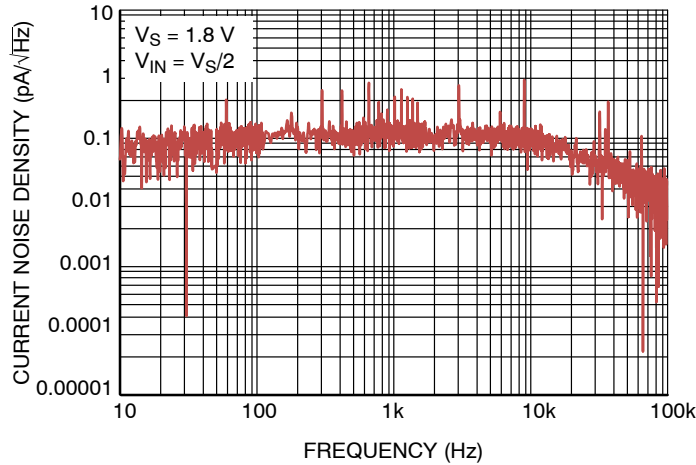


Figure 21. Noise Density vs. Frequency

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCS2003SN2T1G	AN3	SOT23-5 (Pb-Free)	3000 / Tape and Reel
NCV2003SN2T1G* (In Development)	AN3	SOT23-5 (Pb-Free)	3000 / Tape and Reel
NCS2003XV53T2G	A3	SOT553-5 (Pb-Free)	4000 / Tape and Reel

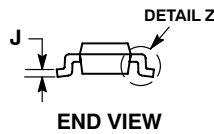
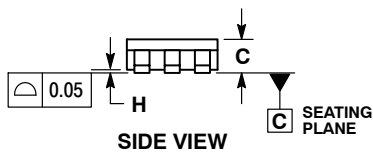
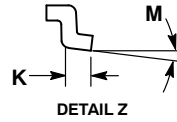
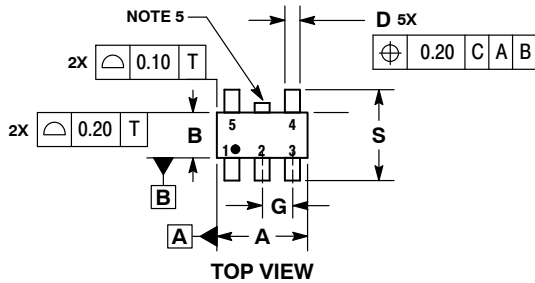
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

NCS2003, NCV2003

PACKAGE DIMENSIONS

TSOP-5 CASE 483-02 ISSUE K

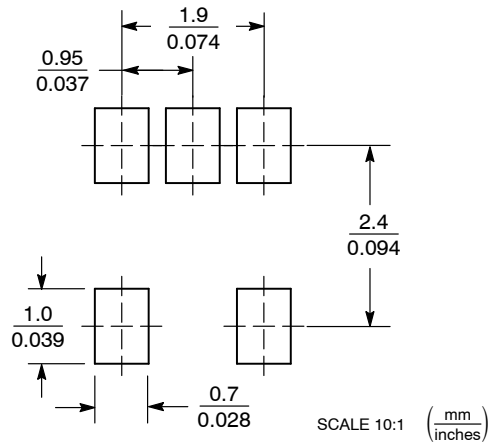


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*

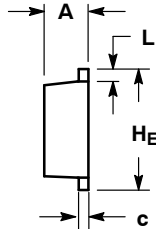
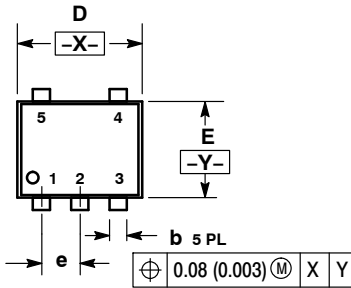


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCS2003, NCV2003

PACKAGE DIMENSIONS

SOT-553, 5 LEAD CASE 463B ISSUE C

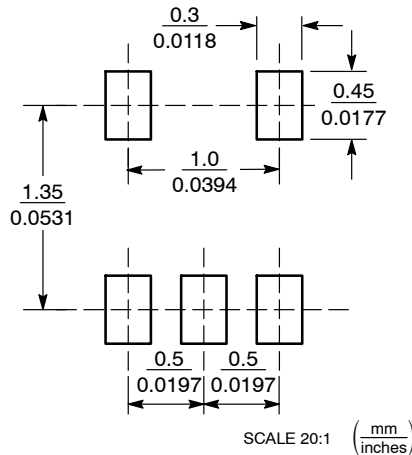


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.55	1.60	1.65	0.061	0.063	0.065

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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