Signetics

FAST Products

FAST 74F1764/1765
74F1764-1/1765-1
1 Megabit DRAM Dual-Ported Controller

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1764/1765	150MHz	150mA
74F1764-1/1765-1	150MHz	125mA

FEATURES

- **Allows two microprocessors to access the same bank of dynamic RAM**
- **Performs arbitration, signal timing, address multiplexing and refresh**
- **10 address output pins allow direct control of up to 1Mbit dynamic RAMs**
- **External address multiplexing enables control of 4Mbit (or greater) dynamic RAMs**
- **Separate refresh clock allows adjustable refresh timing**
- **74F1764/F1764-1 have on-chip 20-bit address input latch**
- **Allows control of dynamic RAMS with row access times down to 40ns**
- **74F1764/F1765 output drivers designed for incident wave switching**
- **74F1764-1/F1765-1 output drivers designed for first reflected wave switching**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
48-Pin Plastic DIP	N74F1764N, N74F1765N, N74F1764-1N, N74F1765-1N
44-Pin PLCC	N74F1764A, N74F1765A, N74F1764-1A, N74F1765-1A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
RA_0 - RA_9		Row address inputs	1.0/1.0	20µA/0.6mA
CA_0 - CA_9		Column address inputs	1.0/1.0	20µA/0.6mA
$\overline{REQ_1}$, $\overline{REQ_2}$		Memory access request inputs	1.0/1.0	20µA/0.6mA
CP		Clock input	1.0/1.0	20µA/0.6mA
RCP		Refresh clock input	1.0/1.0	20µA/0.6mA
$\overline{SEL_1}$, $\overline{SEL_2}$	'F1764/1765	Select outputs	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
MA_0 - MA_9	'F1764/1765	Memory address outputs	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
GNT	'F1764/1765	Grant output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{RAS}$	'F1764/1765	Row address strobe output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
WG	'F1764/1765	Write gate output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{CASEN}$	'F1764/1765	Column address strobe enable output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
DTACK	'F1764/1765	Data transfer acknowledge output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA

NOTE:
1.One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state

DESCRIPTION

The 74F1764/1765 DRAM Dual-ported Controller is a high speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F1764 vs 74F1765

The 74F1764 though functionally and pin to pin compatible with the 74F1765 differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		74F1764, 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.5			V
						±5%V_{CC}	2.7			V
V_{OH2}[3]					I_{OH2}[3]=-35mA	±5%V_{CC}	2.4			V
V_{OH}			74F1764-1, 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-20mA	±10%V_{CC}	2.4	2.7		V
						±5%V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage		74F1764, 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
V_{OL2}[3]					I_{OL2}[4]=60mA	±5%V_{CC}		0.45	0.80	V
V_{OL}			74F1764-1, 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=8mA	±10%V_{CC}		0.30	0.50	V
						±5%V_{CC}		0.30	0.50	V
V_{OL2}[3]					I_{OL2}[3]=75mA	±5%V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} =MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[5]		74F1764, 74F1765	V_{CC} =MAX			-100		-225	mA
			74F1764-1, 74F1765-1	V_{CC} =MAX			-60	100	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F1764, 74F1765	V_{CC} =MAX				150	200	mA
		I_{CCL}						165	210	mA
		I_{CCH}	74F1764-1, 74F1765-1					120	165	mA
		I_{CCL}						125	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Refer to Appendix A.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.