Diode, array, high-speed switching, surface mount

In these single packages, there are one or two diodes as shown in the circuit diagrams.

Features

- available in the following 3-pin packages:
  - — SSD3 (SST, US/European SOT-23) (similar to SC-59)
  - — SMD3 (SMD, SC-59, Japanese SOT-23)
  - — UMD3 (UMD, SC-90, SOT-323)
  - — EMD3 (EMD, SC-90)
- products are marked as follows:

DA112 = AZ	DAN202C = N
DA113 = AY	DAP202C = P
DA114 = AV	DAN202K = N
DA115 = AU	DAP202K =P
DA116 = AZ	DAN202U = N
DA118 = AY	DAP202U = P
DA119 = AU	DAN212C = N
DA120 = AZ	DAN212K =AV
DA121 = AV	DAN222 = N
	DAP222 = P

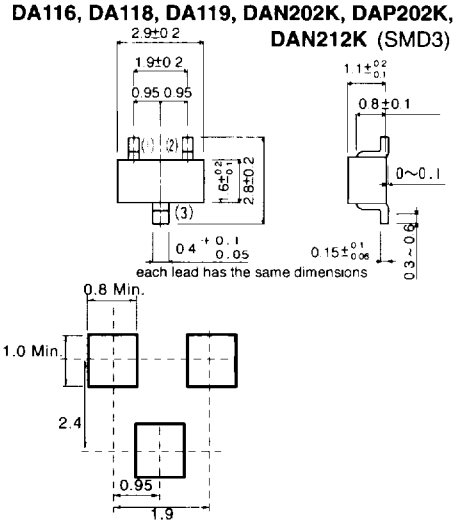
- suitable for automatic mounting on printed circuit board
- high switching speed (t_{rr} = 1.5 ns typically)
- all diodes in the chip have similar characteristics

Applications

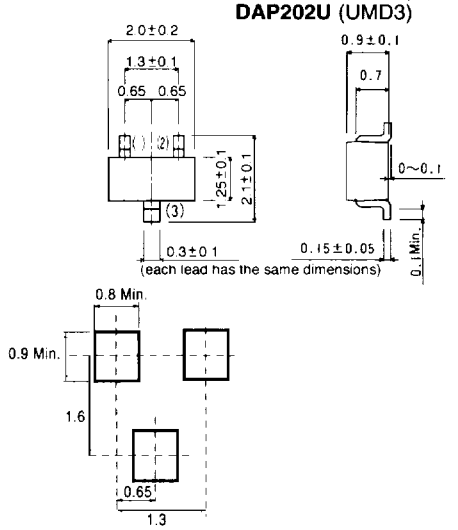
- ultra high speed switching

Dimensions (Units : mm)

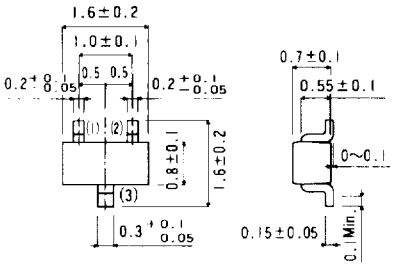
DA116, DA118, DA119, DAN202K, DAP202K, DAN212K (SMD3)



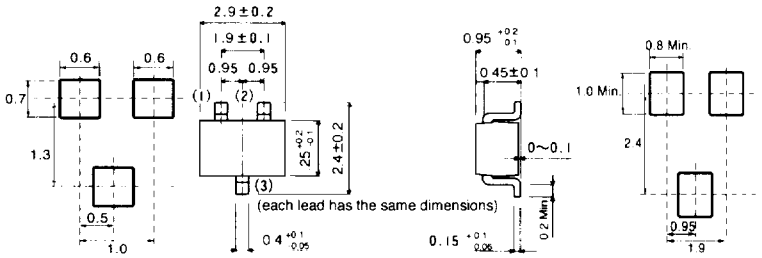
DA112, DA113, DA114, DA115, DAN202U, DAP202U (UMD3)



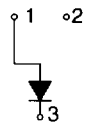
DA120, DA121,
DAN222, DAP222 (EMD3)



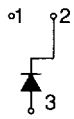
DAN202C, DAP202C,
DAN212C (SSD3)



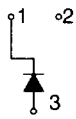
Equivalent circuits



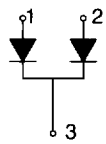
DA115
DA119



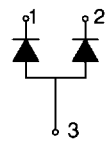
DA112
DA116
DA120



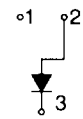
DA113
DA118



DAN202C
DAN202K
DAN202U
DAN222



DAP202C
DAP202K
DAP202U
DAP222



DA114
DA121
DAN212C
DAP212K

Absolute maximum ratings (T_a = 25°C) (Sheet 1 of 2)

Part no.	Peak reverse voltage V_{RM} (V)	DC reverse voltage V_R (V)	Peak forward current I_F (mA)	Mean rectifying current I_O (mA)	Surge current (1μs) I_{surge} (A)	Power dissipation (Total) P_d (mW)	Junction temp. T_j (°C)	Storage temp. T_{stg} (°C)	Type
DA112	80	80	300	100	4	200	150	−55 ~ +150	P
DA113	80	80	300	100	0.5	200	150	−55 ~ +150	P
DA114	80	80	300	100	4	200	150	−55 ~ +150	N
DA115	80	80	300	100	4	200	150	−55 ~ +150	N
DA116	80	80	300	100	4	200	150	−55 ~ +150	P
DA118	80	80	300	100	4	200	150	−55 ~ +150	P
DA119	80	80	300	100	4	200	150	−55 ~ +150	N
DA120	80	80	300	100	4	150	150	−55 ~ +150	P
DA121	80	80	300	100	4	150	150	−55 ~ +150	N
DAN202C	80	80	300	100	4	150	150	−55 ~ +150	N
DAN202K	80	80	300	100	4	150	150	−55 ~ +150	N
DAP202C	80	80	300	100	4	150	150	−55 ~ +150	P
DAP202K	80	80	300	100	4	150	150	−55 ~ +150	P

Absolute maximum ratings (T_a = 25°C) (Sheet 2 of 2)

Part no.	Peak reverse voltage V_{RM} (V)	DC reverse voltage V_R (V)	Peak forward current I_F (mA)	Mean rectifying current I_O (mA)	Surge current (1μs) I_{surge} (A)	Power dissipation (Total) P_d (mW)	Junction temp. T_j (°C)	Storage temp. T_{stg} (°C)	Type
DAN202U	80	80	300	100	4	150	150	−55 ~ +150	N
DAP202U	80	80	300	100	4	150	150	−55 ~ +150	P
DAN212C	80	80	300	100	4	150	150	−55 ~ +150	N
DAN212K	80	80	300	100	4	150	150	−55 ~ +150	N
DAN222	80	80	300	100	4	150	150	−55 ~ +150	N
DAP222	80	80	300	100	4	150	150	−55 ~ +150	P

Electrical characteristics (unless otherwise noted, T_a = 25°C)

Part no.	Forward voltage		Reverse current		Capacitance between terminals			Reverse recovery time			
	V_F (V) Max	I_F (mA)	I_R (μA) Max	V_R (V)	C_T (pF) max.	V_R (V)	f (MHz)	t_{rr} (nS) Max	V_R (V)	I_F (mA)	Ref
DA112	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DA113	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DA114	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DA115	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DA116	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DA118	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DA119	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DA120	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DA121	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAN202C	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAN202K	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAP202C	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAP202K	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAN202U	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAP202U	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAN212C	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAN212K	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAN222	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8
DAP222	1.2	100	0.1	70	3.5	6	1	4	6	5	Figure 8

Electrical characteristic curves

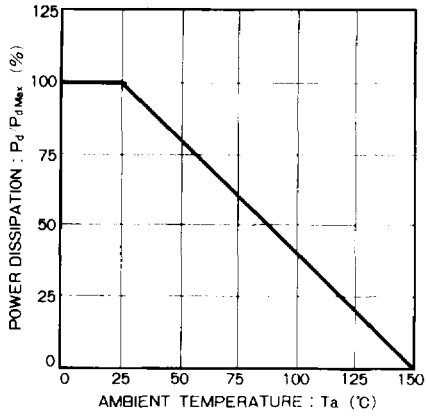


Figure 1

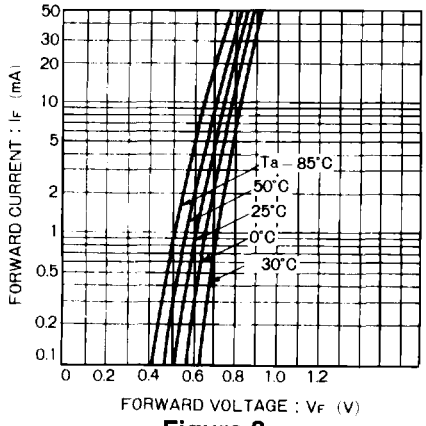


Figure 2

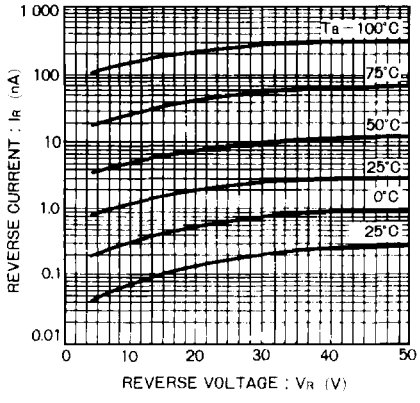


Figure 3

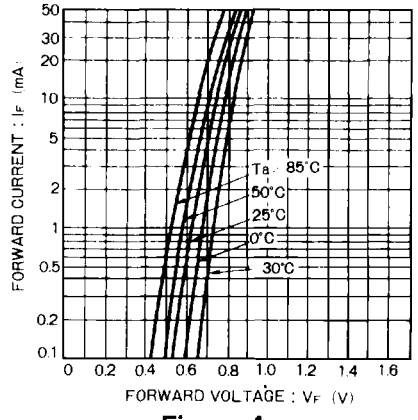


Figure 4

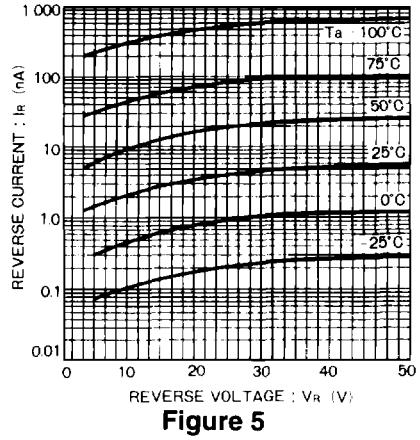


Figure 5

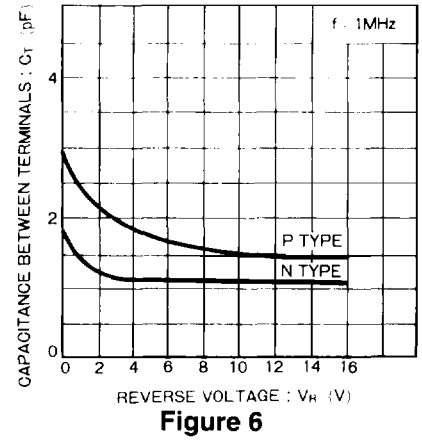


Figure 6

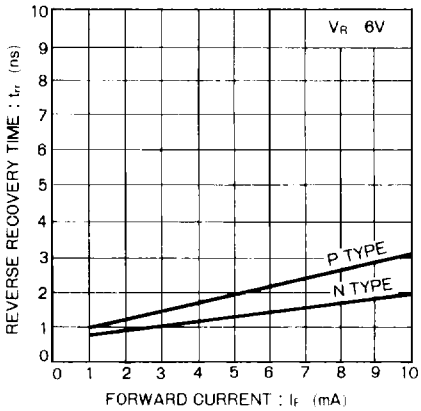
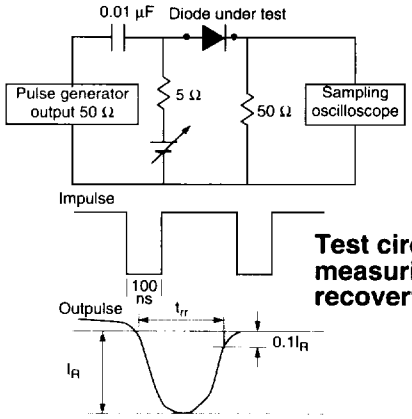


Figure 7



Test circuit for measuring reverse recovery time (t_{rr})

Figure 8