



MwT-101

2-8 GHz

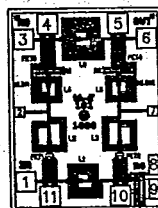
MMIC AMPLIFIER CHIP

MICROWAVE TECHNOLOGY
MICROWAVE TECHNOLOGY

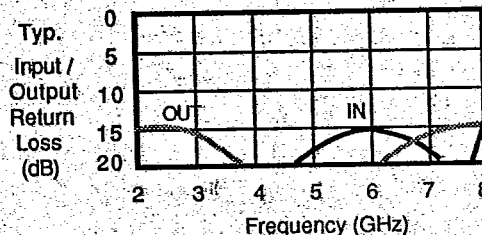
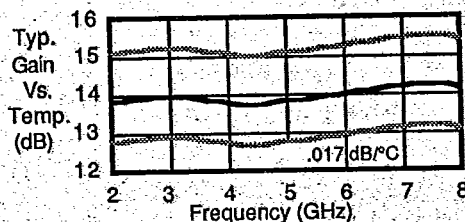
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37E D ■ 6124100 0000080 T ■ MRWV

T-74-13-01



- 35 dB TYPICAL REVERSE ISOLATION
- ± 0.5 dB TYPICAL OUTPUT POWER FLATNESS
- 3 mA/dB TYPICAL GAIN EFFICIENCY
- -16 dBc TYPICAL SECOND HARMONICS AT Psat
- DIAMOND LIKE CARBON (DLC) PASSIVATION
- SINGLE SUPPLY BIAS



ELECTRICAL SPECIFICATIONS¹ (Ta=25°C, VDD=8.0V, 2-8 GHz)

MwT-101-GFP (Model Number)

GAIN (dB)			GAIN FLATNESS ($\pm$ dB)			POWER ² (dBm)			IDD (mA)	
"G"	MIN	TYP	"F"	TYP	MAX	"P"	MIN	TYP	TYP	MAX
-1	11	12	-1	0.6	1.0	-1	11	12	35	45
-3	13	14	-5	0.3	0.5	-3	13	14	45	60
						-5	15	16	60	100

Example: MwT-101-353 = 13 dB Gain, ± 0.5 dB Gain Flatness, +13 dBm P1dB

SYMBOL	PARAMETERS	UNITS	MIN	TYP	MAX
FREQ	Frequency Range	GHz	2.0 ³		8.0
VSWR, IN	Input VSWR	—		1.5:1	1.7:1
VSWR, OUT	Output VSWR	—		1.5:1	1.7:1
NF	Noise Figure	dB		6.5	7.0
ISO	Reverse Isolation	dB		35	
RTH	Thermal Resistance	°C/W		65	

NOTES:

1. Wafers are 100% DC probed and chips are categorized into low (30-40 mA), medium (40-60 mA), and high (60-80 mA) current bins. Four evaluation samples from each of these current bins are assembled per the Assembly Diagram on p. 4 and RF tested. Model numbers are assigned to each bin based on the minimum performance of three out of four of these samples. Chip products are not individually RF tested.
2. Values shown are at 1 dB gain compression. One dB compressed output power above these values may be achieved with increased voltage and/or current. If output power below 11 dBm is acceptable, chips with current below 30 mA are available. Contact MwT for details.
3. Minimum frequency of operation is limited only by off-chip bias circuitry and may be extended as desired. Contact MwT for details.

9000-1443



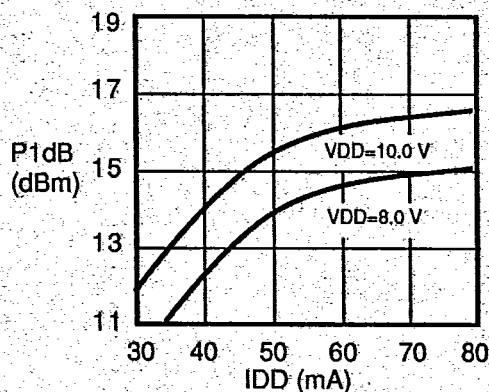
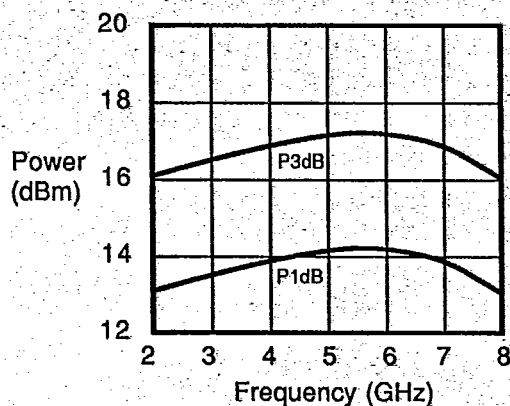
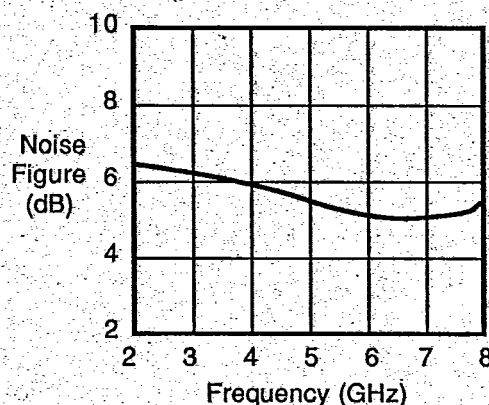
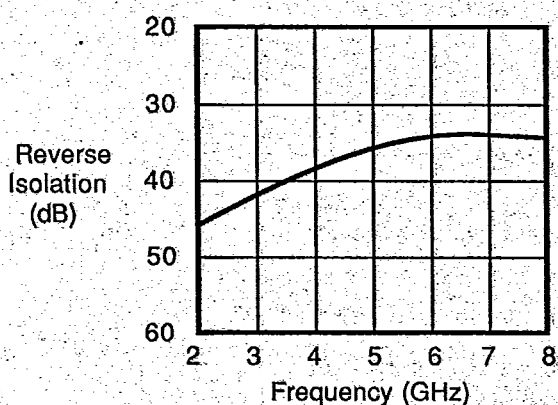
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MAXIMUM RATINGS AT $T_a=25^\circ\text{C}$

SYMBOL	PARAMETER	UNITS	CONT MAX ¹	ABSOLUTE MAX ²
VDD	Supply Voltage	V	10.0	12.0
IDD	Supply current	mA	100	150
Tch	Channel Temperature	$^\circ\text{C}$	+150	+175
Tst	Storage Temperature	$^\circ\text{C}$	-55 to +150	-65 to +175

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.

2. Exceeding any one of these limits may cause permanent damage.

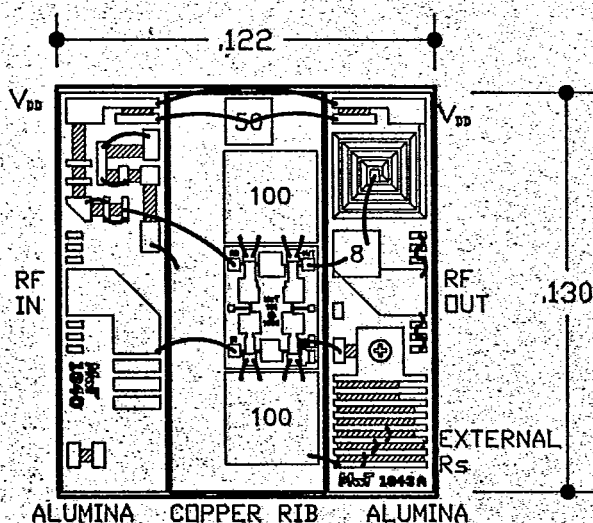
Typical Performance at $T_a=25^\circ\text{C}$, VDD = 8.0V, IDD = 45 mA

The schematic diagram shows a circuit with 11 nodes, numbered 1 through 11 in circles. The components and their connections are as follows:

- FET1** and **FET2** are NMOS transistors with gates connected to node 1. Their sources are connected to node 11. The drain of FET1 is connected to node 2, and the drain of FET2 is connected to node 10.
- FET3** and **FET4** are PMOS transistors with gates connected to node 3. Their sources are connected to node 4. The drain of FET3 is connected to node 2, and the drain of FET4 is connected to node 5.
- MLIN1** and **MLIN2** are linear models connected in parallel with the drains of FET1 and FET2, respectively, and their sources are connected to node 11.
- R1** and **R2** are resistors connected in parallel with the drains of FET3 and FET4, respectively, and their other terminals are connected to node 11.
- L1** is an inductor connected between nodes 1 and 11.
- L2** is an inductor connected between nodes 2 and 11.
- L3** is an inductor connected between nodes 5 and 7.
- L4** and **L5** are inductors connected in parallel with the drains of FET1 and FET2, respectively, and their other terminals are connected to node 11.
- L6** is an inductor connected between nodes 4 and 5.
- RS** is a resistor connected between nodes 10 and 9.

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ASSEMBLY DIAGRAM



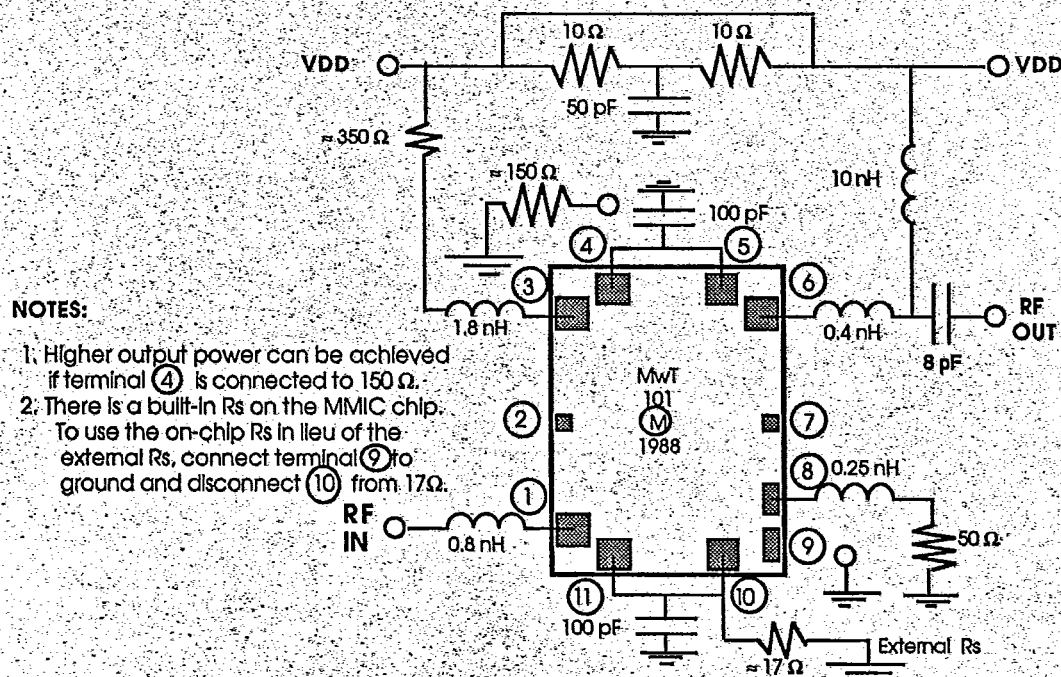
KEY:

-  Via Hole
 Metal Pattern
 Resistor
 Capacitor with value in pF

NOTES:

1. MWT recommends MNOS type capacitors.
2. Alumina substrates are available from MWT.
3. Refer to "Assembly Procedures" for assembly details.

SCHEMATIC DIAGRAM



NOTES:

1. Higher output power can be achieved if terminal ④ is connected to 150 Ω .
2. There is a built-in R_s on the MMIC chip. To use the on-chip R_s in lieu of the external R_s , connect terminal ⑨ to ground and disconnect ⑩ from 170 Ω .