

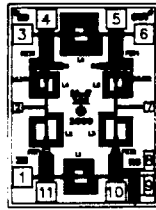
MwT-101

2-8 GHz

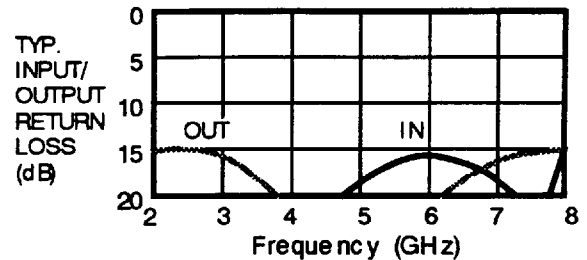
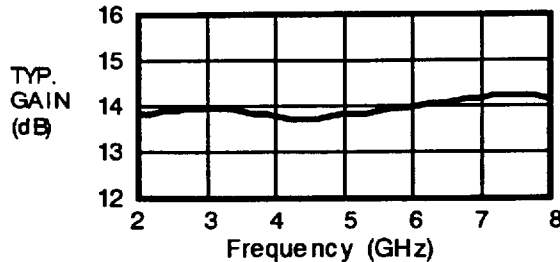
MMIC AMPLIFIER CHIP

MICROWAVE TECHNOLOGY

4268 Solar Way Fremont, CA 94538 510-651-6700 FAX 510-651-2208



- 30 dB TYPICAL REVERSE ISOLATION
- ± 0.6 dB TYPICAL OUTPUT POWER FLATNESS
- 3 mA/dB TYPICAL GAIN EFFICIENCY
- -16 dBc TYPICAL SECOND HARMONICS AT Psat
- DIAMOND LIKE CARBON (DLC) PASSIVATION
- SINGLE SUPPLY BIAS



ELECTRICAL SPECIFICATIONS¹ (Ta = 25°C, VDD = 8.0V, 2 - 8 GHz)

MwT-101-GFP (Model Number)

GAIN (dB)			GAIN FLATNESS ($\pm$ dB)			POWER (dBm) ² IDD (mA)				
"G"	MIN	TYP	"F"	TYP	MAX	"P"	MIN	TYP	TYP	MAX
-1	11	12	-1	0.6	1.0	-0	8	10	40	50
-3	13	14	-5	0.3	0.5	-1	11	12	40	50
						-3	13	14	50	65

Example: MwT-101-353 = 13 dB Gain, ± 0.5 dB Gain Flatness, +13 dBm P1dB

SYMBOL	PARAMETERS	UNITS	MIN	TYP	MAX
FREQ	Frequency Range	GHz	20 ³		8.0
VSWR, IN	Input VSWR	---		1.5:1	1.7:1
VSWR, OUT	Output VSWR	---		1.5:1	1.7:1
$\Delta G/\Delta T$	Gain Variation Over Temperature	2 GHz 8 GHz		0.017 0.019	
NF	Noise Figure	dB		6.5	7.0
ISO	Reverse Isolation	dB		30	
RTH	Thermal Resistance	°C/W		65	

NOTES:

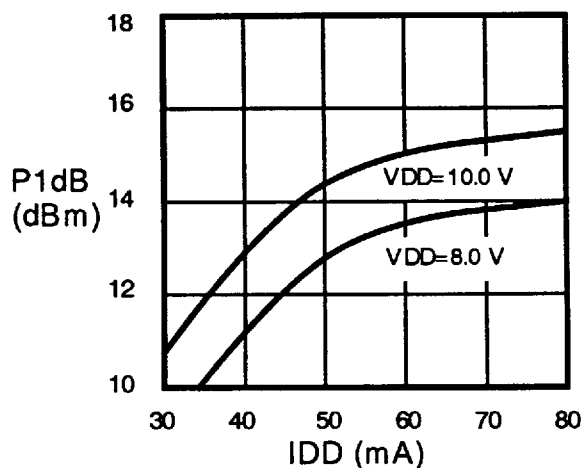
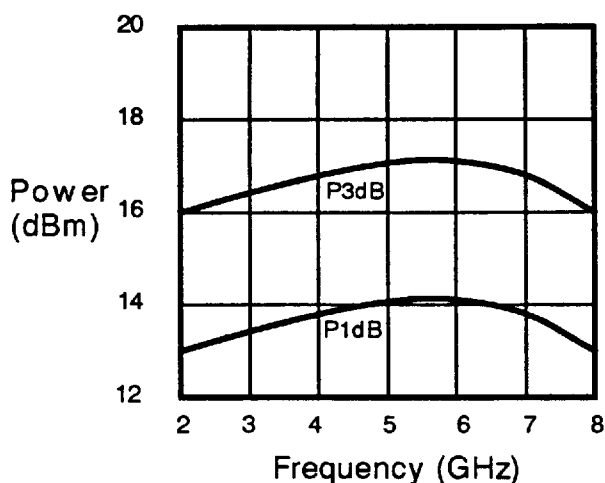
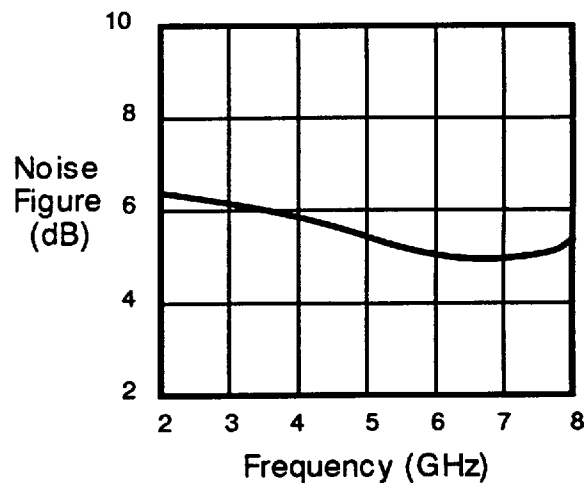
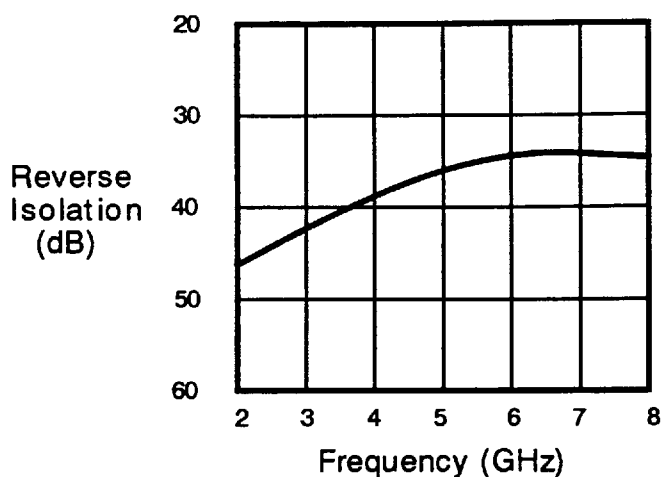
1. Wafers are 100% DC probed and chips are categorized into low (30-40 mA), medium (40-60 mA), and high (60-80 mA) current bins. Four evaluation samples from each of these current bins are assembled per the Assembly Diagram on p. 4 and RF tested. Model numbers are assigned to each bin based on the minimum performance of three out of four of these samples. Chip products are not individually RF tested.
2. Values shown are at 1 dB gain compression. One dB compressed output power above these values may be achieved with increased voltage and/or current.
3. Minimum frequency of operation is limited only by off-chip bias circuitry and may be extended as desired. Contact MwT for details.

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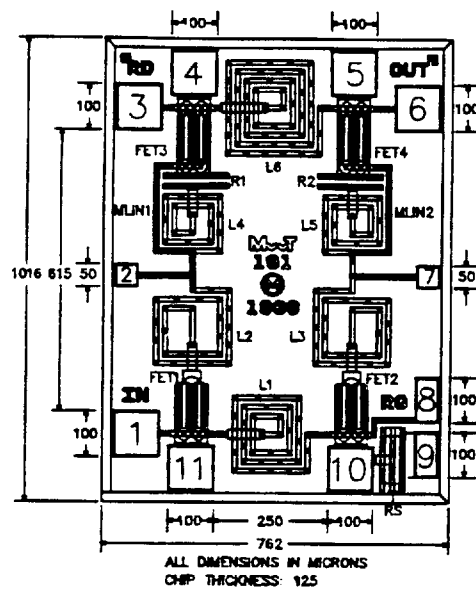
MwT-101**MAXIMUM RATINGS AT Ta=25° C**

SYMBOL	PARAMETER	UNITS	CONT MAX ¹	ABSOLUTE MAX ²
VDD	Supply Voltage	V	10.0	12.0
IDD	Supply current	mA	100	150
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-55 to +150	-65 to +175

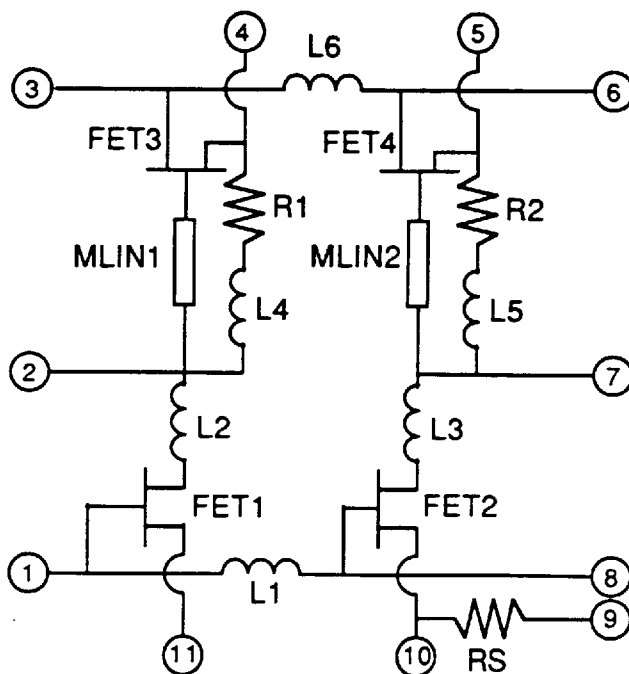
- NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
 2. Exceeding any one of these limits may cause permanent damage.

Typical Performance at Ta=25 °C, VDD = 8.0V, IDD = 45 mA

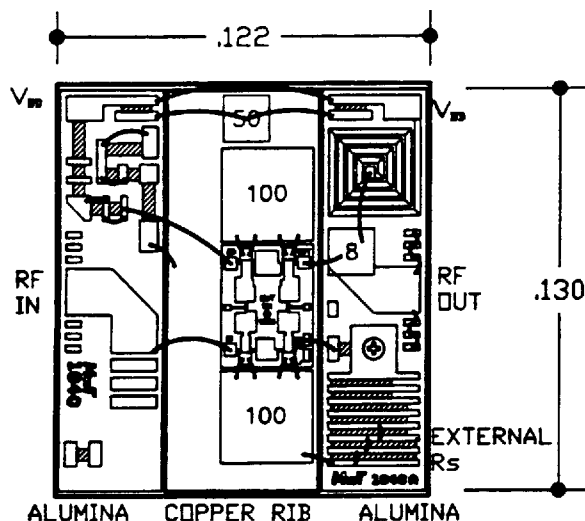
DEVICE LAYOUT



DEVICE SCHEMATIC



ASSEMBLY DIAGRAM



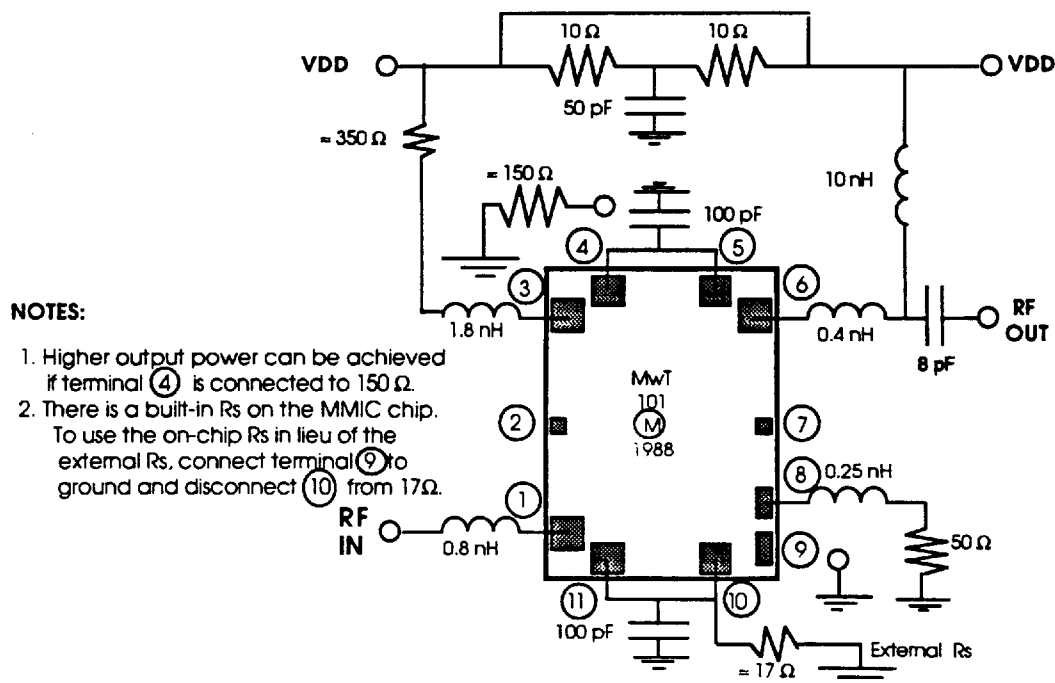
KEY:

-  Via Hole
-  Metal Pattern
-  Resistor
-  Capacitor with value in pF

NOTES:

1. MwT recommends MNOS type capacitors.
2. Alumina substrates are available from MwT.
3. Refer to "Assembly Procedures" for assembly details.

SCHEMATIC DIAGRAM



NOTES:

1. Higher output power can be achieved if terminal (4) is connected to 150 Ω.
2. There is a built-in Rs on the MMIC chip. To use the on-chip Rs in lieu of the external Rs, connect terminal (9) to ground and disconnect (10) from 17 Ω.