M5M44280AJ,TP,RT-8,-8S

FAST PAGE MODE 4718592-BIT(262144-WORD BY 18-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 18-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs.

Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

This device has 2$\overline{CAS}$ and 1$\overline{W}$ terminals, Refresh cycle is 512 cycles every 8.2 ms.

FEATURES

Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	$\overline{OE}$ access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M44280AXX-8, -8S	80	20	40	20	150	620

XX = J, TP, RT

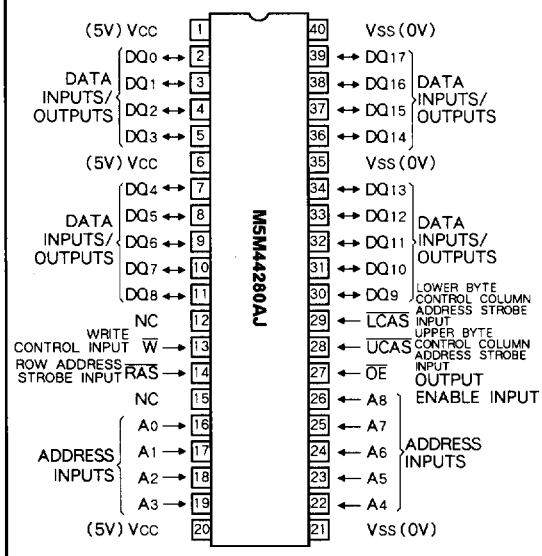
- 40pin 400mil SOJ, 44pin 400mil TSOP(II)
- Single 5V ± 10% supply
- Low stand-by power dissipation
  - 5.5mW (max) ····· CMOS Input level
  - 0.55mW* (max) ····· CMOS Input level
- Low operating power dissipation
  - M5M44280AXX-8, -8S ····· 853mW (max)
- Fast-page mode (256-bit random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Self refresh capability*
  - Self refresh current ····· 300 µs
- Extended refresh capability*
  - Extended refresh current ····· 350 µs
- Early write mode and $\overline{OE}$ to contorol output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 512 refresh cycles every 8.2ms (A_0~A_8)
- 512 refresh cycles every 64ms (A_0~A_8)*
- Byte or Word control for Read/Write operation (2$\overline{CAS}$, 1$\overline{W}$ type)

* : Applicable to self refresh version (M5M44280AJ, TP, RT-8S : option) only.

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

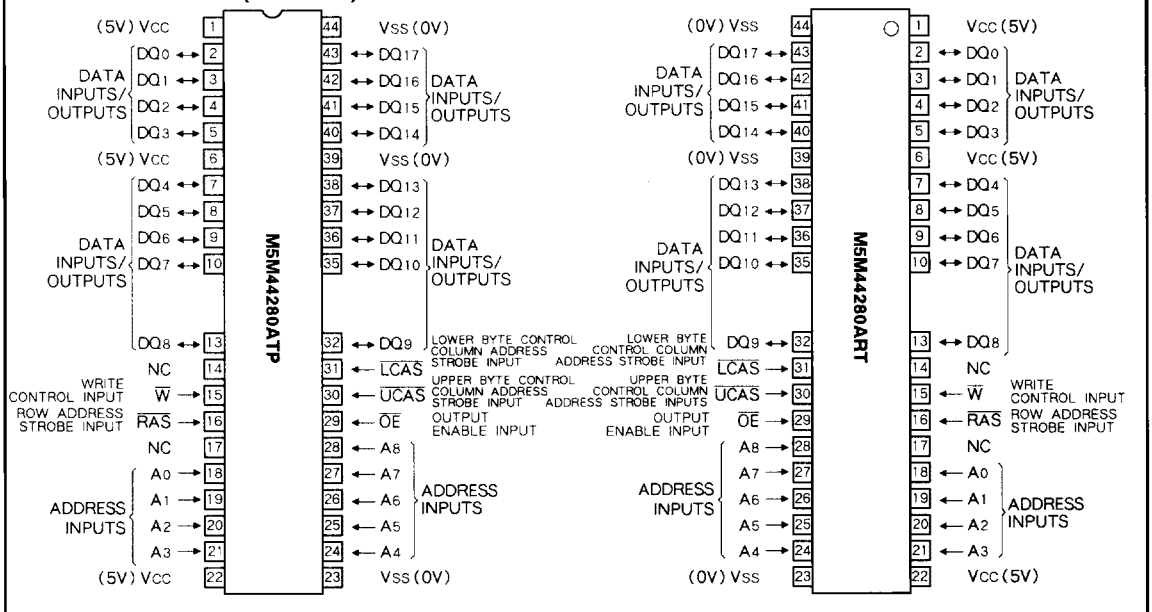
PIN CONFIGURATION (TOP VIEW)



Outline 40P0K (400mil SOJ)

NC : NO CONNECTION

PIN CONFIGURATION (TOP VIEW)



Outline 44P3W-L(400mil TSOP Normal Bend)

Outline 44P3W-M(400mil TSOP Reverse Bend)

NC : NO CONNECTION

FUNCTION

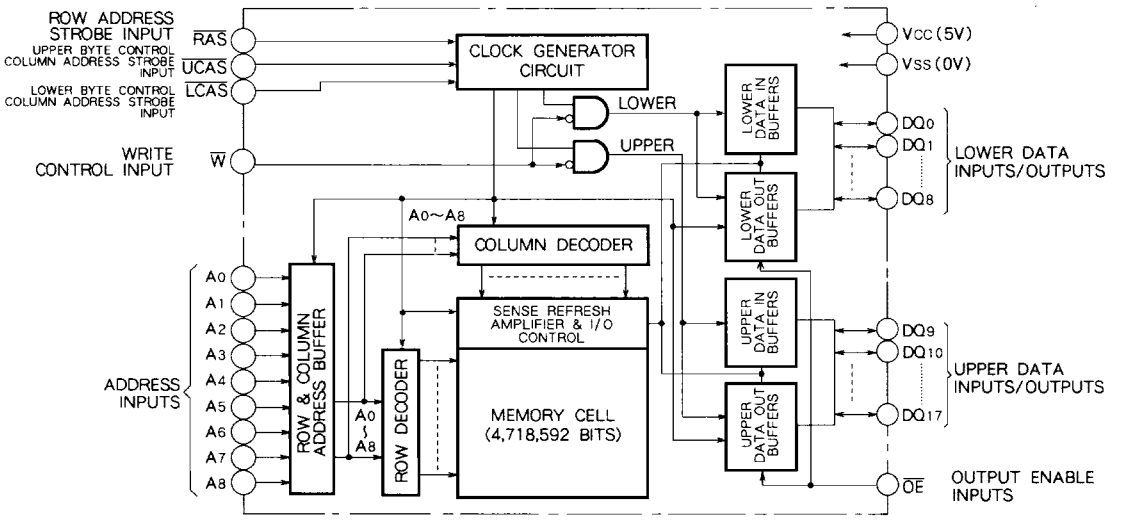
The M5M44280AJ, TP, RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1. Input condition for each mode

Operation	Inputs							Input/Output				Refresh	Remark
								Lower		Upper			
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	D	Q	D	Q		
Read	ACT	ACT	ACT	NAC	ACT	APD	APD	OPN	IVD	OPN	IVD	YES	
Upper read	ACT	NAC	ACT	NAC	ACT	APD	APD	DNC	OPN	OPN	IVD	YES	
Lower read	ACT	ACT	NAC	NAC	ACT	APD	APD	OPN	IVD	DNC	OPN	YES	
Early write	ACT	ACT	ACT	ACT	DNC	APD	APD	IVD	OPN	IVD	OPN	YES	
Upper early	ACT	NAC	ACT	ACT	DNC	APD	APD	DNC	OPN	IVD	OPN	YES	
Lower early	ACT	ACT	NAC	ACT	DNC	APD	APD	IVD	OPN	DNC	OPN	YES	Fast page mode
Delayed write	ACT	ACT	ACT	ACT	DNC	APD	APD	IVD	OPN	IVD	OPN	YES	identical
Upper delayed	ACT	NAC	ACT	ACT	DNC	APD	APD	DNC	OPN	IVD	OPN	YES	
Lower delayed	ACT	ACT	NAC	ACT	DNC	APD	APD	IVD	OPN	DNC	OPN	YES	
Read-Modify-Write	ACT	ACT	ACT	ACT	ACT	APD	APD	IVD	IVD	IVD	IVD	YES	
Upper R-M-W	ACT	NAC	ACT	ACT	ACT	APD	APD	DNC	OPN	IVD	IVD	YES	
Lower R-M-W	ACT	ACT	NAC	ACT	ACT	APD	APD	IVD	IVD	DNC	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	APD	DNC	DNC	OPN	DNC	OPN	YES	
Hidden refresh	ACT	ACT	ACT	DNC	ACT	DNC	DNC	OPN	IVD	OPN	IVD	YES	
Upper Hidden refresh	ACT	NAC	ACT	DNC	ACT	DNC	DNC	DNC	OPN	OPN	IVD	YES	
Lower Hidden refresh	ACT	ACT	NAC	DNC	ACT	DNC	DNC	OPN	IVD	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$(Extended)* refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Upper $\overline{CAS}$ before $\overline{RAS}$	ACT	NAC	ACT	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Lower $\overline{CAS}$ before $\overline{RAS}$	ACT	ACT	NAC	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Self*refresh	ACT	NAC	ACT	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	NO	

Note. ACT : active, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



FAST PAGE MODE 4718592-BIT(262144-WORD BY 18-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage, all inputs		2.4		6.5	V
V_{IL}	Low-level input voltage	DQ_0~DQ_{17}	−1.0		0.8	V
		Others	−2.0		0.8	

Note 1. All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0≦V_{IH}≦6.5V, 0ther inputs pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4, 5)	M5M44280A-8, -8S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min. output open			155	mA
$I_{CC2(AV)}$	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.5V output open			1	
						0.1*	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3, 5)	M5M44280A-8, -8S	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min. output open			155	mA
$I_{CC4(AV)}$	Average supply current from V_{CC}, Fast-Page-Mode (Note 3, 4, 5)	M5M44280A-8, -8S	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC} = min., output open			155	mA
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3, 5)	M5M44280A-8, -8S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling, t_{RC} = min. output open			155	mA
$I_{CC8(AV)}$*	Average supply current from V_{CC} Extended refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$ ≦ 0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{OE}$ ≦ 0.2V or ≧ V_{CC} − 0.2V $\overline{W}$ ≦ 0.2V or ≧ V_{CC}−0.2V, A_0~A_8 ≦ 0.2V or ≧ V_{CC}−0.2V, DQ = open t_{RC} = 125μs, t_{RAS} = $t_{RAS\ min}$~1μs			350	μA
$I_{CC9(AV)}$*	Average supply current from V_{CC} Self refresh mode (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V $\overline{OE}$ ≦ 0.2V or ≧ V_{CC} − 0.2V $\overline{W}$ ≦ 0.2V or ≧ V_{CC} − 0.2V A_0~A_8 ≦ 0.2V or ≧ V_{CC} − 0.2V			300	μA

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5. Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (Ta = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I = V_{SS} f = 1MHz V_i = 25mVrms			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter		Limits M5M44280A-8, -8S Min	Limits M5M44280A-8, -8S Max	Unit
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		80	ns
t_{AA}	Column address access time	(Note 7, 10)		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		45	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		20	ns
t_{CLZ}	Output low impedance from $\overline{CAS}$ low	(Note 7)	5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	20	ns

Note 6. An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 8 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7. Measured with a load circuit equivalent to 2TTL loads and 100pF.
8. Assumes that $t_{RCD} \geqq t_{RCD}(max)$ and $t_{ASC} \geqq t_{ASC}(max)$.
9. Assumes that $t_{RCD} \leqq t_{RCD}(max)$ and $t_{RAD} \leqq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.
10. Assumes that $t_{RAD} \geqq t_{RAD}(max)$ and $t_{ASC} \leqq t_{ASC}(max)$.
11. Assumes that $t_{CP} \leqq t_{CP}(max)$ and $t_{ASC} \geqq t_{ASC}(max)$.
12. $t_{OFF}(max)$ and $t_{OEZ}(max)$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\,\mu A|$) and is not reference to $V_{OH}(min)$ or $V_{OL}(max)$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 13, 14)

symbol	Parameter		Limits M5M44280A-8, -8S Min	Limits M5M44280A-8, -8S Max	Unit
t_{REF}	Refresh cycle time			8.2	ms
t_{REF}	Refresh cycle time *			64	ms
t_{RP}	$\overline{RAS}$ high pulse width		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	15	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note 18)	0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note 19)	20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note 19)	20		ns
t_T	Transition time	(Note 20)	1	50	ns

Note 13. The timing requirements are assumed t_T = 5ns.
14. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals.
15. $t_{RCD}(max)$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD}(max)$, access time is t_{RAC}.
If t_{RCD} is greater than $t_{RCD}(max)$, access time is controlled exclusively by t_{CAC} or t_{AA}.
$t_{RCD}(min)$ is specified as $t_{RCD}(min) = t_{RAH}(min) + 2t_T + t_{ASC}(min)$.
16. $t_{RAD}(max)$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD}(max)$ and $t_{ASC} \leqq t_{ASC}(max)$, access time is controlled exclusively by t_{AA}.
17. $t_{ASC}(max)$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD}(max)$ and $t_{ASC} \geqq t_{ASC}(max)$, access time is controlled exclusively by t_{CAC}.
18. Either t_{DZC} or t_{DZO} must be satisfied.
19. Either t_{CDD} or t_{ODD} must be satisfied.
20. t_T is measured between $V_{IH}(min)$ and $V_{IL}(max)$.

Read and Refresh Cycles

Symbol	Parameter		Limits M5M44280A-8, -8S Min	Limits M5M44280A-8, -8S Max	Unit
t_{RC}	Read cycle time		150		ns
t_{RAS}	$\overline{RAS}$ low pulse width		80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 21)	0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 21)	10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		40		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		20		ns

Note 21. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter		Limits M5M44280A-8, -8S Min	Limits M5M44280A-8, -8S Max	Unit
t_{WC}	Write cycle time		150		ns
t_{RAS}	$\overline{RAS}$ low pulse width		80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 23)	0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		20		ns
t_{WP}	Write pulse width		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits M5M44280A-8, -8S Min	Limits M5M44280A-8, -8S Max	Unit
t_{RWC}	Read Write/read modify write cycle time	(Note 22)	195		ns
t_{RAS}	$\overline{RAS}$ low pulse width		125	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		65	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		125		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		65		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 23)	40		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 23)	100		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 23)	60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		20		ns
t_{WP}	Write pulse width		15		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		20		ns

Note 22. t_{RWC} is specified as $t_{RWC}(min) = t_{RAC}(max) + t_{ODD}(min) + t_{RWL}(min) + t_{RP}(min) + 4t_T$.
23. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS}(min)$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD}(min)$, $t_{RWD} \geqq t_{RWD}(min)$, $t_{AWD} \geqq t_{AWD}(min)$, and $t_{CPWD} \geqq t_{CPWD}(min)$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed-write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter		Limits M5M44280A-8, -8S Min	Limits M5M44280A-8, -8S Max	Unit
t_{PC}	Fast Page mode read/write cycle time		50		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		100		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note 25)	135	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 26)	10	20	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 23)	45		ns

Note 24. All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25. $t_{RAS}(min)$ is specified as two cycles of $\overline{CAS}$ input are performed.
26. $t_{CP}(max)$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, Extended Refresh Cycle* (Note 27)

Symbol	Parameter	Limits M5M44280A-8, -8S Min	Limits M5M44280A-8, -8S Max	Unit
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	30		ns

Note 27. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle* (Note 28)

Symbol	Parameter	Limits M5M44280A-8S Min	Limits M5M44280A-8S Max	Unit
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	150		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	−50		ns

Note 28. Self refresh sequence
Two refreshing ways should be used properly depending on the low pulse width(t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 150ms$
1.1 Distriduted refresh during Read/Write operation
(A) Timing Diagrams

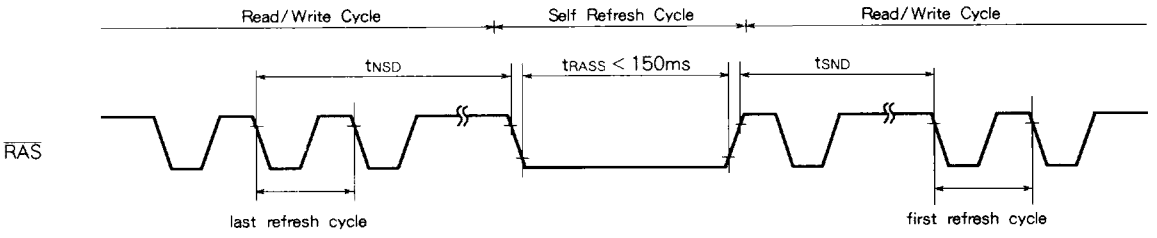


Table 1

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 8.2ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of distributed refresh
Definition of CBR distributed refresh
(Including extended refresh)
The CBR distributed refresh performs more than 512 constant period(125 μs max) CBR cycles within 64 ms.
Definition of $\overline{RAS}$ only distributed refresh
All combination of nine row address signals(A_0~A_8) are selected during 512 constant period(16 μs max) $\overline{RAS}$ only refresh cycles within 8.2 ms.

Note:
Hidden refresh may be used instead of CBR refresh,
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1.1 CBR distributed Refresh
- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD}(shown in table 1).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND}(shown in table 1).

1.1.2 $\overline{RAS}$ only distributed refresh
- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

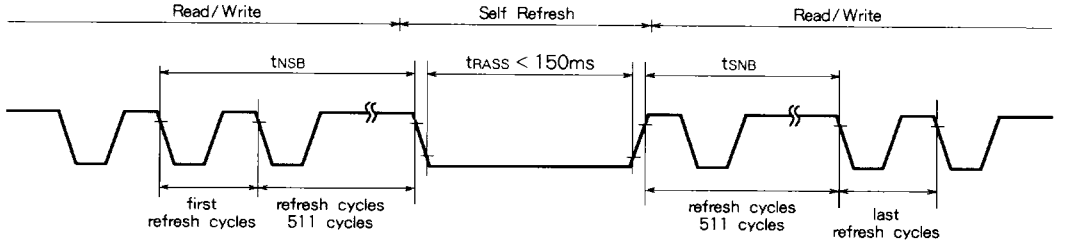


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 8.2ms$	$t_{SNB} \leqq 8.2ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 8.2ms$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more than 512 continuous CBR cycles within 8.2 ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of ten row address signals ($A_0 \sim A_8$) are selected during 512 continuous $\overline{RAS}$ only refresh cycles within 8.2 ms.

1.2.1 CBR distributed Refresh

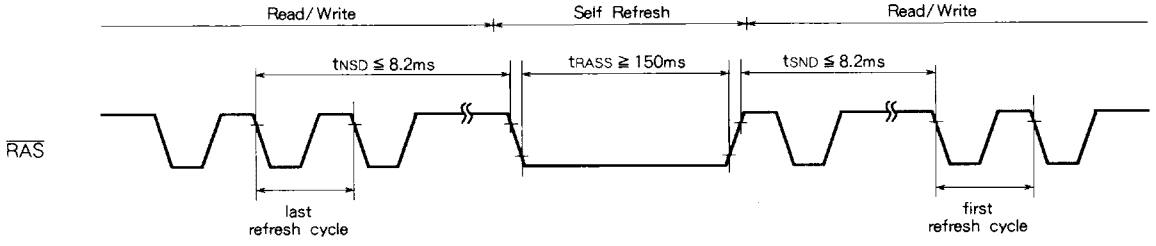
- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 8.2 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read /write operation period should be set within 8.2 ms.

1.2.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read /write operation period should be set within t_{SNB} (shown in table 2).

2. In case of $t_{RASS} \geqq 150ms$

(A) Timing diagram-A



Timing diagram-B

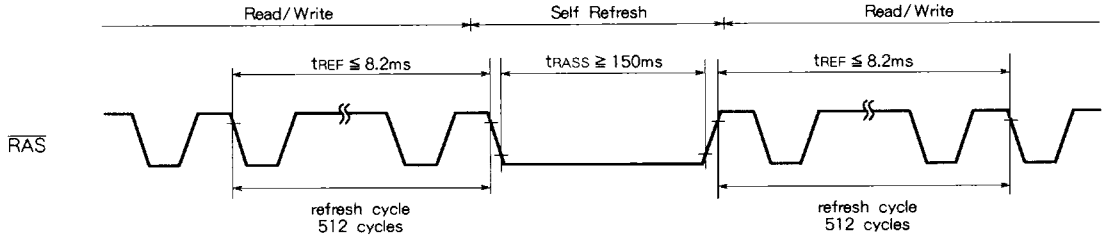


Table 3

Read/Write Cycle	Read/Write→Self Refresh	Self Refresh→Read/Write
CBR distributed refresh	Timing Diagram-A	Timing Diagram-A
$\overline{RAS}$ only distributed CBR burst refresh $\overline{RAS}$ only burst refresh	Timing Diagram-B	Timing Diagaram-B

(B) Definition of refresh

The same as 1.1-(B) and 1.2-(B)

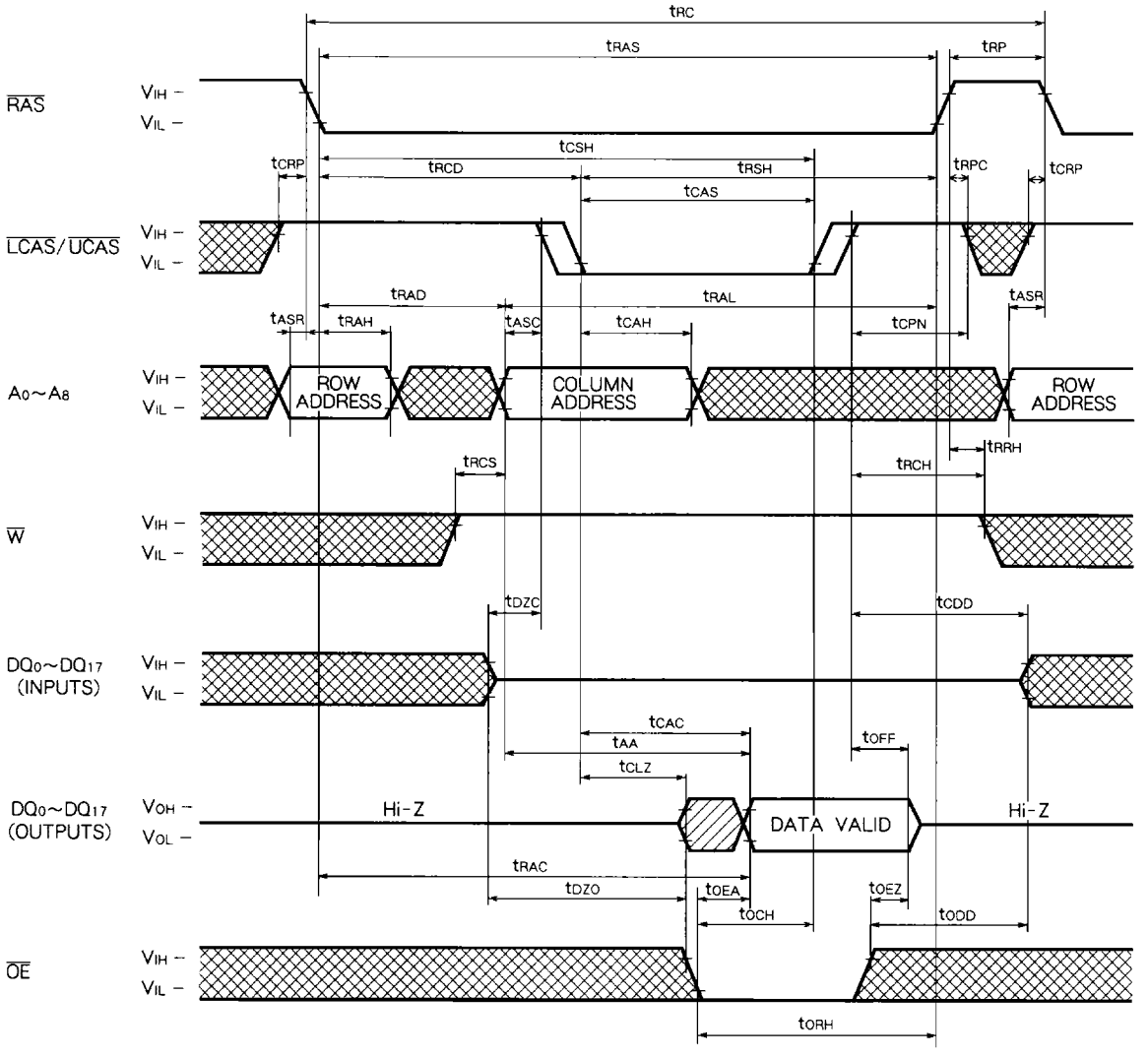
2.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 8.2 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read /write operation period should be set within 8.2 ms.

2.1.2 $\overline{RAS}$ only distributed, CBR burst, $\overline{RAS}$ only burst refresh

- Before and after the self refresh, 512 refresh cycles should be executed within 8.2 ms for each refresh operation.

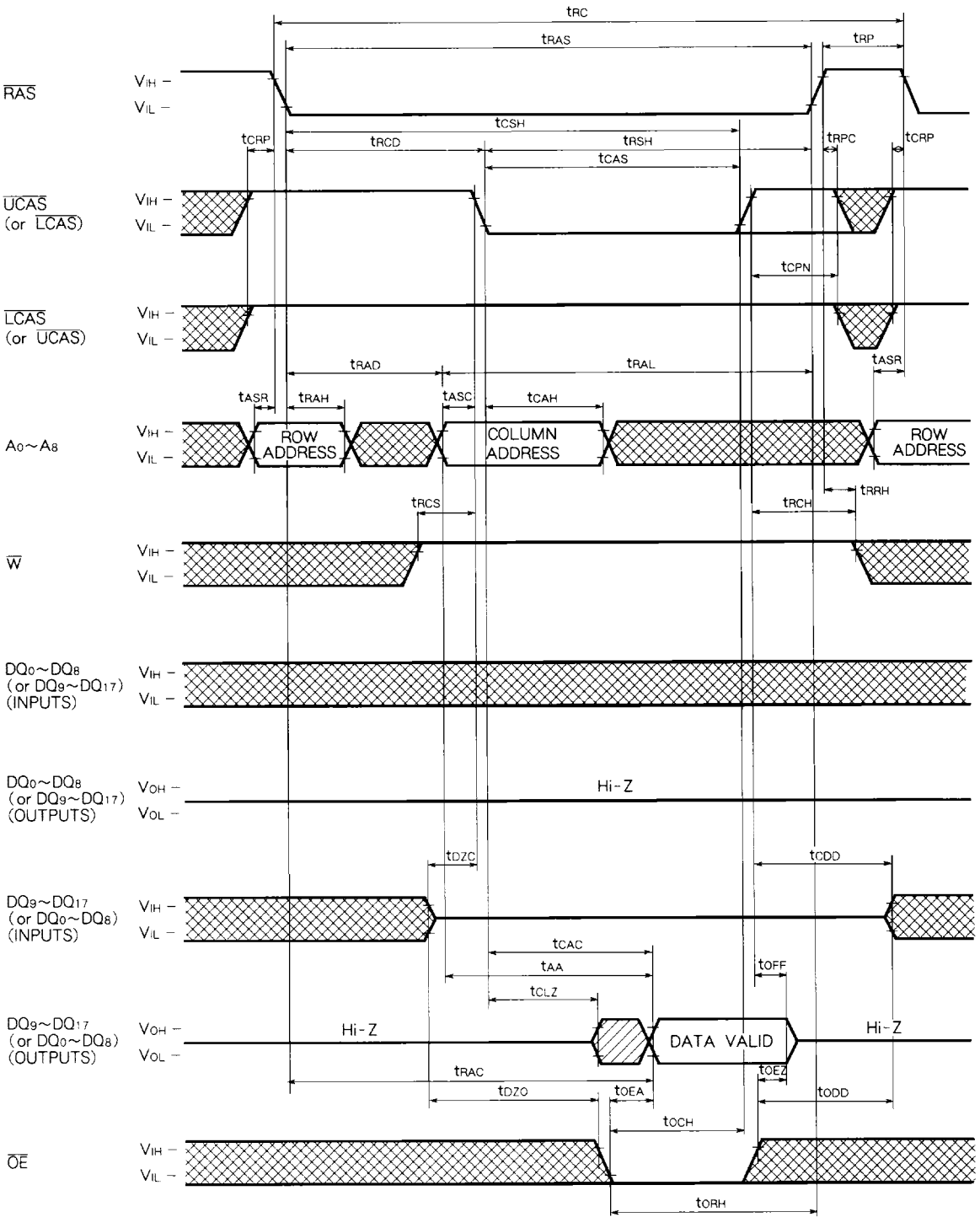
Timing Diagrams (Note 29)
Read Cycle



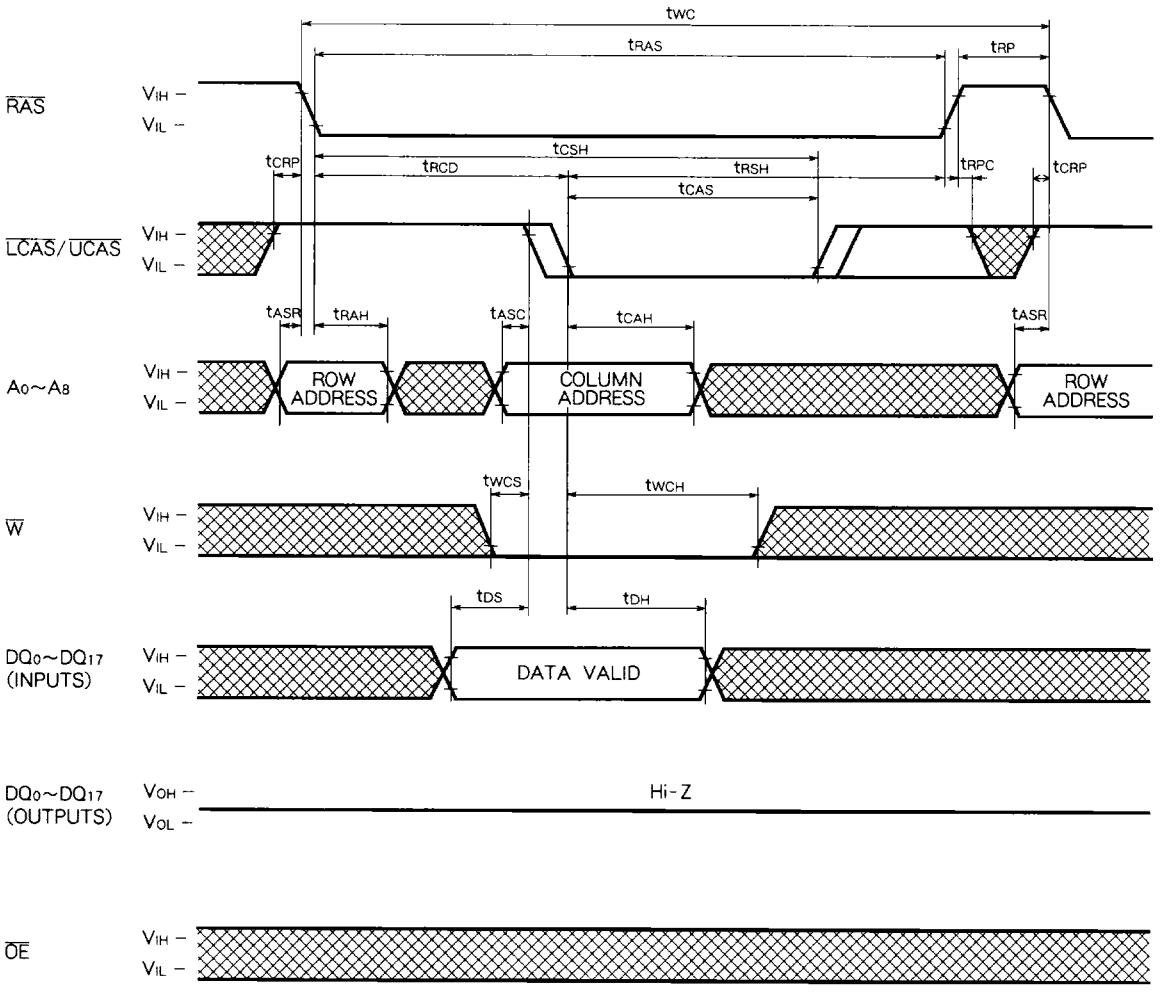
Note 29 — Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$

Indicates the invalid output.

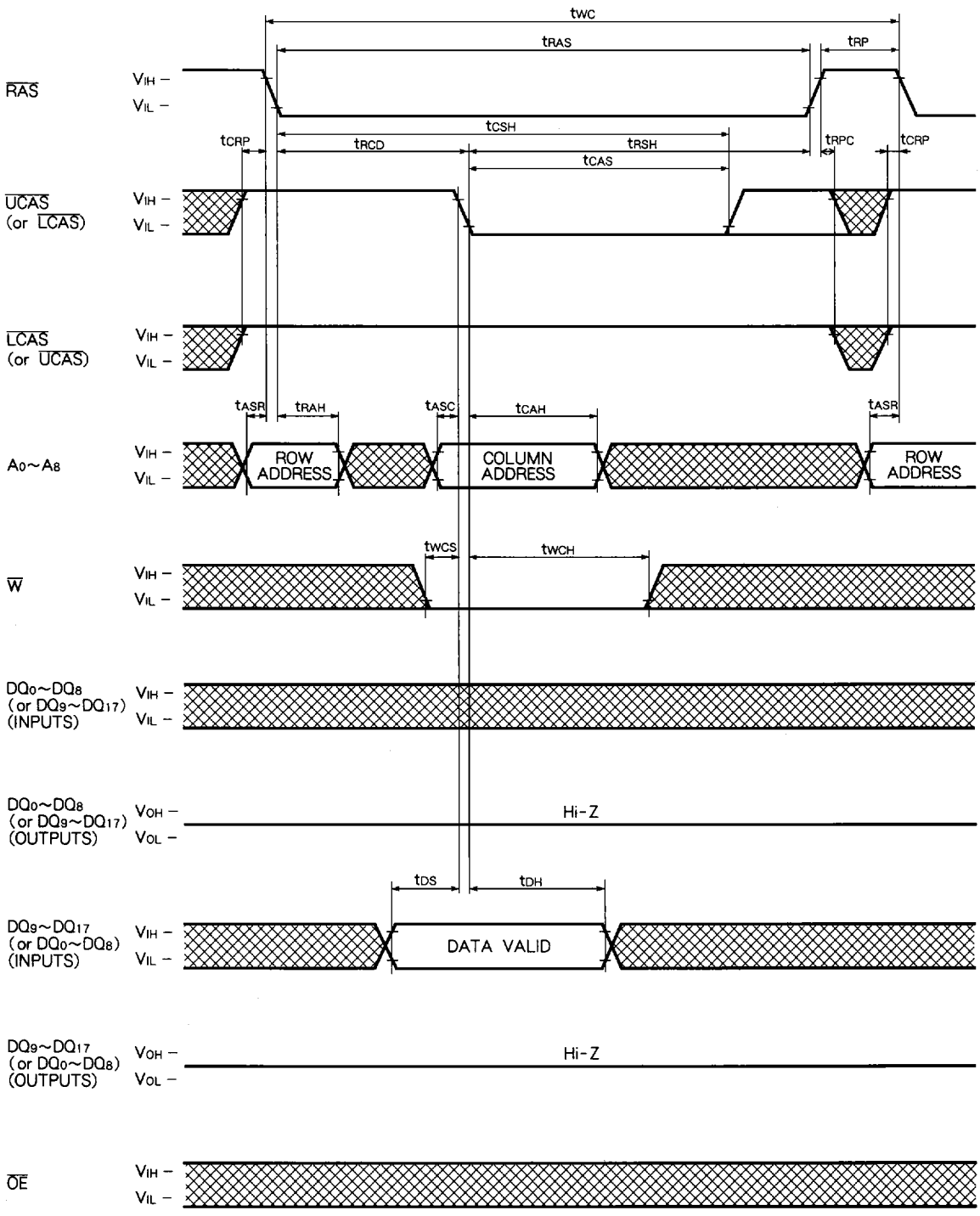
Byte Read Cycle



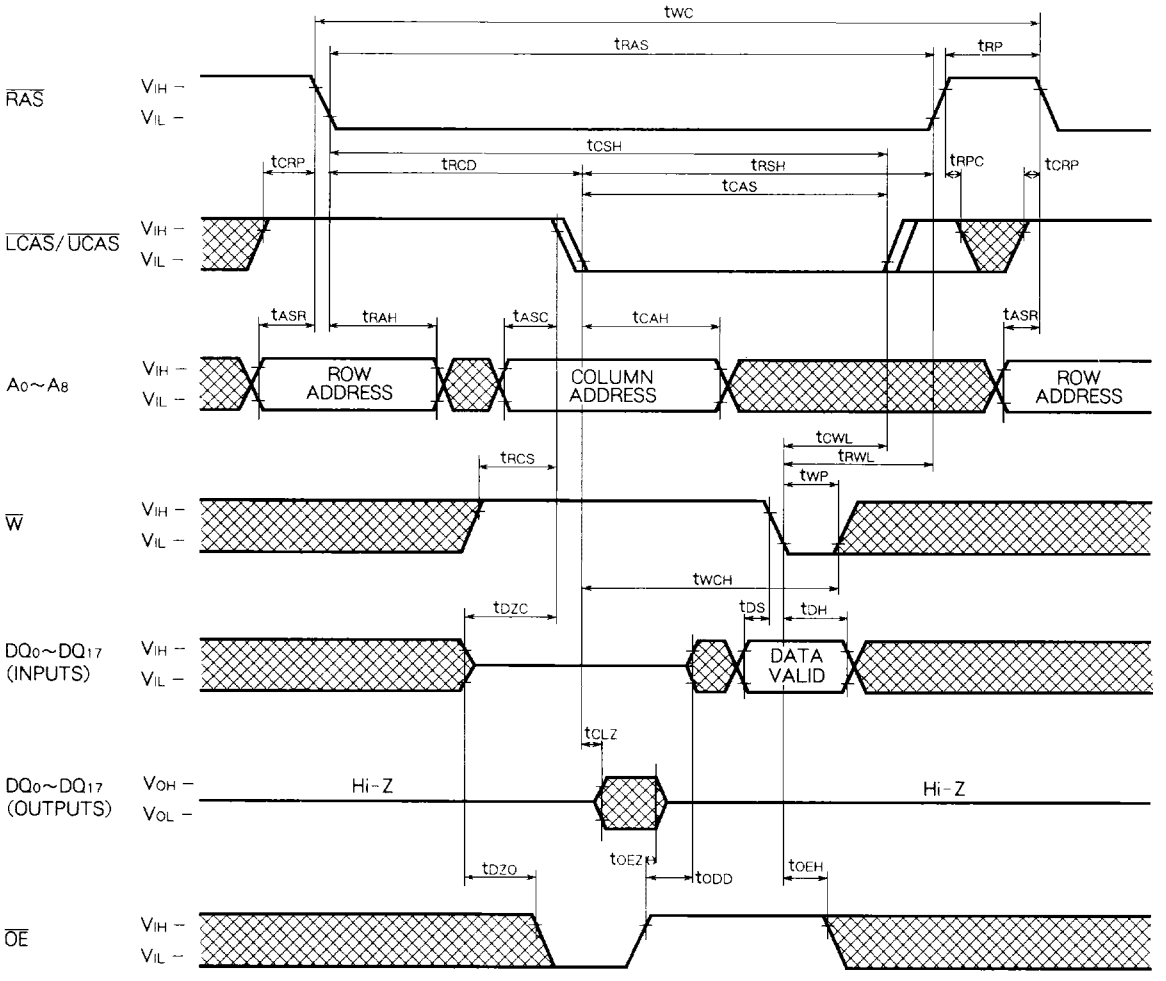
Write Cycle (Early write)



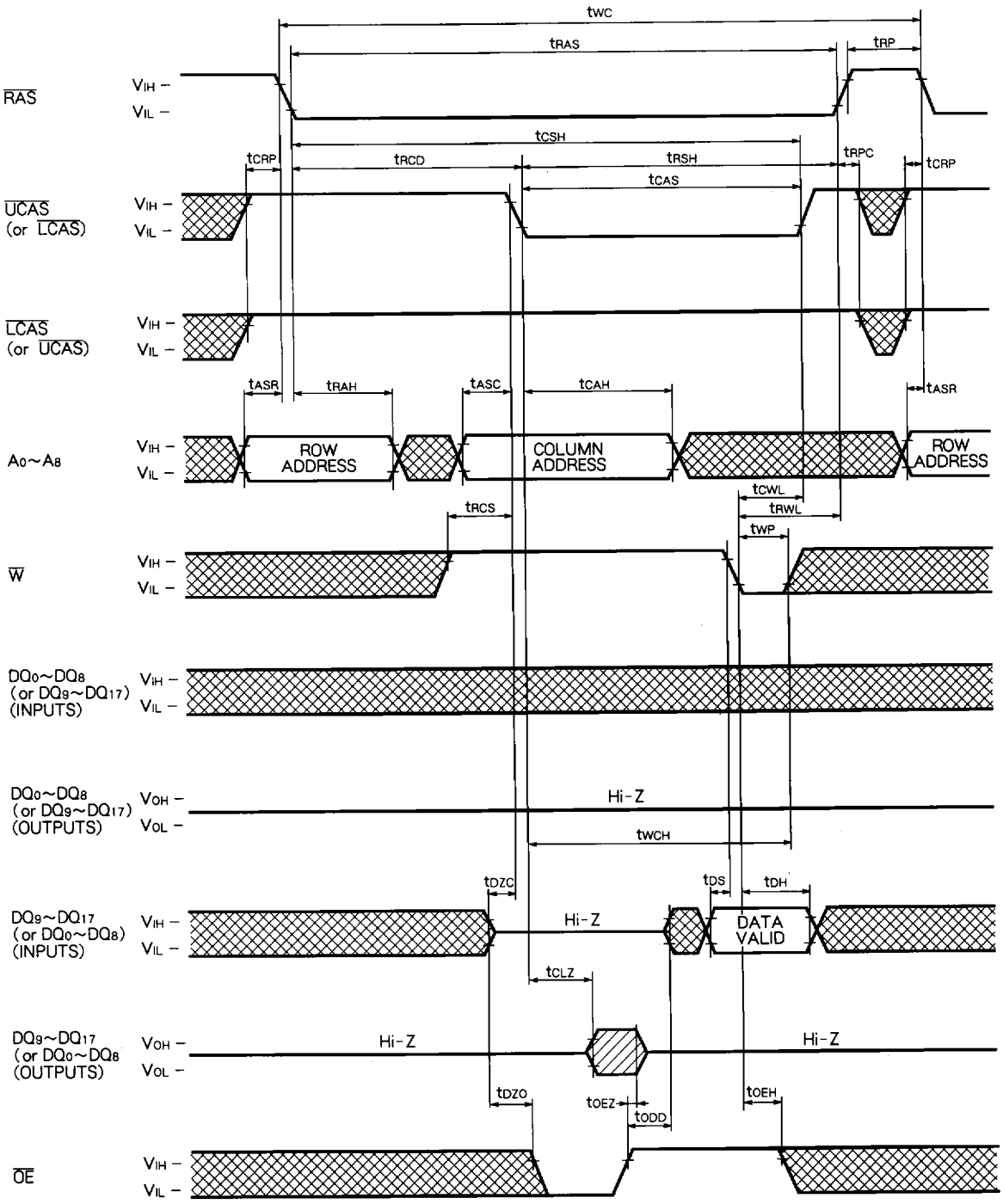
Byte Write Cycle (Early write)



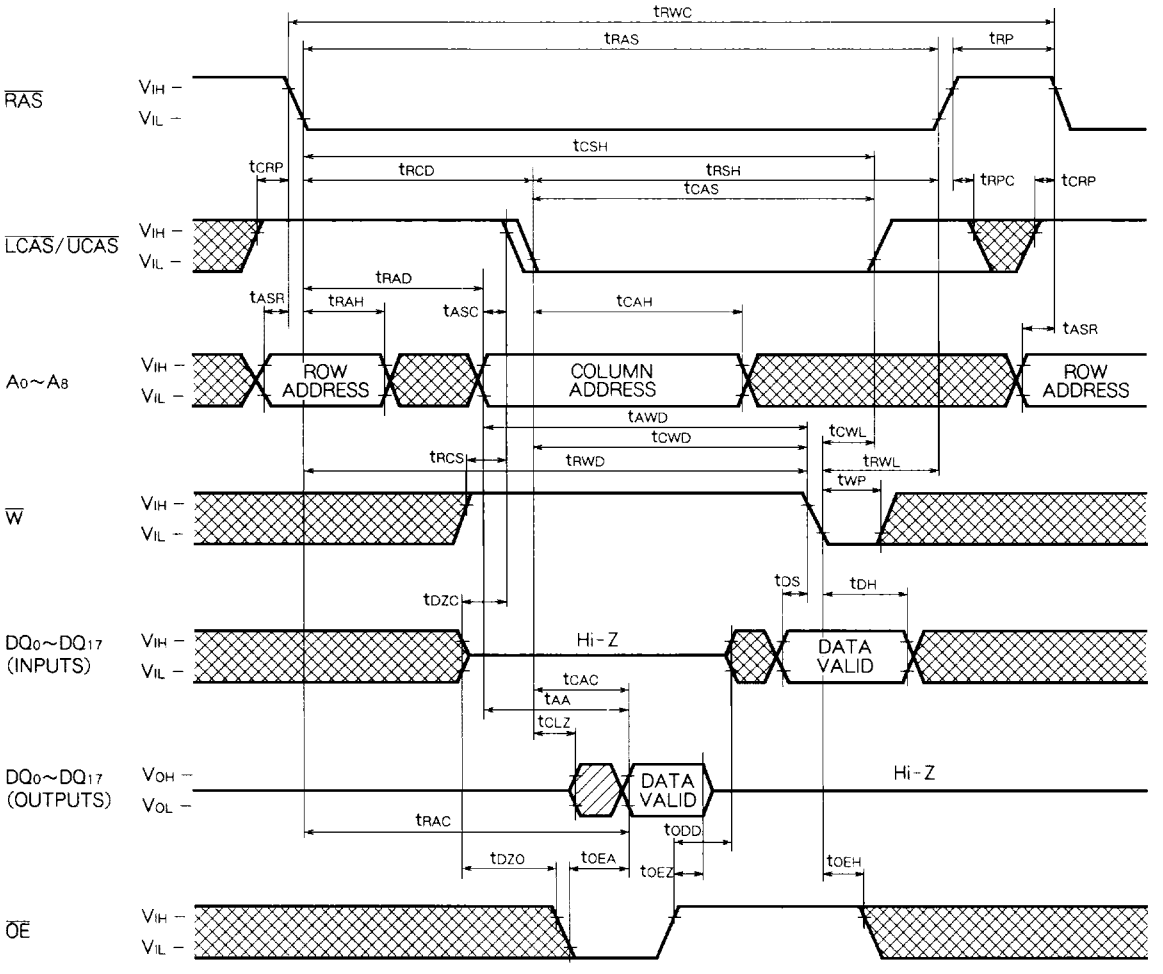
Write Cycle (Delayed write)



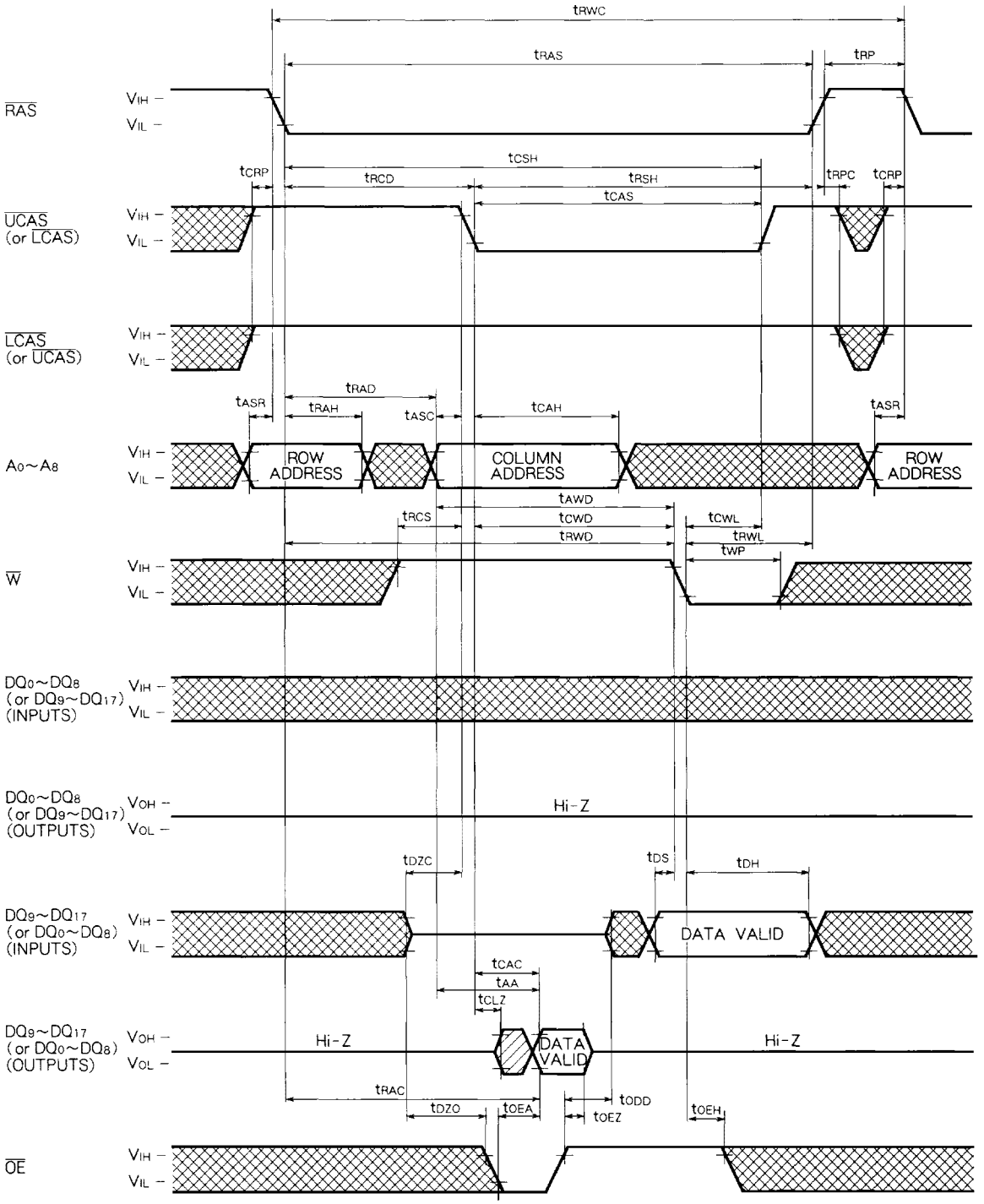
Byte Write Cycle (Delayed write)



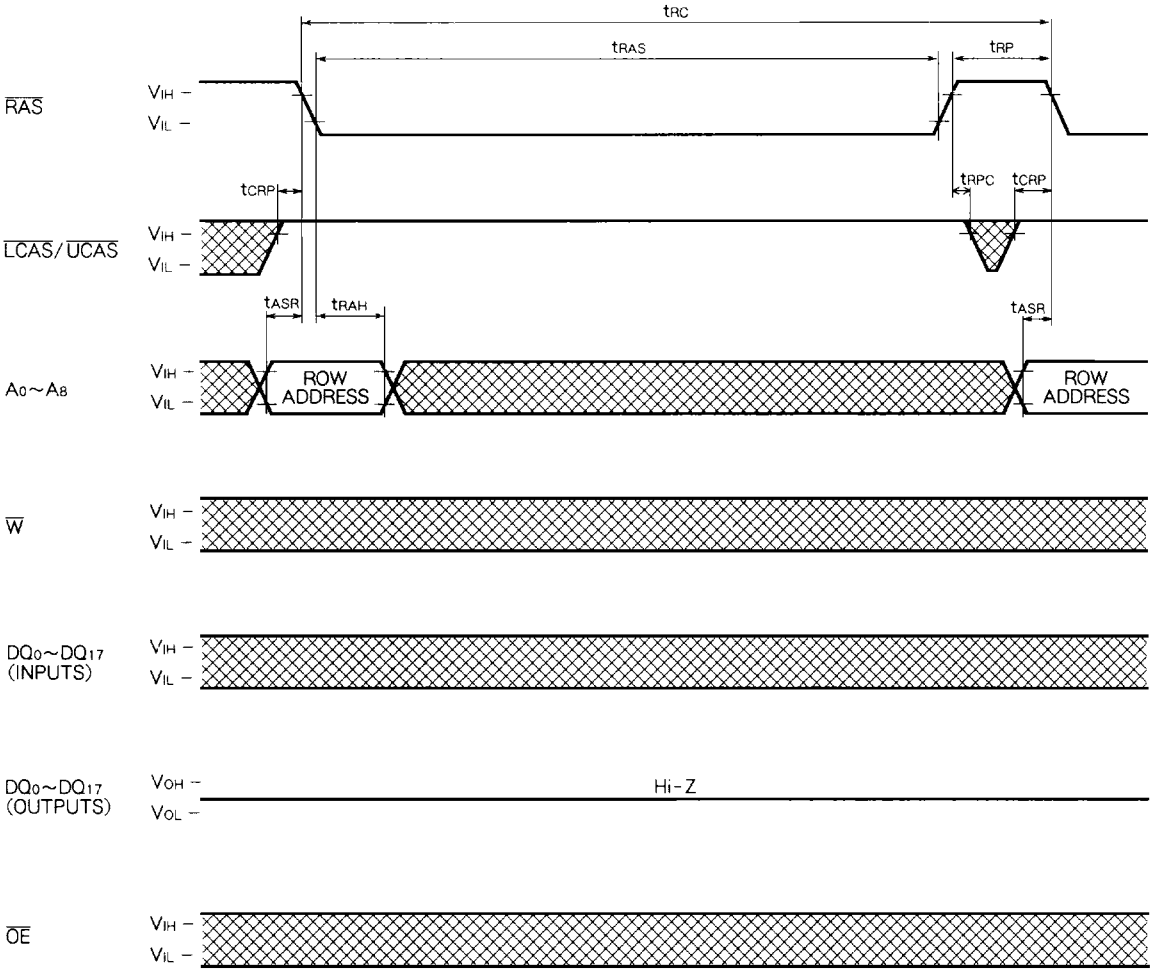
Read - Write, Read - Modify - Write Cycle



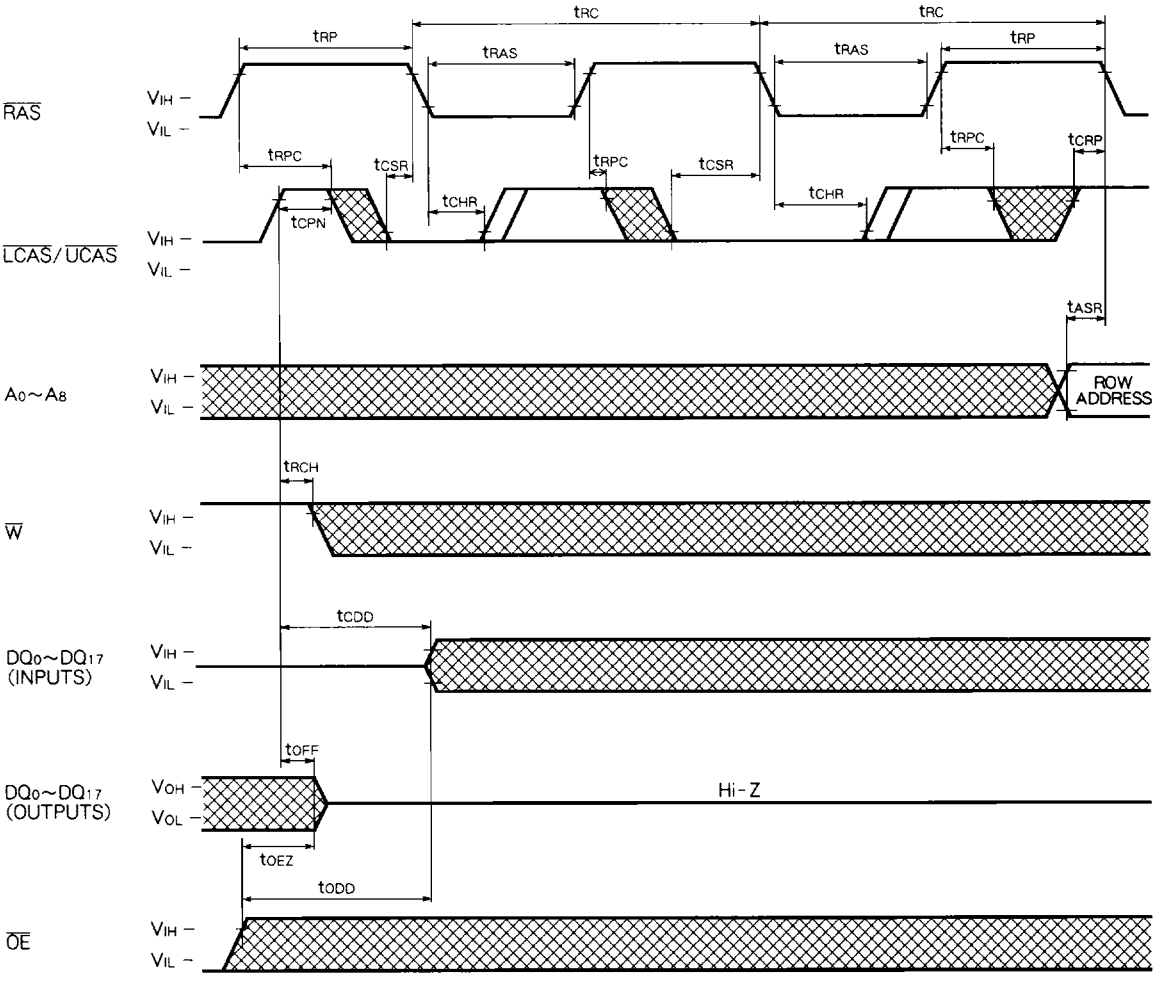
Byte Read Write, Read - Modify Write Cycle



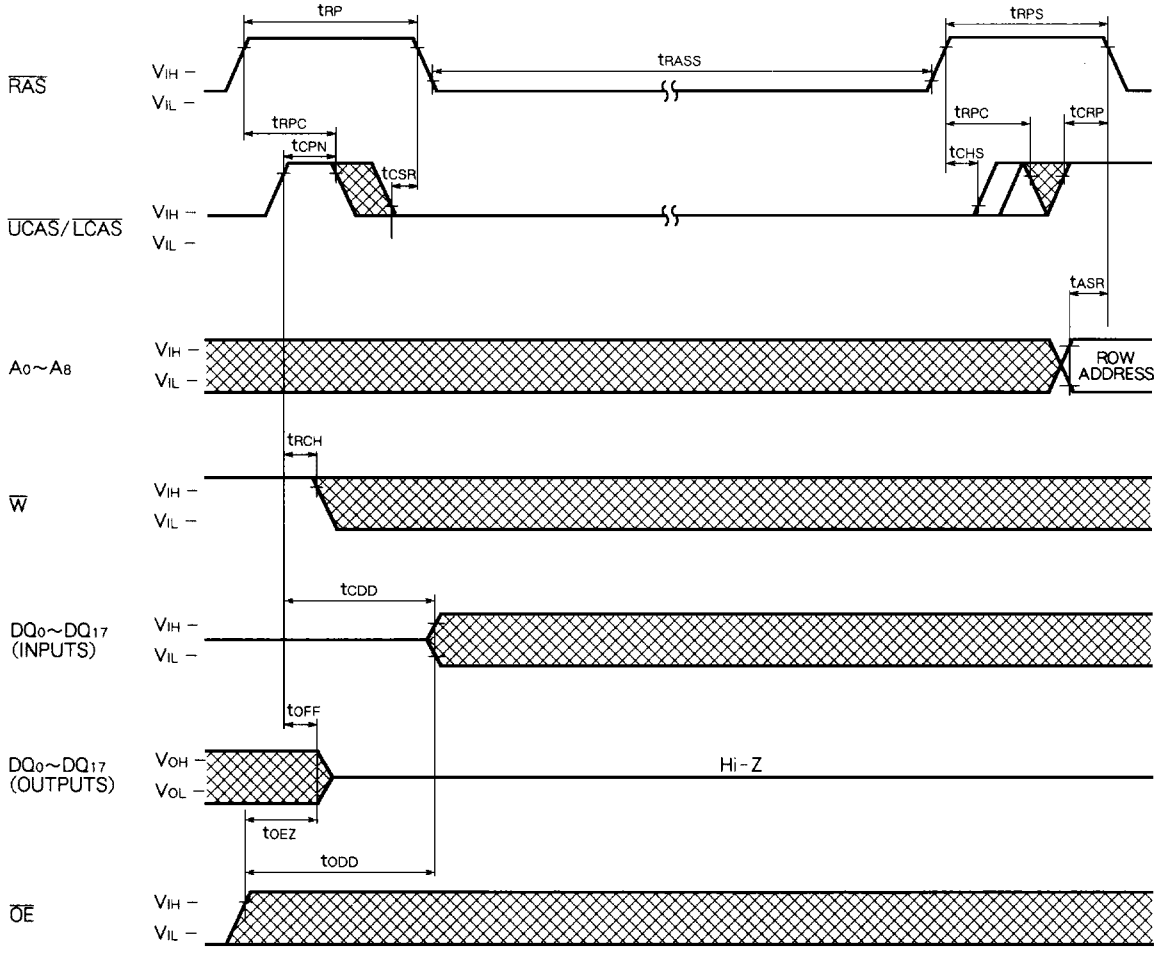
$\overline{RAS}$-only Refresh Cycle



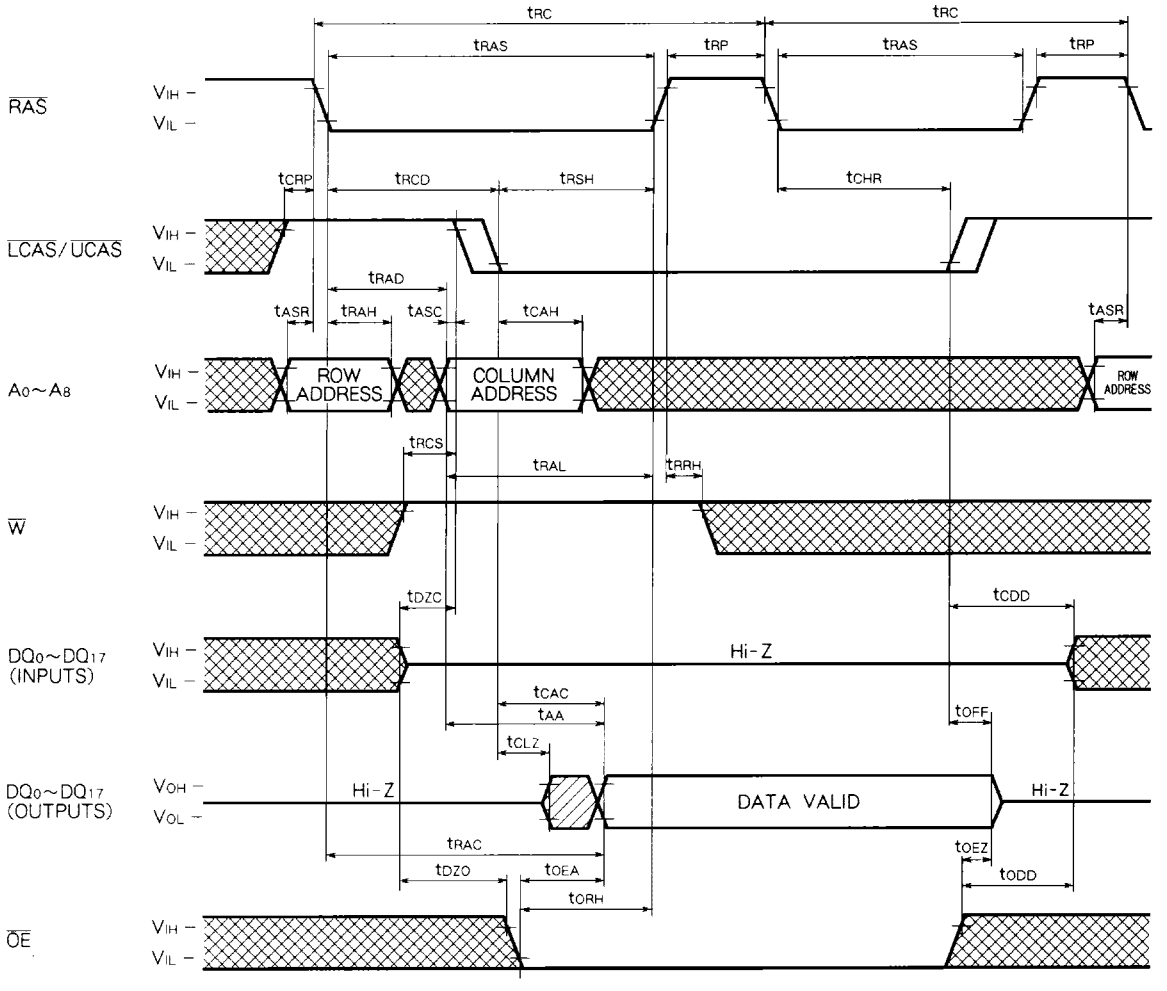
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*



Self Refresh Cycle* (Note 28)

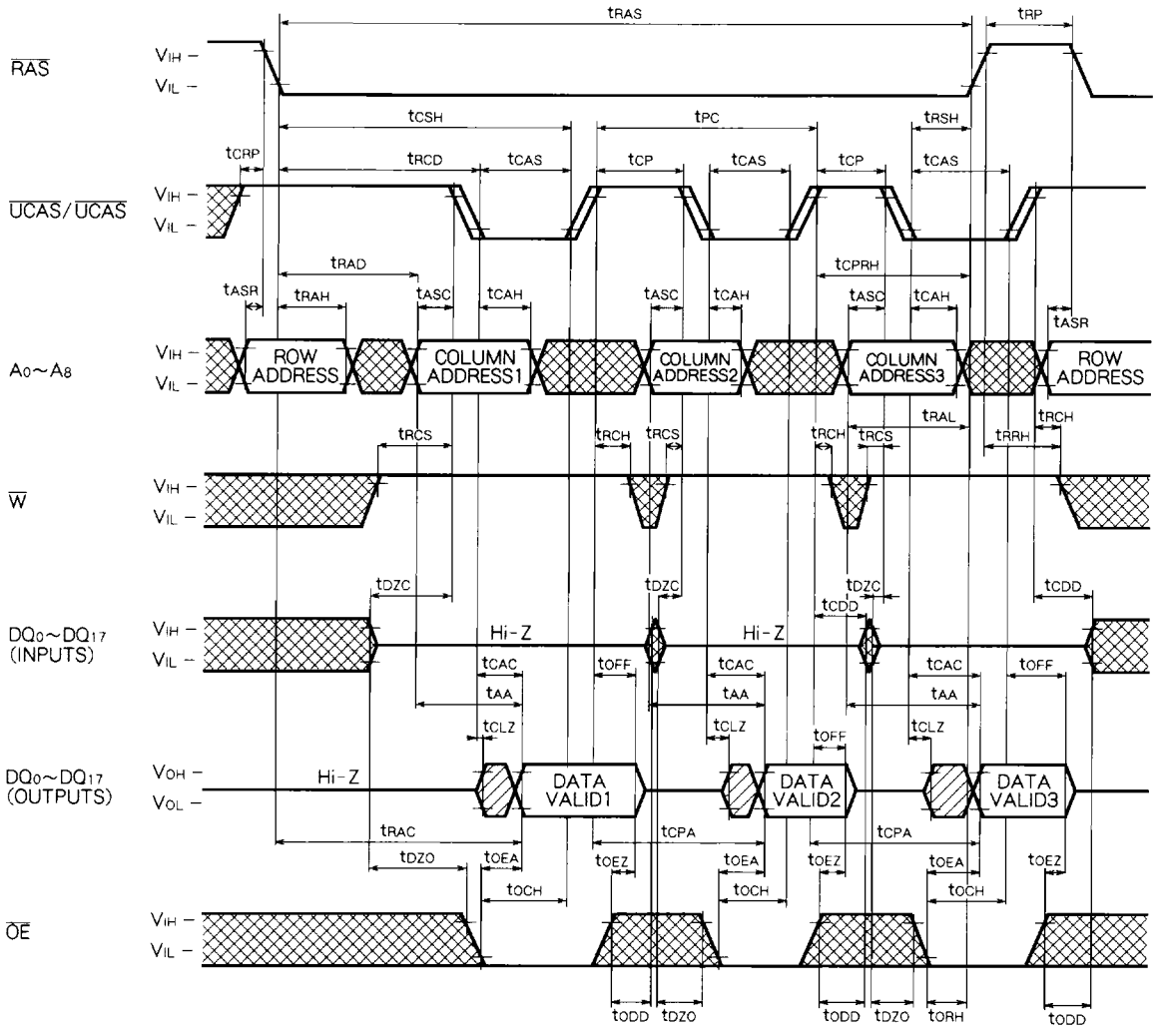


Hidden Refresh Cycle (Read) (Note 30)

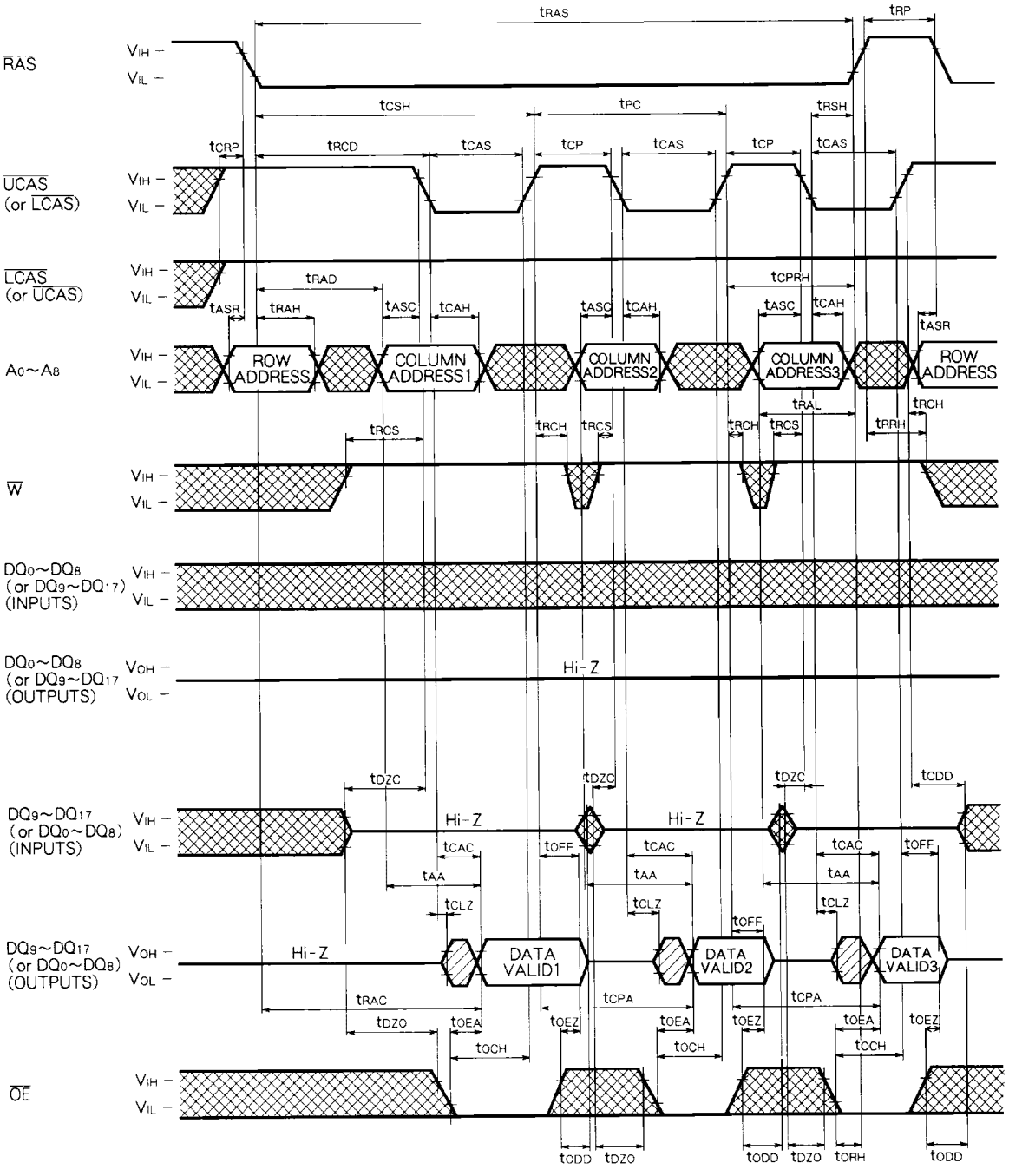


Note 30 Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each ecyle shown above.

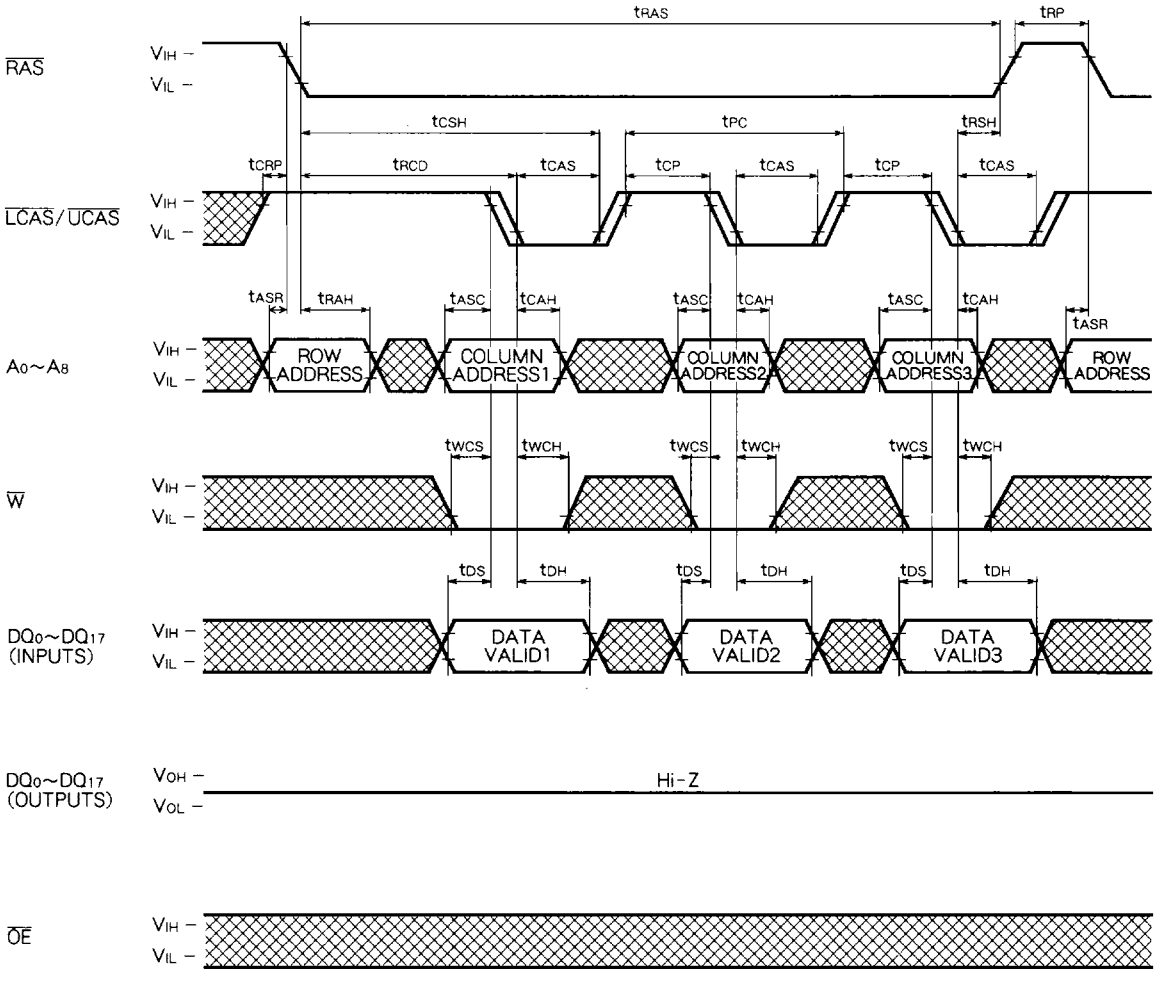
Fast Page Mode Read Cycle



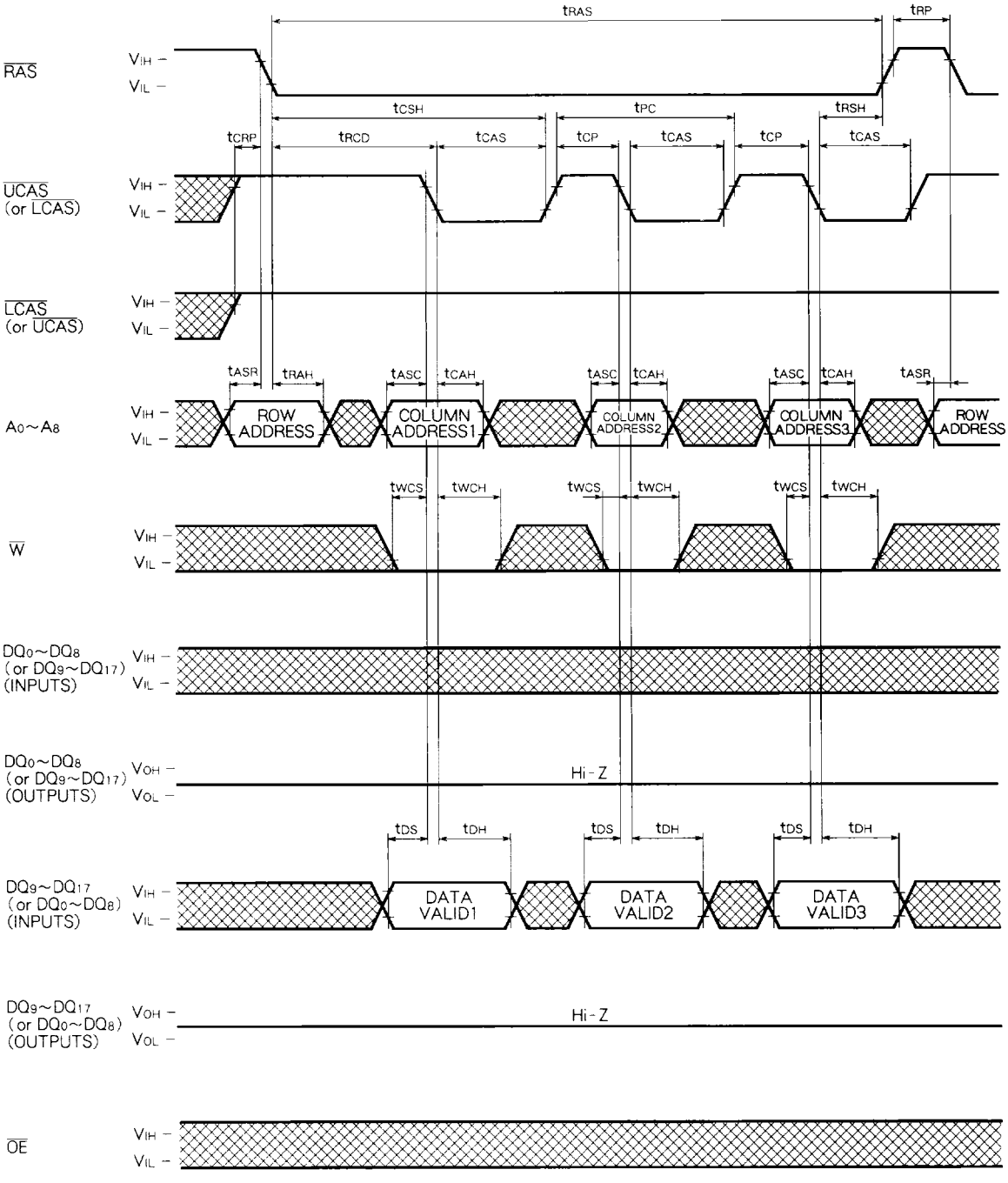
Fast Page Mode Byte Read Cycle



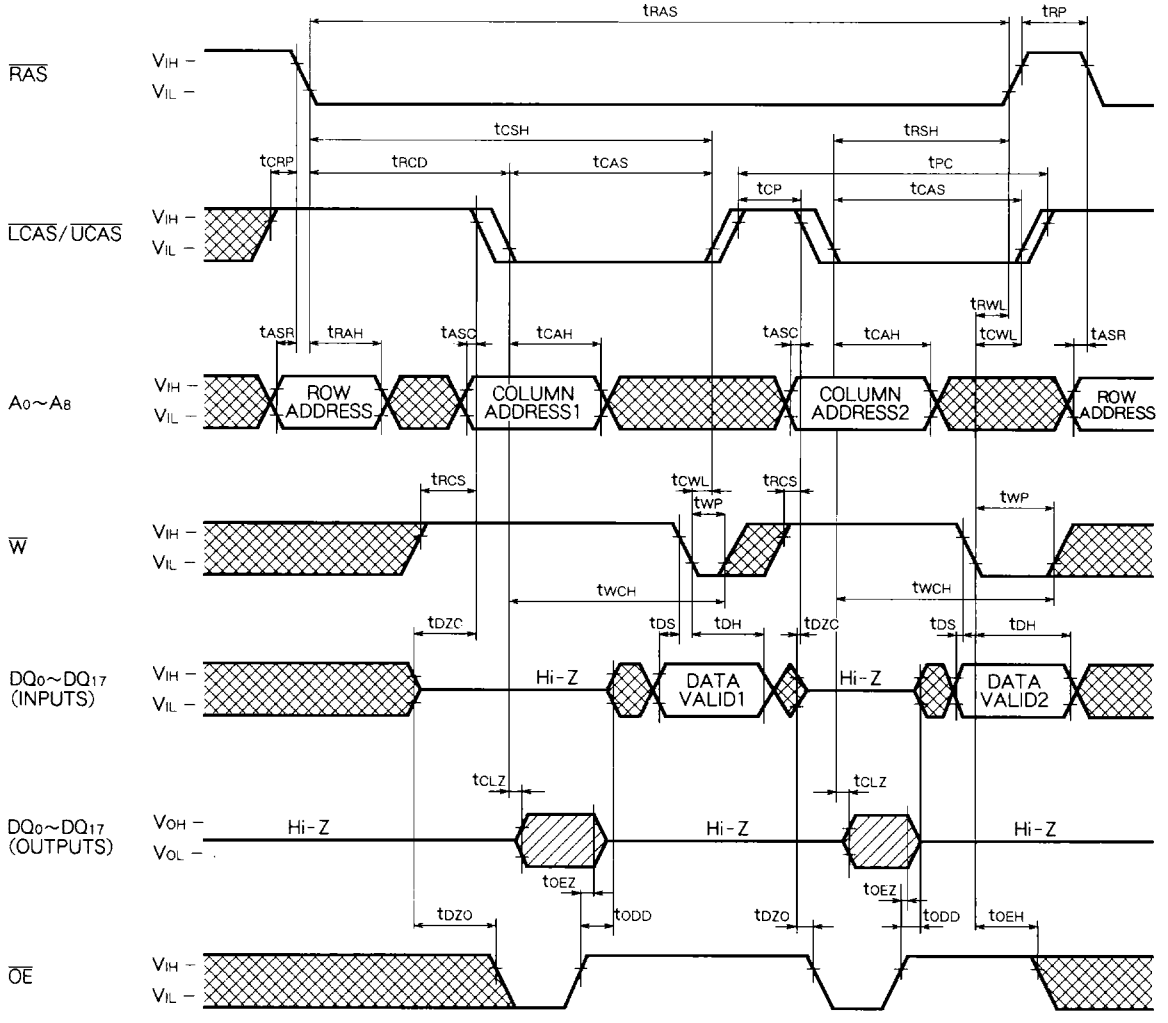
Fast Page Mode Write Cycle (Early Write)



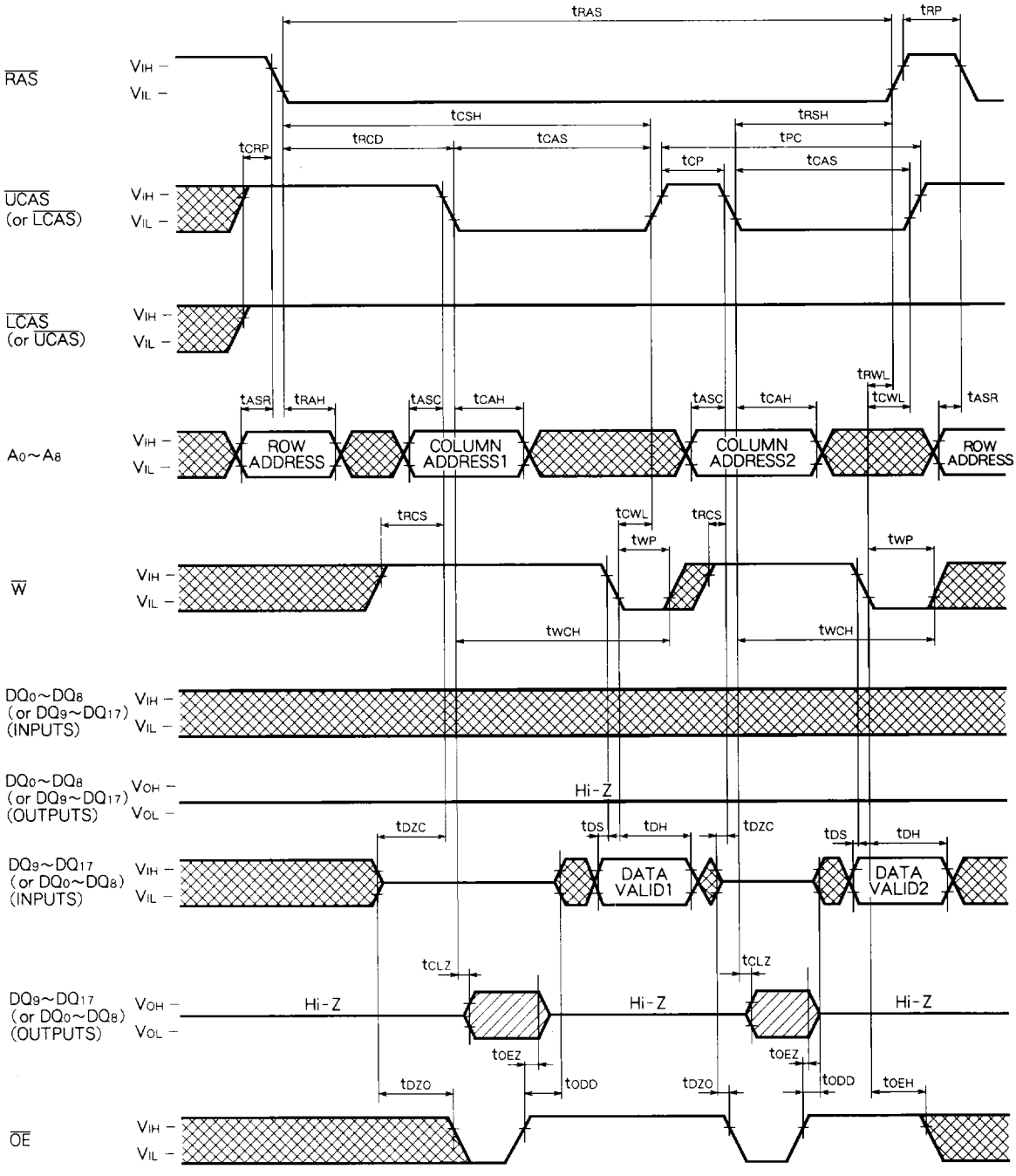
Fast Page Mode Byte Write Cycle (Early Write)



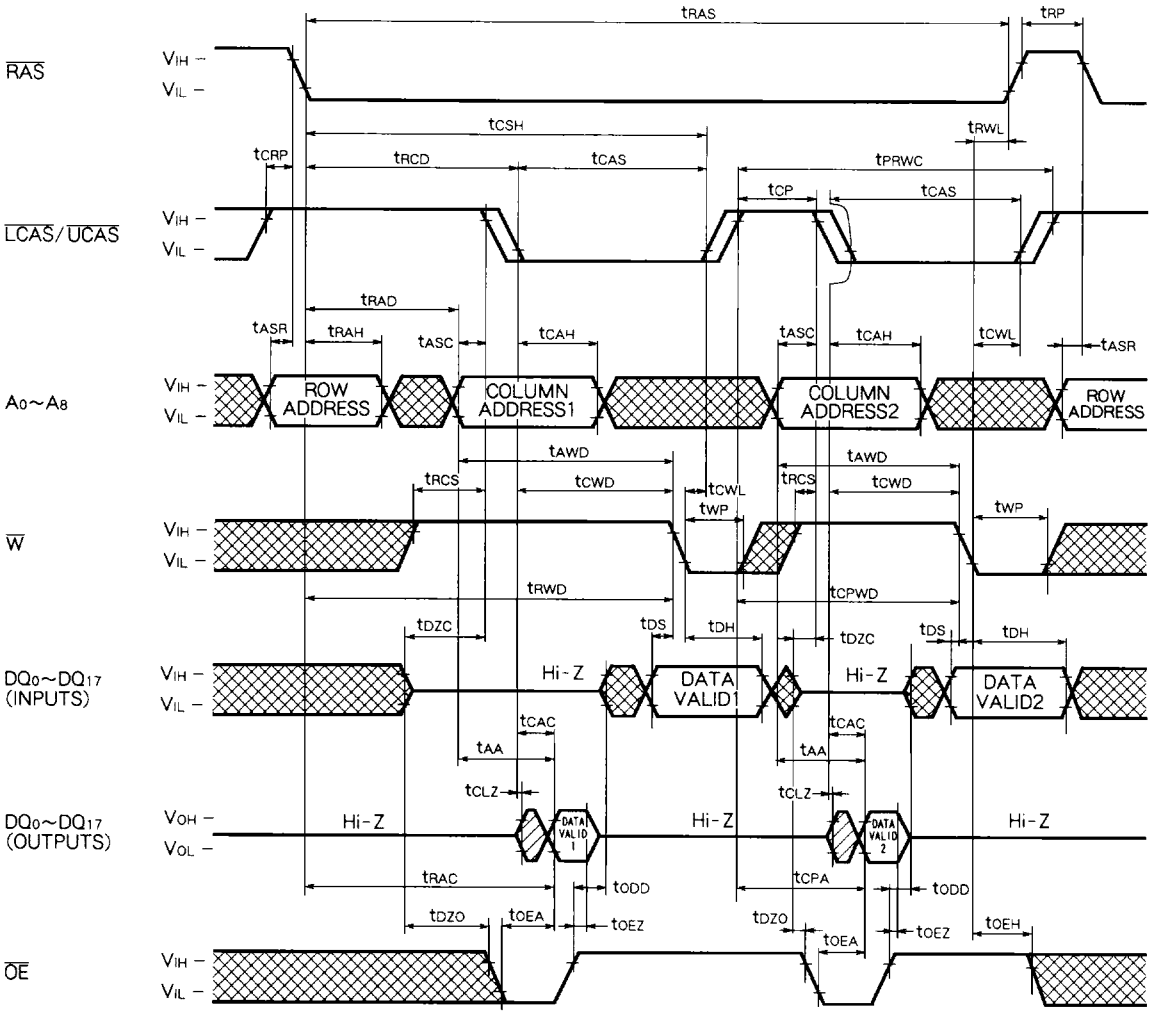
Fast Page Mode Write Cycle (Delayed Write)



Fast Page Mode Byte Write Cycle (Delayed Write)



Fast Page Mode Read - Write, Read - Modify - Write Cycle



Fast Page Mode Byte Read Write, Read - Modify Write Cycle