

M5M44260AJ,TP,RT-7,-8,-7S,-8S

FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs.

Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

This device has 2 $\overline{CAS}$ and 1 $\overline{W}$ terminals. Refresh cycle is 512 cycles every 8 ms.

FEATURES

Type name	RAS access time (max. ns)	CAS access time (max. ns)	Address access time (max. ns)	OE access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M44260AXX-7,-7S	70	20	35	20	140	685
M5M44260AXX-8,-8S	80	20	40	20	160	580

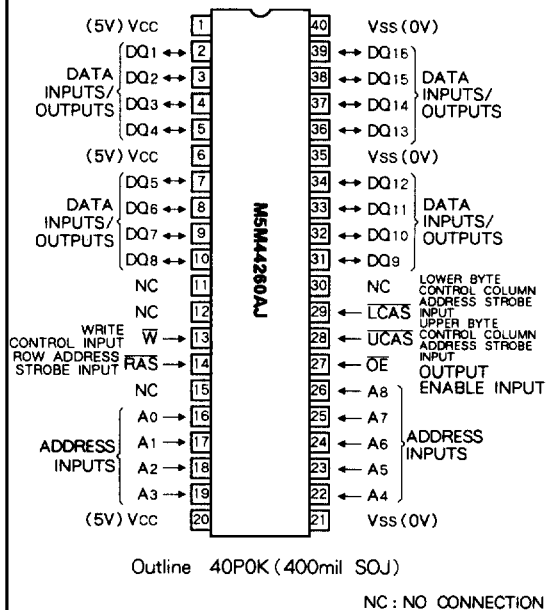
XX = J, TP, RT

- 40pin 400mil SOJ, 44pin 400mil TSOP (II)
- Single 5V $\pm$ 10% supply
- Low stand-by power dissipation
 - 5.5mW (max) CMOS Input level
 - 0.55mW* (max) CMOS Input level
- Low operating power dissipation
 - M5M44260AXX-8,-8S 770mW (max)
- Fast-page mode (512-bit random access), Read-modify-Write, RAS-only refresh, $\overline{CAS}$ before RAS refresh, Hidden refresh capabilities
- Self refresh capability*
 - Self refresh current 300 μ s
- Extended refresh capability*
 - Extended refresh current 350 μ s
- Early write mode and OE to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 512 refresh cycles every 8ms (A₀~A₈)
- 512 refresh cycles every 64ms (A₀~A₈)*
- Byte or Word control for Read/Write operation (2 $\overline{CAS}$, 1 $\overline{W}$ type)
 - * : Applicable to self refresh version (M5M44260AJ, TP, RT-7S,-8S: option) only.

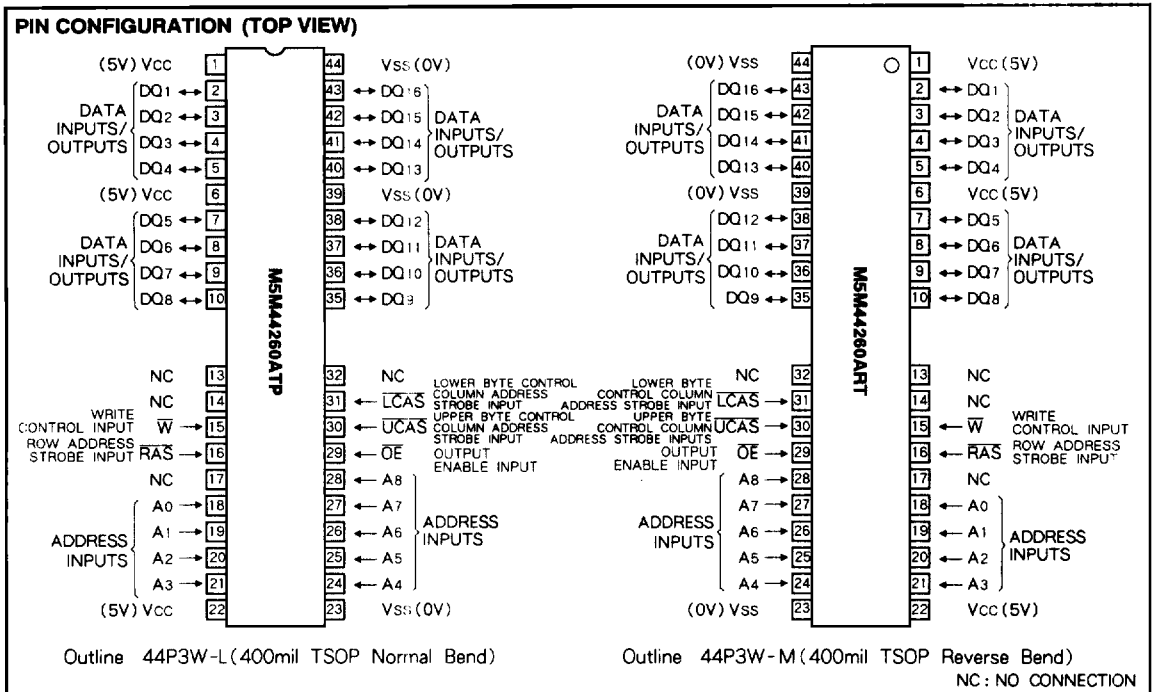
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM



FUNCTION

The M5M44260AJ,TP,RT provide, in addition to normal read, write, and read-modify-write operations, a number of other

functions, e.g., fast page mode, $\overline{\text{RAS}}$ -only refresh, and delayed -write. The input conditions for each are shown in Table 1.

Table 1. Input condition for each mode

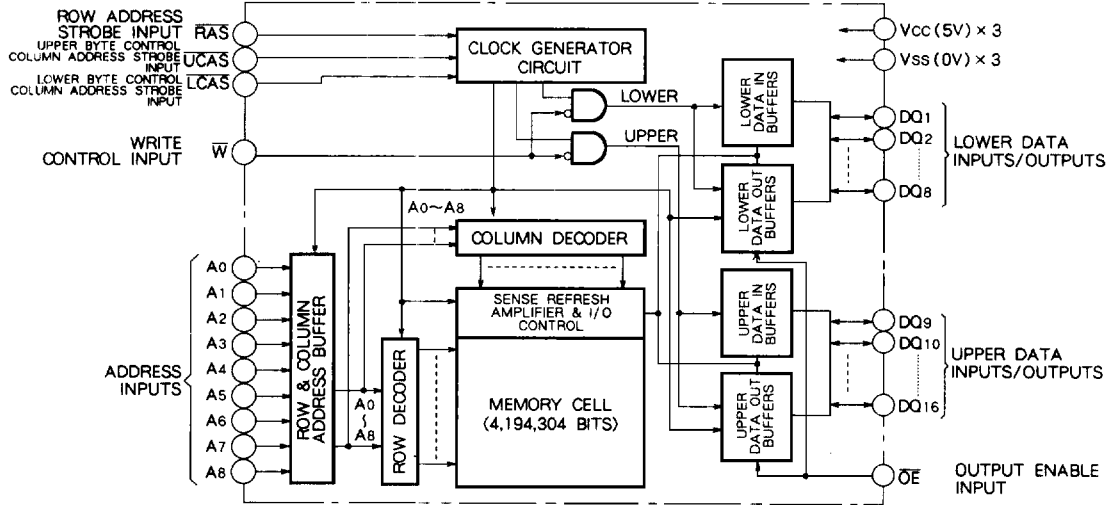
Operation	Inputs							Input/Output				Refresh	Remark
	RAS	LCAS	UCAS	W	OE	Row address	Column address	Lower		Upper			
Read	ACT	ACT	ACT	NAC	ACT	APD	APD	OPN	IVD	OPN	IVD	YES	Fast page mode identical
Upper read	ACT	NAC	ACT	NAC	ACT	APD	APD	DNC	OPN	OPN	IVD	YES	
Lower read	ACT	ACT	NAC	NAC	ACT	APD	APD	OPN	IVD	DNC	OPN	YES	
Early write	ACT	ACT	ACT	ACT	DNC	APD	APD	IVD	OPN	IVD	OPN	YES	
Upper early	ACT	NAC	ACT	ACT	DNC	APD	APD	DNC	OPN	IVD	OPN	YES	
Lower early	ACT	ACT	NAC	ACT	DNC	APD	APD	IVD	OPN	DNC	OPN	YES	
Delayed write	ACT	ACT	ACT	ACT	DNC	APD	APD	IVD	OPN	IVD	OPN	YES	
Upper delayed	ACT	NAC	ACT	ACT	DNC	APD	APD	DNC	OPN	IVD	OPN	YES	
Lower delayed	ACT	ACT	NAC	ACT	DNC	APD	APD	IVD	OPN	DNC	OPN	YES	
Read-Modify-Write	ACT	ACT	ACT	ACT	ACT	APD	APD	IVD	IVD	IVD	IVD	YES	
Upper R-M-W	ACT	NAC	ACT	ACT	ACT	APD	APD	DNC	OPN	IVD	IVD	YES	
Lower R-M-W	ACT	ACT	NAC	ACT	ACT	APD	APD	IVD	IVD	DNC	OPN	YES	
RAS-only refresh	ACT	NAC	NAC	DNC	DNC	APD	DNC	DNC	OPN	DNC	OPN	YES	
Hidden refresh	ACT	ACT	ACT	DNC	ACT	DNC	DNC	OPN	IVD	OPN	IVD	YES	
CAS before RAS(Extended)* refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Self refresh*	ACT	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	NO	

Note ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

M5M44260AJ, TP, RT-7, -8, -7S, -8S

FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT) DYNAMIC RAM

BLOCK DIAGRAM



M5M44260AJ,TP,RT-7,-8,-7S,-8S**FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM****ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1~7	V
V _I	Input voltage		-1~7	V
V _O	Output voltage		-1~7	V
I _O	Output current		50	mA
P _e	Power dissipation	T _a = 25°C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low-level input voltage	DQ ₀ ~DQ ₁₅	-1.0	0.8	V
		Others	-2.0	0.8	

Note 1. All voltage values are with respect to V_{SS}.**ELECTRICAL CHARACTERISTICS** (T_a = 0~70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{O1}	High-level output voltage	I _{OH} = -5mA	2.4		V _{CC}	V
V _{O1}	Low-level output voltage	I _{OL} = 4.2mA			0.4	V
I _{OZ}	Off-state output current	Q floating, 0V ≤ V _{OUT} ≤ 5.5V	-10		10	μA
I _I	Input current	0 ≤ V _{IN} ≤ 6.5V, Other inputs pins=0V	-10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} , operating (Note 3, 4, 5)	M5M44260A-7, -7S RAS, CAS cycling			165	mA
		M5M44260A-8, -8S trc = twc = min. output open			140	
I _{CC2} (AV)	Supply current from V _{CC} , stand-by (Note 6)	RAS = CAS = V _{IH} , output open			2	mA
		RAS = CAS ≤ V _{CC} - 0.5V output open			1	
					0.1*	
I _{CC3} (AV)	Average supply current from V _{CC} , refreshing (Note 3, 5)	M5M44260A-7, -7S RAS cycling, CAS = V _{IH} ,			165	mA
		M5M44260A-8, -8S trc = min. output open			140	
I _{CC4} (AV)	Average supply current from V _{CC} , Fast-Page-Mode (Note 3, 4, 5)	M5M44260A-7, -7S RAS = V _{IL}			165	mA
		M5M44260A-8, -8S CAS cycling tpc = min., output open			140	
I _{CC5} (AV)	Average supply current from V _{CC} , CAS before RAS refresh mode (Note 3, 5)	M5M44260A-7, -7S CAS before RAS refresh cycling, trc = min.			165	mA
		M5M44260A-8, -8S output open			140	
I _{CC8} (AV)*	Average supply current from V _{CC} Extended refresh mode (Note 6)	Stand-by : RAS ≥ V _{CC} - 0.2V CAS ≥ V _{CC} - 0.2V or CAS ≤ 0.2V before RAS refresh : RAS cycling CAS ≤ 0.2V or CAS before RAS refresh cycling W ≤ 0.2V or ≥ V _{CC} - 0.2V OE ≤ 0.2V or ≥ V _{CC} - 0.2V A ₀ ~A ₉ ≤ 0.2V or ≥ V _{CC} - 0.2V DQ = open trc = 125 μs TRAS = TRAS min ~ 1 μs			350	μA
I _{CC9} (AV)*	Average supply current from V _{CC} Self refresh mode (Note 6)	RAS = CAS ≤ 0.2V, OE ≤ 0.2V or ≥ V _{CC} - 0.2V, W ≤ 0.2V or ≥ V _{CC} - 0.2V, A ₀ ~A ₈ ≤ 0.2V or ≥ V _{CC} - 0.2V			300	μA

Note 2. Current flowing into an IC is positive, out is negative.

3. I_{CC1}(AV), I_{CC3}(AV) and I_{CC4}(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.4. I_{CC1}(AV) and I_{CC4}(AV) are dependent on output loading. Specified values are obtained with the output open.5. Column Address can be changed once or less while RAS = V_{IL} and CAS = V_{IH}.

M5M44260AJ,TP,RT-7,-8,-7S,-8S**FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM****CAPACITANCE** ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{i(A)}$	Input capacitance, address inputs	$V_i = V_{SS}$			5	pF
$C_{i(CLK)}$	Input capacitance, clock inputs	$f = 1\text{MHz}$			7	pF
$C_{i/o}$	Input/Output capacitance, data ports	$V_i = 25mV_{rms}$			7	pF

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter	Limits				Unit
		M5M44260A-7, -7S		M5M44260A-8, -8S		
		Min	Max	Min	Max	
tCAC	Access time from CAS (Note 7, 8)		20		20	ns
tRAC	Access time from RAS (Note 7, 9)		70		80	ns
tAA	Column Address access time (Note 7, 10)		35		40	ns
tCPA	Access time from CAS precharge (Note 7, 11)		40		45	ns
tOEA	Access time from OE (Note 7)		20		20	ns
tCLZ	Output low impedance from CAS low (Note 7)	5		5		ns
tOFF	Output disable time after CAS high (Note 12)	0	20	0	20	ns
tOEZ	Output disable time after OE high (Note 12)	0	20	0	20	ns

Note 6. An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$ -only refresh).

Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 8 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7. Measured with a load circuit equivalent to 2TTL loads and 100pF.

8. Assumes that $tr_{CD} \geq tr_{CD}(\text{max})$ and $t_{ASC} \geq t_{ASC}(\text{max})$.

9. Assumes that $tr_{CD} \leq tr_{CD}(\text{max})$ and $tr_{AD} \leq tr_{AD}(\text{max})$. If tr_{CD} or tr_{AD} is greater than the maximum recommended value shown in this table, tr_{AC} will increase by amount that tr_{CD} or tr_{AD} exceeds the value shown.

10. Assumes that $tr_{AD} \geq tr_{AD}(\text{max})$ and $t_{ASC} \leq t_{ASC}(\text{max})$.

11. Assumes that $t_{CP} \leq t_{CP}(\text{max})$ and $t_{ASC} \geq t_{ASC}(\text{max})$.

12. $t_{OFF}(\text{max})$ and $t_{OEZ}(\text{max})$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq |\pm 10 \mu A|$) and is not reference to $V_{OH}(\text{min})$ or $V_{OL}(\text{max})$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Notes 13, 14)

Symbol	Parameter	Limits				Unit
		M5M44260A-7, -7S		M5M44260A-8, -8S		
		Min	Max	Min	Max	
tREF	Refresh cycle time		8		8	ms
tREF*	Refresh cycle time*		64		64	ms
tRP	RAS high pulse width	60		70		ns
tRCD	Delay time, RAS low to CAS low (Note 15)	20	50	20	60	ns
tCRP	Delay time, CAS high to RAS low	10		10		ns
tRPC	Delay time, RAS high to CAS low	0		0		ns
tCPN	CAS high pulse width	10		10		ns
tRAD	Column address delay time from RAS low (Note 16)	15	35	15	40	ns
tASR	Row address setup time before RAS low	0		0		ns
tASC	Column address setup time before CAS low (Note 17)	0	10	0	15	ns
tRAH	Row address hold time after RAS low	10		10		ns
tCAH	Column address hold time after CAS low	15		15		ns
tDZC	Delay time, data to CAS low (Note 18)	0		0		ns
tDZO	Delay time, data to OE low (Note 18)	0		0		ns
tCDD	Delay time, CAS high to data (Note 19)	20		20		ns
tODD	Delay time, OE high to data (Note 19)	20		20		ns
tT	Transition time (Note 20)	1	50	1	50	ns

Note 13. The timing requirements are assumed $t_t = 5ns$.

14. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.

15. $tr_{CD}(\text{max})$ is specified as a reference point only. If tr_{CD} is less than $tr_{CD}(\text{max})$, access time is tr_{AC} .

If tr_{CD} is greater than $tr_{CD}(\text{max})$, access time is controlled exclusively by t_{CAC} or t_{AA} .

$tr_{CD}(\text{min})$ is specified as $tr_{CD}(\text{min}) = tr_{AH}(\text{min}) + 2t_t + t_{ASC}(\text{min})$.

16. $tr_{AD}(\text{max})$ is specified as a reference point only. If $tr_{AD} \geq tr_{AD}(\text{max})$ and $t_{ASC} \leq t_{ASC}(\text{max})$, access time is controlled exclusively by t_{AA} .

17. $t_{ASC}(\text{max})$ is specified as a reference point only. If $tr_{CD} \geq tr_{CD}(\text{max})$ and $t_{ASC} \geq t_{ASC}(\text{max})$, access time is controlled exclusively by t_{CAC} .

18. Either t_{DZC} or t_{DZO} must be satisfied.

19. Either t_{CDD} or t_{ODD} must be satisfied.

20. t_t is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

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Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M44260A-7, -7S		M5M44260A-8, -8S		
		Min	Max	Min	Max	
t _{RC}	Read cycle time	140		160		ns
t _{RAS}	RAS low pulse width	70	10000	80	10000	ns
t _{CAS}	CAS low pulse width	20	10000	20	10000	ns
t _{CSH}	CAS hold time after RAS low	70		80		ns
t _{RS}	RAS hold time after CAS low	20		20		ns
t _{RC_S}	Read setup time before CAS low	0		0		ns
t _{RCH}	Read hold time after CAS high (Note 21)	0		0		ns
t _{RRH}	Read hold time after RAS high (Note 21)	10		10		ns
t _{RA_L}	Column address to RAS hold time	35		40		ns
t _{OCH}	CAS hold time after OE low	20		20		ns
t _{OFH}	RAS hold time after OE low	20		20		ns

Note 21. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter	Limits				Unit
		M5M44260A-7, -7S		M5M44260A-8, -8S		
		Min	Max	Min	Max	
tWC	Write cycle time	140		160		ns
tRAS	RAS low pulse width	70	10000	80	10000	ns
tCAS	CAS low pulse width	20	10000	20	10000	ns
tCSH	CAS hold time after RAS low	70		80		ns
tRS	RAS hold time after CAS low	20		20		ns
tWCS	Write setup time before CAS low	(Note 23) 0		0		ns
tWCH	Write hold time after CAS low	15		15		ns
tCWL	CAS hold time after W low	20		20		ns
tRWL	RAS hold time after W low	20		20		ns
tWP	Write pulse width	15		15		ns
tDS	Data setup time before CAS low or W	0		0		ns
tDH	Data hold time after CAS low or W low	15		15		ns
tOEH	OE hold time after W low	20		20		ns

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Read - Write and Read - Modify - Write Cycles

Symbol	Parameter	Limits				Unit
		M5M44260A-7, -7S		M5M44260A-8, -8S		
		Min	Max	Min	Max	
trWC	Read Write/read modify write cycle time (Note 22)	185		205		ns
trAS	RAS low pulse width	115	10000	125	10000	ns
tcAS	CAS low pulse width	65	10000	65	10000	ns
tcSH	CAS hold time after RAS low	115		125		ns
trSH	RAS hold time after CAS low	65		65		ns
trCS	Read setup time before CAS low	0		0		ns
tcWD	Delay time, CAS low to $\overline{W}$ low (Note 23)	40		40		ns
trWD	Delay time, RAS low to $\overline{W}$ low (Note 23)	90		100		ns
tAWD	Delay time, address to $\overline{W}$ low (Note 23)	55		60		ns
tcWL	CAS hold time after $\overline{W}$ low	20		20		ns
trWL	RAS hold time after $\overline{W}$ low	20		20		ns
twF	Write pulse width	15		15		ns
tdS	Data setup time before $\overline{W}$ low	0		0		ns
tdH	Data hold time after $\overline{W}$ low	15		15		ns
toEH	OE hold time after $\overline{W}$ low	15		20		ns

Note 22. trWC is specified as $trWC(min) = trAC(max) + tODD(min) + trWL(min) + trP(min) + 4tT$.

23. twCS, tcWD, trWD and tAWD and tcPWD are specified as reference points only. If $twCS \geq twCS(min)$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $tcWD \geq tcWD(min)$, $trWD \geq trWD(min)$, $tAWD \geq tAWD(min)$, and $tcPWD \geq tcPWD(min)$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed-write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

Fast - Page Mode Cycle (Read, Write, Read - Write, and Read - Modify - Write Cycles) (Note 24)

Symbol	Parameter	Limits				Unit
		M5M44260A-7, -7S		M5M44260A-8, -8S		
		Min	Max	Min	Max	
tpc	Fast page mode read/write cycle time	45		50		ns
tpRWC	Fast page mode read write/read modify write cycle time	95		100		ns
trAS	RAS low pulse width for read write cycle (Note 25)	115	100000	135	100000	ns
tcP	CAS high pulse width (Note 26)	10	15	10	20	ns
tcPRH	RAS hold time after CAS precharge	40		45		ns
tcPWD	Delay time, CAS precharge to $\overline{W}$ low (Note 23)	40		45		ns

Note 24. All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25. trAS(min) is specified as two cycles of CAS input are performed.

26. tcP(max) is specified as a reference point only.

CAS before RAS Refresh, Extended Refresh Cycle * (Note 27)

Symbol	Parameter	Limits				Unit
		M5M44260A-7, -7S		M5M44260A-8, -8S		
		Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	10		10		ns
tCHR	CAS hold time after RAS low	15		15		ns
tCAS	CAS low pulse width	30		30		ns

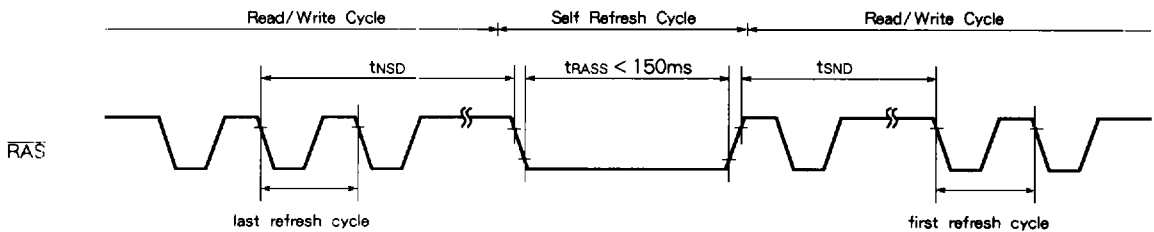
Note 27. Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

Self Refresh Cycle * (Note 28)

Symbol	Parameter	Limits				Unit
		M5M44260A-7S		M5M44260A-8S		
		Min	Max	Min	Max	
trASS	CBR self refresh $\overline{\text{RAS}}$ low pulse width	100		100		μs
trPS	CBR self refresh $\overline{\text{RAS}}$ high precharge time	140		160		ns
tCHS	CBR self refresh $\overline{\text{CAS}}$ hold time	- 50		- 50		ns

FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM**Note 28. Self refresh sequence**

Two refreshing ways should be used properly depending on the low pulse width(t_{RASS}) of $\overline{\text{RAS}}$ signal during self refresh period.

1. In case of $t_{\text{RASS}} < 150\text{ms}$ **1.1 Distributed refresh during Read/Write operation****(A) Timing Diagrams****Table 2**

Read/Write Cycle	Read/Write → Self Refresh	Self Refresh → Read/Write
CBR distributed refresh	$t_{\text{NSD}} + t_{\text{SND}} \leq 8\text{ms}$	
$\overline{\text{RAS}}$ only distributed refresh	$t_{\text{NSD}} \leq 16\ \mu\text{s}$	$t_{\text{SND}} \leq 16\ \mu\text{s}$

(B) Definition of distributed refresh**Definition of CBR distributed refresh****(Including extended refresh)**

The CBR distributed refresh performs more than 512 constant period (125 μs max) CBR cycles within 64 ms.

Definition of $\overline{\text{RAS}}$ only distributed refresh

All combination of nine row address signals ($A_0 \sim A_8$) are selected during 512 constant period (16 μs max) $\overline{\text{RAS}}$ only refresh cycles within 8 ms.

Note:

Hidden refresh may be used instead of CBR refresh.

$\overline{\text{RAS}}/\overline{\text{CAS}}$ refresh may be used instead of $\overline{\text{RAS}}$ only refresh.

1.1.1 CBR distributed Refresh

● Switching from read/write operation to self refresh operation.

The time interval from the falling edge of $\overline{\text{RAS}}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).

● Switching from self refresh operation to read/write operation.

The time interval from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{\text{RAS}}$ only distributed refresh

● Switching from read/write operation to self refresh operation.

The time interval t_{NSD} from the falling edge of $\overline{\text{RAS}}$ signal in the last $\overline{\text{RAS}}$ only refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within 16 μs .

● Switching from self refresh operation to read/write operation.

The time interval t_{SND} from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs .

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1.2 Burst refresh during Read/Write operation

(A) Timing diagram

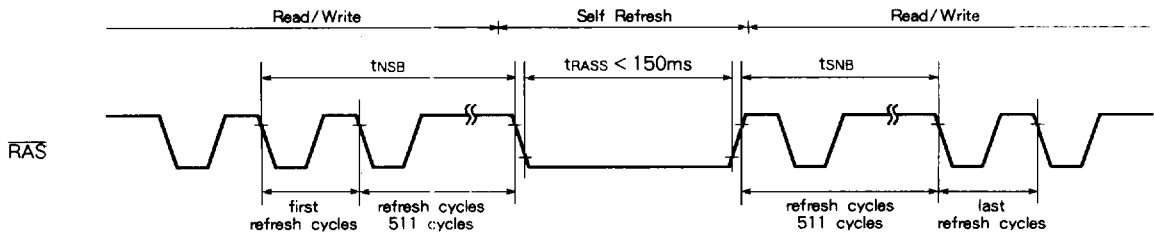


Table 3

Read/Write Cycle	Read/Write → Self Refresh	Self Refresh → Read/Write
CBR burst refresh	$t_{nsb} \leq 8\text{ms}$	$t_{snb} \leq 8\text{ms}$
RAS only burst refresh	$t_{nsb} + t_{snb} \leq 8\text{ms}$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more than 512 continuous CBR cycles within 8 ms.

Definition of RAS only burst refresh

All combination of ten row address signals ($A_0 \sim A_9$) are selected during 512 continuous RAS only refresh cycles within 8 ms.

1.2.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval t_{nsb} from the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within 8 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{snb} from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the last CBR refresh cycle during read/write operation period should be set within 8 ms.

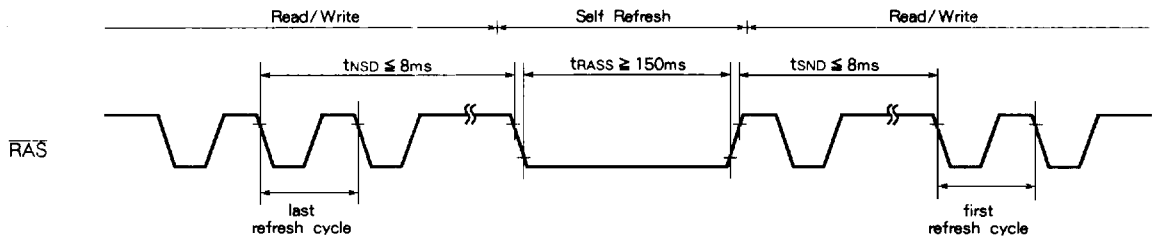
1.2.2 RAS only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{\text{RAS}}$ signal in the first RAS only refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within t_{nsb} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the last RAS only refresh cycle during read/write operation period should be set within t_{snb} (shown in table 3).

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2. In case of $t_{RASS} \geq 150\text{ms}$

(A) Timing diagram-A



Timing diagram-B

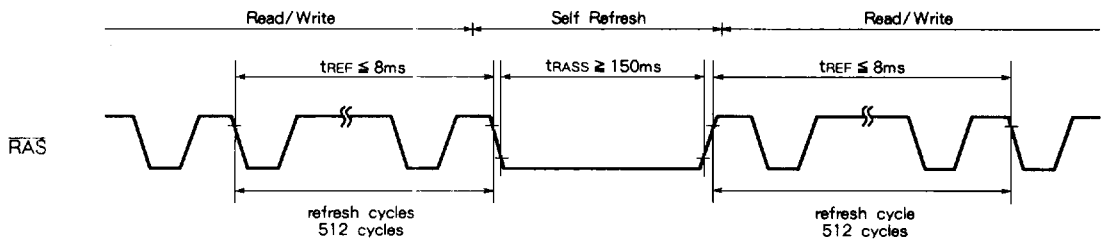


Table 4

Read/Write Cycle	Read/Write → Self Refresh	Self Refresh → Read/Write
CBR distributed refresh	Timing Diagram-A	Timing Diagram-A
$\overline{\text{RAS}}$ only distributed CBR burst refresh	Timing Diagram-B	Timing Diagram-B
$\overline{\text{RAS}}$ only burst refresh		

(B) Definition of refresh

The same as 1.1-(B) and 1.2-(B)

2.1.1 CBR distributed refresh

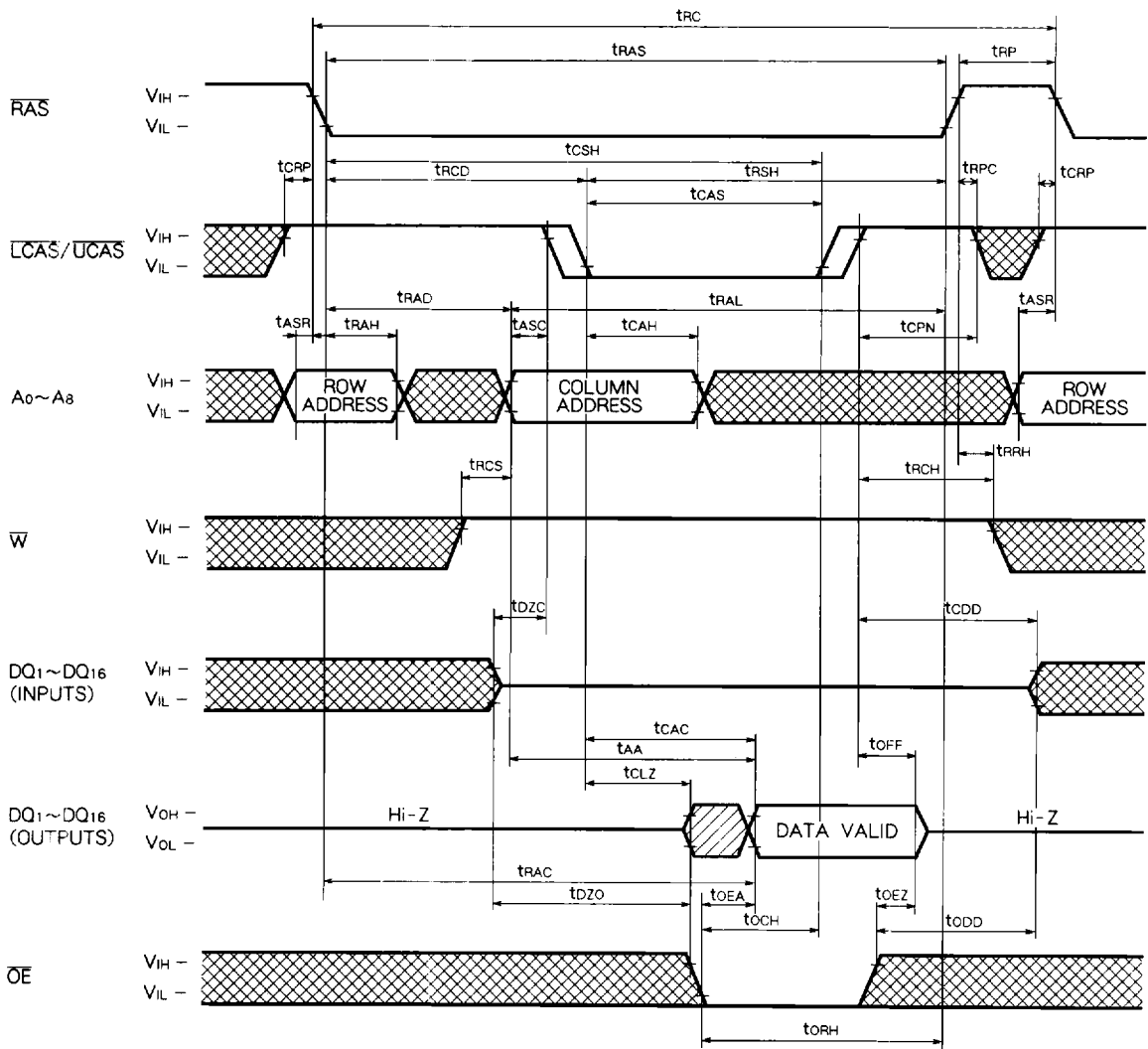
- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of RAS signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within 8 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of RAS signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read/write operation period should be set within 8 ms.

2.1.2 $\overline{\text{RAS}}$ only distributed, CBR burst, $\overline{\text{RAS}}$ only burst refresh

- Before and after the self refresh, 512 refresh cycles should be executed within 8 ms for each refresh operation.

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Timing Diagrams (Note 29)
Read Cycle



Note 29



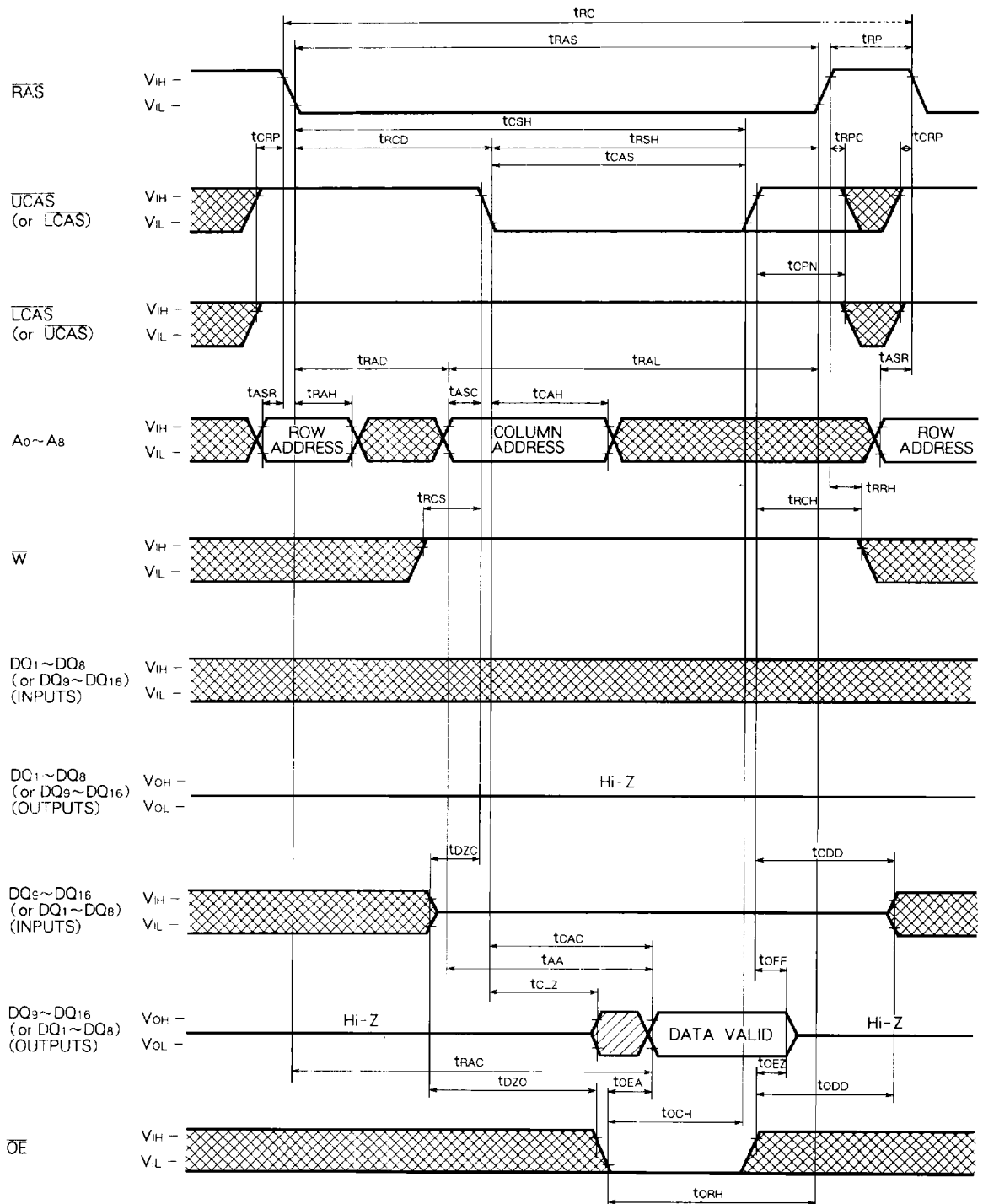
Indicates the don't care input.
 $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ or $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$



Indicates the invalid output.

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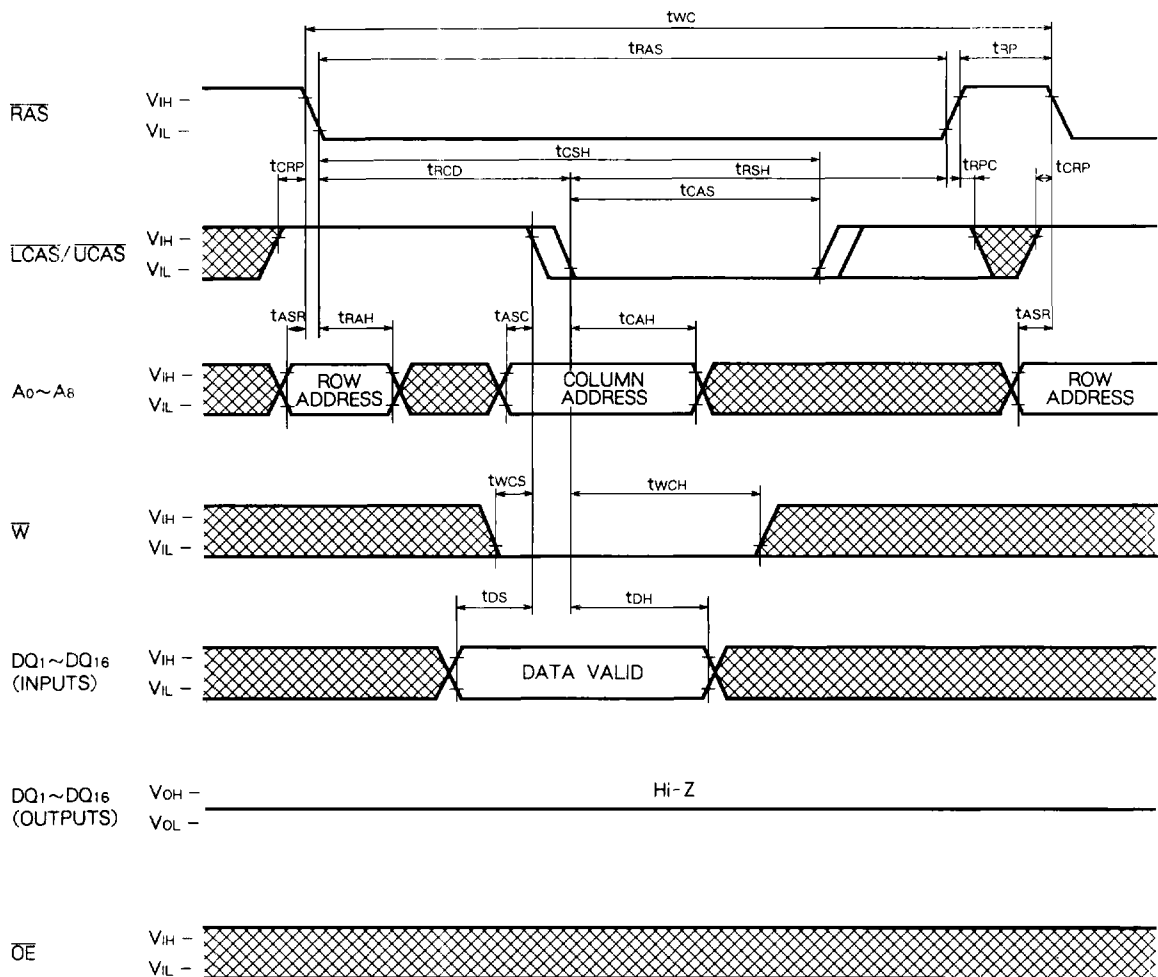
Byte Read Cycle



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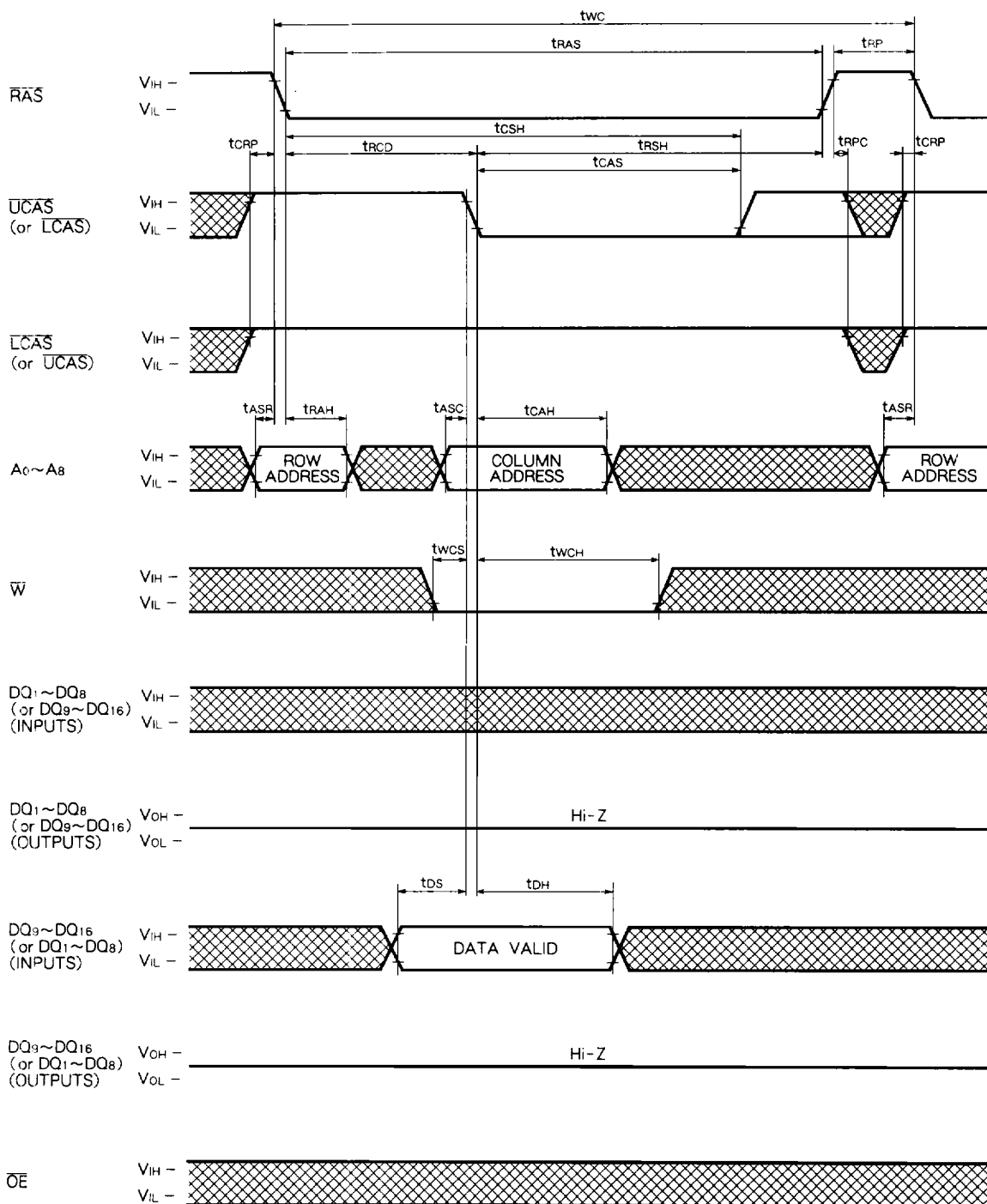
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Write Cycle (Early write)



FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

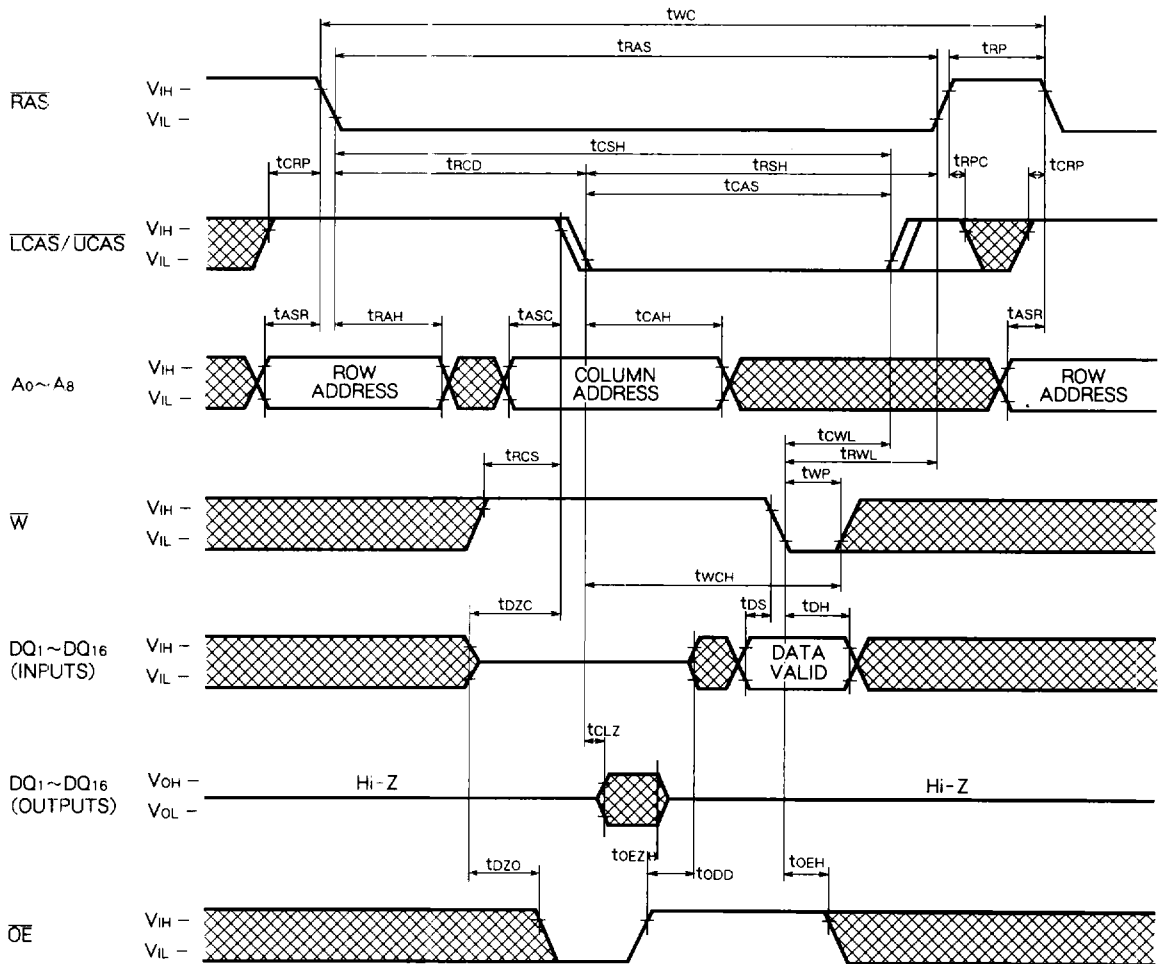
Byte Write Cycle (Early wire)



M5M44260AJ,TP,RT-7,-8,-7S,-8S

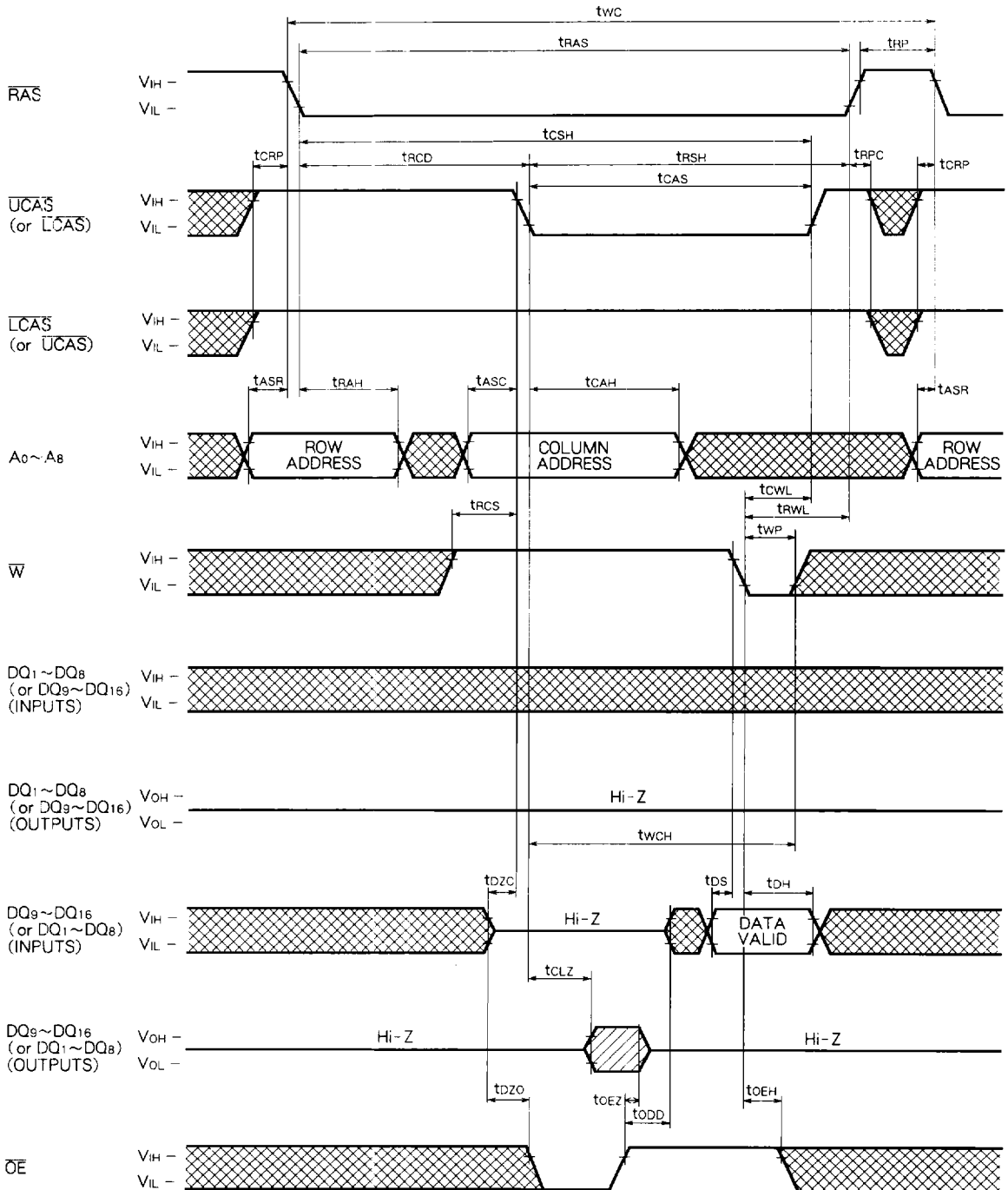
FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

Write Cycle (Delayed write)



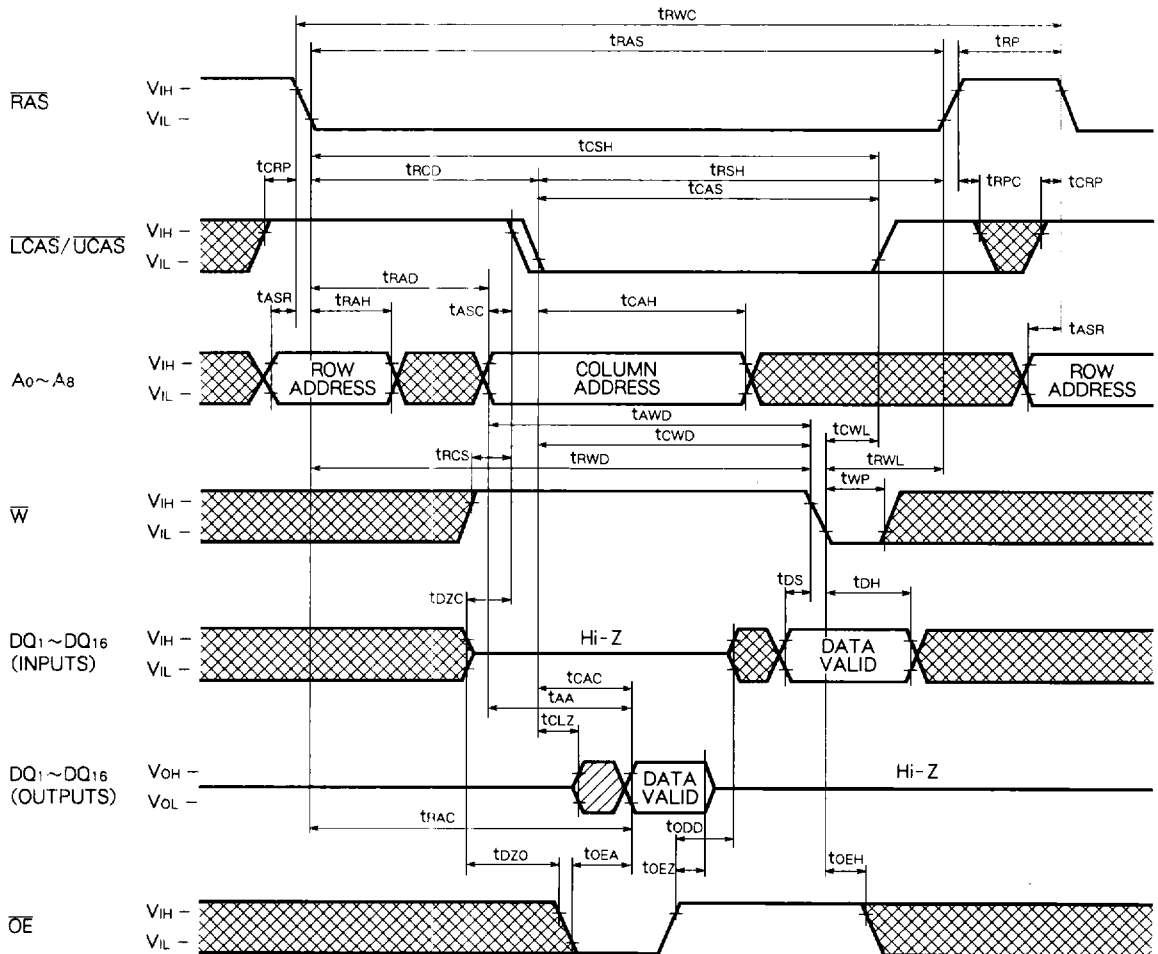
FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

Byte Write Cycle (Delayed write)



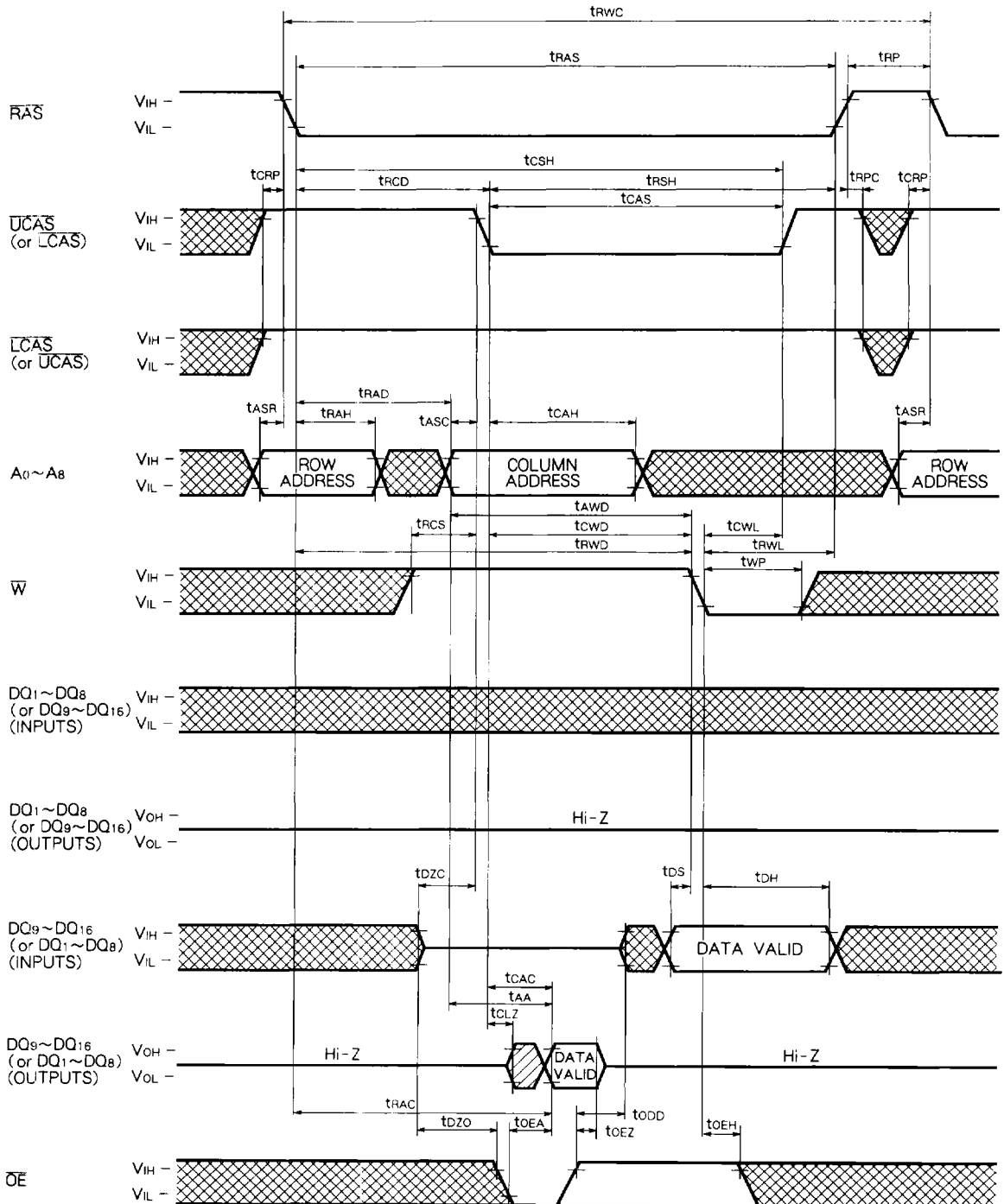
FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

Read - Write, Read - Modify - Write Cycle



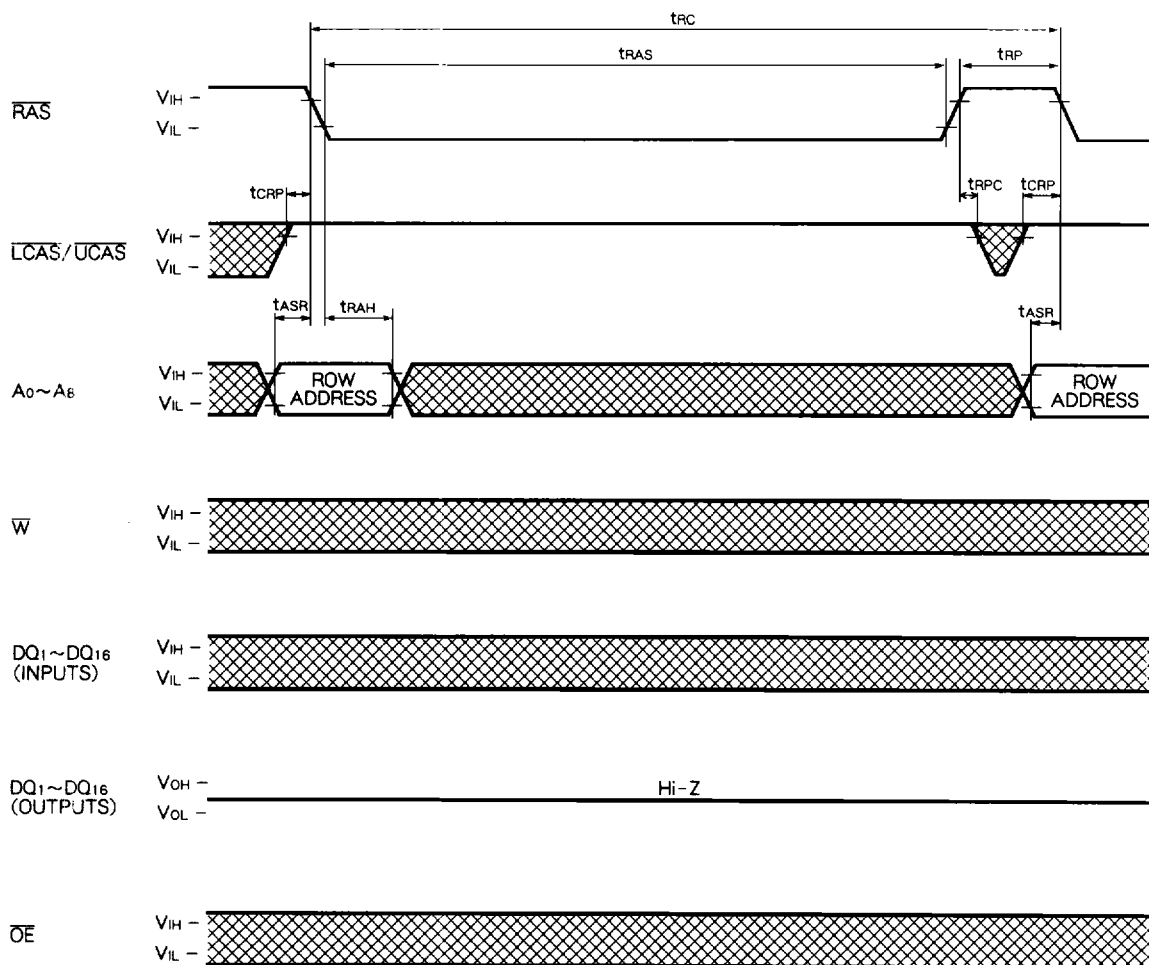
FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

Byte Read Write, Read- Modify Write Cycle



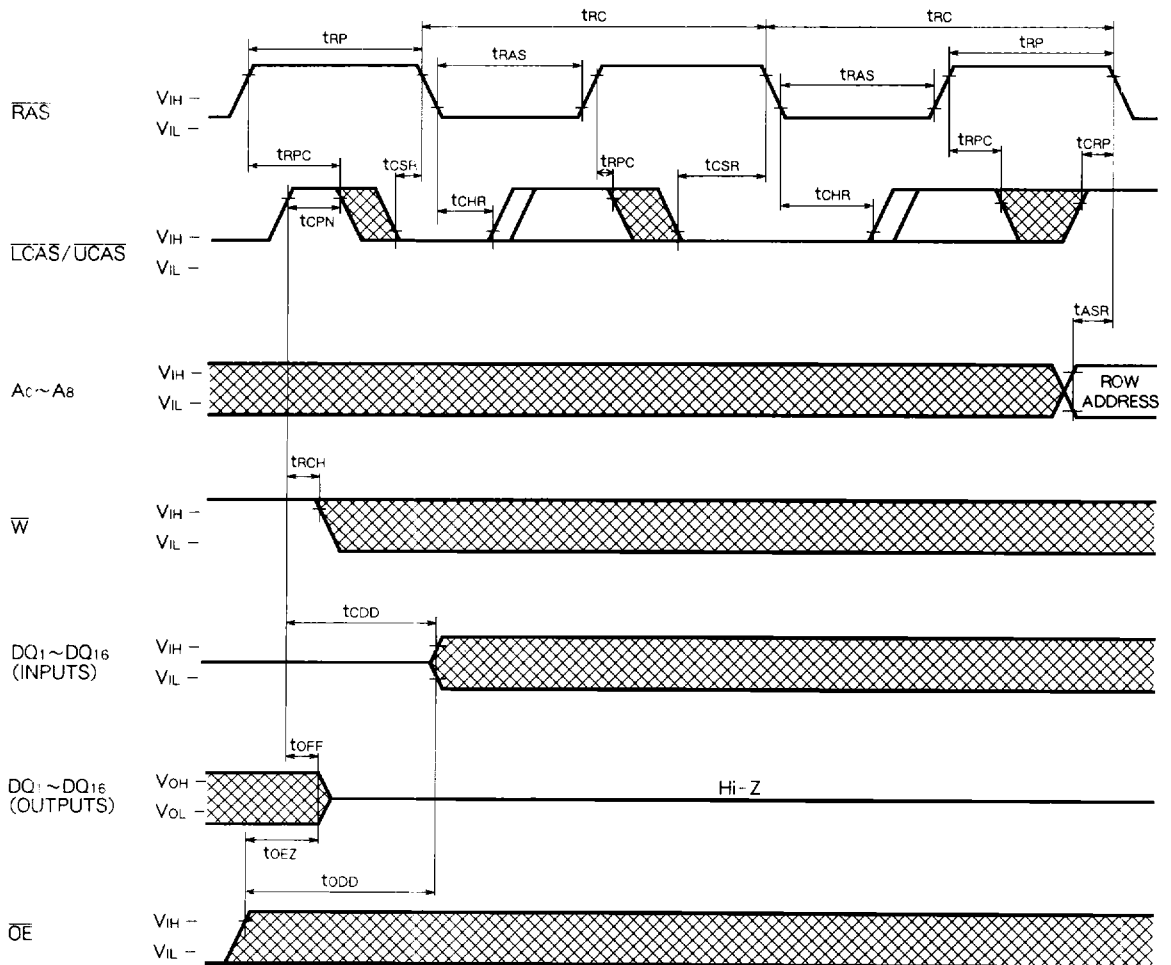
FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

RAS- only Refresh Cycle



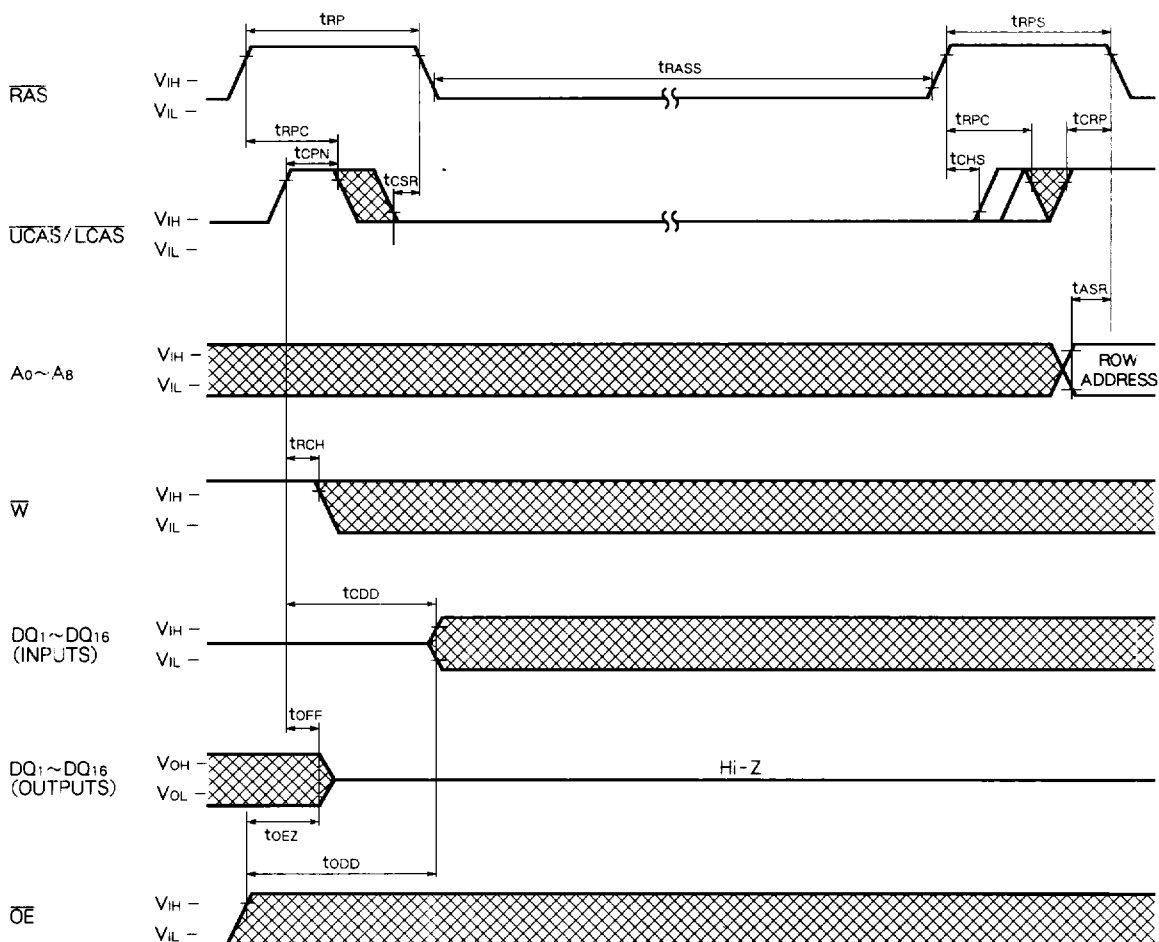
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$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle, Extended Refresh Cycle*



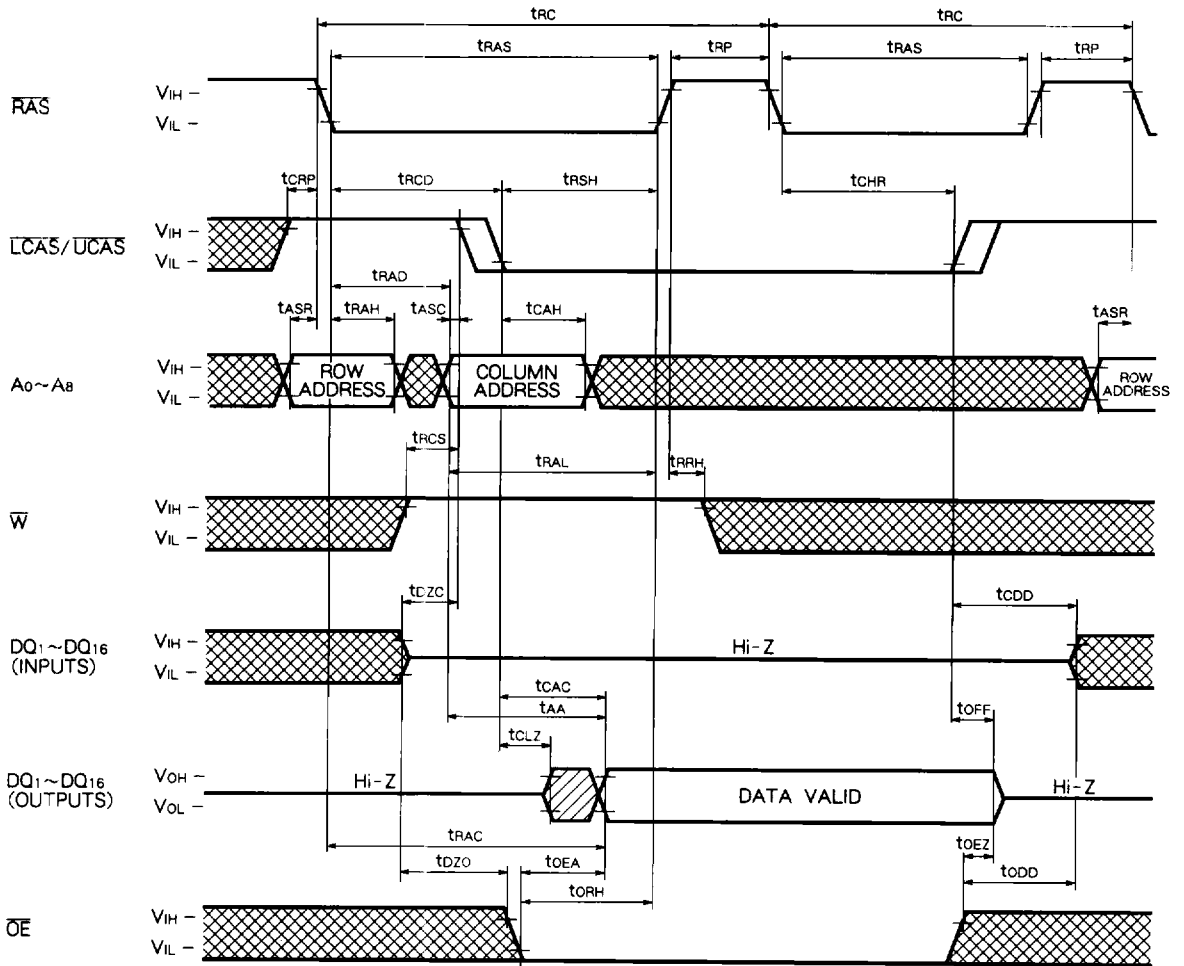
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Self Refresh Cycle* (Note 28)



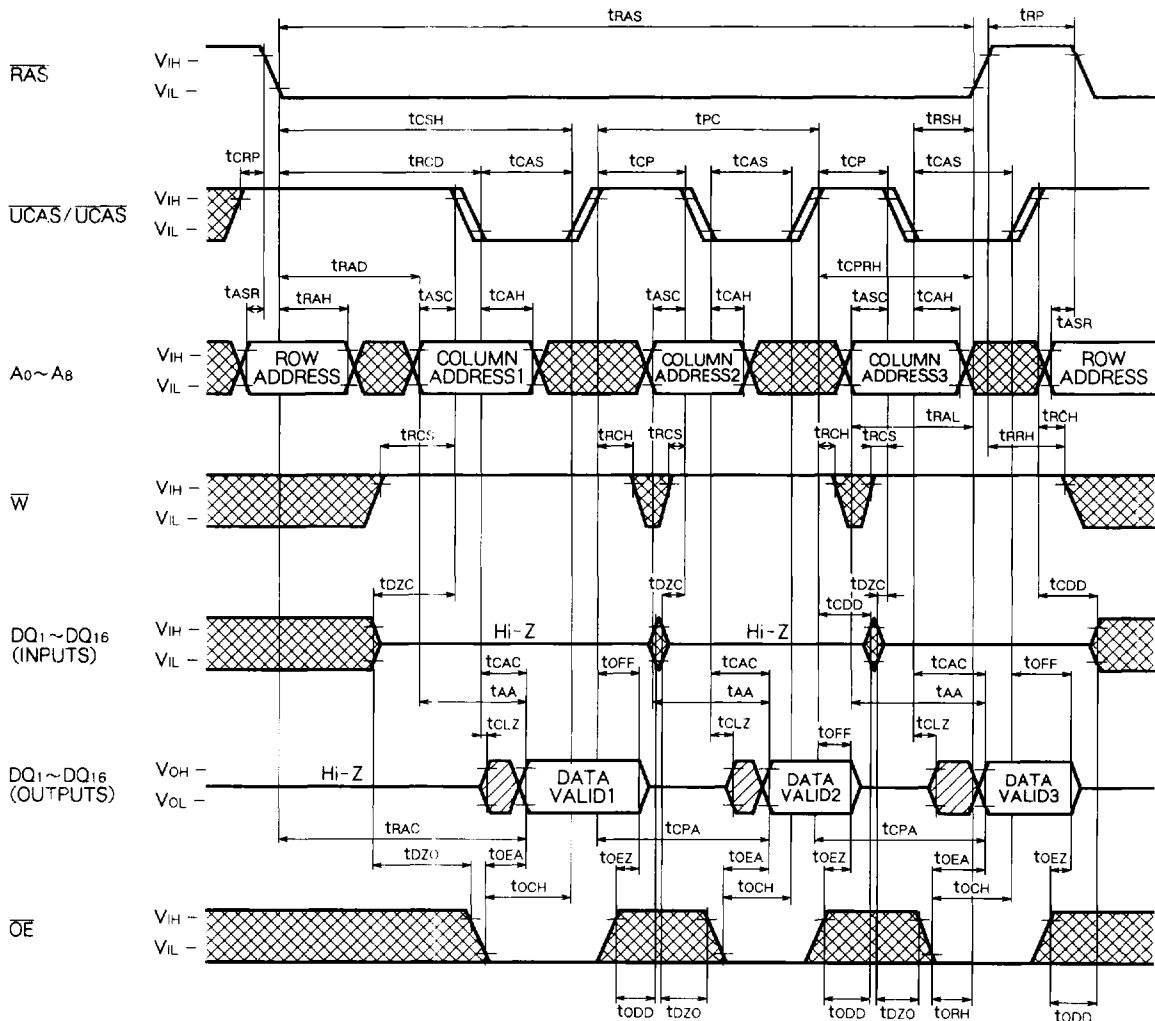
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Hidden Refresh Cycle (Read) (Note 30)



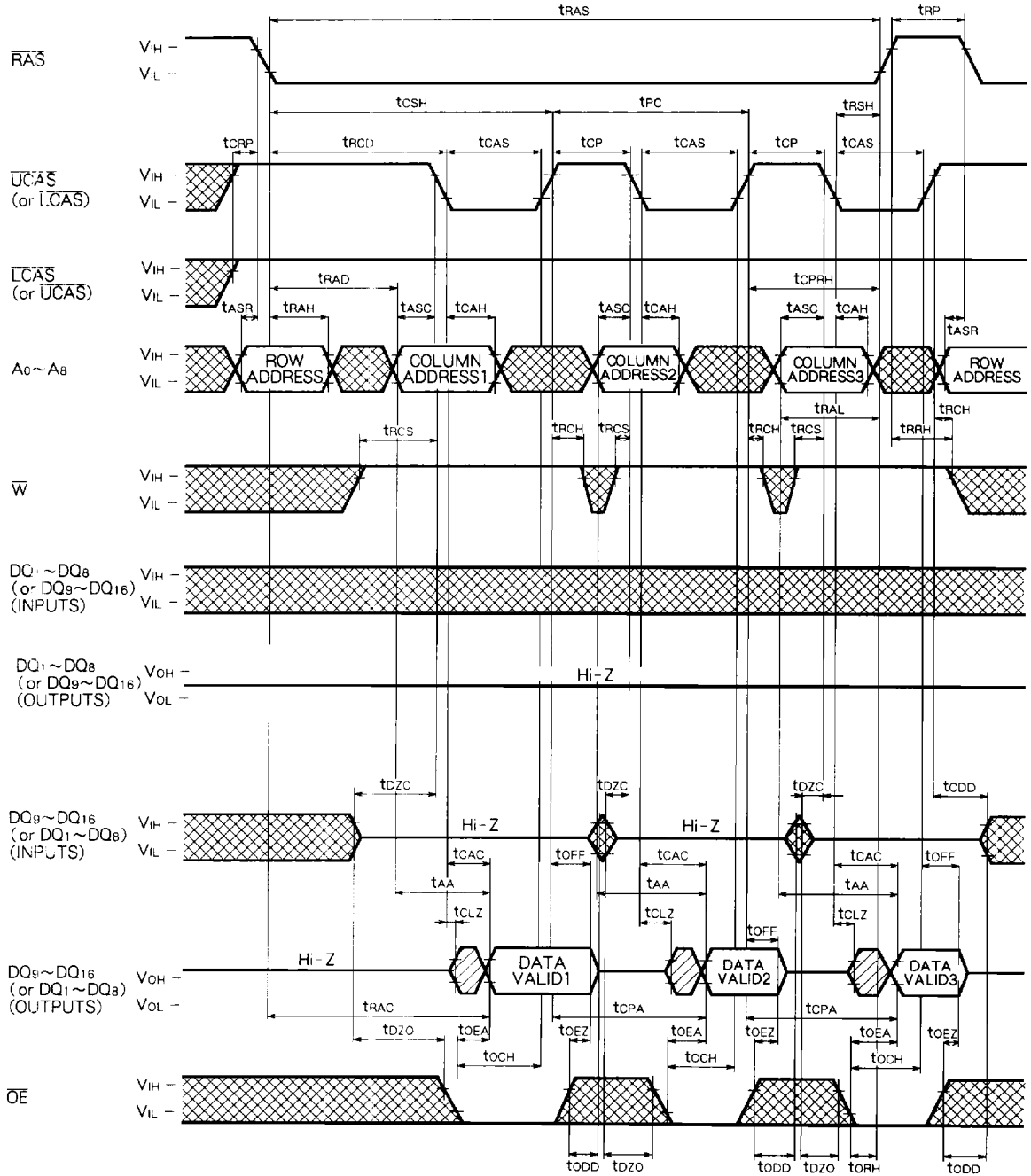
Note 30 Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Read Cycle



FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

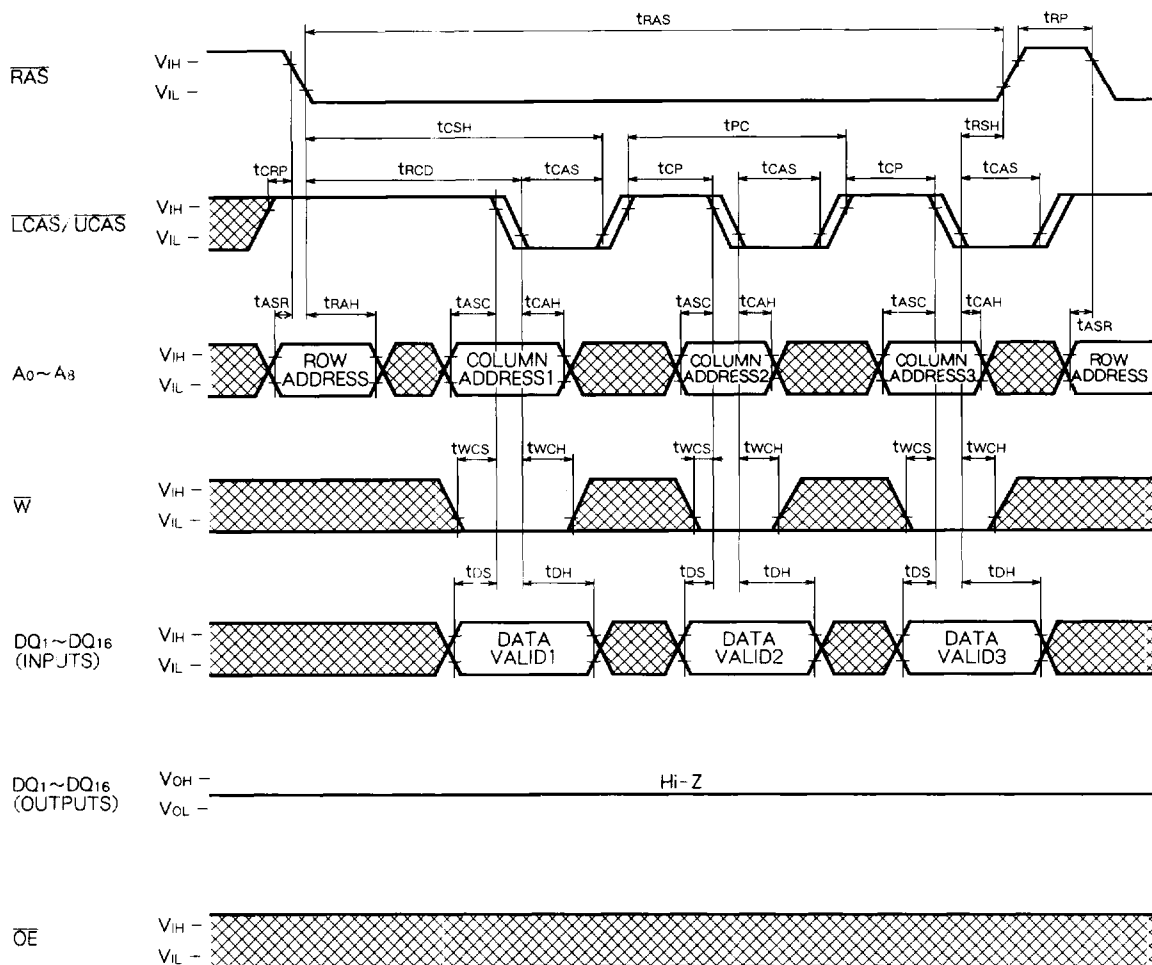
Fast Page Mode Byte Read Cycle



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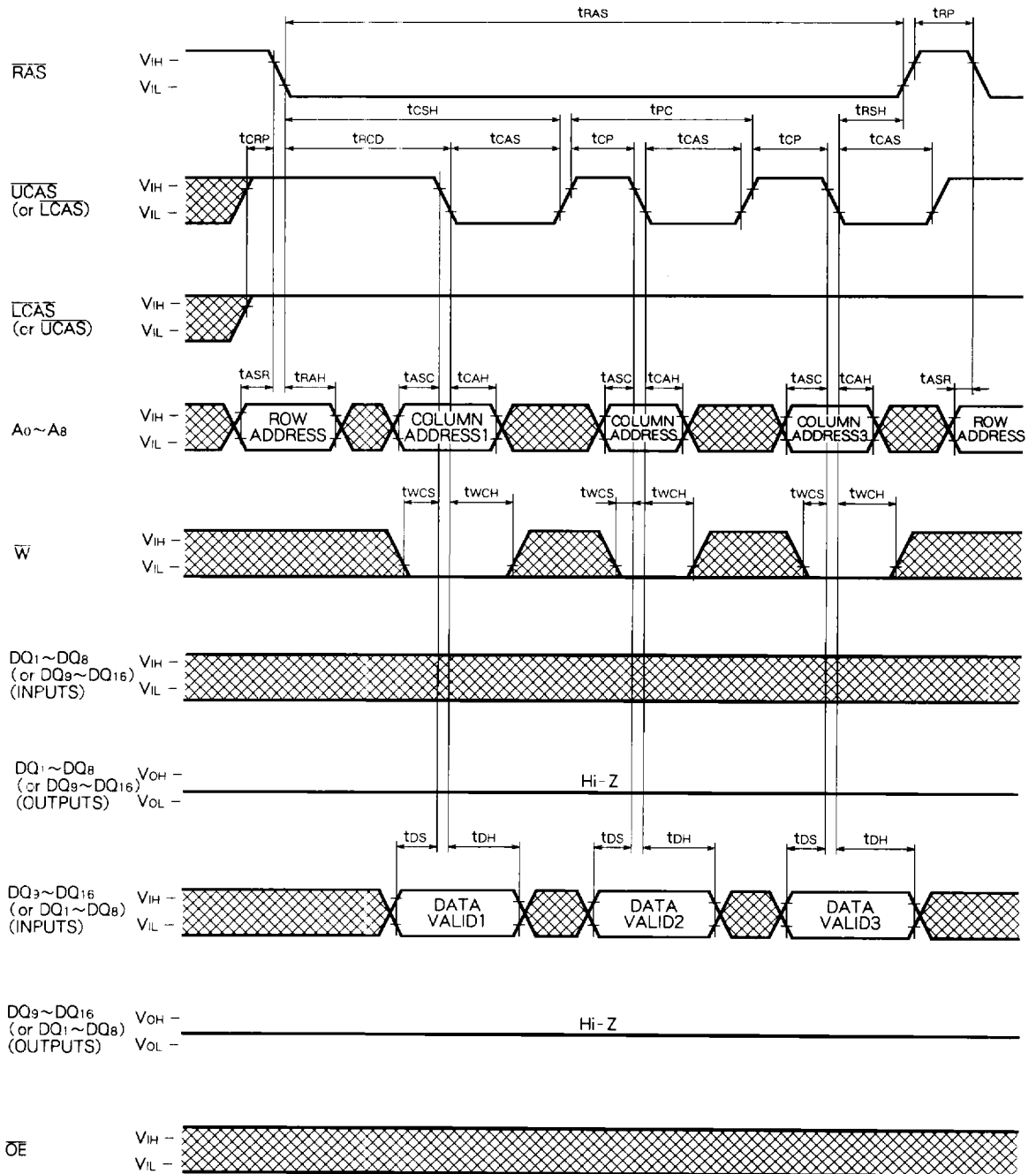
FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

Fast Page Mode Write Cycle (Early Write)

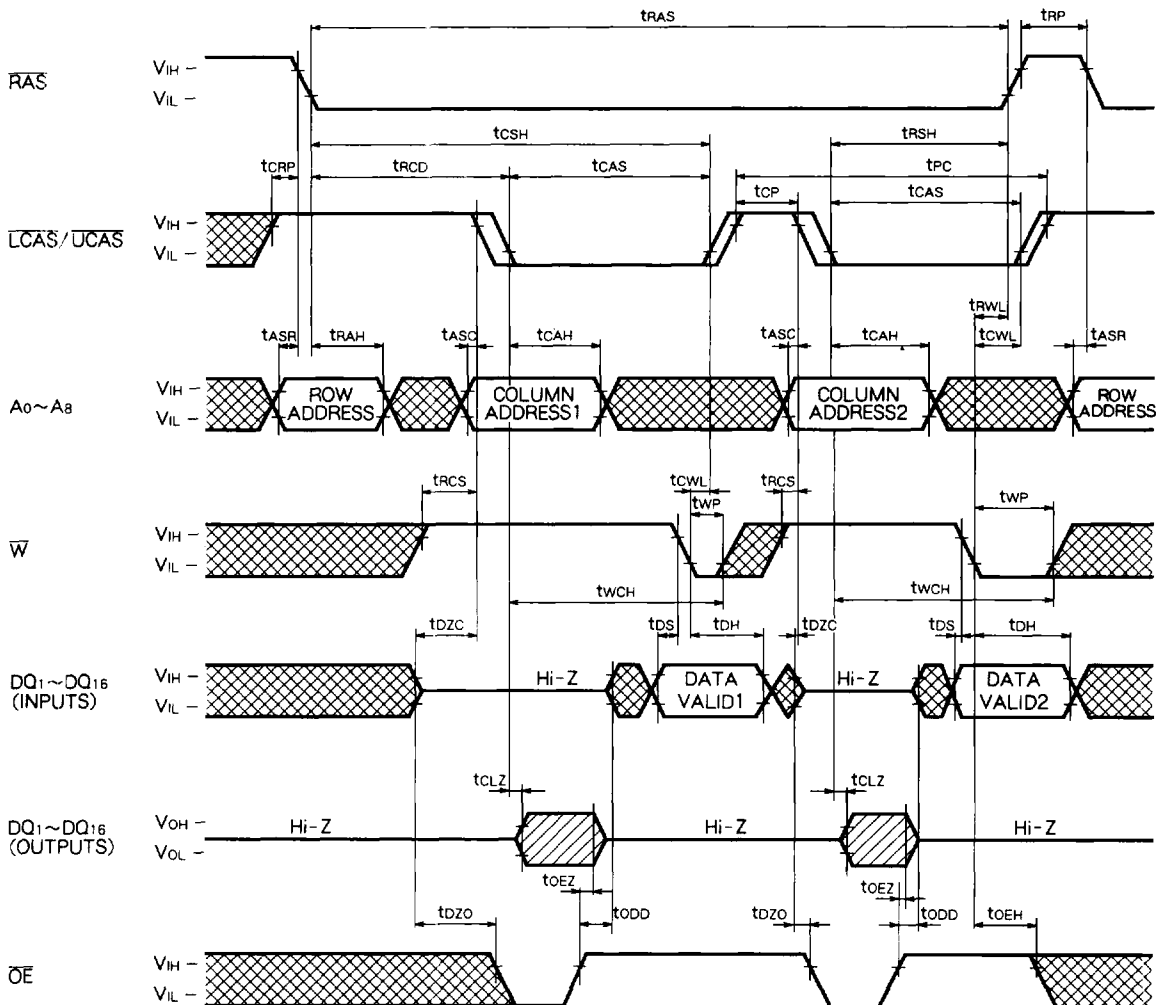


FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

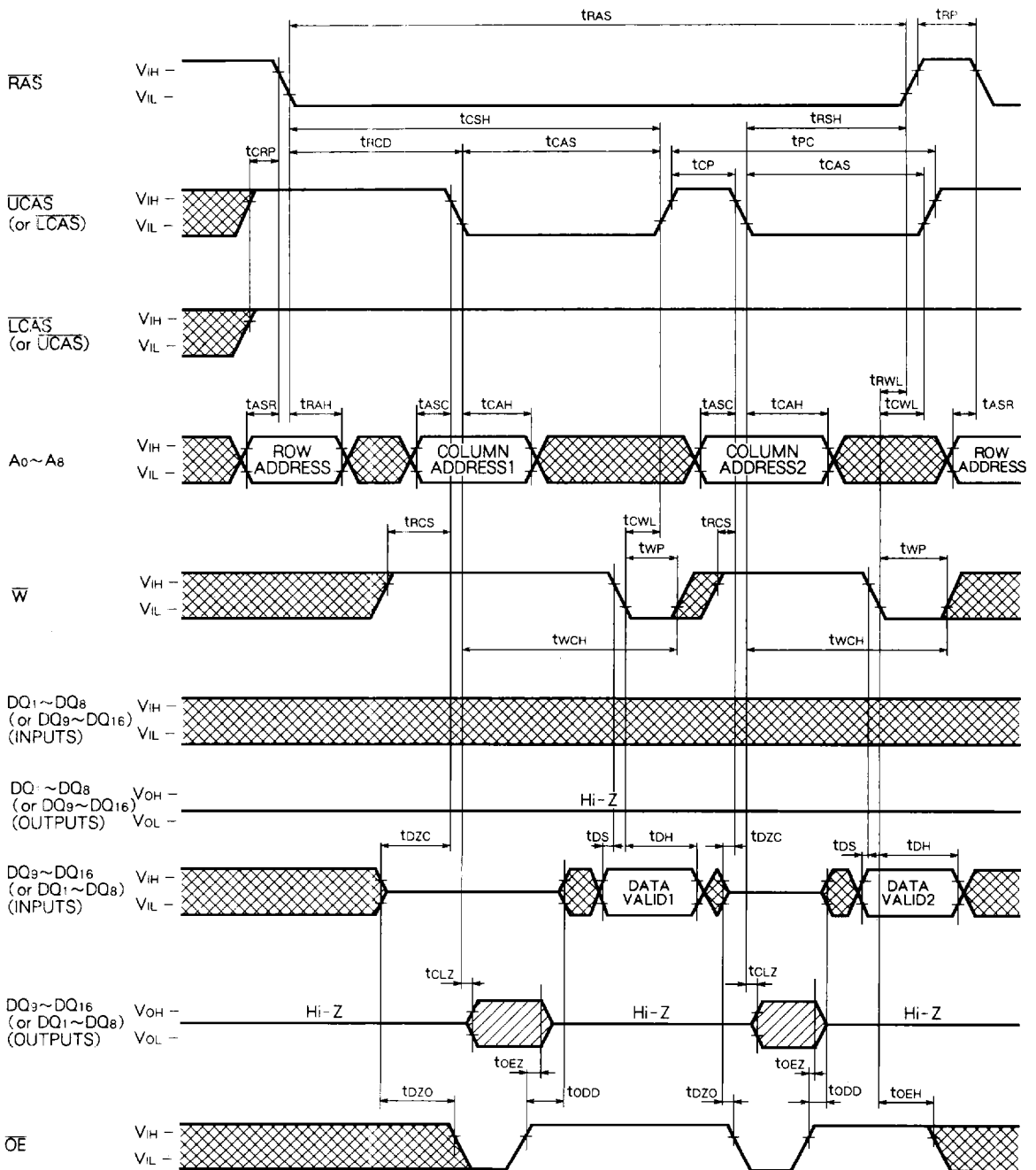
Fast Page Mode Byte Write Cycle (Early Write)



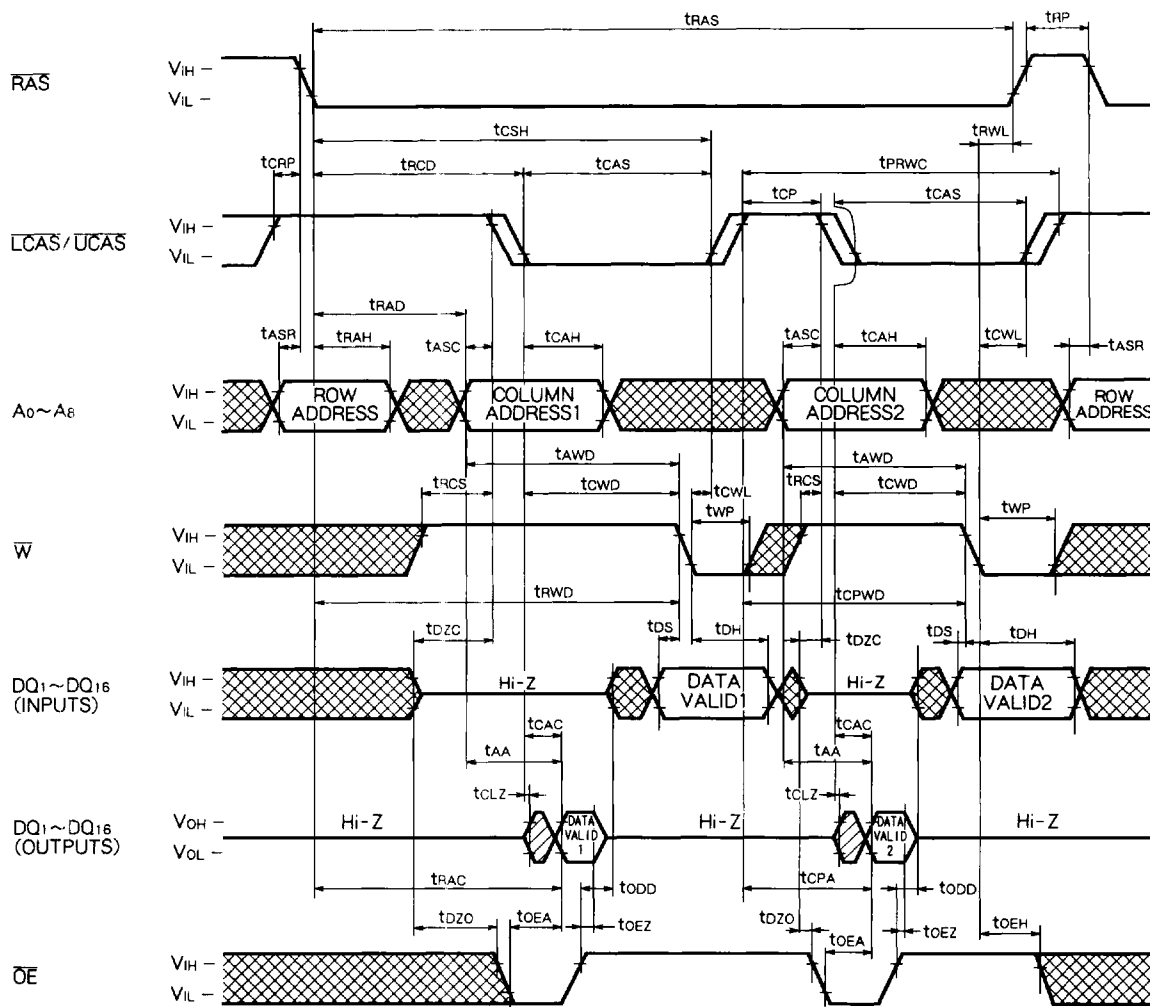
Fast Page Mode Write Cycle (Delayed Write)



Fast Page Mode Byte Write Cycle (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



M5M44260AJ,TP,RT-7,-8,-7'S,-8'S

FAST PAGE MODE 4194304-BIT(262144-WORD BY 16-BIT)DYNAMIC RAM

Fast Page Mode Byte Read Write, Read - Modify Write Cycle

