LTC6804-1/LTC6804-2

Multicell Battery Monitors

FEATURES

- **Measures Up to 12 Battery Cells in Series**
- **Stackable Architecture Supports 100s of Cells**
- **Built-In isoSPI™ Interface:**
  - **1Mbps Isolated Serial Communications**
  - **Uses a Single Twisted Pair, Up to 100 Meters**
  - **Low EMI Susceptibility and Emissions**
- **1.2mV Maximum Total Measurement Error**
- **290µs to Measure All Cells in a System**
- Synchronized Voltage and Current Measurement
- 16-Bit Delta-Sigma ADC with Frequency Programmable 3rd Order Noise Filter
- Engineered for ISO26262 Compliant Systems
- Passive Cell Balancing with Programmable Timer
- 5 General Purpose Digital I/O or Analog Inputs:
  - Temperature or other Sensor Inputs
  - Configurable as an I^{2}C or SPI Master
- 4µA Sleep Mode Supply Current
- 48-Lead SSOP Package

APPLICATIONS

- Electric and Hybrid Electric Vehicles
- Backup Battery Systems
- Grid Energy Storage
- High Power Portable Equipment

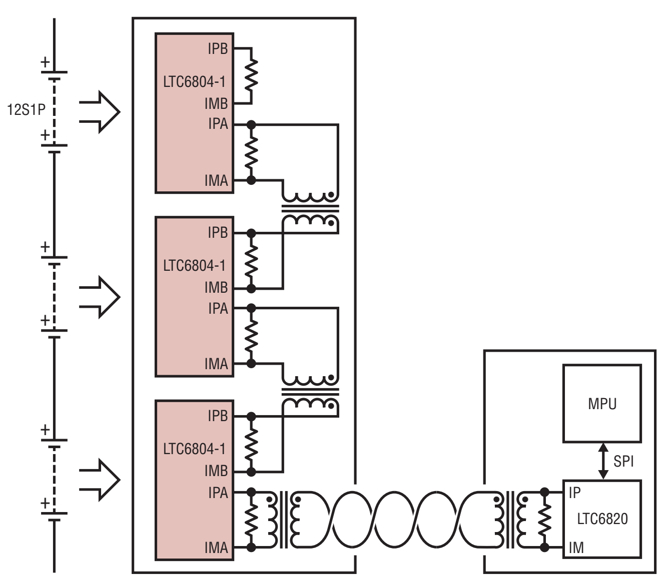
DESCRIPTION

The LTC®6804 is a 3rd generation multicell battery stack monitor that measures up to 12 series connected battery cells with a total measurement error of less than 1.2mV. The cell measurement range of 0V to 5V makes the LTC6804 suitable for most battery chemistries. All 12 cell voltages can be captured in 290µs, and lower data acquisition rates can be selected for high noise reduction.

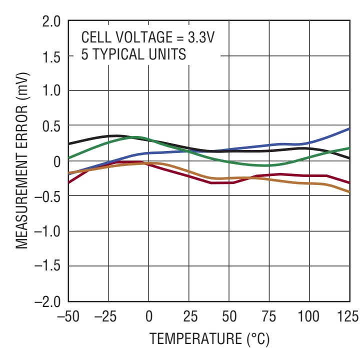
Multiple LTC6804 devices can be connected in series, permitting simultaneous cell monitoring of long, high voltage battery strings. Each LTC6804 has an isoSPI interface for high speed, RF-immune, local area communications. Using the LTC6804-1, multiple devices are connected in a daisy-chain with one host processor connection for all devices. Using the LTC6804-2, multiple devices are connected in parallel to the host processor, with each device individually addressed.

Additional features include passive balancing for each cell, an onboard 5V regulator, and 5 general purpose I/O lines. In sleep mode, current consumption is reduced to 4µA. The LTC6804 can be powered directly from the battery, or from an isolated supply.

TYPICAL APPLICATION



Total Measurement Error vs Temperature of 5 Typical Units



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage V^+ to V^- 75V
Input Voltage (Relative to V^-)
- C0 .... –0.3V to 0.3V
- C12 .... –0.3V to 75V
- C(n) .... –0.3V to MIN (8 • n, 75V)
- S(n) .... –0.3V to MIN (8 • n, 75V)
- IPA, IMA, IPB, IMB .... –0.3V to V_{REG} + 0.3V
- DRIVE Pin .... –0.3V to 7V
- All Other Pins .... –0.3V to 6V

Voltage Between Inputs (Note 2)
- C(n) to C(n – 1) .... –0.3V to 8V
- S(n) to C(n – 1) .... –0.3V to 8V
- C12 to C8 .... –0.3V to 25V
- C8 to C4 .... –0.3V to 25V
- C4 to C0 .... –0.3V to 25V

Current In/Out of Pins
- All Pins Except V_{REG}, IPA, IMA, IPB, IMB, S(n) .. 10mA
- IPA, IMA, IPB, IMB 30mA

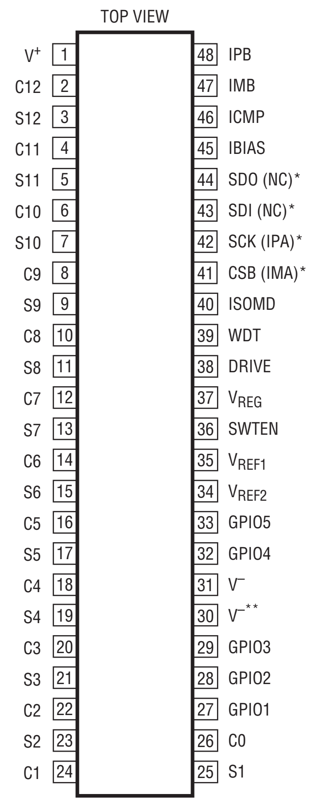
Operating Temperature Range
- LTC6804I .... –40°C to 85°C
- LTC6804H .... –40°C to 125°C

Specified Temperature Range
- LTC6804I .... –40°C to 85°C
- LTC6804H .... –40°C to 125°C

Junction Temperature .... 150°C
Storage Temperature .... –65°C to 150°C
Lead Temperature (Soldering, 10sec) .... 300°C

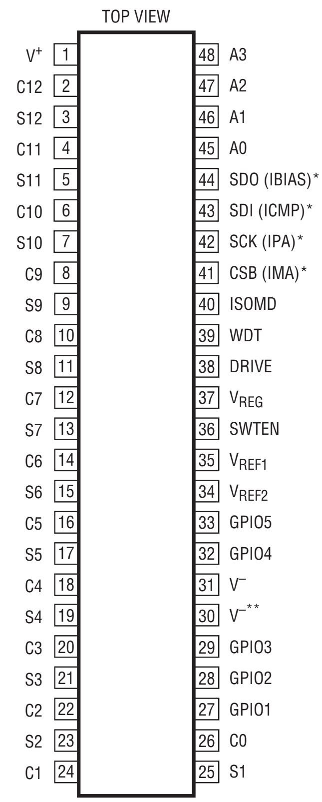
PIN CONFIGURATION

LTC6804-1



G PACKAGE
48-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 55°C/W
*THE FUNCTION OF THESE PINS DEPENDS ON THE CONNECTION OF ISOMD
ISOMD TIED TO V^-: CSB, SCK, SDI, SDO
ISOMD TIED TO V_{REG}: IMA, IPA, NC, NC
**THIS PIN MUST BE CONNECTED TO V^-

LTC6804-2



G PACKAGE
48-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 55°C/W
*THE FUNCTION OF THESE PINS DEPENDS ON THE CONNECTION OF ISOMD
ISOMD TIED TO V^-: CSB, SCK, SDI, SDO
ISOMD TIED TO V_{REG}: IMA, IPA, ICMP, IBIAS
**THIS PIN MUST BE CONNECTED TO V^-

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6804IG-1#PBF	LTC6804IG-1#TRPBF	LTC6804G-1	48-Lead Plastic SSOP	–40°C to 85°C
LTC6804HG-1#PBF	LTC6804HG-1#TRPBF	LTC6804G-1	48-Lead Plastic SSOP	–40°C to 125°C
LTC6804IG-2#PBF	LTC6804IG-2#TRPBF	LTC6804G-2	48-Lead Plastic SSOP	–40°C to 85°C
LTC6804HG-2#PBF	LTC6804HG-2#TRPBF	LTC6804G-2	48-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC DC Specifications							
	Measurement Resolution		●		0.1		mV/bit
	ADC Offset Voltage	(Note 2)	●		0.1		mV
	ADC Gain Error	(Note 2)	 ●		0.01 0.02		% %
	Total Measurement Error (TME) in Normal Mode	C(n) to C(n – 1), GPIO(n) to V^- = 0			±0.2		mV
		C(n) to C(n – 1) = 2.0			±0.1	±0.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 2.0	●			±1.4	mV
		C(n) to C(n – 1) = 3.3			±0.2	±1.2	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 3.3	●			±2.2	mV
		C(n) to C(n – 1) = 4.2			±0.3	±1.6	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 4.2	●			±2.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 5.0			±1		mV
		Sum of Cells	●		±0.2	±0.75	%
		Internal Temperature, T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●		±0.1	±0.25	%
		V_{REF2} Pin	●		±0.02	±0.1	%
		Digital Supply Voltage V_{REGD}	●		±0.1	±1	%

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Total Measurement Error (TME) in Filtered Mode	C(n) to C(n – 1), GPIO(n) to V^- = 0			±0.1		mV
		C(n) to C(n – 1) = 2.0			±0.1	±0.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 2.0	●			±1.4	mV
		C(n) to C(n – 1) = 3.3			±0.2	±1.2	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 3.3	●			±2.2	mV
		C(n) to C(n – 1) = 4.2			±0.3	±1.6	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 4.2	●			±2.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 5.0			±1		mV
		Sum of Cells	●		±0.2	±0.75	%
		Internal Temperature, T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●		±0.1	±0.25	%
		V_{REF2} Pin	●		±0.02	±0.1	%
		Digital Supply Voltage V_{REGD}	●		±0.1	±1	%
	Total Measurement Error (TME) in Fast Mode	C(n) to C(n – 1), GPIO(n) to V^- = 0			±2		mV
		C(n) to C(n – 1), GPIO(n) to V^- = 2.0	●			±4	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 3.3	●			±4.7	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 4.2	●			±8.3	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 5.0			±10		mV
		Sum of Cells	●		±0.3	±1	%
		Internal Temperature, T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●		±0.3	±1	%
		V_{REF2} Pin	●		±0.1	±0.25	%
		Digital Supply Voltage V_{REGD}	●		±0.2	±2	%
	Input Range	C(n), n = 1 to 12	●	C(n – 1)		C(n – 1) + 5	V
		C0	●		0		
		GPIO(n), n = 1 to 5	●	0		5	V
I_L	Input Leakage Current When Inputs Are Not Being Measured	C(n), n = 0 to 12	●		10	±250	nA
		GPIO(n), n = 1 to 5	●		10	±250	nA
	Input Current When Inputs Are Being Measured	C(n), n = 0 to 12			±2		µA
		GPIO(n), n = 1 to 5			±2		µA
	Input Current During Open Wire Detection		●	70	100	130	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Voltage Reference Specifications								
V_{REF1}	1st Reference Voltage	V_{REF1} Pin, No Load		●	3.1	3.2	3.3	V
	1st Reference Voltage TC	V_{REF1} Pin, No Load				3		ppm/°C
	1st Reference Voltage Hysteresis	V_{REF1} Pin, No Load				20		ppm
	1st Reference Long Term Drift	V_{REF1} Pin, No Load				20		ppm/√kHr
V_{REF2}	2nd Reference Voltage	V_{REF2} Pin, No Load		●	2.990	3	3.010	V
		V_{REF2} Pin, 5k Load to V^-		●	2.988	3	3.012	V
	2nd Reference Voltage TC	V_{REF2} Pin, No Load				10		ppm/°C
	2nd Reference Voltage Hysteresis	V_{REF2} Pin, No Load				100		ppm
	2nd Reference Long Term Drift	V_{REF2} Pin, No Load				60		ppm/√kHr
General DC Specifications								
I_{VP}	V^+ Supply Current (See Figure 1: LTC6804 Operation State Diagram)	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 0V			3.8	6	µA
			V_{REG} = 0V	●		3.8	10	µA
			V_{REG} = 5V			1.6	3	µA
			V_{REG} = 5V	●		1.6	5	µA
		State: Core = STANDBY			18	32	50	µA
				●	10	32	60	µA
		State: Core = REFUP or MEASURE			0.4	0.55	0.7	mA
				●	0.375	0.55	0.725	mA
$I_{REG(CORE)}$	V_{REG} Supply Current (See Figure 1: LTC6804 Operation State diagram)	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 5V			2.2	4	µA
			V_{REG} = 5V	●		2.2	6	µA
		State: Core = STANDBY			10	35	60	µA
				●	6	35	65	µA
		State: Core = REFUP			0.2	0.45	0.7	mA
				●	0.15	0.45	0.75	mA
		State: Core = MEASURE			10.8	11.5	12.2	mA
				●	10.7	11.5	12.3	mA
$I_{REG(isoSPI)}$	Additional V_{REG} Supply Current if isoSPI in READY/ACTIVE States Note: ACTIVE State Current Assumes t_{CLK} = 1µs, (Note 3)	LTC6804-2: ISOMD = 1, R_{B1} + R_{B2} = 2k	READY	●	3.9	4.8	5.8	mA
			ACTIVE	●	5.1	6.1	7.3	mA
		LTC6804-1: ISOMD = 0, R_{B1} + R_{B2} = 2k	READY	●	3.7	4.6	5.6	mA
			ACTIVE	●	5.7	6.8	8.1	mA
		LTC6804-1: ISOMD = 1, R_{B1} + R_{B2} = 2k	READY	●	6.5	7.8	9.5	mA
			ACTIVE	●	10.2	11.3	13.3	mA
		LTC6804-2: ISOMD = 1, R_{B1} + R_{B2} = 20k	READY	●	1.3	2.1	3	mA
			ACTIVE	●	1.6	2.5	3.5	mA
		LTC6804-1: ISOMD = 0, R_{B1} + R_{B2} = 20k	READY	●	1.1	1.9	2.8	mA
			ACTIVE	●	1.5	2.3	3.3	mA
		LTC6804-1: ISOMD = 1, R_{B1} + R_{B2} = 20k	READY	●	2.1	3.3	4.9	mA
			ACTIVE	●	2.7	4.1	5.8	mA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V^+ Supply Voltage	TME Specifications Met (Note 6)	●	11	40	55	V
V_{REG}	V_{REG} Supply Voltage	TME Supply Rejection < 1mV/V	●	4.5	5	5.5	V
	DRIVE output voltage	Sourcing 1µA	 ●	5.4 5.2	5.6 5.6	5.8 6.0	V V
		Sourcing 500µA	●	5.1	5.6	6.1	V
V_{REGD}	Digital Supply Voltage		●	2.7	3.0	3.6	V
	Discharge Switch ON Resistance	V_{CELL} = 3.6V	●		10	25	Ω
	Thermal Shutdown Temperature				150		°C
$V_{OL(WDT)}$	Watchdog Timer Pin Low	WDT Pin Sinking 4mA	●			0.4	V
$V_{OL(GPIO)}$	General Purpose I/O Pin Low	GPIO Pin Sinking 4mA (Used as Digital Output)	●			0.4	V
ADC Timing Specifications							
t_{CYCLE} (Figure 3)	Measurement + Calibration Cycle Time When Starting from the REFUP State in Normal Mode	Measure 12 Cells	●	2120	2335	2480	µs
		Measure 2 Cells	●	365	405	430	µs
		Measure 12 Cells and 2 GPIO Inputs	●	2845	3133	3325	µs
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Filtered Mode	Measure 12 Cells	●	183	201.3	213.5	ms
		Measure 2 Cells	●	30.54	33.6	35.64	ms
		Measure 12 Cells and 2 GPIO Inputs	●	244	268.4	284.7	ms
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Fast Mode	Measure 12 Cells	●	1010	1113	1185	µs
		Measure 2 Cells	●	180	201	215	µs
		Measure 12 Cells and 2 GPIO Inputs	●	1420	1564	1660	µs
t_{SKEW1} (Figure 6)	Skew Time. The Time Difference between C12 and GPIO2 Measurements, Command = ADCVAX	Fast Mode	●	189	208	221	µs
		Normal Mode	●	493	543	576	µs
t_{SKEW2} (Figure 3)	Skew Time. The Time Difference between C12 and C0 Measurements, Command = ADCV	Fast Mode	●	211	233	248	µs
		Normal Mode	●	609	670	711	µs
t_{WAKE}	Regulator Start-Up Time	V_{REG} Generated from Drive Pin (Figure 28)	●		100	300	µs
t_{SLEEP}	Watchdog or Software Discharge Timer	SWTEN Pin = 0 or DCTO[3:0] = 0000	●	1.8	2	2.2	sec
		SWTEN Pin = 1 and DCTO[3:0] ≠ 0000		0.5		120	min
t_{REFUP} (Figure 1, Figures 3 to 7)	Reference Wake-Up Time	State: Core = STANDBY	●	2.7	3.5	4.4	ms
		State: Core = REFUP	●			0	ms
f_S	ADC Clock Frequency		●	3.0	3.3	3.5	MHz
SPI Interface DC Specifications							
$V_{IH(SPI)}$	SPI Pin Digital Input Voltage High	Pins CSB, SCK, SDI	●	2.3			V
$V_{IL(SPI)}$	SPI Pin Digital Input Voltage Low	Pins CSB, SCK, SDI	●			0.8	V
$V_{IH(CFG)}$	Configuration Pin Digital Input Voltage High	Pins ISOMD, SWTEN, GPIO1 to GPIO5, A0 to A3	●	2.7			V
$V_{IL(CFG)}$	Configuration Pin Digital Input Voltage Low	Pins ISOMD, SWTEN, GPIO1 to GPIO5, A0 to A3	●			1.2	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{LEAK(DIG)}$	Digital Input Current	Pins CSB, SCK, SDI, ISOMD, SWTEN, A0 to A3	●			±1	µA
$V_{OL(SDO)}$	Digital Output Low	Pin SDO Sinking 1mA	●			0.3	V
isoSPI DC Specifications (See Figure 16)							
V_{BIAS}	Voltage on IBIAS Pin	READY/ACTIVE State IDLE State	●	1.9	2.0 0	2.1	V V
I_B	Isolated Interface Bias Current	R_{BIAS} = 2k to 20k	●	0.1		1.0	mA
A_{IB}	Isolated Interface Current Gain	$V_A \le$ 1.6V I_B = 1mA I_B = 0.1mA	● ●	18 18	20 20	22 24.5	mA/mA mA/mA
V_A	Transmitter Pulse Amplitude	$V_A = \lvert V_{IP} - V_{IM} \rvert$	●			1.6	V
V_{ICMP}	Threshold-Setting Voltage on ICMP Pin	$V_{TCMP} = A_{TCMP} \bullet V_{ICMP}$	●	0.2		1.5	V
$I_{LEAK(ICMP)}$	Input Leakage Current on ICMP Pin	V_{ICMP} = 0V to V_{REG}	●			±1	µA
$I_{LEAK(IP/IM)}$	Leakage Current on IP and IM Pins	IDLE State, V_{IP} or V_{IM} = 0V to V_{REG}	●			±1	µA
A_{TCMP}	Receiver Comparator Threshold Voltage Gain	$V_{CM} = V_{REG}/2$ to V_{REG} – 0.2V, V_{ICMP} = 0.2V to 1.5V	●	0.4	0.5	0.6	V/V
V_{CM}	Receiver Common Mode Bias	IP/IM Not Driving			($V_{REG} - V_{ICMP}/3$ – 167mV)		V
R_{IN}	Receiver Input Resistance	Single-Ended to IPA, IMA, IPB, IMB	●	27	35	43	kΩ
isoSPI Idle/Wakeup Specifications (See Figure 21)							
V_{WAKE}	Differential Wake-Up Voltage	t_{DWELL} = 240ns	●	200			mV
t_{DWELL}	Dwell Time at V_{WAKE} Before Wake Detection	V_{WAKE} = 200mV	●	240			ns
t_{READY}	Startup Time After Wake Detection		●			10	µs
t_{IDLE}	Idle Timeout Duration		●	4.3	5.5	6.7	ms
isoSPI Pulse Timing Specifications (See Figure 19)							
$t_{1/2PW(CS)}$	Chip-Select Half-Pulse Width		●	120	150	180	ns
$t_{INV(CS)}$	Chip-Select Pulse Inversion Delay		●			200	ns
$t_{1/2PW(D)}$	Data Half-Pulse Width		●	40	50	60	ns
$t_{INV(D)}$	Data Pulse Inversion Delay		●			70	ns
SPI Timing Requirements (See Figure 15 and Figure 20)							
t_{CLK}	SCK Period	(Note 4)	●	1			µs
t_1	SDI Setup Time before SCK Rising Edge		●	25			ns
t_2	SDI Hold Time after SCK Rising Edge		●	25			ns
t_3	SCK Low	$t_{CLK} = t_3 + t_4 \ge 1\mu s$	●	200			ns
t_4	SCK High	$t_{CLK} = t_3 + t_4 \ge 1\mu s$	●	200			ns
t_5	CSB Rising Edge to CSB Falling Edge		●	0.65			µs
t_6	SCK Rising Edge to CSB Rising Edge	(Note 4)	●	0.8			µs
t_7	CSB Falling Edge to SCK Rising Edge	(Note 4)	●	1			µs

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
isoSPI Timing Specifications (See Figure 19)							
t_8	SCK Falling Edge to SDO Valid	(Note 5)	●			60	ns
t_9	SCK Rising Edge to Short ±1 Transmit		●			50	ns
t_{10}	CSB Transition to Long ±1 Transmit		●			60	ns
t_{11}	CSB Rising Edge to SDO Rising	(Note 5)	●			200	ns
t_{RTN}	Data Return Delay		●		430	525	ns
$t_{DSY(CS)}$	Chip-Select Daisy-Chain Delay		●		150	200	ns
$t_{DSY(D)}$	Data Daisy-Chain Delay		●		300	360	ns
t_{LAG}	Data Daisy-Chain Lag (vs Chip-Select)		●	0	35	70	ns
$t_{6(GOV)}$	Data to Chip-Select Pulse Governor		●	0.8		1.05	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ADC specifications are guaranteed by the Total Measurement Error specification.

Note 3: The ACTIVE state current is calculated from DC measurements. The ACTIVE state current is the additional average supply current into V_{REG} when there is continuous 1MHz communications on the isoSPI ports with 50% data 1's and 50% data 0's. Slower clock rates reduce the supply current. See Applications Information section for additional details.

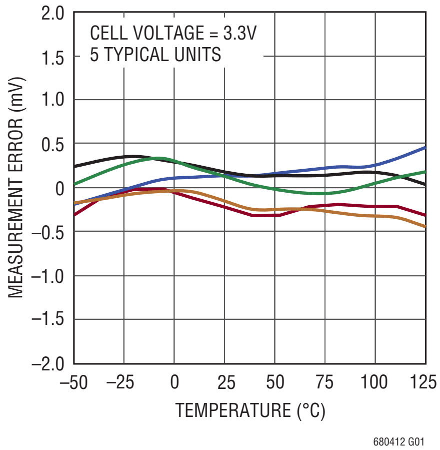
Note 4: These timing specifications are dependent on the delay through the cable, and include allowances for 50ns of delay each direction. 50ns corresponds to 10m of CAT-5 cable (which has a velocity of propagation of 66% the speed of light). Use of longer cables would require derating these specs by the amount of additional delay.

Note 5: These specifications do not include rise or fall time of SDO. While fall time (typically 5ns due to the internal pull-down transistor) is not a concern, rising-edge transition time t_{RISE} is dependent on the pull-up resistance and load capacitance on the SDO pin. The time constant must be chosen such that SDO meets the setup time requirements of the MCU.

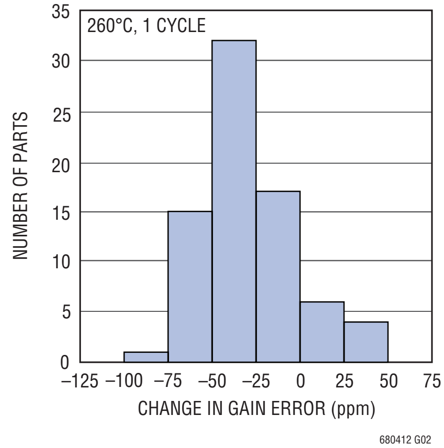
Note 6: V^+ needs to be greater than or equal to the highest C(n) voltage for accurate measurements. See the graph Top Cell Measurement Error vs V^+.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

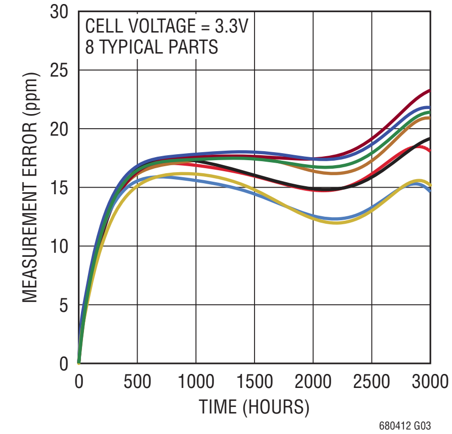
Measurement Error vs Temperature



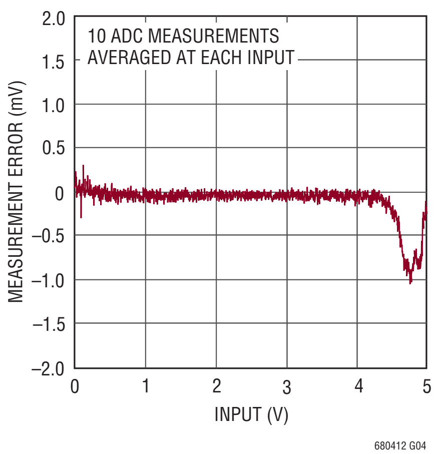
Measurement Error Due to IR Reflow



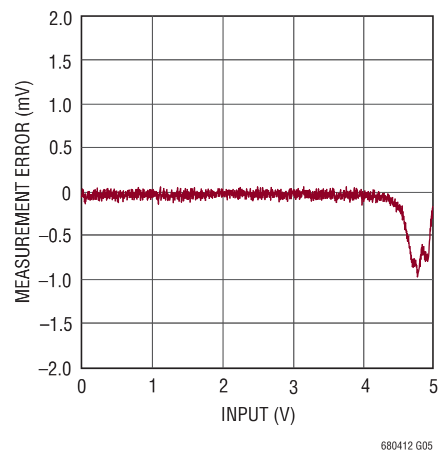
Measurement Error Long-Term Drift



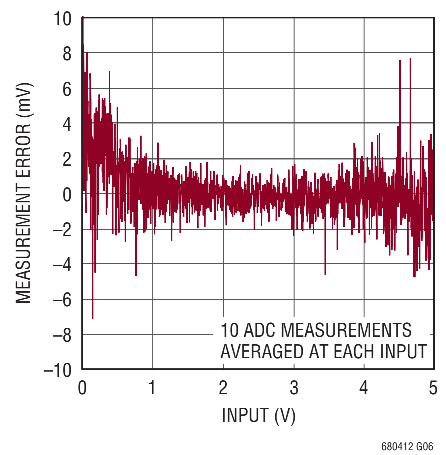
Measurement Error vs Input, Normal Mode



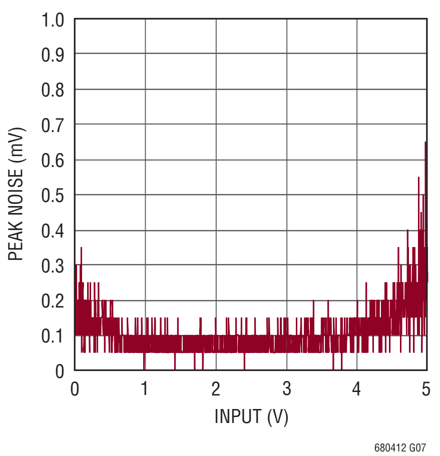
Measurement Error vs Input, Filtered Mode



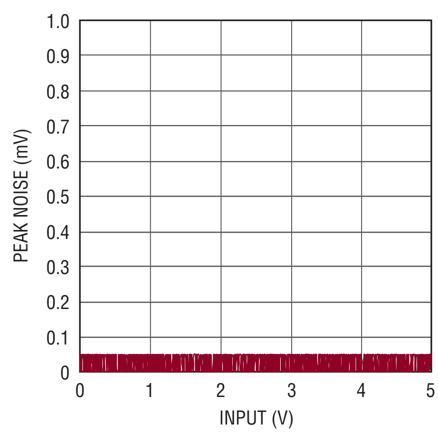
Measurement Error vs Input, Fast Mode



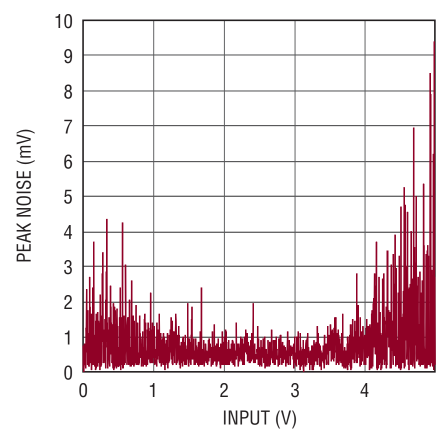
Measurement Noise vs Input, Normal Mode



Measurement Noise vs Input, Filtered Mode

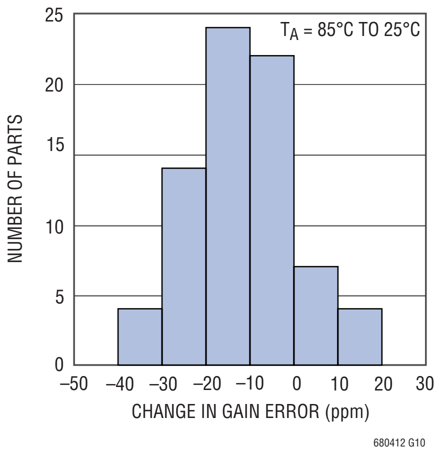


Measurement Noise vs Input, Fast Mode

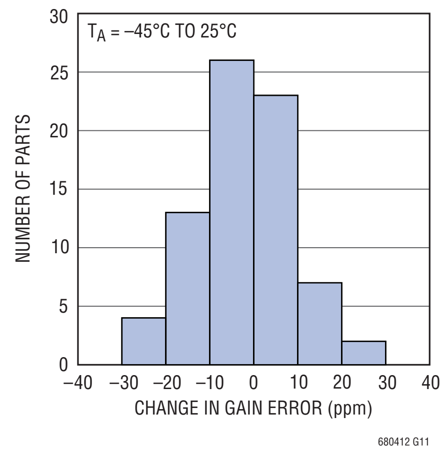


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

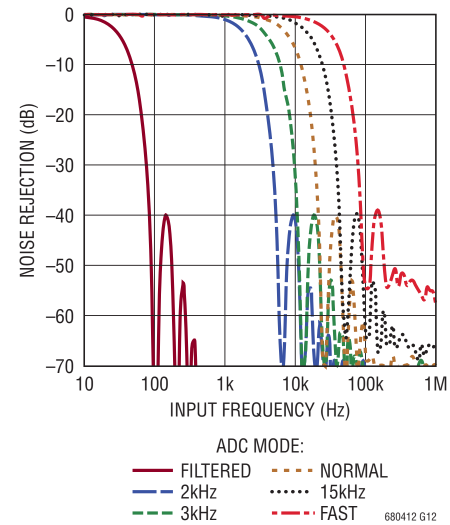
Measurement Gain Error Hysteresis, Hot



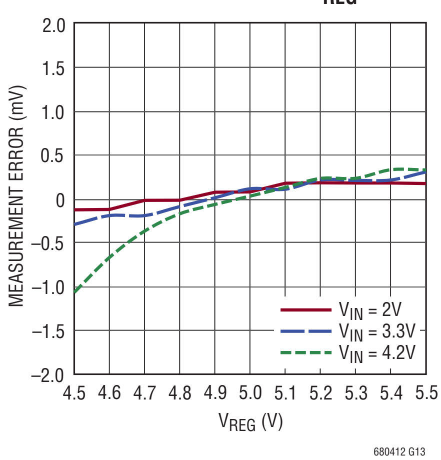
Measurement Gain Error Hysteresis, Cold



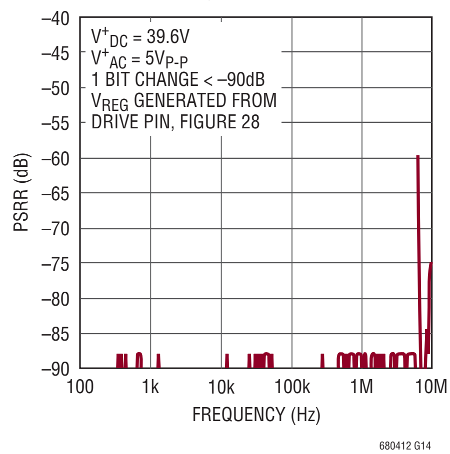
Noise Filter Response



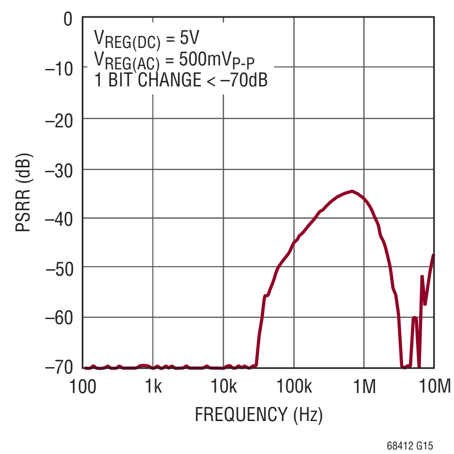
Measurement Error vs V_{REG}



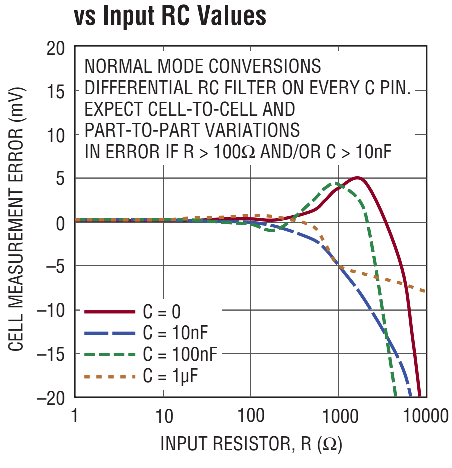
Measurement Error V+ PSRR vs Frequency



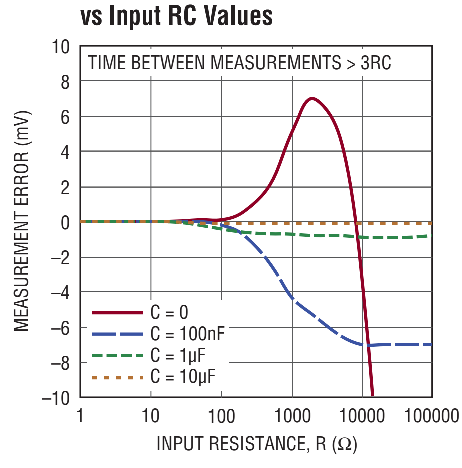
Measurement Error V_{REG} PSRR vs Frequency



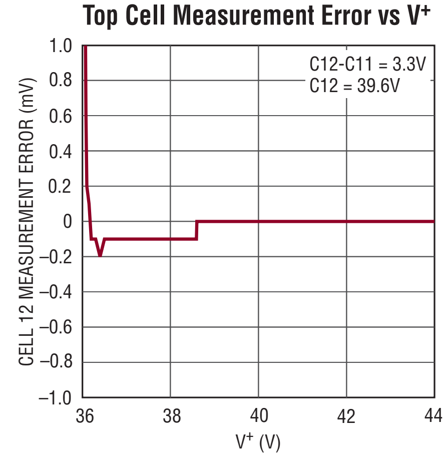
Cell Measurement Error vs Input RC Values



GPIO Measurement Error vs Input RC Values

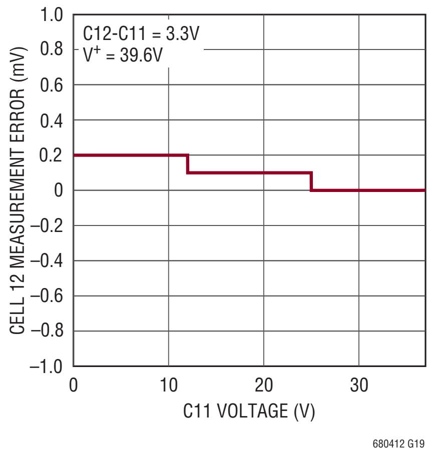


Top Cell Measurement Error vs V+

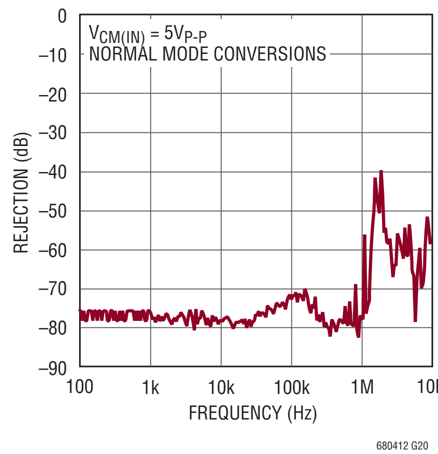


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

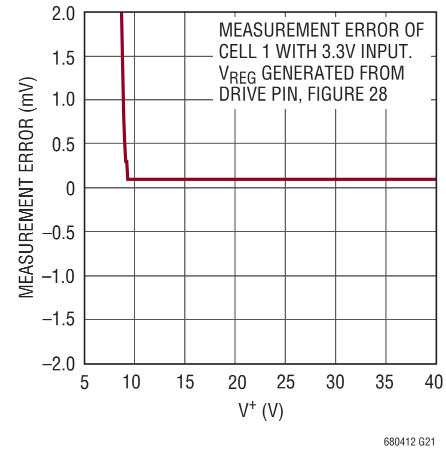
Cell Measurement Error vs Common Mode Voltage



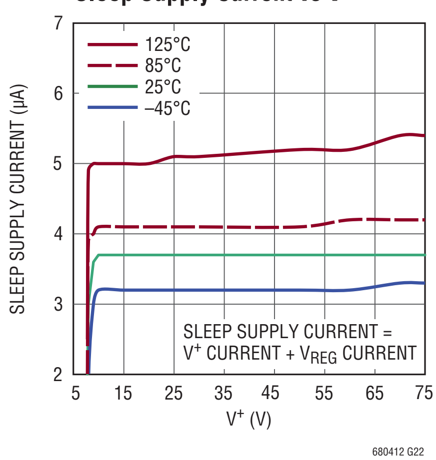
Cell Measurement CMRR vs Frequency



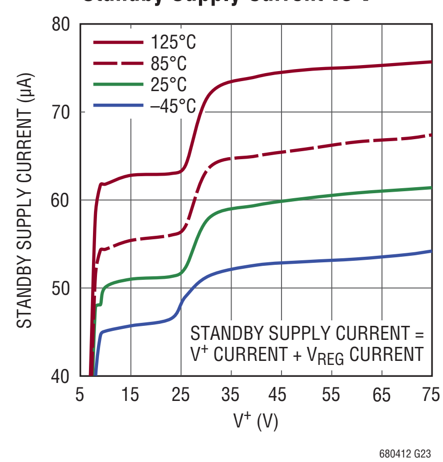
Measurement Error vs V+



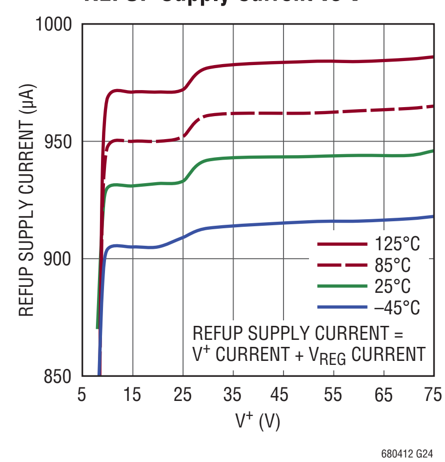
Sleep Supply Current vs V+



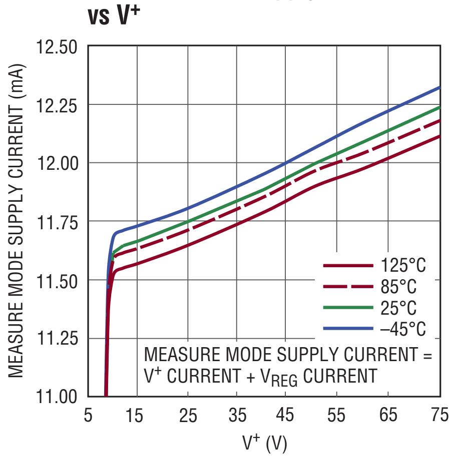
Standby Supply Current vs V+



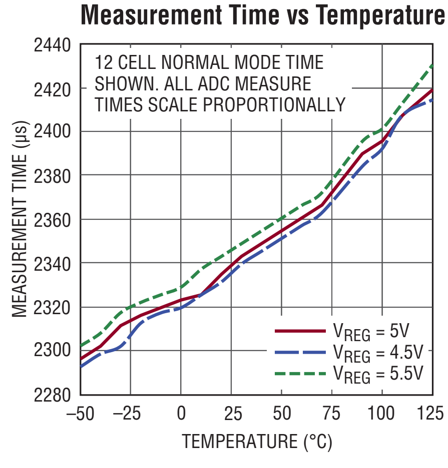
REFUP Supply Current vs V+



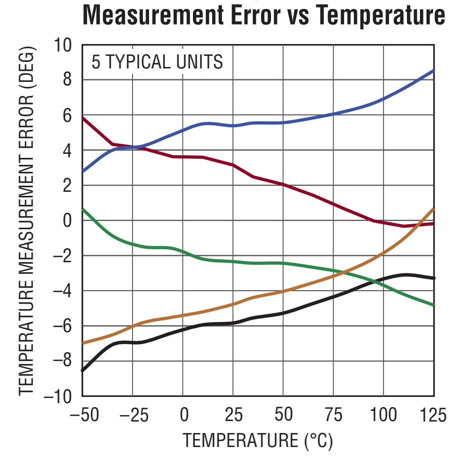
Measure Mode Supply Current vs V+



Measurement Time vs Temperature

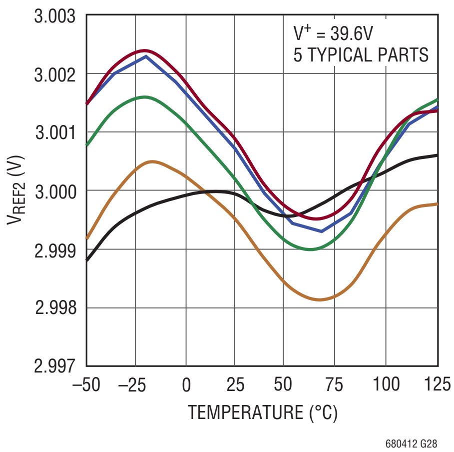


Internal Die Temperature Measurement Error vs Temperature

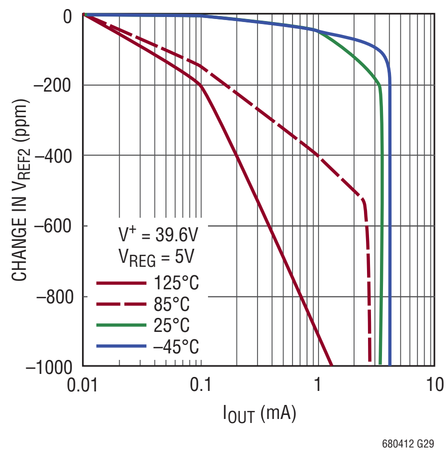


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

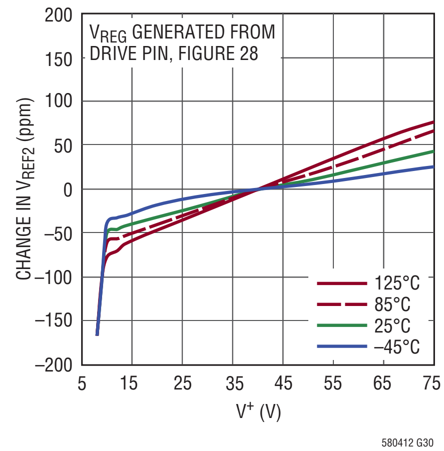
V_{REF2} vs Temperature



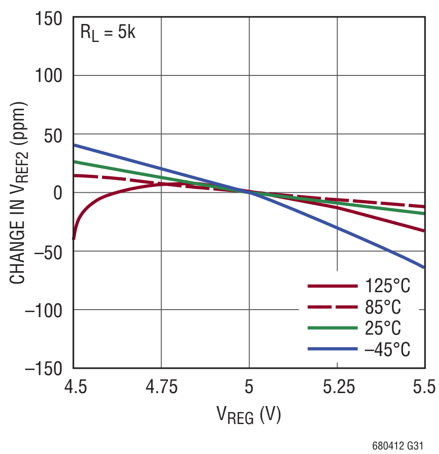
V_{REF2} Load Regulation



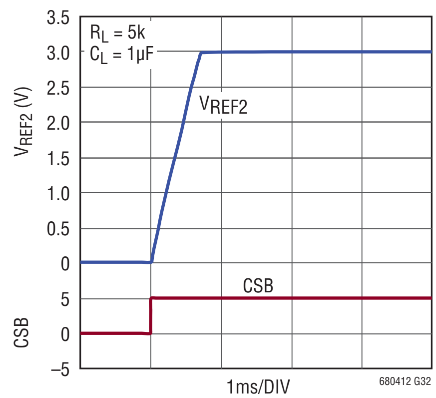
V_{REF2} V^+ Line Regulation



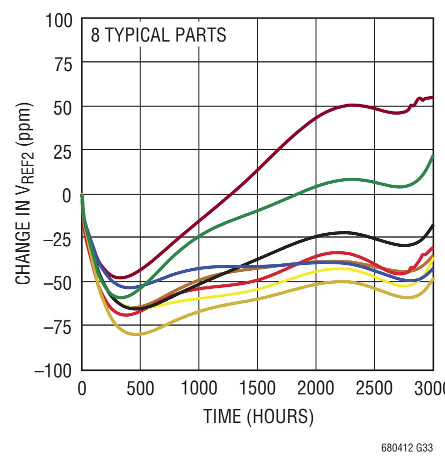
V_{REF2} V_{REG} Line Regulation



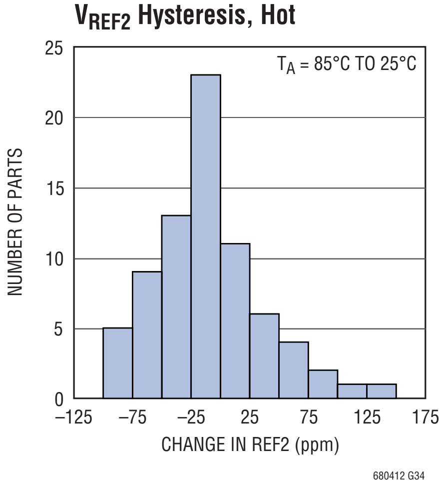
V_{REF2} Power-Up



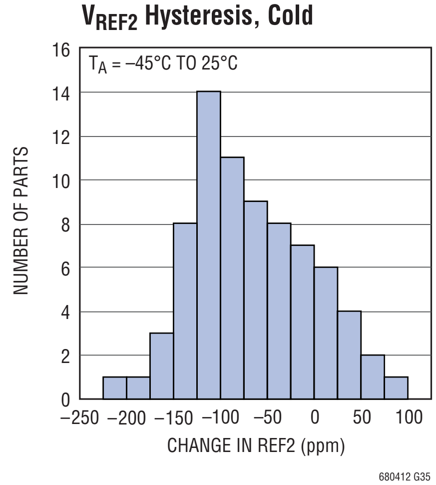
V_{REF2} Long-Term Drift



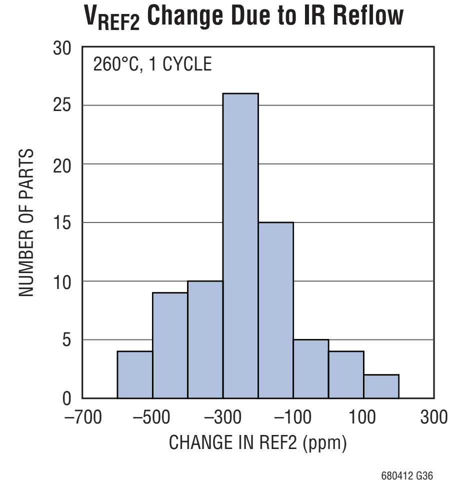
V_{REF2} Hysteresis, Hot



V_{REF2} Hysteresis, Cold

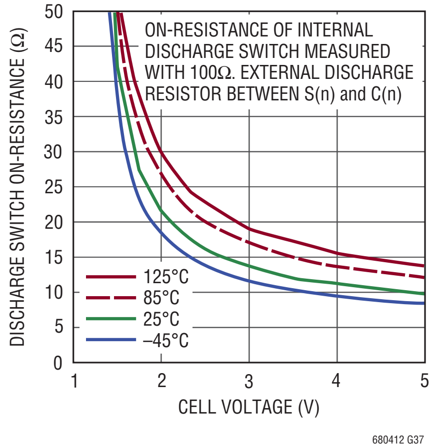


V_{REF2} Change Due to IR Reflow

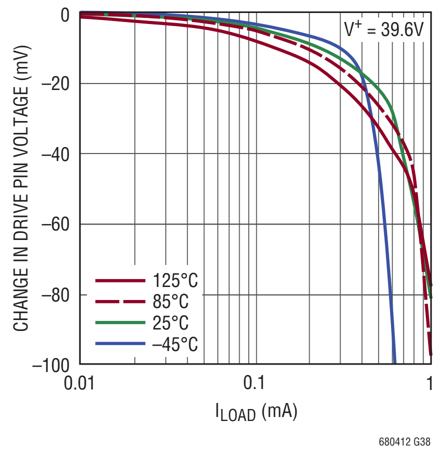


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

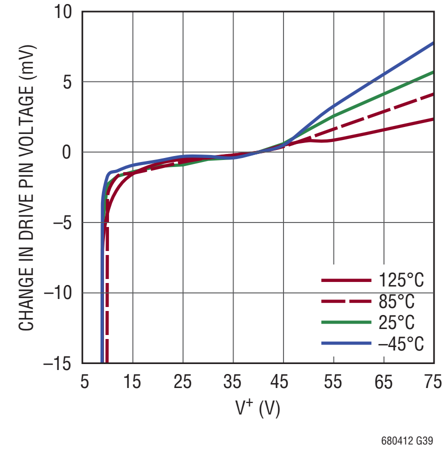
Discharge Switch On-Resistance vs Cell Voltage



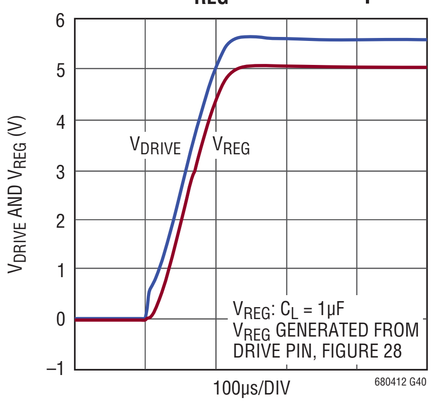
Drive Pin Load Regulation



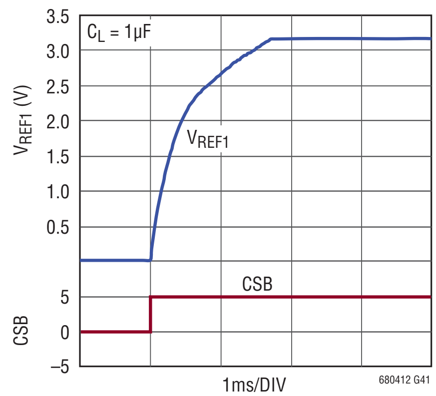
Drive Pin Line Regulation



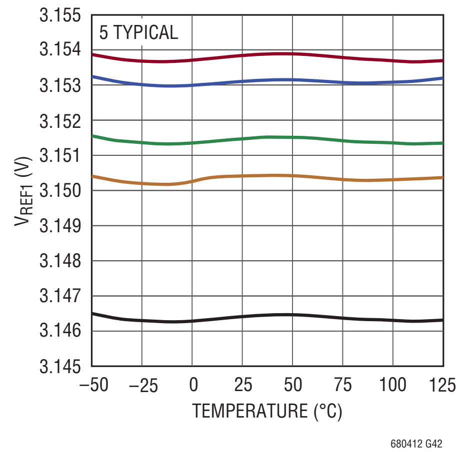
Drive and V_{REG} Pin Power-Up



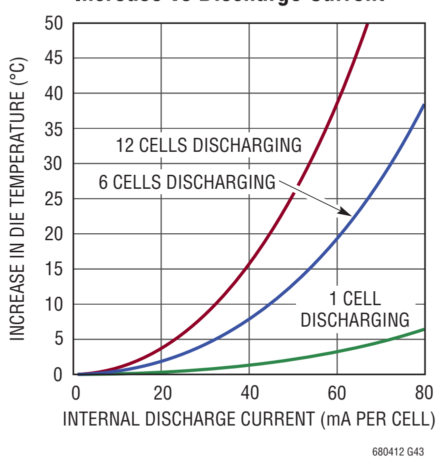
V_{REF1} Power-Up



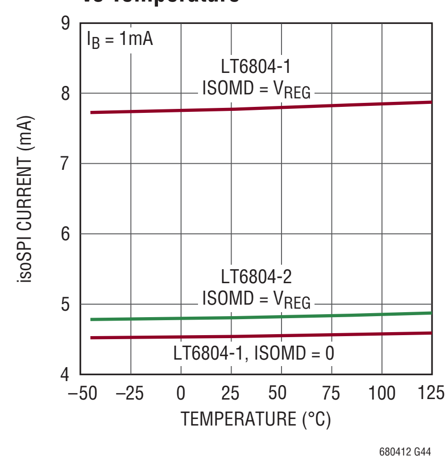
V_{REF1} vs Temperature



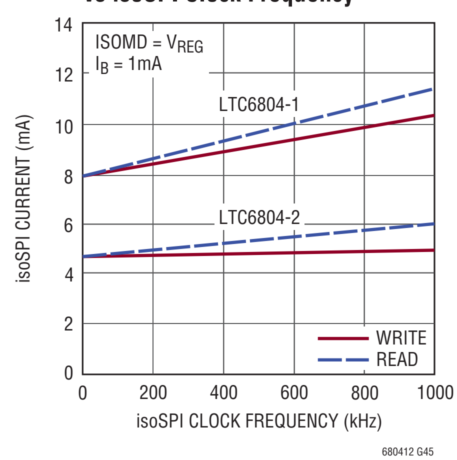
Internal Die Temperature Increase vs Discharge Current



isoSPI Current (READY) vs Temperature

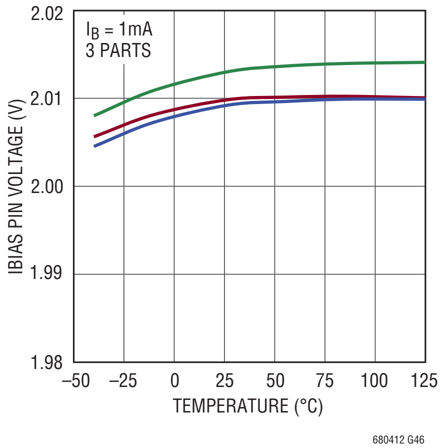


isoSPI Current (READY/ACTIVE) vs isoSPI Clock Frequency

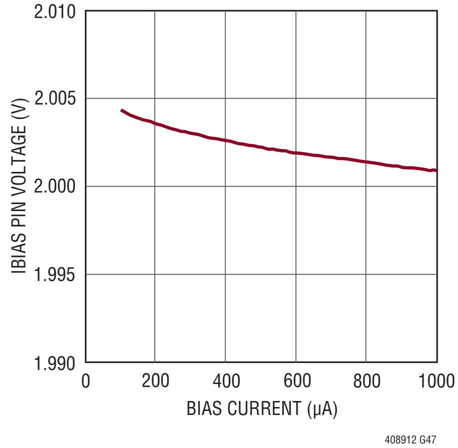


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

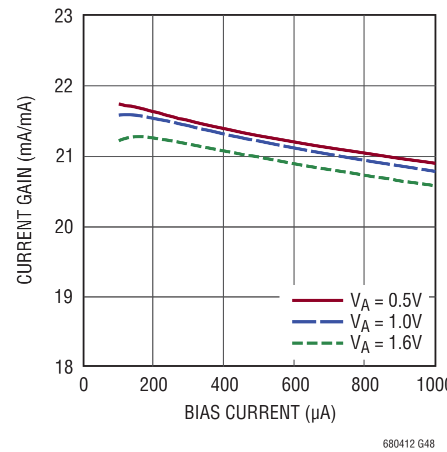
I_{BIAS} Voltage vs Temperature



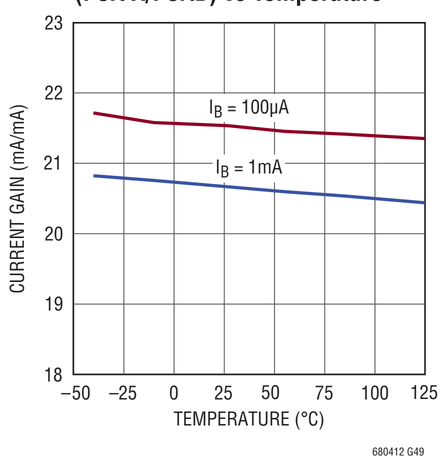
I_{BIAS} Voltage Load Regulation



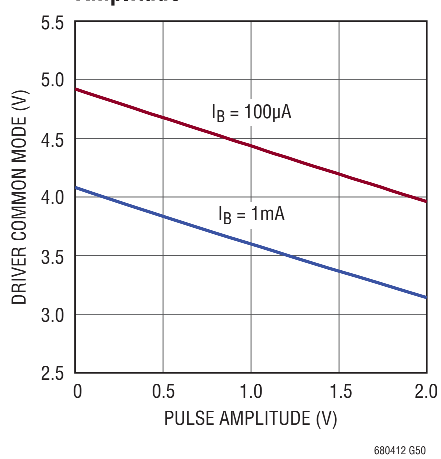
isoSPI Driver Current Gain (Port A/PortB) vs Bias Current



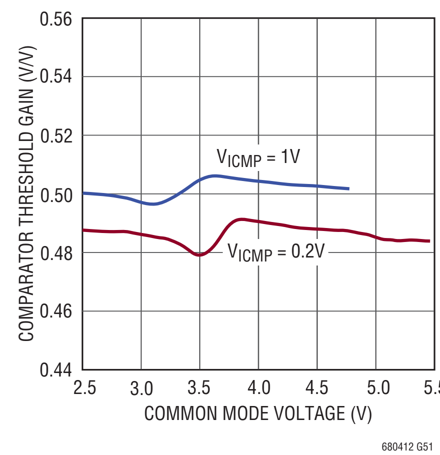
isoSPI Driver Current Gain (Port A/PortB) vs Temperature



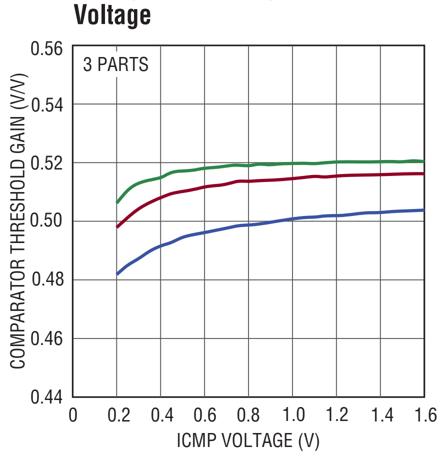
isoSPI Driver Common Mode Voltage (Port A/Port B) vs Pulse Amplitude



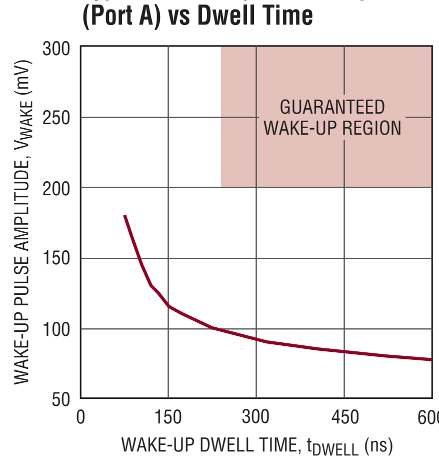
isoSPI Comparator Threshold Gain (Port A/Port B) vs Common Mode



isoSPI Comparator Threshold Gain (Port A/Port B) vs ICMP Voltage

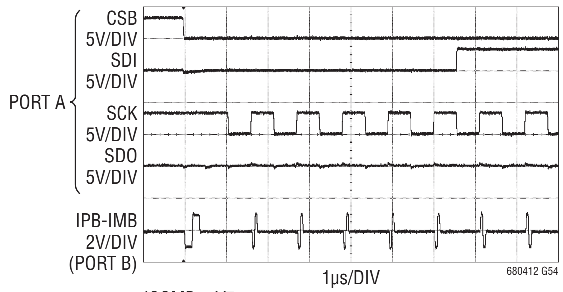


Typical Wake-Up Pulse Amplitude (Port A) vs Dwell Time



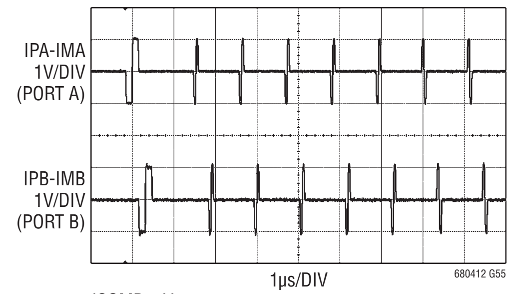
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Write Command to a Daisy-Chained Device (ISOMD = 0)



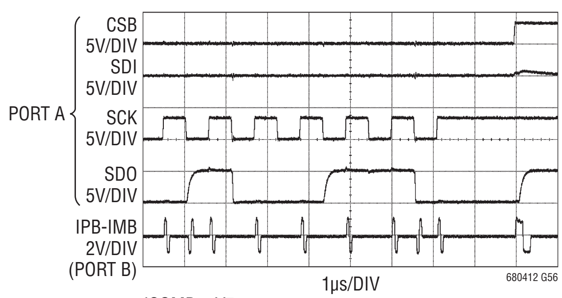
ISOMD = V^-
BEGINNING OF A COMMAND

Write Command to a Daisy-Chained Device (ISOMD = 1)



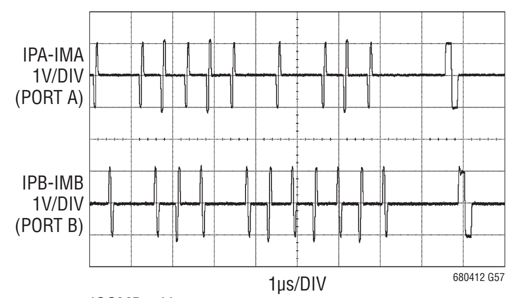
ISOMD = V_{REG}
BEGINNING OF A COMMAND

Data Read-Back from a Daisy-Chained Device (ISOMD = 0)



ISOMD = V^-
END OF A READ COMMAND

Data Read-Back from a Daisy-Chained Device (ISOMD = 1)



ISOMD = V_{REG}
END OF A READ COMMAND

PIN FUNCTIONS

C0 to C12: Cell Inputs.

S1 to S12: Balance Inputs/Outputs. 12 N-MOSFETs are connected between S(n) and C(n – 1) for discharging cells.

V^+: Positive Supply Pin.

$V^–$: Negative Supply Pins. The $V^–$ pins must be shorted together, external to the IC.

V_{REF2}: Buffered 2nd reference voltage for driving multiple 10k thermistors. Bypass with an external 1µF capacitor.

V_{REF1}: ADC Reference Voltage. Bypass with an external 1µF capacitor. No DC loads allowed.

GPIO[1:5]: General Purpose I/O. Can be used as digital inputs or digital outputs, or as analog inputs with a measurement range from $V^–$ to 5V. GPIO [3:5] can be used as an I^2C or SPI port.

SWTEN: Software Timer Enable. Connect this pin to V_{REG} to enable the software timer.

DRIVE: Connect the base of an NPN to this pin. Connect the collector to V^+ and the emitter to V_{REG}.

V_{REG}: 5V Regulator Input. Bypass with an external 1µF capacitor.

ISOMD: Serial Interface Mode. Connecting ISOMD to V_{REG} configures Pins 41 to 44 of the LTC6804 for 2-wire isolated interface (isoSPI) mode. Connecting ISOMD to $V^–$ configures the LTC6804 for 4-wire SPI mode.

WDT: Watchdog Timer Output Pin. This is an open drain NMOS digital output. It can be left unconnected or connected with a 1M resistor to V_{REG}. If the LTC6804 does not receive a valid command within 2 seconds, the watchdog timer circuit will reset the LTC6804 and the WDT pin will go high impedance.

Serial Port Pins

	LTC6804-1 (DAISY-CHAINABLE)		LTC6804-2 (ADDRESSABLE)	
	ISOMD = V_{REG}	ISOMD = $V^–$	ISOMD = V_{REG}	ISOMD = $V^–$
PORT B (Pins 45 to 48)	IPB	IPB	A3	A3
	IMB	IMB	A2	A2
	ICMP	ICMP	A1	A1
	IBIAS	IBIAS	A0	A0
PORT A (Pins 41 to 44)	(NC)	SDO	IBIAS	SDO
	(NC)	SDI	ICMP	SDI
	IPA	SCK	IPA	SCK
	IMA	CSB	IMA	CSB

CSB, SCK, SDI, SDO: 4-Wire Serial Peripheral Interface (SPI). Active low chip select (CSB), serial clock (SCK), and serial data in (SDI) are digital inputs. Serial data out (SDO) is an open drain NMOS output pin. SDO requires a 5k pull-up resistor.

A0 to A3: Address Pins. These digital inputs are connected to V_{REG} or $V^–$ to set the chip address for addressable serial commands.

IPA, IMA: Isolated 2-Wire Serial Interface Port A. IPA (plus) and IMA (minus) are a differential input/output pair.

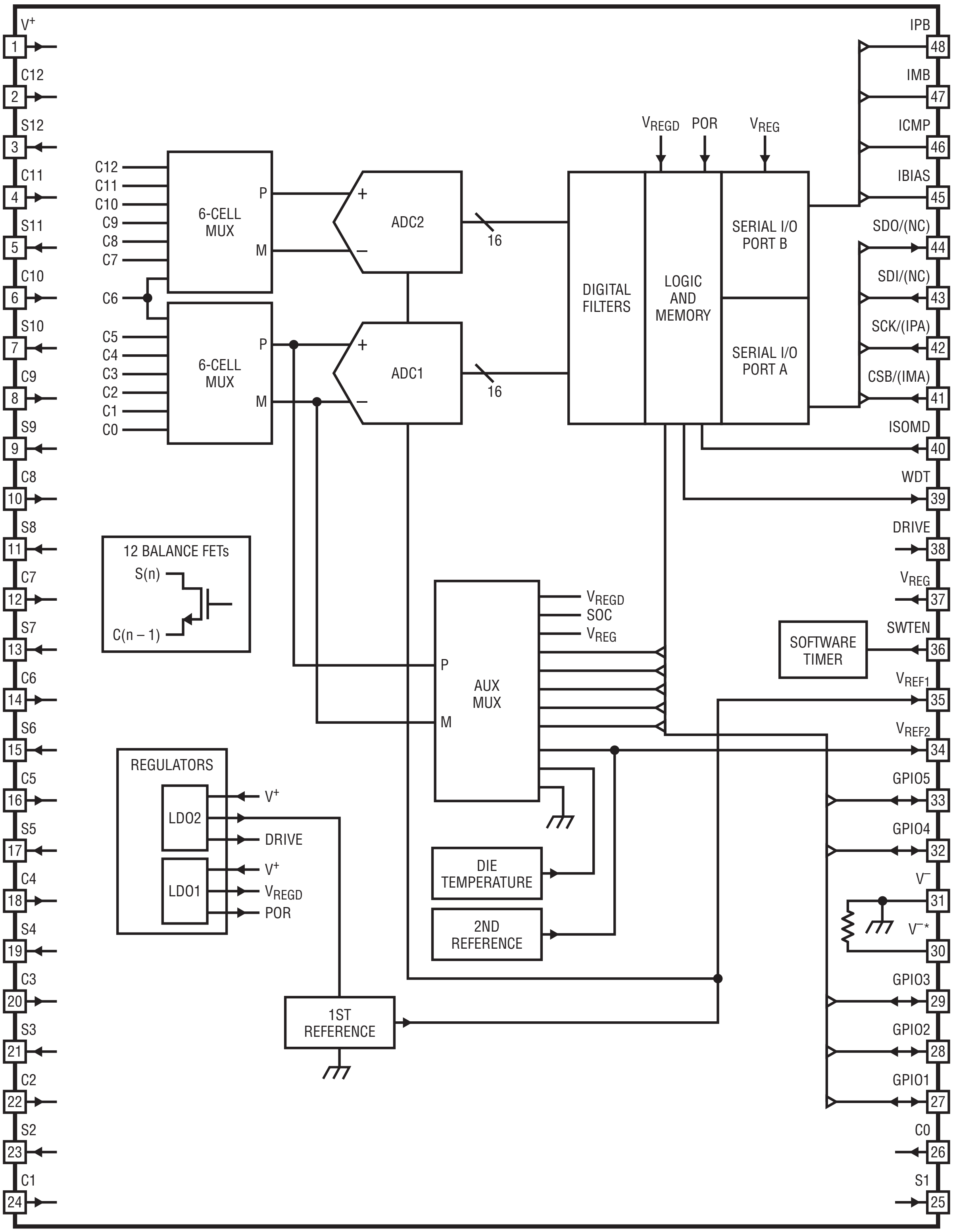
IPB, IMB: Isolated 2-Wire Serial Interface Port B. IPB (plus) and IMB (minus) are a differential input/output pair.

IBIAS: Isolated Interface Current Bias. Tie IBIAS to $V^–$ through a resistor divider to set the interface output current level. When the isoSPI interface is enabled, the IBIAS pin voltage is 2V. The IPA/IMA or IPB/IMB output current drive is set to 20 times the current, I_B, sourced from the IBIAS pin.

ICMP: Isolated Interface Comparator Voltage Threshold Set. Tie this pin to the resistor divider between IBIAS and $V^–$ to set the voltage threshold of the isoSPI receiver comparators. The comparator thresholds are set to 1/2 the voltage on the ICMP pin.

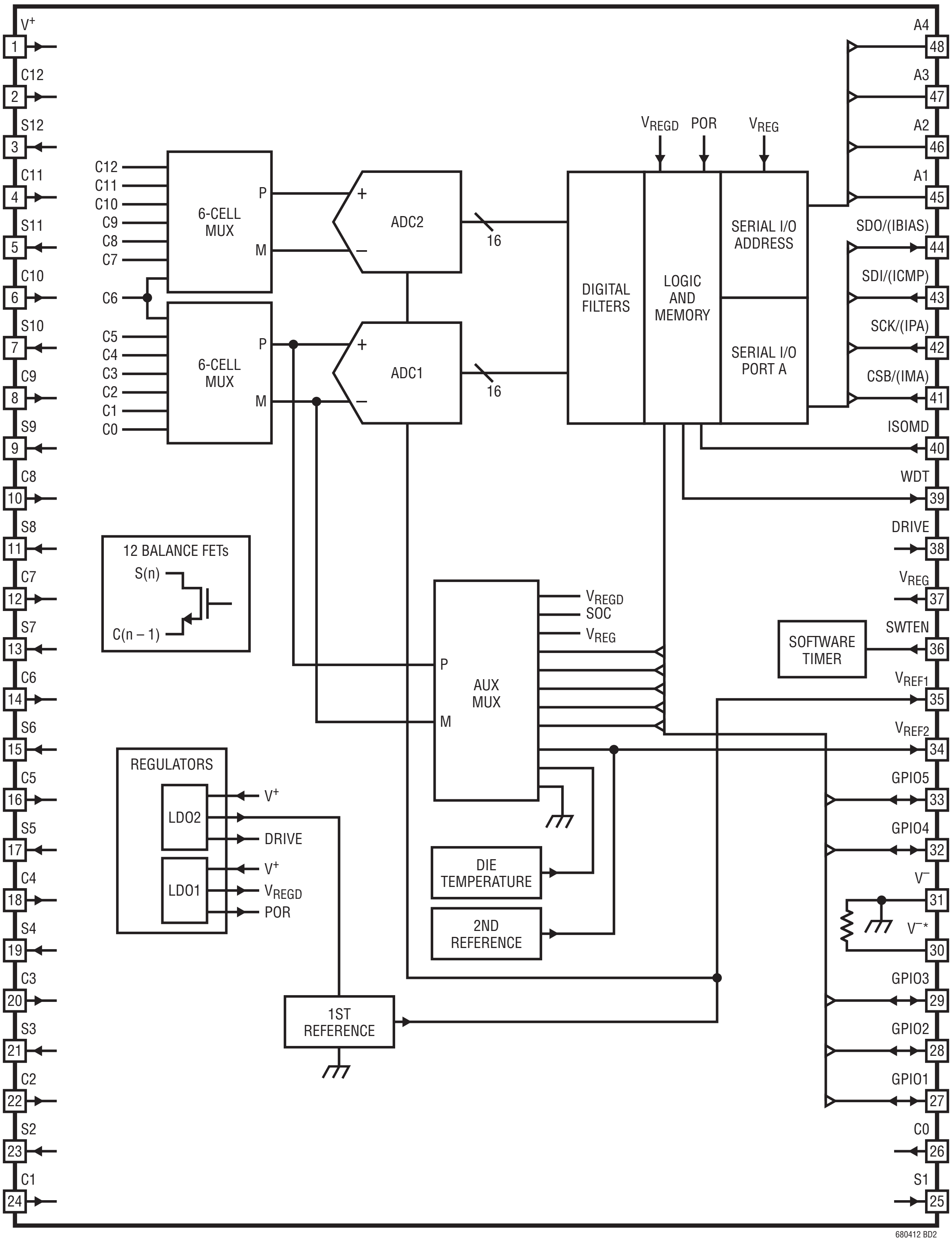
BLOCK DIAGRAM

LTC6804-1



BLOCK DIAGRAM

LTC6804-2



OPERATION

STATE DIAGRAM

The operation of the LTC6804 is divided into two separate sections: the core circuit and the isoSPI circuit. Both sections have an independent set of operating states, as well as a shutdown timeout.

LTC6804 CORE STATE DESCRIPTIONS

SLEEP State

The reference and ADCs are powered down. The watchdog timer (see Watchdog and Software Discharge Timer) has timed out. The software discharge timer is either disabled or timed out. The supply currents are reduced to minimum levels. The isoSPI ports will be in the IDLE state.

If a WAKEUP signal is received (see Waking Up the Serial Interface), the LTC6804 will enter the STANDBY state.

STANDBY State

The reference and the ADCs are off. The watchdog timer and/or the software discharge timer is running. The DRIVE pin powers the V_{REG} pin to 5V through an external transistor. (Alternatively, V_{REG} can be powered by an external supply).

When a valid ADC command is received or the REFON bit is set to 1 in the Configuration Register Group, the IC pauses for t_{REFUP} to allow for the reference to power up and then enters either the REFUP or MEASURE state. Otherwise, after t_{SLEEP} (when both the watchdog and software discharge timer have expired) the LTC6804 returns to the SLEEP state. If the software discharge timer is disabled, only the watchdog timer is relevant.

REFUP State

To reach this state the REFON bit in the Configuration Register Group must be set to 1 (using the WRCFG command, see Table 36). The ADCs are off. The reference is powered up so that the LTC6804 can initiate ADC conversions more quickly than from the STANDBY state.

When a valid ADC command is received, the IC goes to the MEASURE state to begin the conversion. Otherwise, the LTC6804 will return to the STANDBY state when the REFON bit is set to 0, either manually (using WRCFG command) or automatically when the watchdog timer expires. (The LTC6804 will then move straight into the SLEEP state if both timers are expired).

MEASURE State

The LTC6804 performs ADC conversions in this state. The reference and ADCs are powered up.

After ADC conversions are complete the LTC6804 will transition to either the REFUP or STANDBY states, depending on the REFON bit. Additional ADC conversions can be initiated more quickly by setting REFON = 1 to take advantage of the REFUP state.

Note: Non-ADC commands do not cause a Core state transition. Only an ADC conversion or diagnostic commands will place the Core in the MEASURE state.

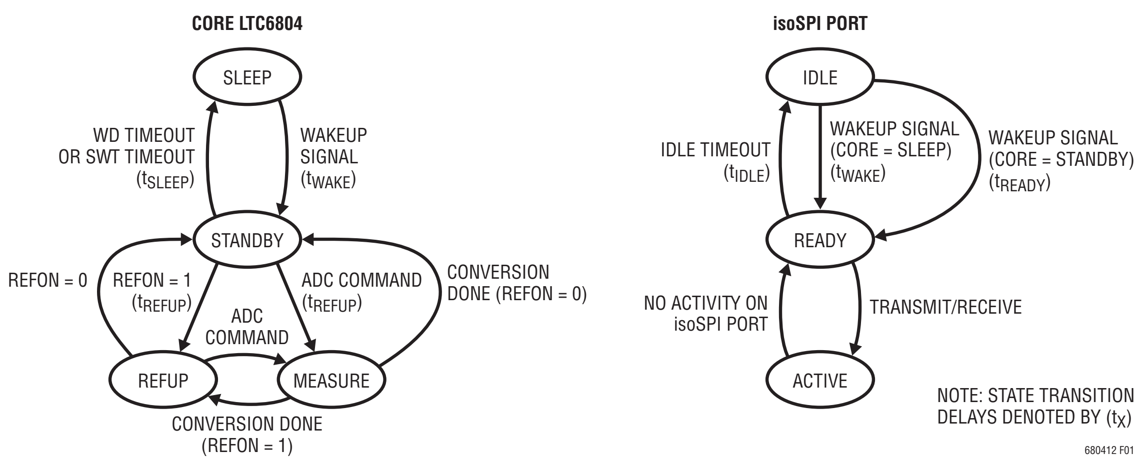


Figure 1. LTC6804 Operation State Diagram

OPERATION

isoSPI STATE DESCRIPTIONS

Note: The LTC6804-1 has two isoSPI ports (A and B), for daisy-chain communication. The LTC6804-2 has only one isoSPI port (A), for parallel-addressable communication.

IDLE State

The isoSPI ports are powered down.

When isoSPI port A receives a WAKEUP signal (see Waking Up the Serial Interface), the isoSPI enters the READY state. This transition happens quickly (within t_{READY}) if the Core is in the STANDBY state because the DRIVE and V_{REG} pins are already biased up. If the Core is in the SLEEP state when the isoSPI receives a WAKEUP signal, then it transitions to the READY state within t_{WAKE}.

READY State

The isoSPI port(s) are ready for communication. Port B is enabled only for LTC6804-1, and is not present on the LTC6804-2. The serial interface current in this state depends on if the part is LTC6804-1 or LTC6804-2, the status of the ISOMD pin, and $R_{BIAS} = R_{B1} + R_{B2}$ (the external resistors tied to the IBIAS pin).

If there is no activity (i.e., no WAKEUP signal) on port A for greater than t_{IDLE} = 5.5ms, the LTC6804 goes to the IDLE state. When the serial interface is transmitting or receiving data the LTC6804 goes to the ACTIVE state.

ACTIVE State

The LTC6804 is transmitting/receiving data using one or both of the isoSPI ports. The serial interface consumes maximum power in this state. The supply current increases with clock frequency as the density of isoSPI pulses increases.

POWER CONSUMPTION

The LTC6804 is powered via two pins: V^+ and V_{REG}. The V^+ input requires voltage greater than or equal to the top cell voltage, and it provides power to the high voltage elements of the core circuitry. V^+ can be directly connected to the top cell of the battery stack, or to an external supply. The V_{REG} input requires 5V and provides power to the remaining core circuitry and the isoSPI circuitry. The V_{REG} input can be powered through an external transistor, driven by the regulated DRIVE output pin. Alternatively, V_{REG} can be powered by an external supply.

The power consumption varies according to the operational states. Table 1 and Table 2 provide equations to approximate the supply pin currents in each state. The V^+ pin current depends only on the Core state and not on the isoSPI state. However, the V_{REG} pin current depends on both the Core state and isoSPI state, and can therefore be divided into two components. The isoSPI interface draws current only from the V_{REG} pin.

$$I_{REG} = I_{REG(CORE)} + I_{REG(isoSPI)}$$

Table 1. Core Supply Current

STATE		I_{V+}	$I_{REG(CORE)}$
SLEEP	V_{REG} = 0V	3.8µA	0µA
	V_{REG} = 5V	1.6µA	2.2µA
STANDBY		32µA	35µA
REFUP		550µA	450µA
MEASURE		550µA	11.5mA

In the SLEEP state the V_{REG} pin will draw approximately 2.2µA if powered by a external supply. Otherwise, the V^+ pin will supply the necessary current.

ADC OPERATION

There are two ADCs inside the LTC6804. The two ADCs operate simultaneously when measuring twelve cells. Only one ADC is used to measure the general purpose inputs. The following discussion uses the term ADC to refer to one or both ADCs, depending on the operation being performed. The following discussion will refer to ADC1 and ADC2 when it is necessary to distinguish between the two circuits, in timing diagrams, for example.

ADC Modes

The ADCOPT bit (CFGR0[0]) in the configuration register group and the mode selection bits MD[1:0] in the conversion command together provide 6 modes of operation for the ADC which correspond to different over sampling ratios (OSR). The accuracy of these modes are summarized in Table 3. In each mode, the ADC first measures the inputs, and then performs a calibration of each channel. The names of the modes are based on the –3dB bandwidth of the ADC measurement.

OPERATION

Table 2. isoSPI Supply Current Equations

isoSPI STATE	DEVICE	ISOMD CONNECTION	$I_{REG(isoSPI)}$
IDLE	LTC6804-1/LTC6804-2	N/A	0mA
READY	LTC6804-1	V_{REG}	$2.8mA + 5 \bullet I_B$
		V^-	$1.6mA + 3 \bullet I_B$
	LTC6804-2	V_{REG}	$1.8mA + 3 \bullet I_B$
		V^-	0mA
ACTIVE	LTC6804-1	V_{REG}	Write: $2.8mA+5\bullet I_B+(2\bullet I_B+0.4mA)\bullet\frac{1\mu s}{t_{CLK}}$ Read: $2.8mA+5\bullet I_B+(3\bullet I_B+0.5mA)\bullet\frac{1\mu s}{t_{CLK}}$
		V^-	$1.6mA+3\bullet I_B+(2\bullet I_B+0.2mA)\bullet\frac{1\mu s}{t_{CLK}}$
	LTC6804-2	V_{REG}	Write: $1.8mA+3\bullet I_B+(0.3mA)\bullet\frac{1\mu s}{t_{CLK}}$ Read: $1.8mA+3\bullet I_B+(I_B+0.3mA)\bullet\frac{1\mu s}{t_{CLK}}$
		V^-	0mA

Table 3. ADC Filter Bandwidth and Accuracy

MODE	–3dB FILTER BW	–40dB FILTER BW	TME SPEC AT 3.3V, 25°C	TME SPEC AT 3.3V,–40°C, 85°C
27kHz (Fast Mode)	27kHz	84kHz	±4.7mV	±4.7mV
14kHz	13.5kHz	42kHz	±4.7mV	±4.7mV
7kHz (Normal Mode)	6.8kHz	21kHz	±1.2mV	±2.2mV
3kHz	3.4kHz	10.5kHz	±1.2mV	±2.2mV
2kHz	1.7kHz	5.3kHz	±1.2mV	±2.2mV
26Hz (Filtered Mode)	26Hz	82Hz	±1.2mV	±2.2mV

Note: TME is the total measurement error.

Mode 7kHz (Normal):

In this mode, the ADC has high resolution and low TME (total measurement error). This is considered the normal operating mode because of the optimum combination of speed and accuracy.

Mode 27kHz (Fast):

In this mode, the ADC has maximum throughput but has some increase in TME (total measurement error). So this mode is also referred to as the fast mode. The increase in speed comes from a reduction in the oversampling ratio. This results in an increase in noise and average measurement error.

Mode 26Hz (Filtered):

In this mode, the ADC digital filter –3dB frequency is lowered to 26Hz by increasing the OSR. This mode is also referred to as the filtered mode due to its low –3dB frequency. The accuracy is similar to the 7kHz (Normal) mode with lower noise.

Modes 14kHz, 3kHz and 2kHz:

Modes 14kHz, 3kHz and 2kHz provide additional options to set the ADC digital filter –3dB frequency at 13.5kHz, 3.4kHz and 1.7kHz respectively. The accuracy of the 14kHz mode is similar to the 27kHz (fast) mode. The accuracy of 3kHz and 2kHz modes is similar to the 7kHz (normal) mode.

OPERATION

The conversion times for these modes are provided in Table 5. If the core is in STANDBY state, an additional t_{REFUP} time is required to power up the reference before beginning the ADC conversions. The reference can remain powered up between ADC conversions if the REFON bit in Configuration Register Group is set to 1 so the core is in REFUP state after a delay t_{REFUP}. Then, the subsequent ADC commands will not have the t_{REFUP} delay before beginning ADC conversions.

ADC Range and Resolution

The C inputs and GPIO inputs have the same range and resolution. The ADC inside the LTC6804 has an approximate range from –0.82V to 5.73V. Negative readings are rounded to 0V. The format of the data is a 16-bit unsigned integer where the LSB represents 100µV. Therefore, a reading of 0x80E8 (33,000 decimal) indicates a measurement of 3.3V.

Delta-Sigma ADCs have quantization noise which depends on the input voltage, especially at low over sampling ratios (OSR), such as in FAST mode. In some of the ADC modes, the quantization noise increases as the input voltage approaches the upper and lower limits of the ADC range. For example, the total measurement noise versus input voltage in normal and filtered modes is shown in Figure 2.

The specified range of the ADC is 0V to 5V. In Table 4, the precision range of the ADC is arbitrarily defined as 0.5V to 4.5V. This is the range where the quantization noise is relatively constant even in the lower OSR modes (see Figure 2). Table 4 summarizes the total noise in this range for all six ADC operating modes. Also shown is the noise

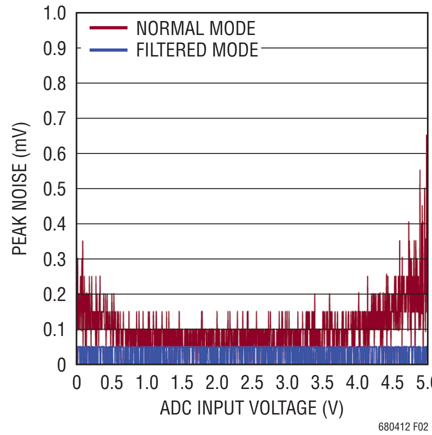


Figure 2. Measurement Noise vs Input Voltage

free resolution. For example, 14-bit noise free resolution in normal mode implies that the top 14 bits will be noise free with a DC input, but that the 15th and 16th least significant bits (LSB) will flicker.

ADC Range vs Voltage Reference Value:

Typical Delta-Sigma ADC's have a range which is exactly twice the value of the voltage reference, and the ADC measurement error is directly proportional to the error in the voltage reference. The LTC6804 ADC is not typical. The absolute value of V_{REF1} is trimmed up or down to compensate for gain errors in the ADC. Therefore, the ADC total measurement error (TME) specifications are superior to the V_{REF1} specifications. For example, the 25°C specification of the total measurement error when measuring 3.300V in 7kHz (normal) mode is ±1.2mV and the 25°C specification for V_{REF1} is 3.200V ±100mV.

Table 4. ADC Range and Resolution

MODE	FULL RANGE[1]	SPECIFIED RANGE	PRECISION RANGE[2]	LSB	FORMAT	MAX NOISE	NOISE FREE RESOLUTION[3]
27kHz (Fast)	–0.8192V to 5.7344V	0V to 5V	0.5V to 4.5V	100µV	Unsigned 16 Bits	±4mV$_{P-P}$	10 Bits
14kHz						±1mV$_{P-P}$	12 Bits
7kHz (Normal)						±250µV$_{P-P}$	14 Bits
3kHz						±150µV$_{P-P}$	14 Bits
2kHz						±100µV$_{P-P}$	15 Bits
26Hz (Filtered)						±50µV$_{P-P}$	16 Bits

1. Negative readings are rounded to 0V.

2. PRECISION RANGE is the range over which the noise is less than MAX NOISE.

3. NOISE FREE RESOLUTION is a measure of the noise level within the PRECISION RANGE.

OPERATION

Measuring Cell Voltages (ADCV Command)

The ADCV command initiates the measurement of the battery cell inputs, pins C0 through C12. This command has options to select the number of channels to measure and the ADC mode. See the section on Commands for the ADCV command format.

Figure 3 illustrates the timing of ADCV command which measures all twelve cells. After the receipt of the ADCV command to measure all 12 cells, ADC1 sequentially measures the bottom 6 cells. ADC2 sequentially measures the top 6 cells. After the cell measurements are complete, each channel is calibrated to remove any offset errors.

Table 5 shows the conversion times for the ADCV command measuring all 12 cells. The total conversion time is given by t_{6C} which indicates the end of the calibration step.

Figure 4 illustrates the timing of the ADCV command that measures only two cells.

Table 6 shows the conversion time for ADCV command measuring only 2 cells. t_{1C} indicates the total conversion time for this command.

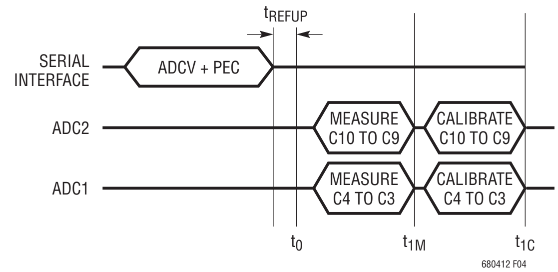


Figure 4. Timing for ADCV Command Measuring 2 Cells

Table 6. Conversion Times for ADCV Command Measuring Only 2 Cells in Different Modes

	CONVERSION TIMES (in µs)		
MODE	**t_0**	**t_{1M}**	**t_{1C}**
27kHz	0	57	201
14kHz	0	86	230
7kHz	0	144	405
3kHz	0	240	501
2kHz	0	493	754
26Hz	0	29,817	33,568

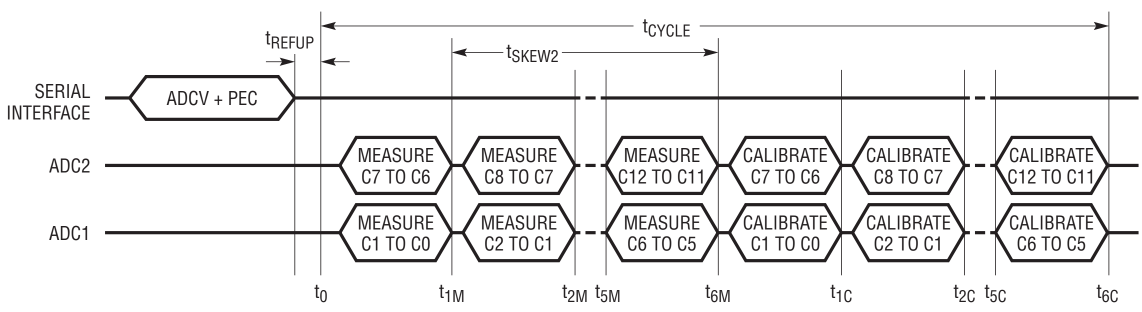


Figure 3. Timing for ADCV Command Measuring All 12 Cells

Table 5. Conversion Times for ADCV Command Measuring All 12 Cells in Different Modes

	CONVERSION TIMES (in µs)								
MODE	**t_0**	**t_{1M}**	**t_{2M}**	**t_{5M}**	**t_{6M}**	**t_{1C}**	**t_{2C}**	**t_{5C}**	**t_{6C}**
27kHz	0	57	103	243	290	432	568	975	1,113
14kHz	0	86	162	389	465	606	742	1,149	1,288
7kHz	0	144	278	680	814	1,072	1,324	2,080	2,335
3kHz	0	260	511	1,262	1,512	1,770	2,022	2,778	3,033
2kHz	0	493	976	2,425	2,908	3,166	3,418	4,175	4,430
26Hz	0	29,817	59,623	149,043	178,850	182,599	186,342	197,571	201,317

OPERATION

Under/Overvoltage Monitoring

Whenever the C inputs are measured, the results are compared to undervoltage and overvoltage thresholds stored in memory. If the reading of a cell is above the overvoltage limit, a bit in memory is set as a flag. Similarly, measurement results below the undervoltage limit cause a flag to be set. The overvoltage and undervoltage thresholds are stored in the configuration register group. The flags are stored in the status register group B.

Auxiliary (GPIO) Measurements (ADAX Command)

The ADAX command initiates the measurement of the GPIO inputs. This command has options to select which GPIO input to measure (GPIO1-5) and which ADC mode. The ADAX command also measures the 2nd reference. There are options in the ADAX command to measure each GPIO and the 2nd reference separately or to measure all 5 GPIOs and the 2nd reference in a single command. See the section on commands for the ADAX command format. All auxiliary measurements are relative to the V^- pin voltage. This command can be used to read external temperature by connecting the temperature sensors to the GPIOs. These sensors can be powered from the 2nd reference which is also measured by the ADAX command, resulting in precise ratiometric measurements.

Figure 5 illustrates the timing of the ADAX command measuring all GPIOs and the 2nd reference. Since all the 6 measurements are carried out on ADC1 alone, the conversion time for the ADAX command is similar to the ADCV command.

Measuring Cell Voltages and GPIOs (ADCVAX Command)

The ADCVAX command combines twelve cell measurements with two GPIO measurements (GPIO1 and GPIO2). This command simplifies the synchronization of battery cell voltage and current measurements when current sensors are connected to GPIO1 or GPIO2 inputs. Figure 6 illustrates the timing of the ADCVAX command. See the section on commands for the ADCVAX command format. The synchronization of the current and voltage measurements, t_{SKEW1}, in FAST MODE is within 208µs.

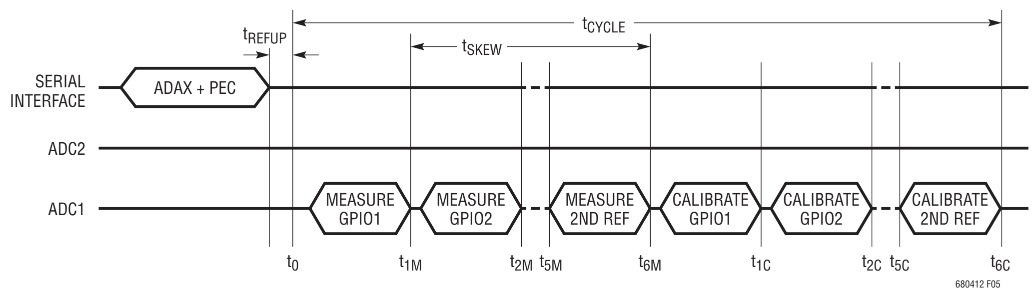


Figure 5. Timing for ADAX Command Measuring All GPIOs and 2nd Reference

Table 7. Conversion Times for ADAX Command Measuring All GPIOs and 2nd Reference in Different Modes

	CONVERSION TIMES (in µs)								
MODE	t_0	t_{1M}	t_{2M}	t_{5M}	t_{6M}	t_{1C}	t_{2C}	t_{5C}	t_{6C}
27kHz	0	57	103	243	290	432	568	975	1,113
14kHz	0	86	162	389	465	606	742	1,149	1,288
7kHz	0	144	278	680	814	1,072	1,324	2,080	2,335
3kHz	0	260	511	1,262	1,512	1,770	2,022	2,778	3,033
2kHz	0	493	976	2,425	2,908	3,166	3,418	4,175	4,430
26Hz	0	29,817	59,623	149,043	178,850	182,599	186,342	197,571	201,317

OPERATION

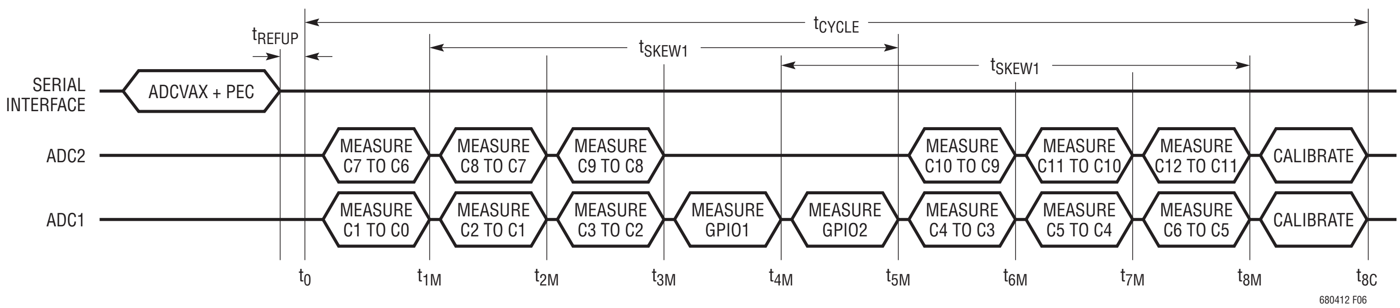


Figure 6. Timing of ADCVAX Command

Table 8. Conversion and Synchronization Times for ADCVAX Command in Different Modes

	CONVERSION TIMES (in µs)										SYNCHRONIZATION TIME (µs)
MODE	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{5M}	t_{6M}	t_{7M}	t_{8M}	t_{8C}	t_{SKEW1}
27kHz	0	57	106	155	216	265	326	375	424	1,564	208
14kHz	0	86	161	237	320	396	479	555	630	1,736	310
7kHz	0	144	278	412	553	687	828	962	1,096	3,133	543
3kHz	0	260	511	761	1,018	1,269	1,526	1,777	2,027	4,064	1009
2kHz	0	493	976	1,459	1,949	2,432	2,923	3,406	3,888	5,925	1939
26Hz	0	29,817	59,623	89,430	119,244	149,051	178,864	208,671	238,478	268,442	119234

Table 8 shows the conversion and synchronization time for the ADCVAX command in different modes. The total conversion time for the command is given by t_{8C}.

DATA ACQUISITION SYSTEM DIAGNOSTICS

The battery monitoring data acquisition system is comprised of the multiplexers, ADCs, 1st reference, digital filters, and memory. To ensure long term reliable performance there are several diagnostic commands which can be used to verify the proper operation of these circuits.

Measuring Internal Device Parameters (ADSTAT Command)

The ADSTAT command is a diagnostic command that measures the following internal device parameters: sum of all cells (SOC), internal die temperature (ITMP), analog power supply (VA) and the digital power supply (VD). These parameters are described in the section below. All 6 ADC modes are available for these conversions. See the section on commands for the ADSTAT command format. Figure 7 illustrates the timing of the ADSTAT command measuring all 4 internal device parameters.

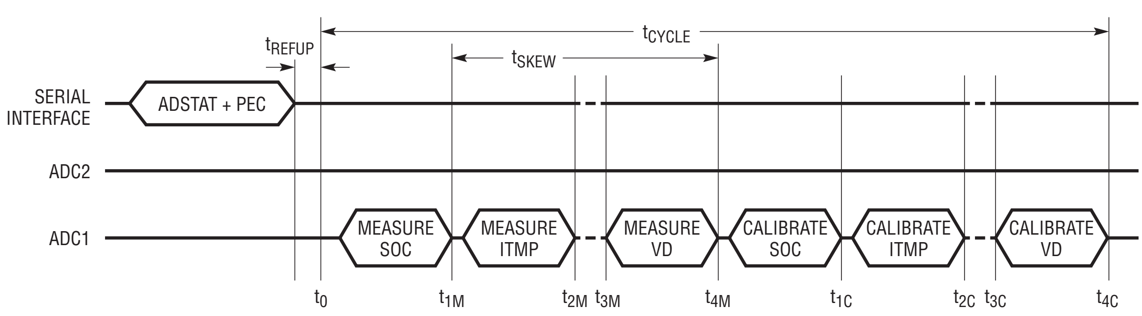


Figure 7. Timing for ADSTAT Command Measuring SOC, ITMP, VA, VD

OPERATION

Table 9 shows the conversion time of the ADSTAT command measuring all 4 internal parameters. t_{4C} indicates the total conversion time for the ADSTAT command.

Sum of Cells Measurement: The sum of all cells measurement is the voltage between C12 and C0 with a 20:1 attenuation. The 16-bit ADC value of sum of cells measurement (SOC) is stored in status register group A. From the SOC value, the sum of all cell voltage measurements is given by:

Sum of all Cells = SOC • 20 • 100µV

Internal Die Temperature: The ADSTAT command can measure the internal die temperature. The 16-bit ADC value of the die temperature measurement (ITMP) is stored in status register group A. From ITMP the actual die temperature is calculated using the expression:

Internal Die Temperature (°C) = (ITMP) • 100µV/(7.5mV)°C – 273°C

Power Supply Measurements: The ADSTAT command is also used to measure the analog power supply (V_{REG}) and digital power supply (V_{REGD}).

The 16-bit ADC value of the analog power supply measurement (VA) is stored in Status Register Group A. The 16-bit ADC value of the digital power supply measurement (VD) is stored in status register group B. From VA and VD, the power supply measurements are given by:

Analog power supply measurement (V_{REG}) = V_A • 100µV

Digital power supply measurement (V_{REGD}) = V_D • 100µV

The nominal range of V_{REG} is 4.5V to 5.5V. The nominal range of V_{REGD} is 2.7V to 3.6V.

Accuracy Check

Measuring an independent voltage reference is the best means to verify the accuracy of a data acquisition system. The LTC6804 contains a 2nd reference for this purpose. The ADAX command will initiate the measurement of the 2nd reference. The results are placed in auxiliary register group B. The range of the result depends on the ADC measurement accuracy and the accuracy of the 2nd reference, including thermal hysteresis and long term drift. Readings outside the range 2.980 to 3.020 indicate the system is out of its specified tolerance.

MUX Decoder Check

The diagnostic command DIAGN ensures the proper operation of each multiplexer channel. The command cycles through all channels and sets the MUXFAIL bit to 1 in status register group B if any channel decoder fails. The MUXFAIL bit is set to 0 if the channel decoder passes the test. The MUXFAIL bit is also set to 1 on power-up (POR) or after a CLRSTAT command.

The DIAGN command takes about 400µs to complete if the core is in REFUP state and about 4.5ms to complete if the core is in STANDBY state. The polling methods described in the section Polling Methods can be used to determine the completion of the DIAGN command.

Digital Filter Check

The delta-sigma ADC is composed of a 1-bit pulse density modulator followed by a digital filter. A pulse density modulated bit stream has a higher percentage of 1s for higher analog input voltages. The digital filter converts this high frequency 1-bit stream into a single 16-bit word.

Table 9. Conversion Times for ADSTAT Command Measuring SOC, ITMP, VA, VD

	CONVERSION TIMES (in µs)								
MODE	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{1C}	t_{2C}	t_{3C}	t_{4C}
27kHz	0	57	103	150	197	338	474	610	748
14kHz	0	86	162	237	313	455	591	726	865
7kHz	0	144	278	412	546	804	1,056	1,308	1,563
3kHz	0	260	511	761	1,011	1,269	1,522	1,774	2,028
2kHz	0	493	976	1,459	1,942	2,200	2,452	2,705	2,959
26Hz	0	29,817	59,623	89,430	119,237	122,986	126,729	130,472	134,218

OPERATION

This is why a delta-sigma ADC is often referred to as an oversampling converter.

The self test commands verify the operation of the digital filters and memory. Figure 8 illustrates the operation of the ADC during self test. The output of the 1-bit pulse density modulator is replaced by a 1-bit test signal. The test signal passes through the digital filter and is converted to a 16-bit value. The 1-bit test signal undergoes the same digital conversion as the regular 1-bit pulse from the modulator, so the conversion time for any self test command is exactly the same as the corresponding regular ADC conversion command. The 16-bit ADC value is stored in the same register groups as the regular ADC conversion command. The test signals are designed to place alternating one-zero patterns in the registers. Table 10 provides a list of the self test commands. If the digital filters and memory are working properly, then the registers will contain the values shown in Table 10. For more details see the section Commands.

ADC Clear Commands

LTC6804 has 3 clear commands – CLRCELL, CLRAUX and CLRSTAT. These commands clear the registers that store all ADC conversion results.

The CLRCELL command clears cell voltage register group A, B, C and D. All bytes in these registers are set to 0xFF by CLRCELL command.

The CLRAUX command clears auxiliary register group A and B. All bytes in these registers are set to 0xFF by CLRAUX command.

The CLRSTAT command clears status register group A and B except the REVCODE in status register group B. A read back of REVCODE will return the revision code of the part. RSVD bits always read back 0s. All OV flags, UV flags, MUXFAIL bit, RSVD bits and THSD bit in status register group B are set to 1 by CLRSTAT command. The THSD bit is set to 0 after RDSTATB command. The registers storing SOC, ITMP, VA and VD are all set to 0xFF by CLRSTAT command.

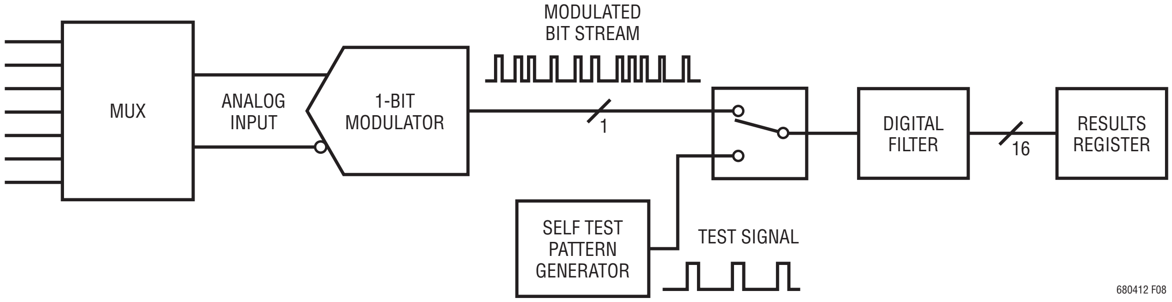


Figure 8. Operation of LTC6804 ADC Self Test

Table 10. Self Test Command Summary

COMMAND	SELF TEST OPTION	OUTPUT PATTERN IN DIFFERENT ADC MODES						RESULTS REGISTER GROUPS
		27kHz	14kHz	7kHz	3kHz	2kHz	26Hz	
CVST	ST[1:0]=01	0x9565	0x9553	0x9555	0x9555	0x9555	0x9555	C1V to C12V (CVA, CVB, CVC, CVD)
	ST[1:0]=10	0x6A9A	0x6AAC	0x6AAA	0x6AAA	0x6AAA	0x6AAA	
AXST	ST[1:0]=01	0x9565	0x9553	0x9555	0x9555	0x9555	0x9555	G1V to G5V, REF (AUXA, AUXB)
	ST[1:0]=10	0x6A9A	0x6AAC	0x6AAA	0x6AAA	0x6AAA	0x6AAA	
STATST	ST[1:0]=01	0x9565	0x9553	0x9555	0x9555	0x9555	0x9555	SOC, ITMP, VA, VD (STATA, STATB)
	ST[1:0]=10	0x6A9A	0x6AAC	0x6AAA	0x6AAA	0x6AAA	0x6AAA	

OPERATION

Open-Wire Check (ADOW Command)

The ADOW command is used to check for any open wires between the ADCs in the LTC6804 and the external cells. This command performs ADC conversions on the C pin inputs identically to the ADCV command, except two internal current sources sink or source current into the two C pins while they are being measured. The pull-up (PUP) bit of the ADOW command determines whether the current sources are sinking or sourcing 100µA.

The following simple algorithm can be used to check for an open wire on any of the 13 C pins (see Figure 9):

1) Run the 12-cell command ADOW with PUP = 1 at least twice. Read the cell voltages for cells 1 through 12 once at the end and store them in array $CELL_{PU(n)}$.

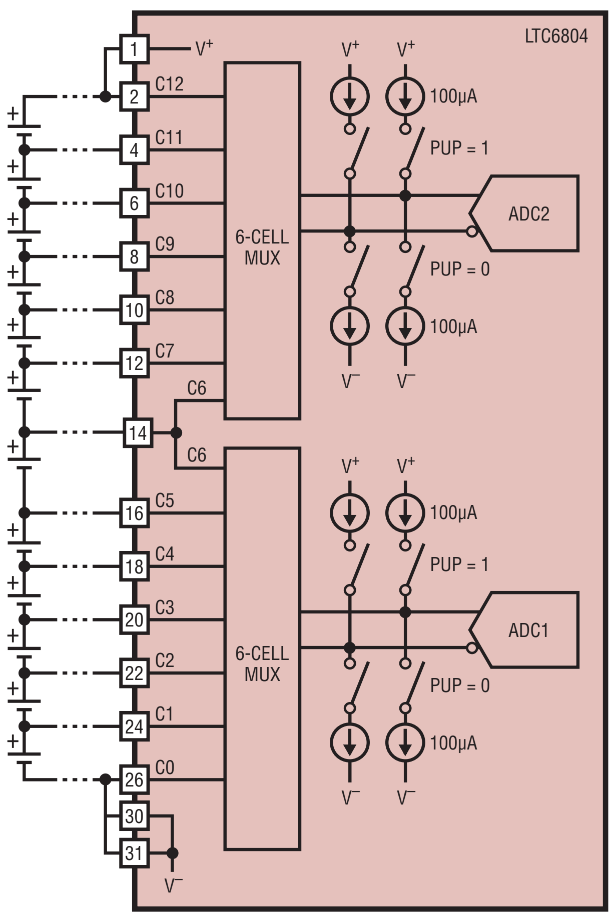


Figure 9. Open-Wire Detection Circuitry

2) Run the 12-cell command ADOW with PUP = 0 at least twice. Read the cell voltages for cells 1 through 12 once at the end and store them in array $CELL_{PD(n)}$.

3) Take the difference between the pull-up and pull-down measurements made in above steps for cells 2-12: $CELL_{\Delta(n)} = CELL_{PU(n)} – CELL_{PD(n)}$.

4) For all values of n from 1 to 11: If $CELL_{\Delta(n+1)} < –400mV$, then C(n) is open. If the $CELL_{PU(1)} = 0.0000$, then C(0) is open. If the $CELL_{PD(12)} = 0.0000$, then C(12) is open.

The above algorithm detects open wires using normal mode conversions with as much as 10nF of capacitance remaining on the LTC6804 side of the open wire. However, if more external capacitance is on the open C pin, then the length of time that the open wire conversions are ran in steps 1 and 2 must be increased to give the 100µA current sources time to create a large enough difference for the algorithm to detect an open connection. This can be accomplished by running more than two ADOW commands in steps 1 and 2, or by using filtered mode conversions instead of normal mode conversions. Use Table 11 to determine how many conversions are necessary:

Table 11

	Number of ADOW Commands Required in Steps 1 and 2	
EXTERNAL C PIN CAPACITANCE	**NORMAL MODE**	**FILTERED MODE**
≤10nF	2	2
100nF	10	2
1µF	100	2
C	1+ROUNDUP(C/10nF)	2

Thermal Shutdown

To protect the LTC6804 from overheating, there is a thermal shutdown circuit included inside the IC. If the temperature detected on the die goes above approximately 150°C, the thermal shutdown circuit trips and resets the configuration register group to its default state. This turns off all discharge switches. When a thermal shutdown event has occurred, the THSD bit in status register group B will go high. This bit is cleared after a read operation has been performed on the status register group B (RDSTATB command). The CLRSTAT command sets the THSD bit

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high for diagnostic purposes, but does not reset the configuration register group.

Revision Code

The status register group B contains a 4-bit revision code. If software detection of device revision is necessary, then contact the factory for details. Otherwise, the code can be ignored. In all cases, however, the values of all bits must be used when calculating the packet error code (PEC) on data reads.

WATCHDOG AND SOFTWARE DISCHARGE TIMER

When there is no valid command for more than 2 seconds, the watchdog timer expires. This resets configuration register bytes CFGR0-CFGR3 in all cases. CFGR4 and CFGR5 are reset by the watchdog timer when the software timer is disabled. The WDT pin is pulled high by the external pull-up when the watchdog time elapses. The watchdog timer is always enabled and it resets after every valid command.

The software discharge timer is used to keep the discharge switches turned ON for programmable time duration. If the software timer is being used, the discharge switches are not turned OFF when the watchdog timer is activated.

To enable the software timer, SWTEN pin needs to be tied high to V_{REG} (Figure 10). The discharge switches can now be kept ON for the programmed time duration that is determined by the DCTO value written to the configuration register. Table 12 shows the various time settings and the corresponding DCTO value. Table 13 summarizes the status of the configuration register group after a watchdog timer or software timer event.

Table 13

	WATCHDOG TIMER	SOFTWARE TIMER
SWTEN = 0, DCTO = XXXX	Resets CFGR0-5 When It Activates	Disabled
SWTEN = 1, DCTO = 0000	Resets CFGR0-5 When It Activates	Disabled
SWTEN = 1, DCTO ! = 0000	Resets CFGR0-3 When It Activates	Resets CFGR4-5 When It Fires

Unlike the watchdog timer, the software timer does not reset when there is a valid command. The software timer can only be reset after a valid WRCFG (write configuration register) command. There is a possibility that the software timer will expire in the middle of some commands.

If software timer activates in the middle of WRCFG command, the configuration register resets as per Table 14.

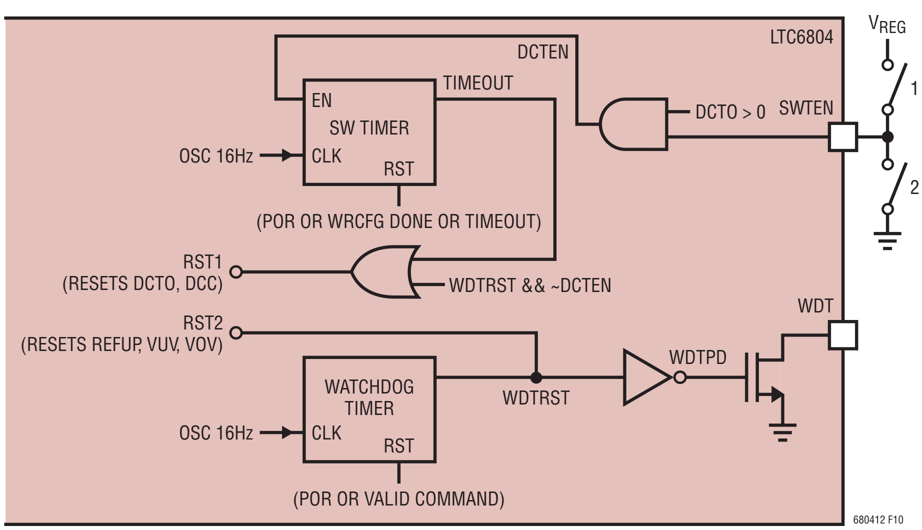

Figure 10. Watchdog and Software Discharge Timer

Table 12. DCTO Settings

DCTO	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Time Min	Disabled	0.5	1	2	3	4	5	10	15	20	30	40	60	75	90	120

OPERATION

However, at the end of the valid WRCFG command, the new data is copied to the configuration register. The new data is not lost when the software timer is activated.

If software timer activates in the middle of RDCFG command, the configuration register group resets as per Table 14. As a result, the read back data from bytes CRFG4 and CRFG5 could be corrupted.

I²C/SPI MASTER ON LTC6804 USING GPIOS

The I/O ports GPIO3, GPIO4 and GPIO5 on LTC6804-1 and LTC6804-2 can be used as an I²C or SPI master port to communicate to an I²C or SPI slave. In the case of an I²C master, GPIO4 and GPIO5 form the SDA and SCL ports of the I²C interface respectively. In the case of a SPI master, GPIO3, GPIO5 and GPIO4 become the chip select (CSBM), clock (SCKM) and data (SDIOM) ports of the SPI interface respectively.

The GPIOs are open drain outputs, so an external pull-up is required on these ports to operate as an I²C or SPI master. It is also important to write the GPIO bits to 1 in the CFG register group so these ports are not pulled low internally by the device.

Table 14

DCTO (READ VALUE)	TIME LEFT (MIN)
0	Disabled (or) Timer Has Timed Out
1	0 < Timer ≤ 0.5
2	0.5 < Timer ≤ 1
3	1 < Timer ≤ 2
4	2 < Timer ≤ 3
5	3 < Timer ≤ 4
6	4 < Timer ≤ 5
7	5 < Timer ≤ 10
8	10 < Timer ≤ 15
9	15 < Timer ≤ 20
A	20 < Timer ≤ 30
B	30 < Timer ≤ 40
C	40 < Timer ≤ 60
D	60 < Timer ≤ 75
E	75 < Timer ≤ 90
F	90 < Timer ≤ 120

COMM Register

LTC6804 has a 6-byte COMM register as shown in Table 15. This register stores all data and control bits required for I²C or SPI communication to a slave. The COMM register contains 3 bytes of data Dn[7:0] to be transmitted to or received from the slave device. ICOMn [3:0] specify control actions before transmitting/receiving the data byte. FCOMn [3:0] specify control actions after transmitting/receiving the data byte.

If the bit ICOMn[3] in the COMM register is set to 1 the part becomes an I²C master and if the bit is set to 0 the part becomes a SPI master.

Table 16 describes the valid write codes for ICOMn[3:0] and FCOMn[3:0] and their behavior when using the part as an I²C master.

Table 17 describes the valid codes for ICOMn[3:0] and FCOMn[3:0] and their behavior when using the part as a SPI master.

Note that only the codes listed in Tables 16 and 17 are valid for ICOMn[3:0] and FCOMn[3:0]. Writing any other code that is not listed in Tables 16 and 17 to ICOMn[3:0] and FCOMn[3:0] may result in unexpected behavior on the I²C and SPI ports.

Table 15. COMM Register Memory Map

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMM0	RD/WR	ICOM0[3]	ICOM0[2]	ICOM0[1]	ICOM0[0]	D0[7]	D0[6]	D0[5]	D0[4]
COMM1	RD/WR	D0[3]	D0[2]	D0[1]	D0[0]	FCOM0[3]	FCOM0[2]	FCOM0[1]	FCOM0[0]
COMM2	RD/WR	ICOM1[3]	ICOM1[2]	ICOM1[1]	ICOM1[0]	D1[7]	D1[6]	D1[5]	D1[4]
COMM3	RD/WR	D1[3]	D1[2]	D1[1]	D1[0]	FCOM1[3]	FCOM1[2]	FCOM1[1]	FCOM1[0]
COMM4	RD/WR	ICOM2[3]	ICOM2[2]	ICOM2[1]	ICOM2[0]	D2[7]	D2[6]	D2[5]	D2[4]
COMM5	RD/WR	D2[3]	D2[2]	D2[1]	D2[0]	FCOM2[3]	FCOM2[2]	FCOM2[1]	FCOM2[0]

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Table 16. Write Codes for ICOMn[3:0] and FCOMn[3:0] on I²C Master

CONTROL BITS	CODE	ACTION	DESCRIPTION
ICOMn[3:0]	0110	START	Generate a START Signal on I²C Port Followed By Data Transmission
	0001	STOP	Generate a STOP Signal on I²C port
	0000	BLANK	Proceed Directly to Data Transmission on I²C Port
	0111	No Transmit	Release SDA and SCL and Ignore the Rest of the Data
FCOMn[3:0]	0000	Master ACK	Master Generates an ACK Signal on Ninth Clock Cycle
	1000	Master NACK	Master Generates a NACK Signal on Ninth Clock Cycle
	1001	Master NACK + STOP	Master Generates a NACK Signal Followed by STOP Signal

Table 17. Write Codes for ICOMn[3:0] and FCOMn[3:0] on SPI Master

CONTROL BITS	CODE	ACTION	DESCRIPTION
ICOMn[3:0]	1000	CSBM low	Generates a CSBM Low Signal on SPI Port (GPIO3)
	1001	CSBM high	Generates a CSBM High Signal on SPI Port (GPIO3)
	1111	No Transmit	Releases the SPI Port and Ignores the Rest of the Data
FCOMn[3:0]	X000	CSBM low	Holds CSBM Low at the End of Byte Transmission
	1001	CSBM high	Transitions CSBM High at the End of Byte Transmission

COMM Commands

Three commands help accomplish I²C or SPI communication to the slave device: WRCOMM, STCOMM, RDCOMM

WRCOMM Command: This command is used to write data to the COMM register. This command writes 6 bytes of data to the COMM register. The PEC needs to be written at the end of the data. If the PEC does not match, all data in the COMM register is cleared to 1's when CSB goes high. See the section Bus Protocols for more details on a write command format.

STCOMM Command: This command initiates I²C/SPI communication on the GPIO ports. The COMM register contains 3 bytes of data to be transmitted to the slave. During this command, the data bytes stored in the COMM register are transmitted to the slave I²C or SPI device and the data received from the I²C or SPI device is stored in the COMM register. This command uses GPIO4 (SDA) and GPIO5 (SCL) for I²C communication or GPIO3 (CSBM), GPIO4 (SDIOM) and GPIO5 (SCKM) for SPI communication.

The STCOMM command is to be followed by 24 clock cycles for each byte of data to be transmitted to the slave device while holding CSB low. For example, to transmit 3 bytes of data to the slave, send STCOMM command and its PEC followed by 72 clock cycles. Pull CSB high at the end of the 72 clock cycles of STCOMM command.

During I²C or SPI communication, the data received from the slave device is updated in the COMM register.

RDCOMM Command: The data received from the slave device can be read back from the COMM register using the RDCOMM command. The command reads back 6 bytes of data followed by the PEC. See the section Bus Protocols for more details on a read command format.

Table 18 describes the possible read back codes for ICOMn[3:0] and FCOMn[3:0] when using the part as an I²C master. Dn[3:0] contains the data byte either transmitted by the I²C master or received from the I²C slave.

In case of the SPI master, the read back codes for ICOMn[3:0] and FCOMn[3:0] are always 0111 and 1111 respectively. Dn[3:0] contains the data byte either transmitted by the SPI master or received from the SPI slave.

Figure 11 illustrates the operation of LTC6804 as an I²C or SPI master using the GPIOs.

Any number of bytes can be transmitted to the slave in groups of 3 bytes using these commands. The GPIO ports will not get reset between different STCOMM commands. However, if the wait time between the commands is greater than 2 seconds, the watchdog will timeout and reset the ports to their default values.

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Table 18. Read Codes for ICOMn[3:0] and FCOMn[3:0] on I^2C Master

CONTROL BITS	CODE	DESCRIPTION
ICOMn[3:0]	0110	Master Generated a START Signal
	0001	Master Generated a STOP Signal
	0000	Blank, SDA Was Held Low Between Bytes
	0111	Blank, SDA Was Held High Between Bytes
FCOMn[3:0]	0000	Master Generated an ACK Signal
	0111	Slave Generated an ACK Signal
	1111	Slave Generated a NACK Signal
	0001	Slave Generated an ACK Signal, Master Generated a STOP Signal
	1001	Slave Generated a NACK Signal, Master Generated a STOP Signal

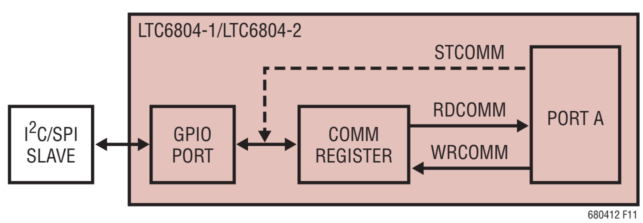

Figure 11. LTC6804 I^2C/SPI Master Using GPIOs

To transmit several bytes of data using an I^2C master, a START signal is only required at the beginning of the entire data stream. A STOP signal is only required at the end of the data stream. All intermediate data groups can use a BLANK code before the data byte and an ACK/NACK signal as appropriate after the data byte. SDA and SCL will not get reset between different STCOMM commands.

To transmit several bytes of data using SPI master, a CSBM low signal is sent at the beginning of the 1st data byte. CSBM can be held low or taken high for intermediate data groups using the appropriate code on FCOMn[3:0]. A CSBM high signal is sent at the end of the last byte of data. CSBM, SDIOM and SCKM will not get reset between different STCOMM commands.

Figure 12 shows the 24 clock cycles following STCOMM command for an I^2C master in different cases. Note that if ICOMn[3:0] specified a STOP condition, after the STOP signal is sent, the SDA and SCL lines are held high and all data in the rest of the word is ignored. If ICOMn[3:0] is a NO TRANSMIT, both SDA and SCL lines are released, and rest of the data in the word is ignored. This is used when a particular device in the stack does not have to communicate to a slave.

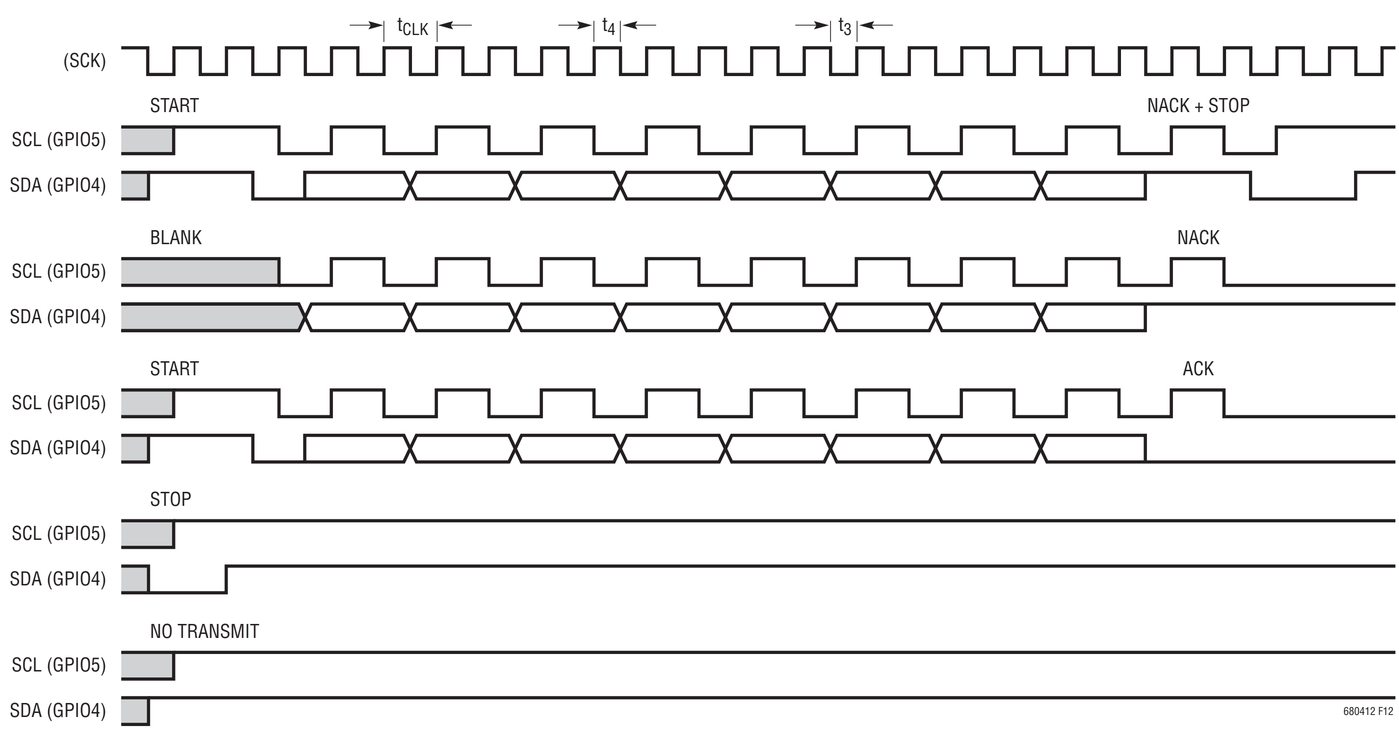

Figure 12. STCOMM Timing Diagram for an I^2C Master

OPERATION

Figure 13 shows the 24 clock cycles following STCOMM command for a SPI master. Similar to the I^{2}C master, if ICOMn[3:0] specified a CSBM HIGH or a NO TRANSMIT condition, the CSBM, SCKM and SDIOM lines of the SPI master are released and the rest of the data in the word is ignored.

Timing Specifications of I^{2}C and SPI master

The timing of the LTC6804 I^{2}C or SPI master will be controlled by the timing of the communication at the LTC6804's primary SPI interface. Table 19 shows the I^{2}C master timing relationship to the primary SPI clock. Table 20 shows the SPI master timing specifications.

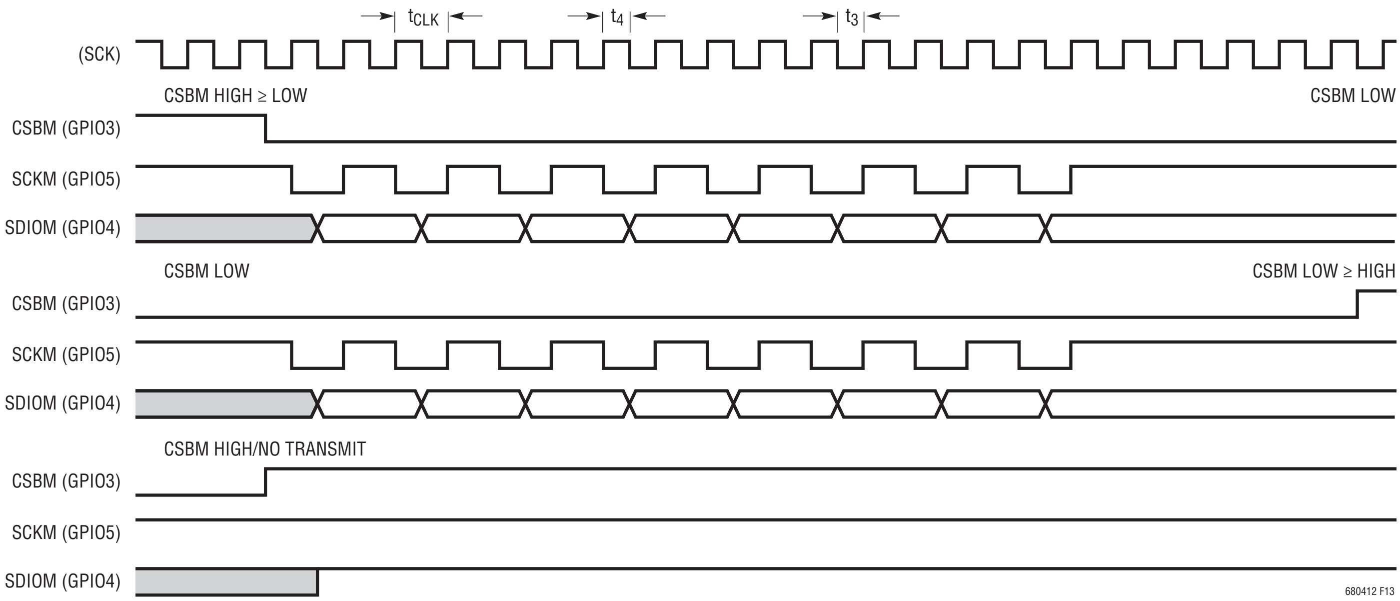

Figure 13. STCOMM Timing Diagram for a SPI Master

Table 19. I^{2}C Master Timing

I^{2}C MASTER PARAMETER	TIMING RELATIONSHIP TO PRIMARY SPI INTERFACE	TIMING SPECIFICATIONS AT t_{CLK} = 1µs
SCL Clock Frequency	$1/(2 \bullet t_{CLK})$	Max 500kHz
t_{HD}; STA	t_3	Min 200ns
t_{LOW}	t_{CLK}	Min 1µs
t_{HIGH}	t_{CLK}	Min 1µs
t_{SU}; STA	$t_{CLK} + t_4$*	Min 1.03µs
t_{HD}; DAT	t_4*	Min 30ns
t_{SU}; DAT	t_3	Min 1µs
t_{SU}; STO	$t_{CLK} + t_4$*	Min 1.03µs
t_{BUF}	$3 \bullet t_{CLK}$	Min 3µs

*Note: When using isoSPI, t_4 is generated internally and is a minimum of 30ns. Also, $t_3 = t_{CLK} – t_4$. When using SPI, t_3 and t_4 are the low and high times of the SCK input, each with a specified minimum of 200ns.

Table 20. SPI Master Timing

SPI MASTER PARAMETER	TIMING RELATIONSHIP TO PRIMARY SPI INTERFACE	TIMING SPECIFICATIONS AT t_{CLK} = 1µs
SDIOM Valid to SCKM Rising Setup	t_3	Min 200ns
SDIOM Valid from SCKM Rising Hold	$t_{CLK} + t_4$*	Min 1.03µs
SCKM Low	t_{CLK}	Min 1µs
SCKM High	t_{CLK}	Min 1µs
SCKM Period (SCKM_Low + SCKM_High)	$2 \bullet t_{CLK}$	Min 2µs
CSBM Pulse Width	$3 \bullet t_{CLK}$	Min 3µs
SCKM Rising to CSBM Rising	$5 \bullet t_{CLK} + t_4$*	Min 5.03µs
CSBM Falling to SCKM Falling	t_3	Min 200ns
CSBM Falling to SCKM Rising	$t_{CLK} + t_3$	Min 1.2µs
SCKM Falling to SDIOM Valid	Master requires < t_{CLK}	

*Note: When using isoSPI, t_4 is generated internally and is a minimum of 30ns. Also, $t_3 = t_{CLK} – t_4$. When using SPI, t_3 and t_4 are the low and high times of the SCK input, each with a specified minimum of 200ns.

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SERIAL INTERFACE OVERVIEW

There are two types of serial ports on the LTC6804, a standard 4-wire serial peripheral interface (SPI) and a 2-wire isolated interface (isoSPI). Pins 41 through 44 are configurable as 2-wire or 4-wire serial port, based on the state of the ISOMD pin.

There are two versions of the LTC6804: the LTC6804-1 and the LTC6804-2. The LTC6804-1 is used in a daisy chain configuration, and the LTC6804-2 is used in an addressable bus configuration. The LTC6804-1 provides a second isoSPI interface using pins 45 through 48. The LTC6804-2 uses pins 45 through 48 to set the address of the device, by tying these pins to V^- or V_{REG}.

4-WIRE SERIAL PERIPHERAL INTERFACE (SPI) PHYSICAL LAYER

External Connections

Connecting ISOMD to V^- configures serial Port A for 4-wire SPI. The SDO pin is an open drain output which requires a pull-up resistor tied to the appropriate supply voltage (Figure 14).

Timing

The 4-wire serial port is configured to operate in a SPI system using CPHA = 1 and CPOL = 1. Consequently, data on SDI must be stable during the rising edge of SCK. The timing is depicted in Figure 15. The maximum data rate is 1Mbps.

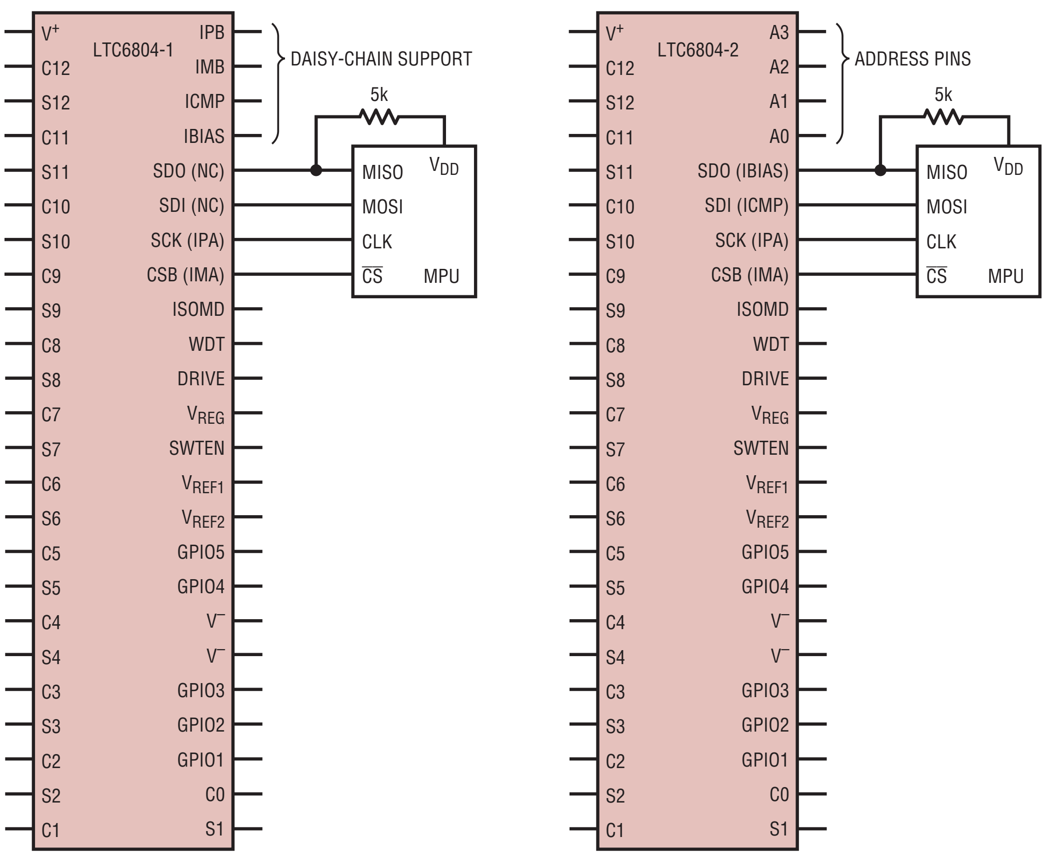

Figure 14. 4-Wire SPI Configuration

OPERATION

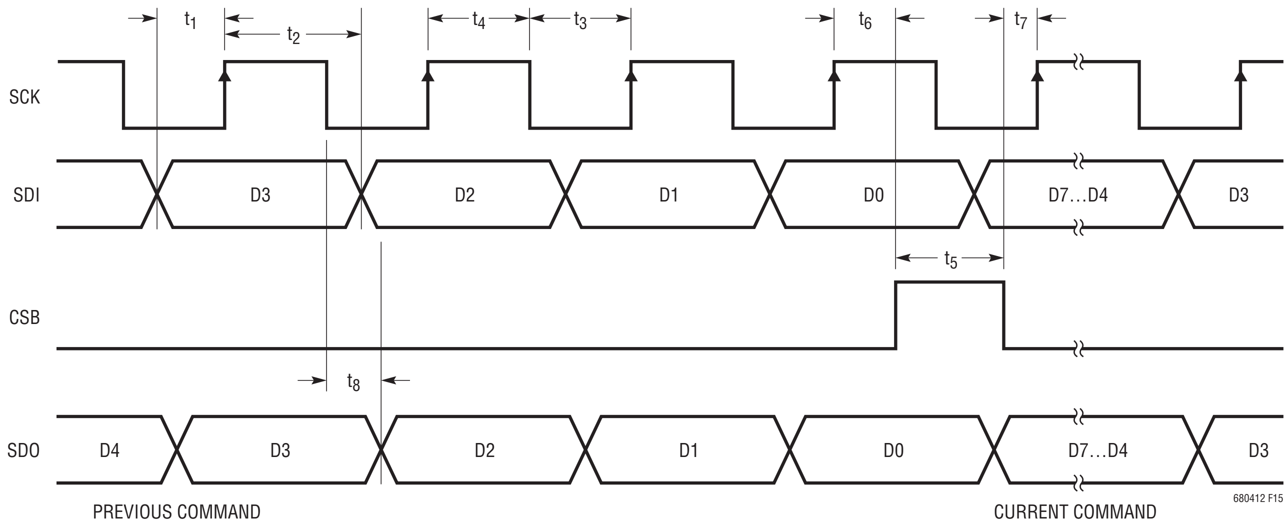

Figure 15. Timing Diagram of 4-Wire Serial Peripheral Interface

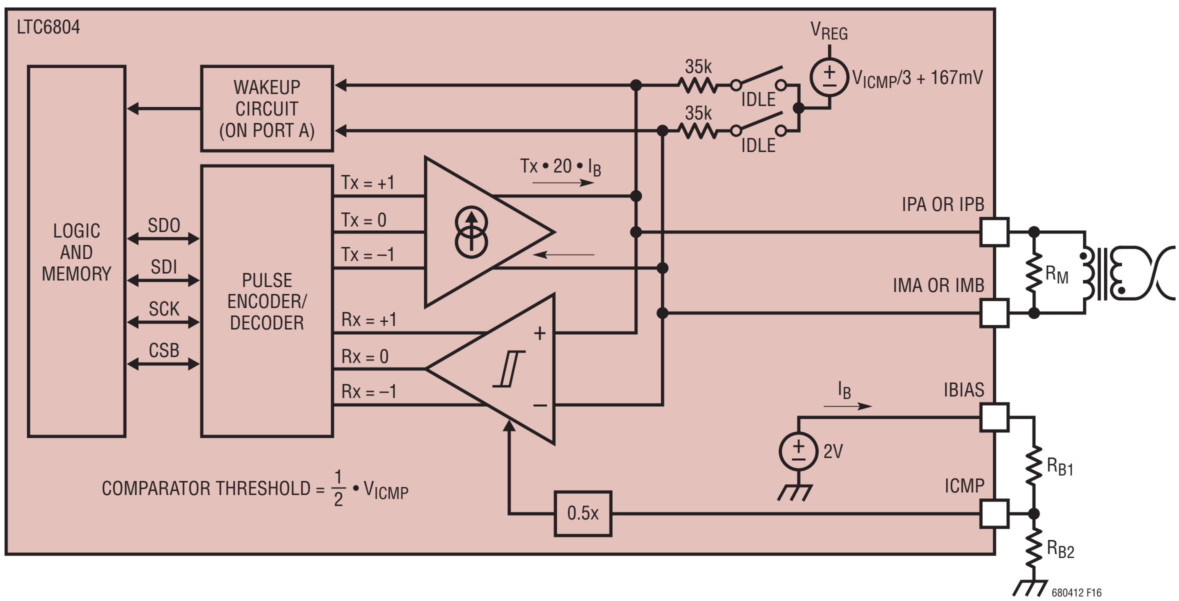

Figure 16. isoSPI Interface

2-WIRE ISOLATED INTERFACE (isoSPI) PHYSICAL LAYER

The 2-wire interface provides a means to interconnect LTC6804 devices using simple twisted pair cabling. The interface is designed for low packet error rates when the cabling is subjected to high RF fields. Isolation is achieved through an external transformer.

Standard SPI signals are encoded into differential pulses. The strength of the transmission pulse and the threshold level of the receiver are set by two external resistors. The values of the resistors allow the user to trade off power dissipation for noise immunity.

Figure 16 illustrates how the isoSPI circuit operates. A 2V reference drives the IBIAS pin. External resistors R_{B1} and R_{B2} create the reference current I_B. This current sets the drive strength of the transmitter. R_{B1} and R_{B2} also form a voltage divider of the 2V reference at the ICMP pin. This sets the threshold voltage of the receiver circuit.

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External Connections

The LTC6804-1 has 2 serial ports which are called Port B and Port A. Port B is always configured as a 2-wire interface (master). The final device in the daisy chain does not use this port, and it should be terminated into R_M. Port A is either a 2-wire or 4-wire interface (slave), depending on the connection of the ISOMD pin.

Figure 17 is an example of a robust interconnection of multiple identical PCBs, each containing one LTC6804-1. The microprocessor is located on a separate PCB. To achieve 2-wire isolation between the microprocessor PCB and the 1st LTC6804-1 PCB, use the LTC6820 support IC. The LTC6820 is functionally equivalent to the diagram in Figure 16.

The LTC6804-2 has a single serial port (Port A) which can be 2-wire or 4-wire, depending on the state of the ISOMD pin. When configured for 2-wire communications, several devices can be connected in a multi-drop configuration, as shown in Figure 18. The LTC6820 IC is used to interface the MPU (master) to the LTC6804-2's (slaves).

Selecting Bias Resistors

The adjustable signal amplitude allows the system to trade power consumption for communication robustness, and the adjustable comparator threshold allows the system to account for signal losses.

The isoSPI transmitter drive current and comparator voltage threshold are set by a resistor divider ($R_{BIAS} = R_{B1} + R_{B2}$) between the IBIAS and V^-. The divided voltage is connected to the ICMP pin which sets the comparator threshold to 1/2 of this voltage (V_{ICMP}). When either isoSPI interface is enabled (not IDLE) IBIAS is held at 2V, causing a current I_B to flow out of the IBIAS pin. The IP and IM pin drive currents are $20 \bullet I_B$.

As an example, if divider resistor R_{B1} is 2.8k and resistor R_{B2} is 1.21k (so that R_{BIAS} = 4k), then:

$$I_B = \frac{2V}{R_{B1} + R_{B2}} = 0.5mA$$

$$I_{DRV} = I_{IP} = I_{IM} = 20 \bullet I_B = 10mA$$

$$V_{ICMP} = 2V \bullet \frac{R_{B2}}{R_{B1} + R_{B2}} = I_B \bullet R_{B2} = 603mV$$

$$V_{TCMP} = 0.5 \bullet V_{ICMP} = 302mV$$

In this example, the pulse drive current I_{DRV} will be 10mA, and the receiver comparators will detect pulses with IP-IM amplitudes greater than ±302mV.

If the isolation barrier uses 1:1 transformers connected by a twisted pair and terminated with 120Ω resistors on each end, then the transmitted differential signal amplitude (±) will be:

$$V_A = I_{DRV} \bullet \frac{R_M}{2} = 0.6V$$

(This result ignores transformer and cable losses, which may reduce the amplitude).

isoSPI Pulse Detail

Two LTC6804 devices can communicate by transmitting and receiving differential pulses back and forth through an isolation barrier. The transmitter can output three voltage levels: $+V_A$, 0V, and $–V_A$. A positive output results from IP sourcing current and IM sinking current across load resistor R_M. A negative voltage is developed by IP sinking and IM sourcing. When both outputs are off, the load resistance forces the differential output to 0V.

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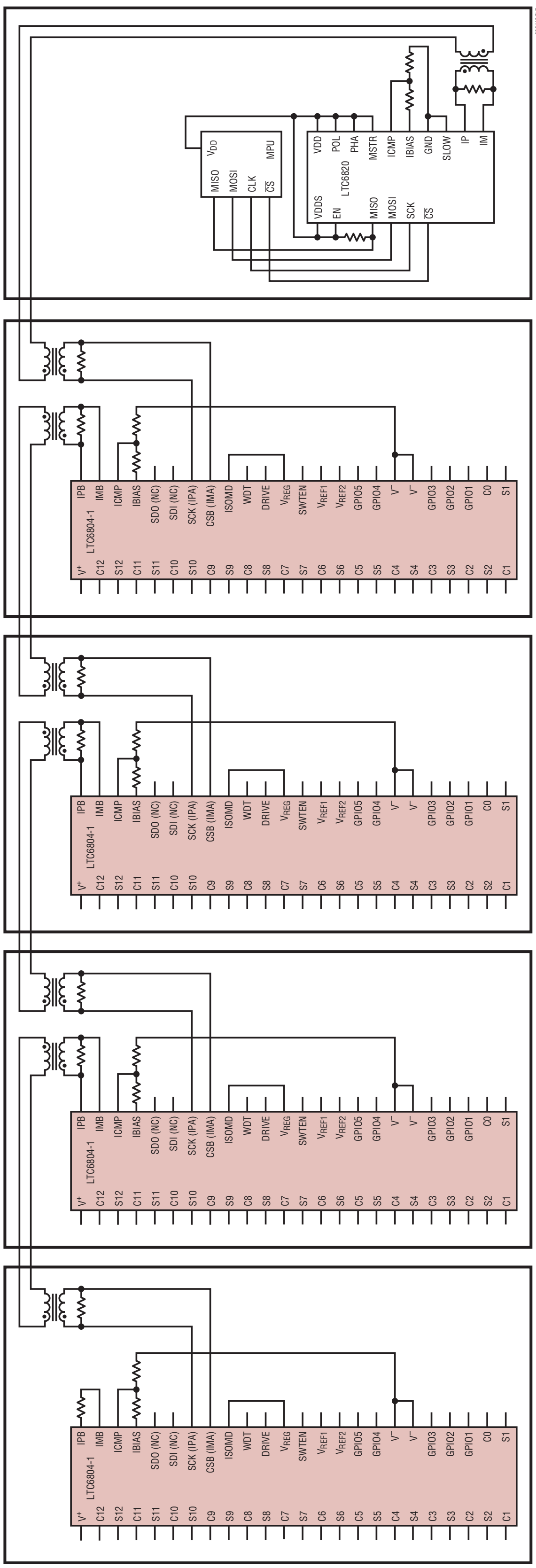

Figure 17. Transformer-Isolated Daisy-Chain Configuration Using LTC6804-1

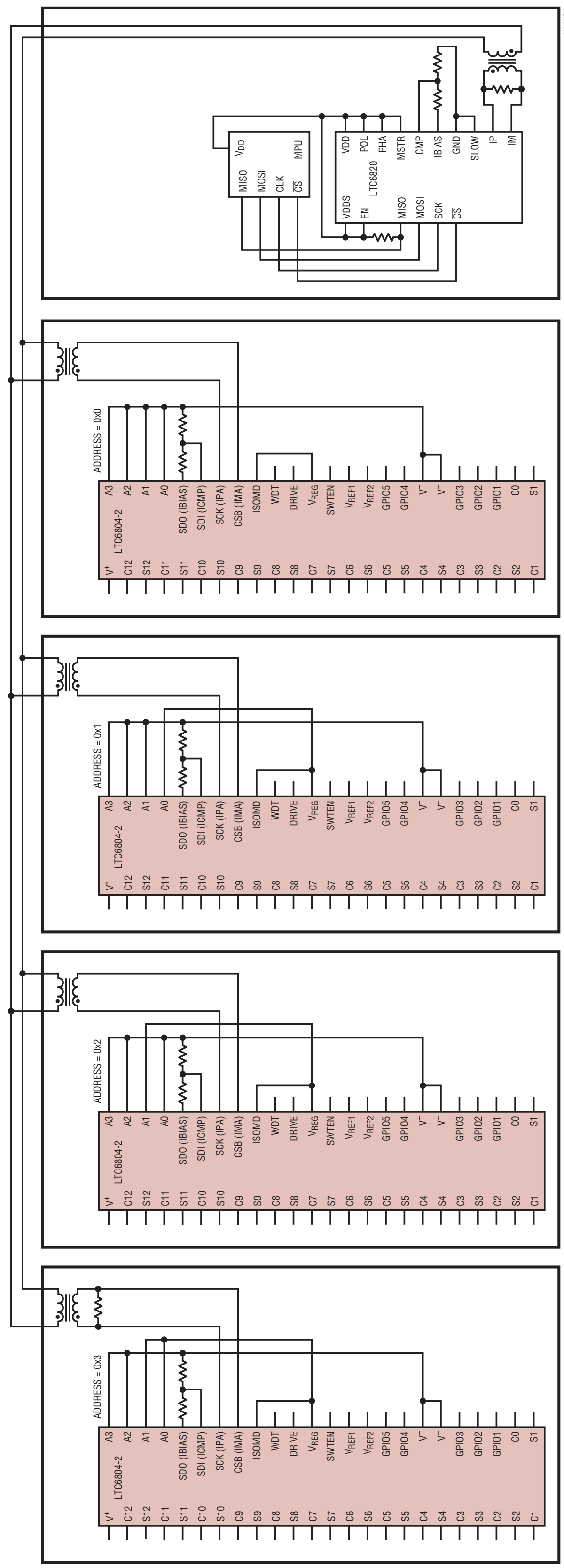

Figure 18. Multi-Drop Configuration Using LTC6804-2

OPERATION

To eliminate the DC signal component and enhance reliability, the isoSPI uses two different pulse lengths. This allows for four types of pulses to be transmitted, as shown in Table 21. A +1 pulse will be transmitted as a positive pulse followed by a negative pulse. A –1 pulse will be transmitted as a negative pulse followed by a positive pulse. The duration of each pulse is defined as $t_{1/2PW}$, since each is half of the required symmetric pair. (The total isoSPI pulse duration is 2 • $t_{1/2PW}$).

Table 21. isoSPI Pulse Types

PULSE TYPE	FIRST LEVEL ($t_{1/2PW}$)	SECOND LEVEL ($t_{1/2PW}$)	ENDING LEVEL
Long +1	$+V_A$ (150ns)	$–V_A$ (150ns)	0V
Long –1	$–V_A$ (150ns)	$+V_A$ (150ns)	0V
Short +1	$+V_A$ (50ns)	$–V_A$ (50ns)	0V
Short –1	$–V_A$ (50ns)	$+V_A$ (50ns)	0V

A host microcontroller does not have to generate isoSPI pulses to use this 2-wire interface. The first LTC6804 in the system can communicate to the microcontroller using the 4-wire SPI interface on its Port A, then daisy-chain to other LTC6804s using the 2-wire isoSPI interface on its Port B. Alternatively, an LTC6820 can be used to translate the SPI signals into isoSPI pulses.

LTC6804-1 Operation with Port A Configured for SPI

When the LTC6804-1 is operating with port A as an SPI (ISOMD = $V^–$), the SPI detects one of four communication events: CSB falling, CSB rising, SCK rising with SDI = 0, and SCK rising with SDI = 1. Each event is converted into one of the four pulse types for transmission through the LTC6804-1 daisy chain. Long pulses are used to transmit CSB changes and short pulses are used to transmit data, as explained in Table 22.

Table 22. LTC6804-1 Port B (Master) isoSPI Port Function

COMMUNICATION EVENT (PORT A SPI)	TRANSMITTED PULSE (PORT B isoSPI)
CSB Rising	Long +1
CSB Falling	Long –1
SCK Rising Edge, SDI = 1	Short +1
SCK Rising Edge, SDI = 0	Short –1

On the other side of the isolation barrier (i.e. at the other end of the cable), the 2nd LTC6804 will have ISOMD = V_{REG}. Its Port A operates as a slave isoSPI interface. It receives each transmitted pulse and reconstructs the SPI signals internally, as shown in Table 23. In addition, during a READ command this port may transmit return data pulses.

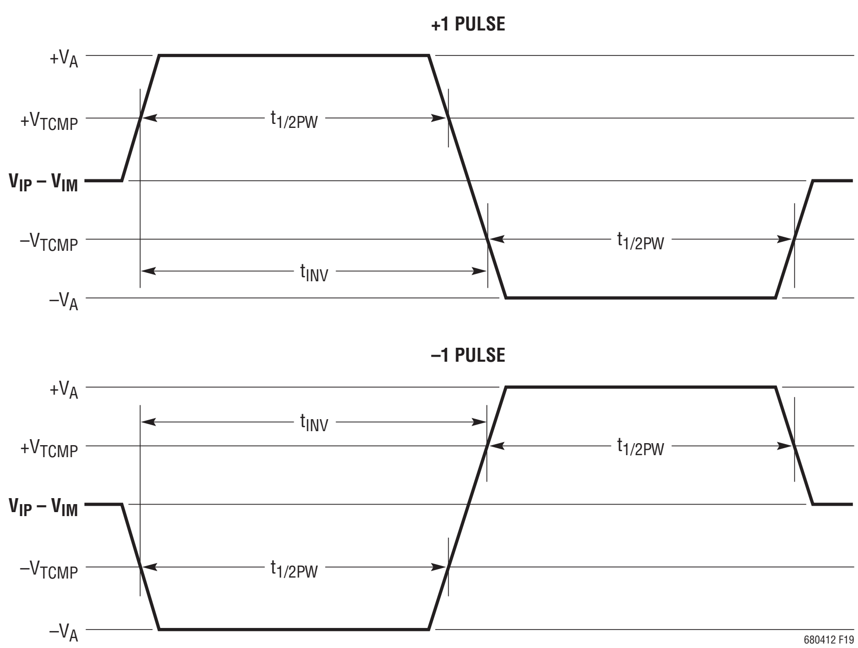

Figure 19. isoSPI Pulse Detail

OPERATION

Table 23. LTC6804-1 Port A (Slave) isoSPI Port Function

RECEIVED PULSE (PORT A isoSPI)	INTERNAL SPI PORT ACTION	RETURN PULSE
Long +1	Drive CSB High	None
Long –1	Drive CSB Low	
Short +1	1. Set SDI = 1 2. Pulse SCK	Short –1 Pulse if Reading a 0 bit
Short –1	1. Set SDI = 0 2. Pulse SCK	(No Return Pulse if Not in READ Mode or if Reading a 1 bit)

The lower isoSPI port (Port A) never transmits long (CSB) pulses. Furthermore, a slave isoSPI port will only transmit short –1 pulses, never a +1 pulse. The master port recognizes a null response as a logic 1. This allows for multiple slave devices on a single cable without risk of collisions (Multidrop).

Figure 20 shows the isoSPI timing diagram for a READ command to daisy-chained LTC6804-1 parts. The ISOMD pin is tied to V^- on the bottom part so its Port A is configured as a SPI port (CSB, SCK, SDI and SDO). The isoSPI signals of three stacked devices are shown, labeled with the port (A or B) and part number. Note that ISO B1 and ISO A2 is actually the same signal, but shown on each end of the transmission cable that connects parts 1 and 2. Likewise, ISO B2 and ISO A3 is the same signal, but with the cable delay shown between parts 2 and 3.

Bits W_n-W_0 refers to the 16-bit command code and the 16-bit PEC of a READ command. At the end of bit W_0 the 3 parts decode the READ command and begin shifting out data which is valid on the next rising edge of clock SCK. Bits X_n-X_0 refer to the data shifted out by Part 1. Bits Y_n-Y_0

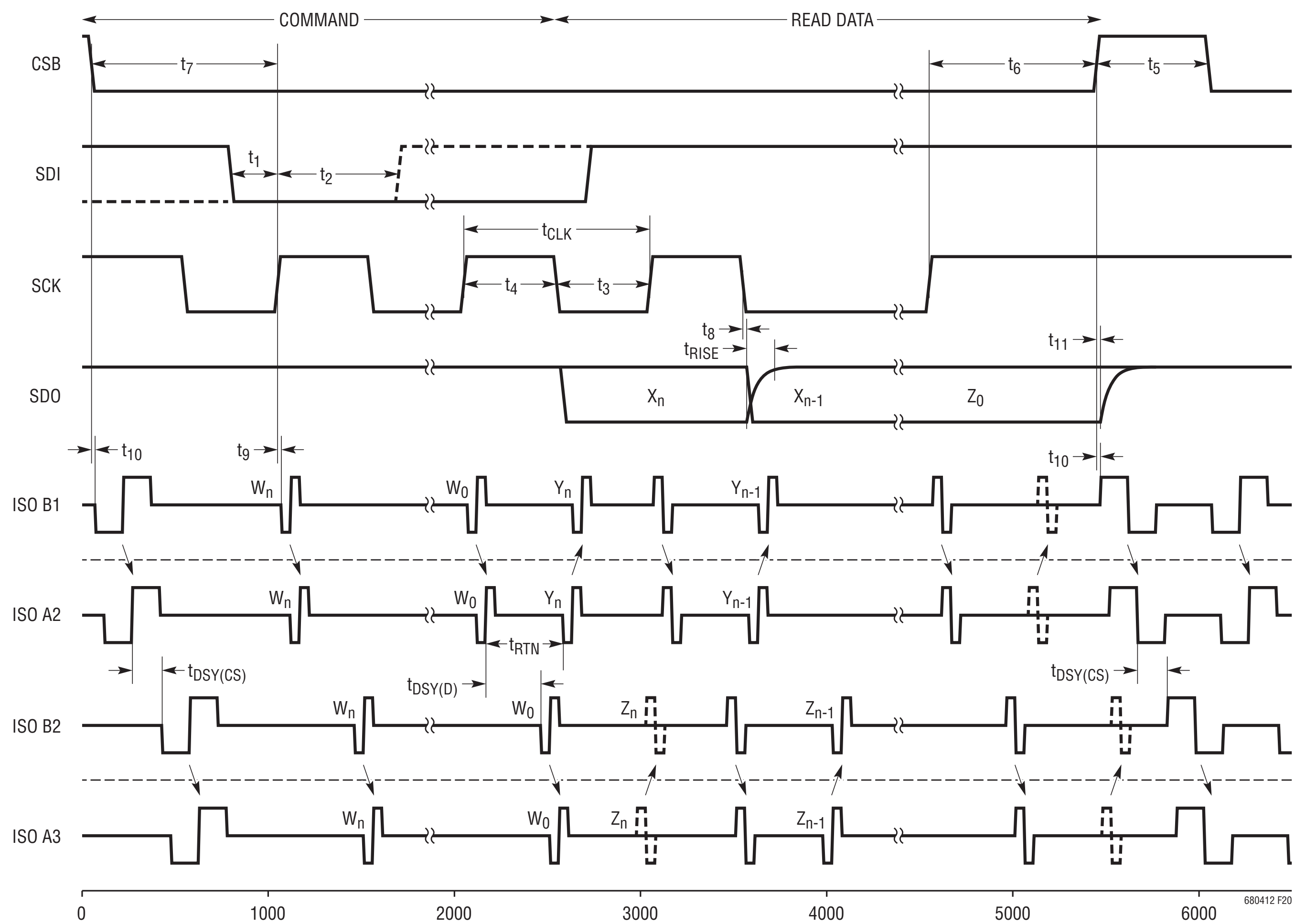

Figure 20. isoSPI Timing Diagram

OPERATION

refer to the data shifted out by Part 2 and bits Z_n-Z_0 refer to the data shifted out by Part 3. All this data is read back from the SDO port on Part 1 in a daisy-chained fashion.

Waking Up the Serial Interface

The serial ports (SPI or isoSPI) will enter the low power IDLE state if there is no activity on Port A for a time of t_{IDLE}. The WAKEUP circuit monitors activity on pins 41 and 42.

If ISOMD = V^-, Port A is in SPI mode. Activity on the CSB or SCK pin will wake up the SPI interface. If ISOMD = V_{REG}, Port A is in isoSPI mode. Differential activity on IPA-IMB wakes up the isoSPI interface. The LTC6804 will be ready to communicate when the isoSPI state changes to READY within t_{WAKE} or t_{READY}, depending on the Core state (see Figure 1 and state descriptions for details.)

The LTC6804-1 sends a Long +1 pulse on Port B after it is ready to communicate. In a daisy-chained configuration, this pulse wakes up the next device in the stack which will, in turn, wake up the next device. If there are 'N' devices in the stack, all the devices are powered up within the time N • t_{WAKE} or N • t_{READY}, depending on the Core State. For large stacks, the time N • t_{WAKE} may be equal to or larger than t_{IDLE}. In this case, after waiting longer than the time of N • t_{WAKE}, the host may send another dummy byte and wait for the time N • t_{READY}, in order to ensure that all devices are in the READY state.

Figure 21 illustrates the timing and the functionally equivalent circuit. Common mode signals will not wake up the serial interface. The interface is designed to wake up after receiving a large signal single-ended pulse, or a low-amplitude symmetric pulse. The differential signal |SCK(IPA) – CSB(IMA)|, must be at least V_{WAKE} = 200mV for a minimum duration of t_{DWELL} = 240ns to qualify as a wake up signal that powers up the serial interface.

DATA LINK LAYER

All Data transfers on LTC6804 occur in byte groups. Every byte consists of 8 bits. Bytes are transferred with the most significant bit (MSB) first. CSB must remain low for the entire duration of a command sequence, including between a command byte and subsequent data. On a write command, data is latched in on the rising edge of CSB.

NETWORK LAYER

Packet Error Code

The packet error code (PEC) is a 15-bit cyclic redundancy check (CRC) value calculated for all of the bits in a register group in the order they are passed, using the initial PEC seed value of 000000000010000 and the following characteristic polynomial: x15 + x14 + x10 + x8 + x7 + x4 + x3 + 1. To calculate the 15-bit PEC value, a simple procedure can be established:

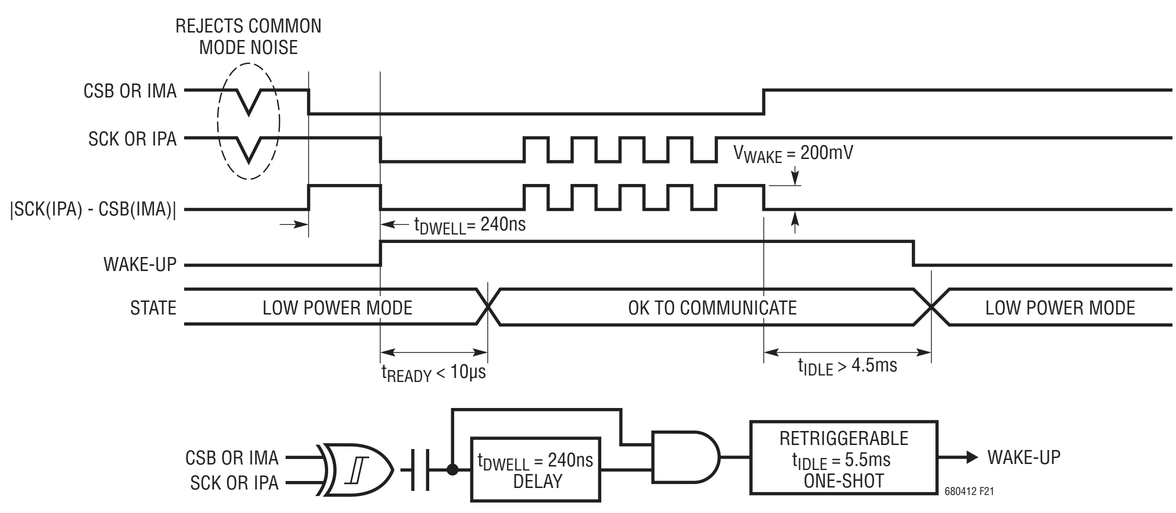

Figure 21. Wake-Up Detection and IDLE Timer

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1. Initialize the PEC to 000000000010000 (PEC is a 15-bit register group)
2. For each bit DIN coming into the PEC register group, set

   IN0 = DIN XOR PEC [14]

   IN3 = IN0 XOR PEC [2]

   IN4 = IN0 XOR PEC [3]

   IN7 = IN0 XOR PEC [6]

   IN8 = IN0 XOR PEC [7]

   IN10 = IN0 XOR PEC [9]

   IN14 = IN0 XOR PEC [13]
3. Update the 15-bit PEC as follows

   PEC [14] = IN14,

   PEC [13] = PEC [12],

   PEC [12] = PEC [11],

   PEC [11] = PEC [10],

   PEC [10] = IN10,

   PEC [9] = PEC [8],

   PEC [8] = IN8,

   PEC [7] = IN7,

   PEC [6] = PEC [5],

   PEC [5] = PEC [4],

   PEC [4] = IN4,

   PEC [3] = IN3,

   PEC [2] = PEC [1],

   PEC [1] = PEC [0],

   PEC [0] = IN0
4. Go back to step 2 until all the data is shifted. The final PEC (16 bits) is the 15-bit value in the PEC register with a 0 bit appended to its LSB

Figure 22 illustrates the algorithm described above. An example to calculate the PEC for a 16-bit word (0x0001) is listed in Table 24. The PEC for 0x0001 is computed as 0x3D6E after stuffing a 0 bit at the LSB. For longer data streams, the PEC is valid at the end of the last bit of data sent to the PEC register.

LTC6804 calculates PEC for any command or data received and compares it with the PEC following the command or data. The command or data is regarded as valid only if the PEC matches. LTC6804 also attaches the calculated PEC at the end of the data it shifts out. Table 25 shows the format of PEC while writing to or reading from LTC6804.

While writing any command to LTC6804, the command bytes CMD0 and CMD1 (See Table 32 and Table 33) and the PEC bytes PEC0 and PEC1 are sent on Port A in the following order:

CMD0, CMD1, PEC0, PEC1

After a broadcast write command to daisy-chained LTC6804-1 devices, data is sent to each device followed by the PEC. For example, when writing the configuration register group to two daisy-chained devices (primary device P, stacked device S), the data will be sent to the primary device on Port A in the following order:

CFGR0(S), … , CFGR5(S), PEC0(S), PEC1(S), CFGR0(P), …, CFGR5(P), PEC0(P), PEC1(P)

After a read command for daisy-chained devices, each device shifts out its data and the PEC that it computed for its data on Port A followed by the data received on Port B. For example, when reading status register group B from

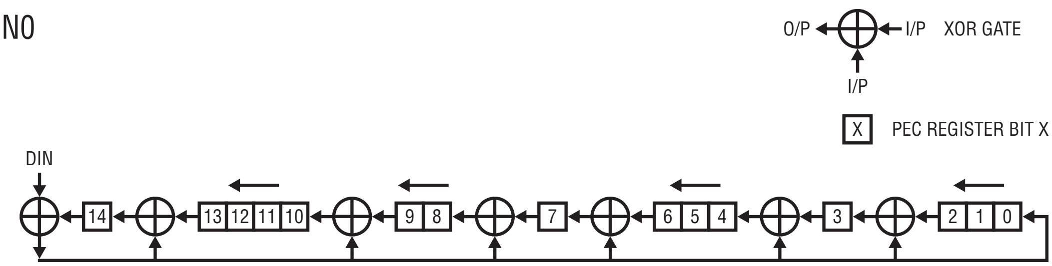

Figure 22. 15-Bit PEC Computation Circuit

680412f

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Table 24. PEC Calculation for 0x0001

PEC[14]	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	**0**
PEC[13]	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	**0**
PEC[12]	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	**1**
PEC[11]	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	**1**
PEC[10]	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	**1**
PEC[9]	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[8]	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	**0**
PEC[7]	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1	**1**
PEC[6]	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	**0**
PEC[5]	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[4]	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	**1**
PEC[3]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	**0**
PEC[2]	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	**1**
PEC[1]	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	**1**
PEC[0]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	**1**
IN14	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0		**0**
IN10	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1		**PEC Word**
IN8	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0		
IN7	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1		
IN4	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1		
IN3	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0		
IN0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1		
DIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
Clock Cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Table 25. Write/Read PEC Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PEC0	RD/WR	PEC[14]	PEC[13]	PEC[12]	PEC[11]	PEC[10]	PEC[9]	PEC[8]	PEC[7]
PEC1	RD/WR	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	0

two daisy-chained devices (primary device P, stacked device S), the primary device sends out data on port A in the following order:

STBR0(P), …, STBR5(P), PEC0(P), PEC1(P), STBR0(S), … , STBR5(S), PEC0(S), PEC1(S)

Broadcast Commands

A broadcast command is one to which all devices on the bus will respond, regardless of device address. This command can be used with LTC6804-1 and LTC6804-2 parts. See Bus Protocols for Broadcast command format. With broadcast commands all devices can be sent commands simultaneously.

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In parallel configurations, this is useful for ADC conversion and polling commands. It can also be used with write commands when all parts are being written with the same data. Broadcast read commands should not be used in the parallel configuration.

Daisy-chained configurations only support broadcast commands. All devices in the chain receive the command bytes simultaneously. For example, to initiate ADC conversions in a stack of devices, a single ADCV command is sent, and all devices will start conversions at the same time. For read and write commands, a single command is sent, and then the stacked devices effectively turn into a cascaded shift register, in which data is shifted through each device to the next device in the stack. See the Serial Programming Examples section.

Address Commands

An address command is one in which only the addressed device on the bus responds. Address commands are used only with LTC6804-2 parts. See Bus Protocols for Address command format.

Polling Methods

The simplest method to determine ADC completion is for the controller to start an ADC conversion and wait for the specified conversion time to pass before reading the results. Polling is not supported with daisy-chain communication.

In parallel configurations that communicate in SPI mode (ISOMD pin tied low), there are two methods of polling. The first method is to hold CSB low after an ADC

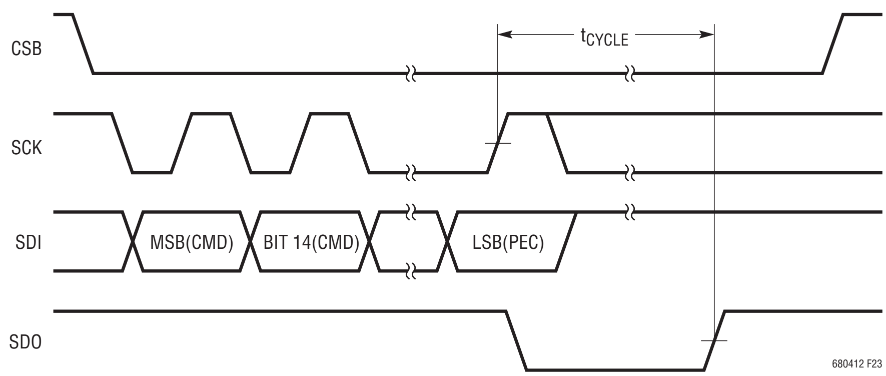

Figure 23. SDO Polling After an ADC Conversion Command

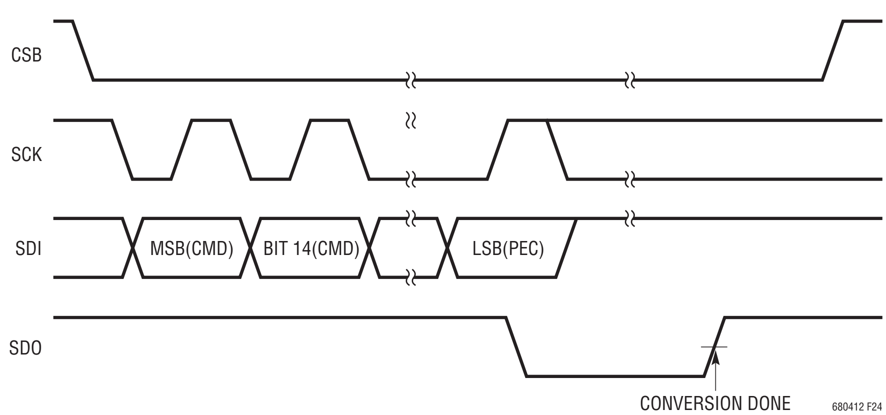

Figure 24. SDO Polling Using PLADC Command

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conversion command is sent. After entering a conversion command, the SDO line is driven low when the device is busy performing conversions (Figure 23). SDO is pulled high when the device completes conversions. However, the SDO will also go back high when CSB goes high even if the device has not completed the conversion. An addressed device drives the SDO line based on its status alone. A problem with this method is that the controller is not free to do other serial communication while waiting for ADC conversions to complete. The next method overcomes this limitation. The controller can send an ADC start command, perform other tasks, and then send a poll ADC converter status (PLADC) command to determine the status of the ADC conversions (Figure 24). After entering the PLADC command, SDO will go low if the device is busy performing conversions. SDO is pulled high at the end of conversions. However, the SDO will also go high when CSBI goes high even if the device has not completed the conversion. See Programming Examples on how to use the PLADC command with devices in parallel configuration.

In parallel configurations that communicate in isoSPI mode, the low side port transmits a data pulse only in response to a master isoSPI pulse received by it. So, after entering the command in either method of polling described above, isoSPI data pulses are sent to the part to update the conversion status. These pulses can be sent using LTC6820 by simply clocking its SCK pin. In response to this pulse, the LTC6804 returns an isoSPI pulse if it is still busy performing conversions and does not return a pulse if it has completed conversions. If a CSB high isoSPI pulse is sent to the LTC6804, it exits the polling command.

Bus Protocols

Protocol Format: The protocol formats for both broadcast and address commands are depicted in Table 27 through Table 31. Table 26 is the key for reading the protocol diagrams.

Table 26. Protocol Key

CMD0	First Command Byte (See Tables 32 and 33)
CMD1	Second Command Byte (See Tables 32 and 33)
PEC0	First PEC Byte (See Table 25)
PEC1	Second PEC Byte (See Table 25)
n	Number of Bytes
…	Continuation of Protocol
	Master to Slave
(shaded)	Slave to Master

Command Format: The formats for the broadcast and address commands are shown in Table 32 and Table 33 respectively. The 11-bit command code CC[10:0] is the same for a broadcast or an address command. A list of all the command codes is shown in Table 34. A broadcast command has a value 0 for CMD0[7] through CMD0[3]. An address command has a value 1 for CMD0[7] followed by the 4-bit address of the device (a3, a2, a1, a0) in bits CMD0[6:3]. An addressed device will respond to an address command only if the physical address of the device on pins A3 to A0 match the address specified in the address command. The PEC for broadcast and address commands must be computed on the entire 16-bit command (CMD0 and CMD1).

Commands

Table 34 lists all the commands and its options for both LTC6804-1 and LTC6804-2

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Table 27. Broadcast/Address Poll Command

8	8	8	8	
CMD0	CMD1	PEC0	PEC1	Poll Data

Table 28. Broadcast Write Command

8	8	8	8	8		8	8	8	8		8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1	Shift Byte 1	…	Shift Byte *n*

Table 29. Address Write Command

8	8	8	8	8		8	8	8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1

Table 30. Broadcast Read Command

8	8	8	8	8		8	8	8	8		8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1	Shift Byte 1	…	Shift Byte *n*

Table 31. Address Read Command

8	8	8	8	8		8	8	8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1

Table 32. Broadcast Command Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMD0	WR	0	0	0	0	0	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

Table 33. Address Command Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMD0	WR	1	a3*	a2*	a1*	a0*	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

*ax is Address Bit x

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Table 34. Command Codes

COMMAND DESCRIPTION	NAME	CC[10:0] - COMMAND CODE										
		10	9	8	7	6	5	4	3	2	1	0
Write Configuration Register Group	WRCFG	0	0	0	0	0	0	0	0	0	0	1
Read Configuration Register Group	RDCFG	0	0	0	0	0	0	0	0	0	1	0
Read Cell Voltage Register Group A	RDCVA	0	0	0	0	0	0	0	0	1	0	0
Read Cell Voltage Register Group B	RDCVB	0	0	0	0	0	0	0	0	1	1	0
Read Cell Voltage Register Group C	RDCVC	0	0	0	0	0	0	0	1	0	0	0
Read Cell Voltage Register Group D	RDCVD	0	0	0	0	0	0	0	1	0	1	0
Read Auxiliary Register Group A	RDAUXA	0	0	0	0	0	0	0	1	1	0	0
Read Auxiliary Register Group B	RDAUXB	0	0	0	0	0	0	0	1	1	1	0
Read Status Register Group A	RDSTATA	0	0	0	0	0	0	1	0	0	0	0
Read Status Register Group B	RDSTATB	0	0	0	0	0	0	1	0	0	1	0
Start Cell Voltage ADC Conversion and Poll Status	ADCV	0	1	MD[1]	MD[0]	1	1	DCP	0	CH[2]	CH[1]	CH[0]
Start Open Wire ADC Conversion and Poll Status	ADOW	0	1	MD[1]	MD[0]	PUP	1	DCP	1	CH[2]	CH[1]	CH[0]
Start Self-Test Cell Voltage Conversion and Poll Status	CVST	0	1	MD[1]	MD[0]	ST[1]	ST[0]	0	0	1	1	1
Start GPIOs ADC Conversion and Poll Status	ADAX	1	0	MD[1]	MD[0]	1	1	0	0	CHG [2]	CHG [1]	CHG [0]
Start Self-Test GPIOs Conversion and Poll Status	AXST	1	0	MD[1]	MD[0]	ST[1]	ST[0]	0	0	1	1	1
Start Status group ADC Conversion and Poll Status	ADSTAT	1	0	MD[1]	MD[0]	1	1	0	1	CHST [2]	CHST [1]	CHST [0]
Start Self-Test Status group Conversion and Poll Status	STATST	1	0	MD[1]	MD[0]	ST[1]	ST[0]	0	1	1	1	1
Start Combined Cell Voltage and GPIO1, GPIO2 Conversion and Poll Status	ADCVAX	1	0	MD[1]	MD[0]	1	1	DCP	1	1	1	1
Clear Cell Voltage Register Group	CLRCELL	1	1	1	0	0	0	1	0	0	0	1
Clear Auxiliary Register Group	CLRAUX	1	1	1	0	0	0	1	0	0	1	0
Clear Status Register Group	CLRSTAT	1	1	1	0	0	0	1	0	0	1	1
Poll ADC Conversion Status	PLADC	1	1	1	0	0	0	1	0	1	0	0
Diagnose MUX and Poll Status	DIAGN	1	1	1	0	0	0	1	0	1	0	1
Write COMM Register Group	WRCOMM	1	1	1	0	0	1	0	0	0	0	1
Read COMM Register Group	RDCOMM	1	1	1	0	0	1	0	0	0	1	0
Start I^2C/SPI Communication	STCOMM	1	1	1	0	0	1	0	0	0	1	1

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Table 35. Command Bit Descriptions

NAME	DESCRIPTION	VALUES							
MD[1:0]	ADC Mode	MD	ADCOPT(CFGR0[0]) = 0			ADCOPT (CFGR0[0]) = 1			
		01	27kHz Mode (Fast)			14kHz Mode			
		10	7kHz Mode (Normal)			3kHz Mode			
		11	26Hz Mode (Filtered)			2kHz Mode			
DCP	Discharge Permitted	DCP							
		0	Discharge Not Permitted						
		1	Discharge Permitted						
CH[2:0]	Cell Selection for ADC Conversion			Total Conversion Time in the 6 ADC Modes					
		CH		27kHz	14kHz	7kHz	3kHz	2kHz	26Hz
		000	All Cells	1.1ms	1.3ms	2.3ms	3.0ms	4.4ms	201ms
		001	Cell 1 and Cell 7	201µs	230µs	405µs	501µs	754µs	34ms
		010	Cell 2 and Cell 8						
		011	Cell 3 and Cell 9						
		100	Cell 4 and Cell 10						
		101	Cell 5 and Cell 11						
		110	Cell 6 and Cell 12						
PUP	Pull-Up/Pull-Down Current for Open-Wire Conversions	PUP							
		0	Pull-Down Current						
		1	Pull-Up Current						
ST[1:0]	Self-Test Mode Selection			Self-Test Conversion Result					
		ST		27kHz	14kHz	7kHz	3kHz	2kHz	26Hz
		01	Self Test 1	0x9565	0x9553	0x9555	0x9555	0x9555	0x9555
		10	Self test 2	0x6A9A	0x6AAC	0x6AAA	0x6AAA	0x6AAA	0x6AAA
CHG[2:0]	GPIO Selection for ADC Conversion			Total Conversion Time in the 6 ADC Modes					
		CHG		27kHz	14kHz	7kHz	3kHz	2kHz	26Hz
		000	GPIO 1-5, 2nd Ref	1.1ms	1.3ms	2.3ms	3.0ms	4.4ms	201ms
		001	GPIO 1	201µs	230µs	405µs	501µs	754µs	34ms
		010	GPIO 2						
		011	GPIO 3						
		100	GPIO 4						
		101	GPIO 5						
		110	2nd Reference						
CHST[2:0]*	Status Group Selection			Total Conversion Time in the 6 ADC Modes					
		CHST		27kHz	14kHz	7kHz	3kHz	2kHz	26Hz
		000	SOC, ITMP, VA, VD	748µs	865µs	1.6ms	2.0ms	3.0ms	134ms
		001	SOC	201µs	230µs	405µs	501µs	754µs	34ms
		010	ITMP						
		011	VA						
		100	VD						

*Note: Valid options for CHST in ADSTAT command are 0-4. If CHST is set to 5/6 in ADSTAT command, the LTC6804 treats it like ADAX command with CHG = 5/6.

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Table 36. Configuration Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGR0	RD/WR	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	REFON	SWTRD	ADCOPT
CFGR1	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGR2	RD/WR	VOV[3]	VOV[2]	VOV[1]	VOV[0]	VUV[11]	VUV[10]	VUV[9]	VUV[8]
CFGR3	RD/WR	VOV[11]	VOV[10]	VOV[9]	VOV[8]	VOV[7]	VOV[6]	VOV[5]	VOV[4]
CFGR4	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGR5	RD/WR	DCTO[3]	DCTO[2]	DCTO[1]	DCTO[0]	DCC12	DCC11	DCC10	DCC9

Table 37. Cell Voltage Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVAR0	RD	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
CVAR1	RD	C1V[15]	C1V[14]	C1V[13]	C1V[12]	C1V[11]	C1V[10]	C1V[9]	C1V[8]
CVAR2	RD	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
CVAR3	RD	C2V[15]	C2V[14]	C2V[13]	C2V[12]	C2V[11]	C2V[10]	C2V[9]	C2V[8]
CVAR4	RD	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
CVAR5	RD	C3V[15]	C3V[14]	C3V[13]	C3V[12]	C3V[11]	C3V[10]	C3V[9]	C3V[8]

Table 38. Cell Voltage Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVBR0	RD	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]
CVBR1	RD	C4V[15]	C4V[14]	C4V[13]	C4V[12]	C4V[11]	C4V[10]	C4V[9]	C4V[8]
CVBR2	RD	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
CVBR3	RD	C5V[15]	C5V[14]	C5V[13]	C5V[12]	C5V[11]	C5V[10]	C5V[9]	C5V[8]
CVBR4	RD	C6V[7]	C6V[6]	C6V[5]	C6V[4]	C6V[3]	C6V[2]	C6V[1]	C6V[0]
CVBR5	RD	C6V[15]	C6V[14]	C6V[13]	C6V[12]	C6V[11]	C6V[10]	C6V[9]	C6V[8]

Table 39. Cell Voltage Register Group C

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVCR0	RD	C7V[7]	C7V[6]	C7V[5]	C7V[4]	C7V[3]	C7V[2]	C7V[1]	C7V[0]
CVCR1	RD	C7V[15]	C7V[14]	C7V[13]	C7V[12]	C7V[11]	C7V[10]	C7V[9]	C7V[8]
CVCR2	RD	C8V[7]	C8V[6]	C8V[5]	C8V[4]	C8V[3]	C8V[2]	C8V[1]	C8V[0]
CVCR3	RD	C8V[15]	C8V[14]	C8V[13]	C8V[12]	C8V[11]	C8V[10]	C8V[9]	C8V[8]
CVCR4	RD	C9V[7]	C9V[6]	C9V[5]	C9V[4]	C9V[3]	C9V[2]	C9V[1]	C9V[0]
CVCR5	RD	C9V[15]	C9V[14]	C9V[13]	C9V[12]	C9V[11]	C9V[10]	C9V[9]	C9V[8]

Table 40. Cell Voltage Register Group D

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVDR0	RD	C10V[7]	C10V[6]	C10V[5]	C10V[4]	C10V[3]	C10V[2]	C10V[1]	C10V[0]
CVDR1	RD	C10V[15]	C10V[14]	C10V[13]	C10V[12]	C10V[11]	C10V[10]	C10V[9]	C10V[8]
CVDR2	RD	C11V[7]	C11V[6]	C11V[5]	C11V[4]	C11V[3]	C11V[2]	C11V[1]	C11V[0]
CVDR3	RD	C11V[15]	C11V[14]	C11V[13]	C11V[12]	C11V[11]	C11V[10]	C11V[9]	C11V[8]
CVDR4	RD	C12V[7]	C12V[6]	C12V[5]	C12V[4]	C12V[3]	C12V[2]	C12V[1]	C12V[0]
CVDR5	RD	C12V[15]	C12V[14]	C12V[13]	C12V[12]	C12V[11]	C12V[10]	C12V[9]	C12V[8]

OPERATION

Table 41. Auxiliary Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVAR0	RD	G1V[7]	G1V[6]	G1V[5]	G1V[4]	G1V[3]	G1V[2]	G1V[1]	G1V[0]
AVAR1	RD	G1V[15]	G1V[14]	G1V[13]	G1V[12]	G1V[11]	G1V[10]	G1V[9]	G1V[8]
AVAR2	RD	G2V[7]	G2V[6]	G2V[5]	G2V[4]	G2V[3]	G2V[2]	G2V[1]	G2V[0]
AVAR3	RD	G2V[15]	G2V[14]	G2V[13]	G2V[12]	G2V[11]	G2V[10]	G2V[9]	G2V[8]
AVAR4	RD	G3V[7]	G3V[6]	G3V[5]	G3V[4]	G3V[3]	G3V[2]	G3V[1]	G3V[0]
AVAR5	RD	G3V[15]	G3V[14]	G3V[13]	G3V[12]	G3V[11]	G3V[10]	G3V[9]	G3V[8]

Table 42. Auxiliary Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVBR0	RD	G4V[7]	G4V[6]	G4V[5]	G4V[4]	G4V[3]	G4V[2]	G4V[1]	G4V[0]
AVBR1	RD	G4V[15]	G4V[14]	G4V[13]	G4V[12]	G4V[11]	G4V[10]	G4V[9]	G4V[8]
AVBR2	RD	G5V[7]	G5V[6]	G5V[5]	G5V[4]	G5V[3]	G5V[2]	G5V[1]	G5V[0]
AVBR3	RD	G5V[15]	G5V[14]	G5V[13]	G5V[12]	G5V[11]	G5V[10]	G5V[9]	G5V[8]
AVBR4	RD	REF[7]	REF[6]	REF[5]	REF[4]	REF[3]	REF[2]	REF[1]	REF[0]
AVBR5	RD	REF[15]	REF[14]	REF[13]	REF[12]	REF[11]	REF[10]	REF[9]	REF[8]

Table 43. Status Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STAR0	RD	SOC[7]	SOC[6]	SOC[5]	SOC[4]	SOC[3]	SOC[2]	SOC[1]	SOC[0]
STAR1	RD	SOC[15]	SOC[14]	SOC[13]	SOC[12]	SOC[11]	SOC[10]	SOC[9]	SOC[8]
STAR2	RD	ITMP[7]	ITMP[6]	ITMP[5]	ITMP[4]	ITMP[3]	ITMP[2]	ITMP[1]	ITMP[0]
STAR3	RD	ITMP[15]	ITMP[14]	ITMP[13]	ITMP[12]	ITMP[11]	ITMP[10]	ITMP[9]	ITMP[8]
STAR4	RD	VA[7]	VA[6]	VA[5]	VA[4]	VA[3]	VA[2]	VA[1]	VA[0]
STAR5	RD	VA[15]	VA[14]	VA[13]	VA[12]	VA[11]	VA[10]	VA[9]	VA[8]

Table 44. Status Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STBR0	RD	VD[7]	VD[6]	VD[5]	VD[4]	VD[3]	VD[2]	VD[1]	VD[0]
STBR1	RD	VD[15]	VD[14]	VD[13]	VD[12]	VD[11]	VD[10]	VD[9]	VD[8]
STBR2	RD	C4OV	C4UV	C3OV	C3UV	C2OV	C2UV	C1OV	C1UV
STBR3	RD	C8OV	C8UV	C7OV	C7UV	C6OV	C6UV	C5OV	C5UV
STBR4	RD	C12OV	C12UV	C11OV	C11UV	C10OV	C10UV	C9OV	C9UV
STBR5	RD	REV[3]	REV[2]	REV[1]	REV[0]	RSVD	RSVD	MUXFAIL	THSD

Table 45. COMM Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMM0	RD/WR	ICOM0[3]	ICOM0[2]	ICOM0[1]	ICOM0[0]	D0[7]	D0[6]	D0[5]	D0[4]
COMM1	RD/WR	D0[3]	D0[2]	D0[1]	D0[0]	FCOM0[3]	FCOM0[2]	FCOM0[1]	FCOM0[0]
COMM2	RD/WR	ICOM1[3]	ICOM1[2]	ICOM1[1]	ICOM1[0]	D1[7]	D1[6]	D1[5]	D1[4]
COMM3	RD/WR	D1[3]	D1[2]	D1[1]	D1[0]	FCOM1[3]	FCOM1[2]	FCOM1[1]	FCOM1[0]
COMM4	RD/WR	ICOM2[3]	ICOM2[2]	ICOM2[1]	ICOM2[0]	D2[7]	D2[6]	D2[5]	D2[4]
COMM5	RD/WR	D2[3]	D2[2]	D2[1]	D2[0]	FCOM2[3]	FCOM2[2]	FCOM2[1]	FCOM2[0]

OPERATION

Table 46. Memory Bit Descriptions

<table>
<tr><th>NAME</th><th>DESCRIPTION</th><th colspan="17">VALUES</th></tr>
<tr><td>GPIOx</td><td>GPIOx Pin Control</td><td colspan="17">Write: 0 -> GPIOx Pin Pull-Down ON; 1-> GPIOx Pin Pull-Down OFF
Read: 0 -> GPIOx Pin at Logic 0; 1 -> GPIOx Pin at Logic 1</td></tr>
<tr><td>REFON</td><td>Reference Powered Up</td><td colspan="17">1 -> Reference Remains Powered Up Until Watchdog Timeout
0 -> Reference Shuts Down after Conversions</td></tr>
<tr><td>SWTRD</td><td>SWTEN Pin Status (Read Only)</td><td colspan="17">1 -> SWTEN Pin at Logic 1
0 -> SWTEN Pin at Logic 0</td></tr>
<tr><td>ADCOPT</td><td>ADC Mode Option Bit</td><td colspan="17">ADCOPT: 0 -> Selects Modes 27kHz, 7kHz or 26Hz with MD[1:0] Bits in ADC Conversion Commands.
1 -> Selects Modes 14kHz, 3kHz or 2kHz with MD[1:0] Bits in ADC Conversion Commands.</td></tr>
<tr><td>VUV</td><td>Undervoltage Comparison Voltage*</td><td colspan="17">Comparison voltage = (VUV + 1) • 16 • 100µV
Default: VUV = 0x000</td></tr>
<tr><td>VOV</td><td>Overvoltage Comparison Voltage*</td><td colspan="17">Comparison voltage = VOV • 16 • 100µV
Default: VUV = 0x000</td></tr>
<tr><td>DCC[x]</td><td>Discharge Cell x</td><td colspan="17">x = 1 to 12 1 -> Turn ON Shorting Switch for Cell x
0 -> Turn OFF Shorting Switch for Cell x (Default)</td></tr>
<tr><td>DCTO</td><td>Discharge Time Out Value</td><td>DCTO (Write)</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td></tr>
<tr><td></td><td></td><td>Time (Min)</td><td>Disabled</td><td>0.5</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>10</td><td>15</td><td>20</td><td>30</td><td>40</td><td>60</td><td>75</td><td>90</td><td>120</td></tr>
<tr><td></td><td></td><td>DCTO (Read)</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td></tr>
<tr><td></td><td></td><td>Time Left (Min)</td><td>Disabled or Timeout</td><td>0 to 0.5</td><td>0.5 to 1</td><td>1 to 2</td><td>2 to 3</td><td>3 to 4</td><td>4 to 5</td><td>5 to 10</td><td>10 to 15</td><td>15 to 20</td><td>20 to 30</td><td>30 to 40</td><td>40 to 60</td><td>60 to 75</td><td>75 to 90</td><td>90 to 120</td></tr>
<tr><td>CxV</td><td>Cell x Voltage*</td><td colspan="17">x = 1 to 12 16-Bit ADC Measurement Value for Cell x
Cell Voltage for Cell x = CxV • 100µV
CxV Is Reset to 0xFFFF on Power-Up and After Clear Command</td></tr>
<tr><td>GxV</td><td>GPIO x Voltage*</td><td colspan="17">x = 1 to 5 16-Bit ADC Measurement Value for GPIOx
Voltage for GPIOx = GxV • 100µV
GxV Is Reset to 0xFFFF on Power-Up and After Clear Command</td></tr>
<tr><td>REF</td><td>2nd Reference Voltage*</td><td colspan="17">16-Bit ADC Measurement Value for 2nd Reference
Voltage for 2nd Reference = REF • 100µV
Normal Range Is within 2.980V to 3.020V</td></tr>
<tr><td>SOC</td><td>Sum of Cells Measurement*</td><td colspan="17">16-Bit ADC Measurement Value of the Sum of All Cell Voltages
Sum of All Cells Voltage = SOC • 100µV • 20</td></tr>
<tr><td>ITMP</td><td>Internal Die Temperature*</td><td colspan="17">16-Bit ADC Measurement Value of Internal Die Temperature
Temperature Measurement Voltage = ITMP • 100µV/7.5mV/°C – 273°C</td></tr>
<tr><td>VA</td><td>Analog Power Supply Voltage*</td><td colspan="17">16-Bit ADC Measurement Value of Analog Power Supply Voltage
Analog Power Supply Voltage = VA • 100µV
Normal Range Is within 4.5V to 5.5V</td></tr>
<tr><td>VD</td><td>Digital Power Supply Voltage*</td><td colspan="17">16-Bit ADC Measurement Value of Digital Power Supply Voltage
Digital Power Supply Voltage = VA • 100µV
Normal Range Is within 2.7V to 3.6V</td></tr>
<tr><td>CxOV</td><td>Cell x Overvoltage Flag</td><td colspan="17">x = 1 to 12 Cell Voltage Compared to VOV Comparison Voltage
0 -> Cell x Not Flagged for Overvoltage Condition. 1 -> Cell x Flagged</td></tr>
<tr><td>CxUV</td><td>Cell x Undervoltage Flag</td><td colspan="17">x = 1 to 12 Cell Voltage Compared to VUV Comparison Voltage
0 -> Cell x Not Flagged for Undervoltage Condition. 1 -> Cell x Flagged</td></tr>
<tr><td>REV</td><td>Revision Code</td><td colspan="17">Device Revision Code</td></tr>
<tr><td>RSVD</td><td>Reserved Bits</td><td colspan="17">Read: Read Back Value Is Always 0</td></tr>
</table>

OPERATION

Table 46. Memory Bit Descriptions

NAME	DESCRIPTION	VALUES						
MUXFAIL	Multiplexer Self-Test Result	Read: 0 -> Multiplexer Passed Self Test 1 -> Multiplexer Failed Self Test						
THSD	Thermal Shutdown Status	Read: 0 -> Thermal Shutdown Has Not Occurred 1 -> Thermal Shutdown Has Occurred THSD Bit Cleared to 0 on Read of Status RegIster Group B						
ICOMn	Initial Communication Control Bits	Write	I2C	0110	0001	0000	0111	
				START	STOP	BLANK	NO TRANSMIT	
			SPI	1000	1001	1111		
				CSB Low	CSB High	NO TRANSMIT		
		Read	I2C	0110	0001	0000	0111	
				START from Master	STOP from Master	SDA Low Between Bytes	SDA High Between Bytes	
			SPI	0111				
Dn	I^2C/SPI Communication Data Byte	Data Transmitted (Received) to (From) I^2C/SPI Slave Device						
FCOMn	Final Communication Control Bits	Write	I2C	0000	1000	1001		
				Master ACK	Master NACK	Master NACK + STOP		
			SPI	X000	1001			
				CSB Low	CSB High			
		Read	I2C	0000	0111	1111	0001	1001
				ACK from Master	ACK from Slave	NACK from Slave	ACK from Slave + STOP from Master	NACK from Slave + STOP from Master
			SPI	1111				

*Voltage equations use the decimal value of registers, 0 to 4095 for 12 bits and 0 to 65535 for 16 bits.

PROGRAMMING EXAMPLES

The following examples use a configuration of 3 stacked LTC6804-1 devices: S1, S2, S3. Port A on device S1 is configured in SPI mode (ISOMD pin low). Port A on devices S2 and S3 is configured in isoSPI mode (ISOMD pin high). Port B on S1 is connected to Port A on S2. Port B on S2 is connected to Port A on S3. The microcontroller communicates to the stack through Port A on S1.

Waking Up Serial Interface

1. Send a dummy byte. The activity on CSB and SCK will wake up the serial interface on device S1.
2. Wait for the amount of time 3 • t_{WAKE} in order to power up all devices S1, S2 and S3.

For large stacks where some devices may go to the IDLE state after waking, apply steps 3 and 4:

3. Send a second dummy byte.
4. Wait for the amount of time 3 • t_{READY}
5. Send commands

Write Configuration Registers

1. Pull CSB low
2. Send WRCFG command (0x00 0x01) and its PEC (0x3D 0x6E)
3. Send CFGR0 byte of device S3, then CFGR1(S3), … CFGR5(S3), PEC of CFGR0(S3) to CFGR5(S3)
4. Send CFGR0 byte of device S2, then CFGR1(S2), … CFGR5(S2), PEC of CFGR0(S2) to CFGR5(S2)
5. Send CFGR0 byte of device S1, then CFGR1(S1), … CFGR5(S1), PEC of CFGR0(S1) to CFGR5(S1)
6. Pull CSB high, data latched into all devices on rising edge of CSB

OPERATION

Calculation of serial interface time for sequence above:

Number of LTC6804-1s in daisy chain stack = *n*

Number of bytes in sequence (B):

Command: 2 (command byte) + 2 (command PEC) = 4

Data: 6 (Data bytes) + 2 (Data PEC) per LTC6804 = 8 bytes per device

B = 4 + 8 • *n*

Serial port frequency per bit = F

Time = (1/F) • B • 8 bits/byte = (1/F) • [4 + 8 • *n*] • 8

Time for 3 LTC6804 example above, with 1MHz serial port = (1/1e6) • (4 + 8 • 3) • 8 = 224µs

Note: This time will remain the same for all write and read commands.

Read Cell Voltage Register Group A

1. Pull CSB low
2. Send RDCVA command (0x00 0x04) and its PEC (0x07 0xC2)
3. Read CVAR0 byte of device S1, then CVAR1(S1), … CVAR5(S1), PEC of CVAR0(S1) to CVAR5(S1)
4. Read CVAR0 byte of device S2, then CVAR1(S2), … CVAR5(S2), PEC of CVAR0(S2) to CVAR0(S2)
5. Read CVAR0 byte of device S3, then CVAR1(S3), … CVAR5(S3), PEC of CVAR0(S3) to CVAR5(S3)
6. Pull CSB high

Start Cell Voltage ADC Conversion

(All cells, normal mode with discharge permitted) and poll status

1. Pull CSB low
2. Send ADCV command with MD[1:0] = 10 and DCP = 1 i.e. 0x03 0x70 and its PEC (0xAF 0x42)
3. Pull CSB high

Clear Cell Voltage Registers

1. Pull CSB low
2. Send CLRCELL command (0x07 0x11) and its PEC (0xC9 0xC0)
3. Pull CSB high

Poll ADC Status

(Parallel configuration and ISOMD = 0)

This example uses an addressed LTC6804-2 with address A [3:0] = 0011 and ISOMD = 0

1. Pull CSB low
2. Send PLADC command (0x9F 0x14) and its PEC (0x1C 0x48)
3. SDO output is pulled low if the LTC6804-2 is busy. The host needs to send clocks on SCK in order for the polling status to be updated from the addressed device.
4. SDO output is high when the LTC6804-2 has completed conversions
5. Pull CSB high to exit polling

Talk to an I²C Slave Connected to LTC6804

The LTC6804 supports I²C slave devices by connection to GPIO4(SDA) and GPIO5(SCL). One valuable use for this capability is to store production calibration constants or other information in a small serial EEPROM using a connection like shown in Figure 25.

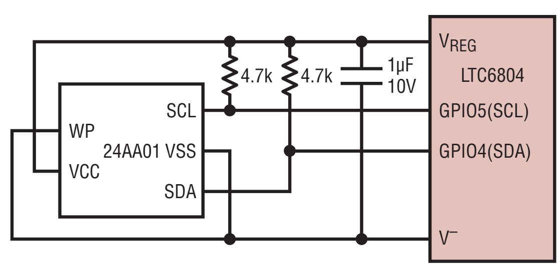


Figure 25. Connecting I²C EEPROM to LTC6804 GPIO Pins

OPERATION

This example uses a single LTC6804-1 to write a byte of data to an I^{2}C EEPROM. The LTC6804 will send three bytes of data to the I^{2}C slave device. The data sent will be B0 = 0xA0 (EEPROM address), B1 = 0x01 (write command), and B2 = 0xAA (data to be stored in EEPROM). The three bytes will be transmitted to the I^{2}C slave device in the following format:

START – B0 – NACK – B1 – NACK – B2 – NACK – STOP

1. Write data to COMM register using WRCOMM command
   a. Pull CSB low
   b. Send WRCOMM command (0x07 0x21) and its PEC (0x24 0xB2)
   c. Send
      COMM0 = 0x6A, COMM1 = 0x08 ([START] [B0 [NACK]),
      COMM2 = 0x00, COMM3 = 0x18 ([BLANK] [B1] [NACK]),
      COMM4 = 0x0A, COMM5 = 0xA9 ([BLANK] [B2] [NACK+STOP])
      and PEC = 0x6D 0xFB for the above data
   d. Pull CSB high
2. Send the 3 bytes of data to I^{2}C slave device using STCOMM command
   a. Pull CSB low
   b. Send STCOMM command (0x07 0x23) and its PEC (0xB9 0xE4)
   c. Send 72 clock cycles on SCK
   d. Pull CSB high
3. Data transmitted to slave during the STCOMM command is stored in the COMM register. Use the RDCOMM command to retrieve the data
   a. Pull CSB low
   b. Send RDCOMM command (0x07 0x22) and its PEC (0x32 0xD6)
   c. Read COMM0-COMM5 and the PEC for the 6 bytes of data.

      Assuming the slave acknowledged all 3 bytes of data, the read back data in this example would look like:

      COMM0 = 0x6A, COMM1 = 0x07, COMM2 = 0x70, COMM3 = 0x17, COMM4 = 0x7A, COMM5 = 0xA1, PEC = 0xD0 0xDE
   d. Pull CSB high

Note: If the slave returns data, this data will be placed in COMM0-COMM5.

Figure 26 shows the activity on GPIO5 (SCL) and GPIO4 (SDA) ports of the I^{2}C master for 72 clock cycles during the STCOMM command in the above example.

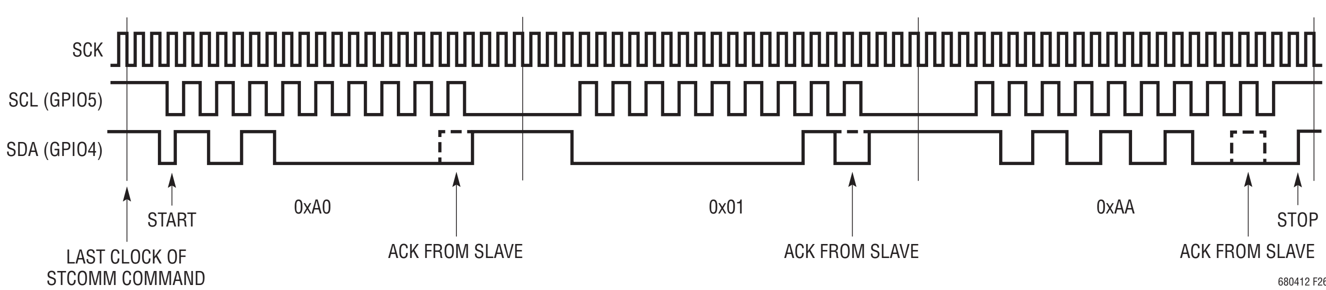


Figure 26. LTC6804 I^{2}C Communication Example

OPERATION

Talk to a SPI Slave Connected to LTC6804

This example uses a single LTC6804-1 device which has a SPI device connected to it through GPIO3 (CSBM), GPIO4 (SDOM) and GPIO5 (SCKM). In this example, the LTC6804 device sends out 3 bytes of data B0 = 0x55, B1 = 0xAA and B2 = 0xCC to the SPI slave device in the following format: CSB low – B0 – B1 – B2 – CSB high

1. Write data to COMM register using WRCOMM command
   a. Pull CSBM low
   b. Send WRCOMM command (0x07 0x21) and its PEC (0x24 0xB2)
   c. Send
      COMM0 = 0x85, COMM1 = 0x50 ([CSBM low] [B0] [CSBM low]),
      COMM2 = 0x8A, COMM3 = 0xA0 ([CSBM low] [B1] [CSBM low]),
      COMM4 = 0x8C, COMM5 = 0xC9 ([CSBM low] [B2] [CSBM high])
      and PEC = 0x89 0xA4 for the above data.
   d. Pull CSB high
2. Send the 3 bytes of data to SPI slave device using STCOMM command
   a. Pull CSB low
   b. Send STCOMM command (0x07 0x23) and its PEC (0xB9 0xE4)
   c. Send 72 clock cycles on SCK
   d. Pull CSB high
3. Data transmitted to slave during the STCOMM command is stored in the COMM register. Use the RDCOMM command to retrieve the data.
   a. Pull CSB low
   b. Send RDCOMM command (0x07 0x22) and its PEC (0x32 0xD6)
   c. Read COMM0-COMM5 and the PEC for the 6 bytes of data. The read back data in this example would look like:
      COMM0 = 0x755F, COMM1 = 0x7AAF, COMM2 = 7CCF, PEC = 0xF2BA
   d. Pull CSB high

Note: If the slave returns data, this data will be placed in COMM0-COMM5.

Figure 27 shows the activity on GPIO3 (CSBM), GPIO5 (SCKM) and GPIO4 (SDOM) ports of SPI master for 72 clock cycles during the STCOMM command in the above example.

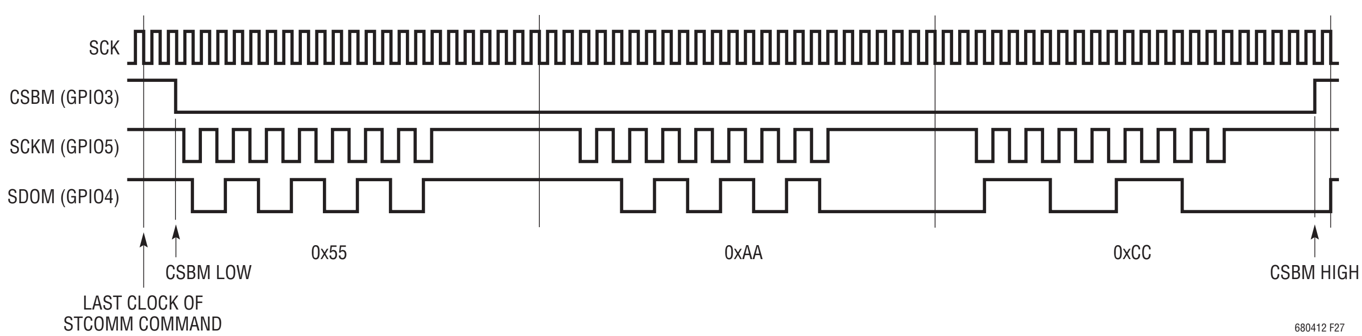


Figure 27. LTC6804 SPI Communication Example

APPLICATIONS INFORMATION

SIMPLE LINEAR REGULATOR

The LTC6804 draws most of its power from the V_{REG} input pin. 5V ±0.5V should be applied to V_{REG}. A regulated DC/DC converter can power V_{REG} directly, or the DRIVE pin may be used to form a discrete regulator with the addition of a few external components. When active, the DRIVE output pin provides a low current 5.6V output that can be buffered using a discrete NPN transistor, as shown in Figure 28. The collector power for the NPN can come from any potential of 6V or more above V^-, including the cells being monitored or an unregulated converter supply. A 100Ω/100nF RC decoupling network is recommended for the collector power connection to protect the NPN from transients. The emitter of the NPN should be bypassed with a 1µF capacitor. Larger capacitor values should be avoided because they increase the wake-up time of the LTC6804. Some attention to the thermal characteristic of the NPN is needed, as there can be significant heating with a high collector voltage. The CZT5551 shown is a SOT-223 part that provides good design margin.

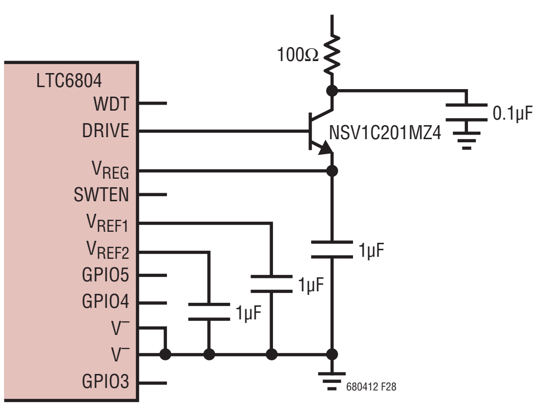


Figure 28. Simple V_{REG} Power Source Using NPN Pass Transistor

IMPROVED REGULATOR POWER EFFICIENCY

To minimize power consumption within the LTC6804, the current drawn on the V^+ pin has been designed to be very small (500µA). The voltage on the V^+ pin must be at least as high as the top cell to provide accurate measurement. The V^+ and V_{REG} pins can be unpowered to provide an exceptionally low battery drain shutdown mode. In many applications, the V^+ will be permanently connected to the top cell potential through a decoupling RC to protect against transients (100Ω/100nF is recommended).

For better running efficiency when powering from the cell stack, the V_{REG} may be powered from a buck converter rather than the NPN pass transistor. An ideal circuit for this is based on the LT3990 as shown in Figure 29. A 1k resistor should be used in series with the input to prevent inrush current when connecting to the stack and to reduce conducted EMI. The EN/UVLO pin should be connected to DRIVE so that the converter sleeps along with the LTC6804.

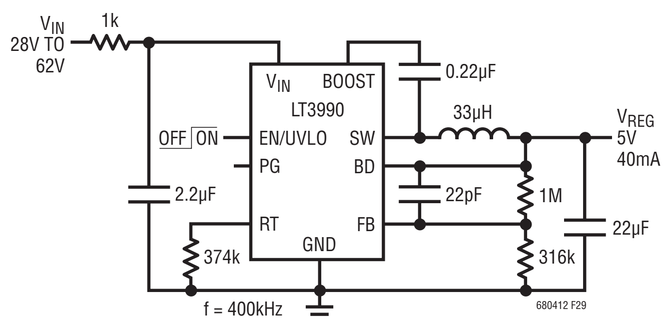


Figure 29. V_{REG} Powered from Cell Stack with High Efficiency

APPLICATIONS INFORMATION

FULLY ISOLATED POWER

A simple DC/DC flyback converter can provide isolated power for an LTC6804 from a remote 12V power source as shown in Figure 30. This circuit, along with the isoSPI transformer isolation, results in LTC6804 circuitry that is completely floating and uses almost no power from the batteries. Aside from reducing the amount of circuitry that operates at battery potential, such an arrangement prevents battery load imbalance.

READING EXTERNAL TEMPERATURE PROBES

Figure 31 shows the typical biasing circuit for a negative-temperature-coefficient (NTC) thermistor. The 10kΩ at 25°C is the most popular sensor value and the V_{REF2} output stage is designed to provide the current required to directly bias several of these probes. The biasing resistor is selected to correspond to the NTC value so the circuit will provide 1.5V at 25°C (V_{REF2} is 3V nominal). The overall circuit response is approximately –1%/°C in the range of typical cell temperatures, as shown in the chart of Figure 31 .

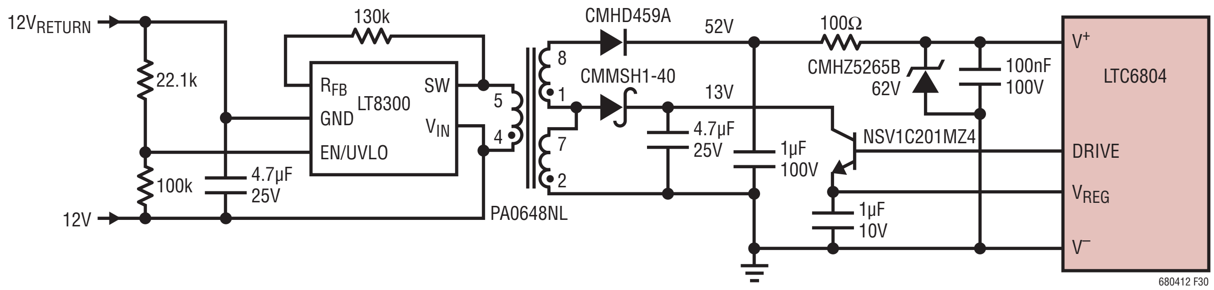


Figure 30. Powering LTC6804 from a Remote 12V Source

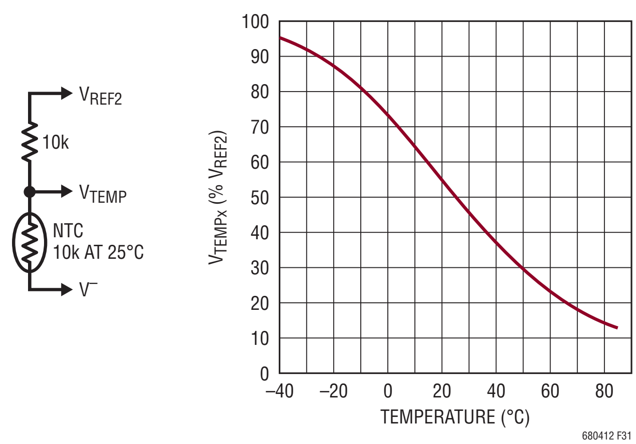


Figure 31. Typical Temperature Probe Circuit and Relative Output

APPLICATIONS INFORMATION

EXPANDING THE NUMBER OF AUXILIARY MEASUREMENTS

The LTC6804 provides five GPIO pins, each of which is capable of performing as an ADC input. In some applications there is need to measure more signals than this, so one means of supporting higher signal count is to add a MUX circuit such as shown in Figure 32. This circuit digitizes up to sixteen source signals using the GPIO1 ADC input and MUX control is provided by two other GPIO lines configured as an I^2C port. The buffer amplifier provides for fast settling of the selected signal to increase the usable conversion rate.

INTERNAL PROTECTION FEATURES

The LTC6804 incorporates various ESD safeguards to ensure a robust performance. An equivalent circuit showing the specific protection structures is shown in Figure 33. While pins 43 to 48 have different functionality for the -1 and -2 variants, the protection structure is the same. Zener-like suppressors are shown with their nominal clamp voltage, other diodes exhibit standard PN junction behavior.

FILTERING OF CELL AND GPIO INPUTS

The LTC6804 uses a delta-sigma ADC, which has delta-sigma modulator followed by a SINC3 finite impulse response (FIR) digital filter. This greatly reduces input filtering requirements. Furthermore, the programmable oversampling ratio allows the user to determine the best trade-off between measurement speed and filter cutoff frequency. Even with this high order lowpass filter, fast transient noise can still induce some residual noise in measurements, especially in the faster conversion modes. This can be minimized by adding an RC lowpass decoupling to each ADC input, which also helps reject potentially damaging high energy transients. Adding more than about 100Ω to the ADC inputs begins to introduce a systematic error in the measurement, which can be improved by raising the filter capacitance or mathematically compensating in software with a calibration procedure. For situations that demand the highest level of battery voltage ripple rejection, grounded capacitor filtering is recommended. This configuration has a series resistance and capacitors that decouple HF noise to V^-. In systems where noise is less

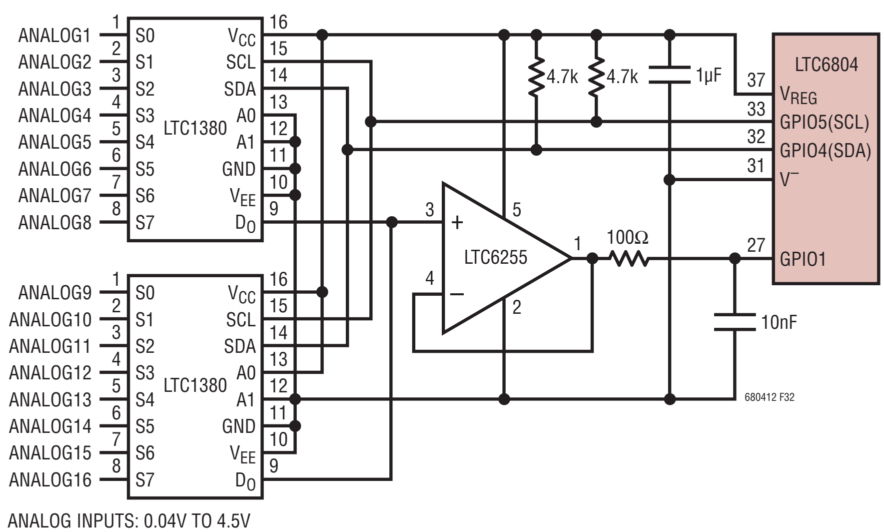
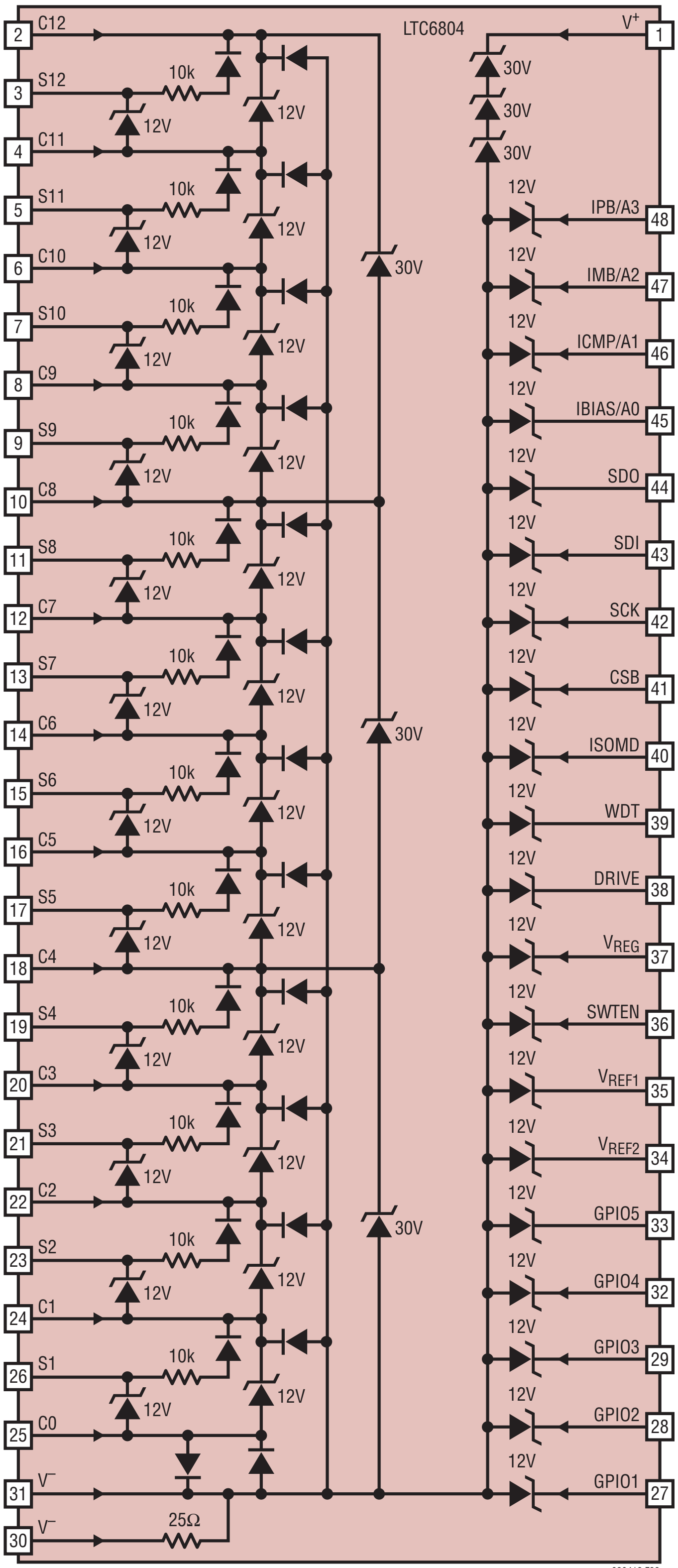


Figure 32. MUX Circuit Supports Sixteen Additional Analog Measurements

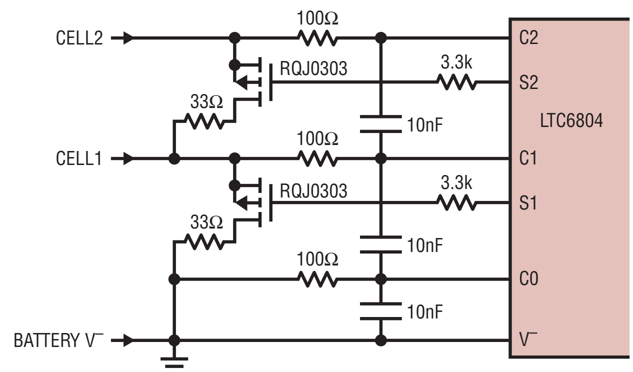
APPLICATIONS INFORMATION



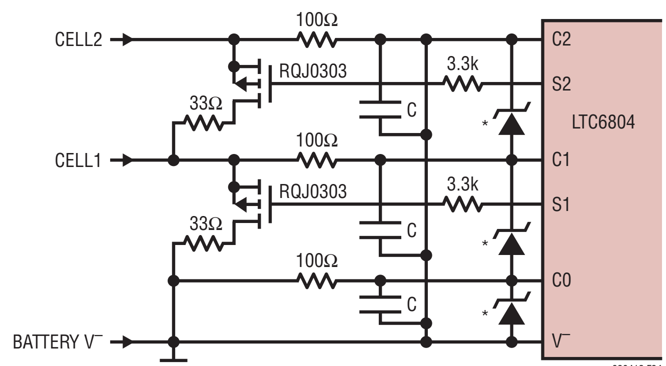
NOTE: NOT SHOWN ARE PN DIODES TO ALL OTHER PINS FROM PIN 31

Figure 33. Internal ESD Protection Structure of LTC6804

periodic or higher oversample rates are in use, a differential capacitor filter structure is adequate. In this configuration there are series resistors to each input, but the capacitors connect between the adjacent C pins. However, the differential capacitor sections interact. As a result, the filter response is less consistent and results in less attenuation than predicted by the RC, by approximately a decade. Note that the capacitors only see one cell of applied voltage (thus smaller and lower cost) and tend to distribute transient energy uniformly across the IC (reducing stress events on the internal protection structure). Figure 34 shows the two methods schematically. Basic ADC accuracy varies with R, C as shown in the Typical Performance curves, but error is minimized if R = 100Ω and C = 10nF. The GPIO pins will always use a grounded capacitor configuration because the measurements are all with respect to V⁻.



Differential Capacitor Filter



*6.8V ZENERS RECOMMENDED IF C > 100nF

Grounded Capacitor Filter

Figure 34. Input Filter Structure Configurations

APPLICATIONS INFORMATION

CELL BALANCING WITH INTERNAL MOSFETS

The S1 through S12 pins are used to balance battery cells. If one cell in a series becomes overcharged, an S output can be used to discharge the cell. Each S output has an internal N-channel MOSFET for discharging. The NMOS has a maximum on resistance of 20Ω. An external resistor should be connected in series with the NMOS to dissipate heat outside of the LTC6804 package as illustrated in Figure 35. It is still possible to use an RC to add additional filtering to cell voltage measurements but the filter R must remain small, typically around 10Ω to reduce the effect on the programmed balance current. When using the internal MOSFETs to discharge cells, the die temperature should be monitored. See Power Dissipation and Thermal Shutdown section.

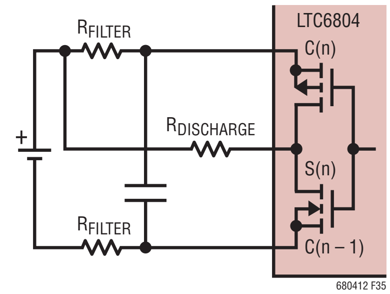


Figure 35. Internal Discharge Circuit

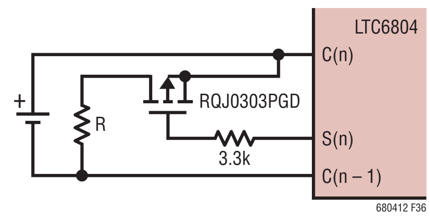


Figure 36. External Discharge Circuit

CELL BALANCING WITH EXTERNAL MOSFETS

The S outputs include an internal pull-up PMOS transistor. The S pins can act as digital outputs suitable for driving the gate of an external MOSFET. For applications requiring high battery discharge currents, connect a discrete PMOS switch device and suitable discharge resistor to the cell, and the gate terminal to the S output pin, as illustrated in Figure 36. Figure 34 shows external MOSFET circuits that include RC filtering.

DISCHARGE CONTROL DURING CELL MEASUREMENTS

If the discharge permited (DCP) command bit is high in a cell measurement command, then the S pin discharge states are not altered during the cell measurements. However, if the DCP bit is low, any discharge that is turned on will be turned off when the corresponding cell or adjacent cells are being measured. Table 47 illustrates this during an

Table 47. Discharge Control During an ADCV Command with DCP = 0

	CELL MEASUREMENT PERIODS						CELL CALIBRATION PERIODS					
	CELL1/7	CELL2/8	CELL3/9	CELL4/10	CELL5/11	CELL6/12	CELL1/7	CELL2/8	CELL3/9	CELL4/10	CELL5/11	CELL6/12
DISCHARGE PIN	t_0 to t_{1M}	t_{1M} to t_{2M}	t_{2M} to t_{3M}	t_{3M} to t_{4M}	t_{4M} to t_{5M}	t_{5M} to t_{6M}	t_{6M} to t_{1C}	t_{1C} to t_{2C}	t_{2C} to t_{3C}	t_{3C} to t_{4C}	t_{4C} to t_{5C}	t_{5C} to t_{6C}
S1	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF
S2	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON
S3	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON
S4	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
S5	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
S6	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
S7	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF
S8	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON
S9	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON
S10	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
S11	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
S12	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF

APPLICATIONS INFORMATION

ADCV command with DCP = 0. In this table, OFF implies that a discharge is forced off during that period even if the corresponding DCC[x] bit is high in the configuration register. ON implies that if the discharge is turned on, it will stay on during that period. Refer to Figure 3 for the timing of the ADCV command.

POWER DISSIPATION AND THERMAL SHUTDOWN

The internal MOSFETs connected to the pins S1 through S12 pins can be used to discharge battery cells. An external resistor should be used to limit the power dissipated by the MOSFETs. The maximum power dissipation in the MOSFETs is limited by the amount of heat that can be tolerated by the LTC6804. Excessive heat results in elevated die temperatures. Little or no degradation will be observed in the measurement accuracy for die temperatures up to 125°C. Damage may occur above 150°C, therefore the recommended maximum die temperature is 125°C. To protect the LTC6804 from damage due to overheating a thermal shutdown circuit is included. Overheating of the device can occur when dissipating significant power in the cell discharge switches. The thermal shutdown circuit is enabled whenever the device is not in sleep mode (see Modes of Operation). If the temperature detected on the device goes above approximately 150°C the configuration registers will be reset to default states turning off all discharge switches. When a thermal shutdown has occurred, the THSD bit in the status register group B will go high. The bit is cleared after a read operation of the status register group B. The bit can also be set using the CLRSTAT command. Since thermal shutdown interrupts normal operation, the internal temperature monitor should be used to determine when the device temperature is approaching unacceptable levels.

METHOD TO VERIFY BALANCING CIRCUITRY

The functionality of the discharge circuitry is best verified by cell measurements. Figure 37 shows an example using the LTC6804 battery monitor IC. The resistor between the battery and the source of the discharge MOSFET causes cell voltage measurements to decrease. The amount of measurement change depends on the resistor values and the MOSFET on resistance.

The following algorithm could be used in conjunction with Figure 37:

1. Measure all cells with no discharging (all S outputs off) and read and store the results.
2. Turn on S1 and S7
3. Measure C1-C0, C7-C6
4. Turn off S1 and S7
5. Turn on S2 and S8
6. Measure C2-C1, C8-C7
7. Turn off S2 and S8

…

14. Turn on S6 and S12
15. Measure C6-C5, C12-C11
16. Turn off S6 and S12
17. Read the voltage register group to get the results of steps 2 thru 16.
18. Compare new readings with old readings. Each cell voltage reading should have decreased by a fixed percentage set by R_{B1} and R_{B2} (Figure 37). The exact amount of decrease depends on the resistor values and MOSFET characteristics.

Improved PEC Calculation

The PEC allows the user to have confidence that the serial data read from the LTC6804 is valid and has not been corrupted by any external noise source. This is a critical feature for reliable communication and the LTC6804 requires that a PEC be calculated for all data being read from and written to the LTC6804. For this reason it is important to have an efficient method for calculating the PEC. The code below demonstrates a simple implementation of a lookup table derived PEC calculation method. There are two functions, the first function init_PEC15_Table() should only be called once when the microcontroller starts and will initialize a PEC15 table array called pec15Table[]. This table will be used in all future PEC calculations. The pec15 table can also be hard coded into the microcontroller rather than running the init_PEC15_Table() function at startup. The pec15() function calculates the PEC and will return the correct 15 bit PEC for byte arrays of any given length.

APPLICATIONS INFORMATION

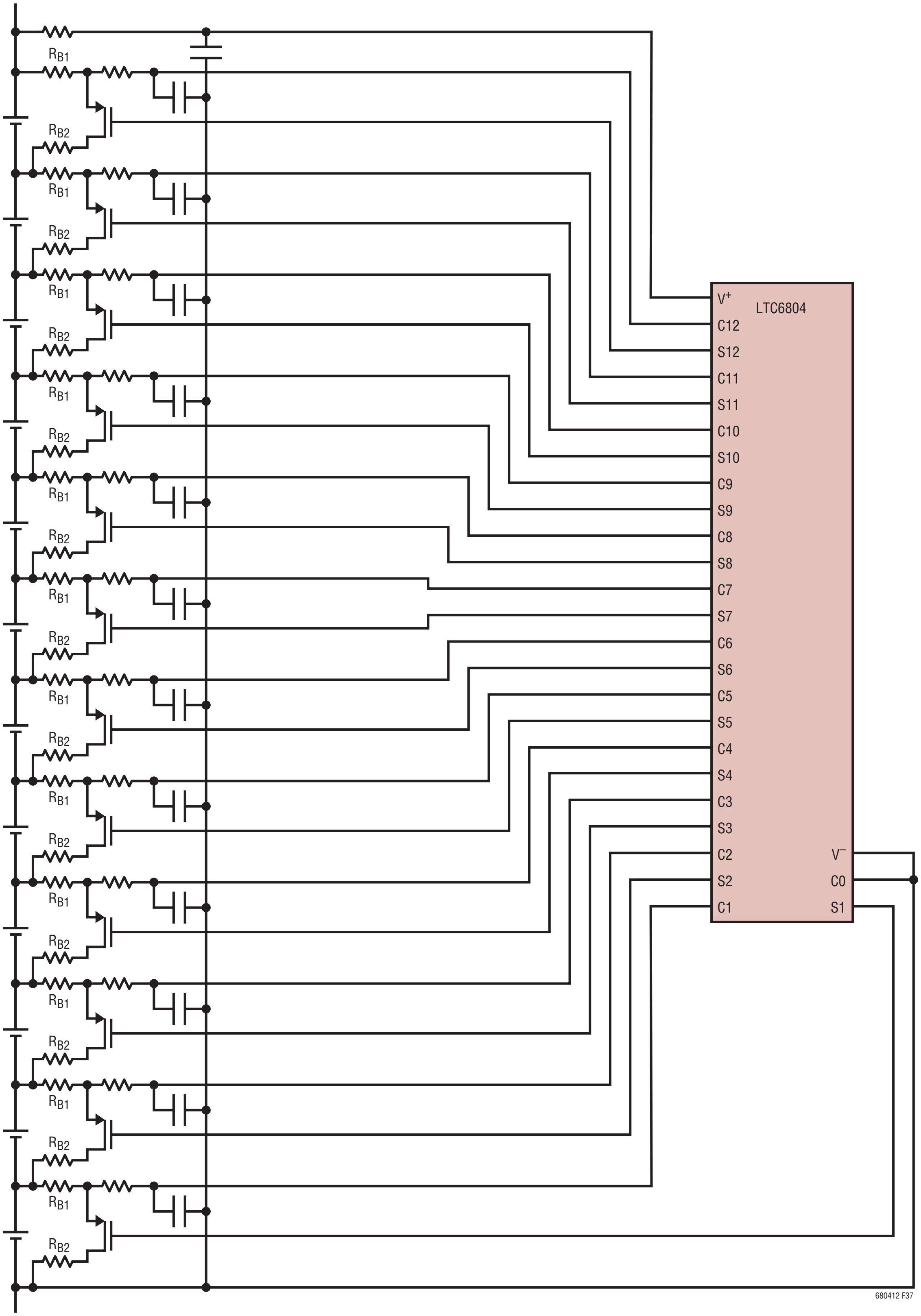


Figure 37. Balancing Self Test Circuit

APPLICATIONS INFORMATION

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/************************************
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OR OTHER TORTUOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR
PERFORMANCE OF THIS SOFTWARE.
********************************************************/


int16 pec15Table[256];
int16 CRC15_POLY = 0x4599;
void init_PEC15_Table()
{
    for (int i = 0; i < 256; i++)
    {
        remainder = i << 7;
        for (int bit = 8; bit > 0; --bit)
        {
            if (remainder & 0x4000)
            {
                remainder = ((remainder << 1));
                remainder = (remainder ^ CRC15poly)
            }
            else
            {
                remainder = ((remainder << 1));
            }
        }
        pec15Table[i] = remainder&0xFFFF;
    }
}

unsigned int16 pec15 (char *data , int len)
{
    int16 remainder,address;

    remainder = 16;//PEC seed
    for (int i = 0; i < len; i++)
    {
        address = ((remainder >> 7) ^ data[i]) & 0xff;//calculate PEC table address
        remainder = (remainder << 8 ) ^ pec15Table[address];
    }
    return (remainder*2);//The CRC15 has a 0 in the LSB so the final value must be multiplied by 2
}
```

APPLICATIONS INFORMATION

CURRENT MEASUREMENT WITH A HALL EFFECT SENSOR

The LTC6804 auxiliary ADC inputs (GPIO pins) may be used for any analog signal, including those from various active sensors that generate a compatible voltage. One such example that may be useful in a battery management setting is the capture of battery current. Hall-effect sensors are popular for measuring large battery currents since the technology provides a non-contact, low power dissipation solution. Figure 38 shows schematically a typical Hall sensor that produces two outputs that proportion to the V_{CC} provided. The sensor is powered from a 5V source and produces analog outputs that are connected to GPIO pins or inputs of the MUX application shown in Figure 32. The use of GPIO1 and GPIO2 as the ADC inputs has the possibility of being digitized within the same conversion sequence as the cell inputs (using the ADCVAX command), thus synchronizing cell voltage and cell current measurements.

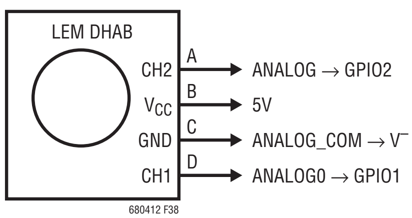
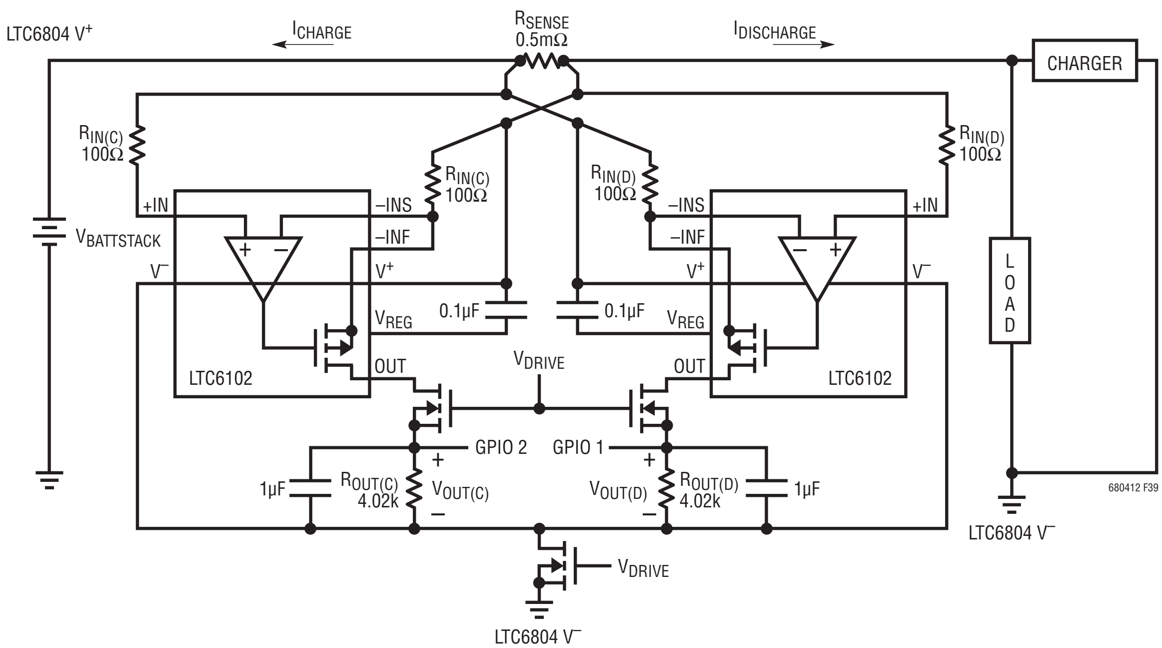


Figure 38. Interfacing a Typical Hall-Effect Battery Current Sensor to Auxiliary ADC Inputs

CURRENT MEASUREMENT WITH A SHUNT RESISTOR

It is possible to measure the battery current on the LTC6804 GPIO pins with a high performance current sense amplifier and a shunt. Figure 39 shows 2 LTC6102s being used to measure the discharge and charge currents on a 12-cell battery stack. To achieve a large dynamic range while maintaining a high level of accuracy the LTC6102 is required. The circuit shown is able to accurately measure ±200Amps to 0.1Amps. The offset of the LTC6102 will only contribute a 20mA error. To maintain a very low sleep current the V_{DRIVE} is used to disable the LTC6102 circuits so that they draw no current when the LTC6804 goes to sleep.



$$\text{DISCHARGING: } V_{OUT\ D} = I_{DISCHARGE} \bullet R_{SENSE} \left(\frac{R_{OUT(D)}}{R_{IN(D)}}\right) \text{ WHEN } I_{DISCHARGE} \geq 0$$

$$\text{CHARGING: } V_{OUT\ C} = I_{CHARGE} \bullet R_{SENSE} \left(\frac{R_{OUT(C)}}{R_{IN(C)}}\right) \text{ WHEN } I_{CHARGE} \geq 0$$

Figure 39. Monitoring Charge and Discharge Currents with a LTC6102

APPLICATIONS INFORMATION

USING THE LTC6804 WITH LESS THAN 12 CELLS

If the LTC6804 is powered by the battery stack, the minimum number of cells that can be monitored by the LTC6804 is governed by the supply voltage requirements of the LTC6804. The sum of the cell voltages must be at least 11V to properly bias the LTC6804. Figure 40 shows an example of the LTC6804 when used to monitor eight cells with best cell measurement synchronization. The 12 cells monitored by the LTC6804 are split into two groups of 6 cells and are measured using two internal multiplexers and two ADCs. To optimize measurement synchronization in applications with less than 12 Cells the unused C pins should be equally distributed between the top of the second mux (C12) and the top of the first mux (C6). If there are an odd number of cells being used, the top mux should have fewer cells connected. The unused cell channels should be tied to the other unused channels on the same mux and then connected to the battery stack through a 100Ω resistor. The unused inputs will result in a reading of 0V for those cells channels. It is also acceptable to connect in the conventional sequence with all unused cell inputs at the top.

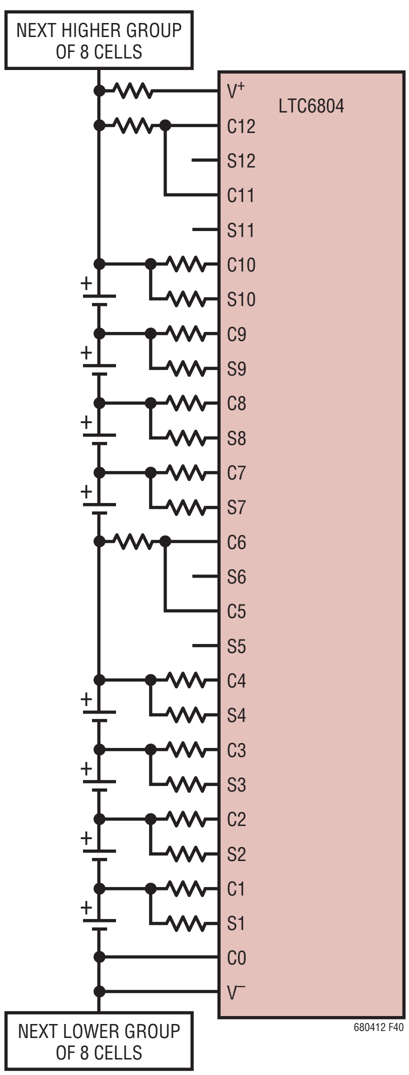


Figure 40. 8 Cell Connection Scheme

CONNECTING MULTIPLE LTC6804-1 ON THE SAME PCB

When connecting multiple LTC6804-1 devices on the same PCB, only a single transformer is required between the LTC6804-1 isoSPI ports. With multiple LTC6804-1 devices on the same PCB, the noise rejection requirements are significantly lower and the isolation requirements are simplified. For this reason, a single transformer should be adequate to provide the required isolation and noise rejection between ICs on the battery stack. Figure 41 shows an example application that has multiple LTC6804-1s on the same PCB, communicating to the bottom MCU through a LTC6820.

CONNECTING A MCU TO AN LTC6804-1 WITH AN isoSPI DATA LINK

A separate device, the LTC6820, will convert standard 4-wire SPI into a 2-wire isoSPI link that can communicate directly with the LTC6804. An example is shown in Figure 42. The LTC6820 can be used in applications to easily provide isolation between the controller and the stack of LTC6804s. The LTC6820 also enables system configurations that have the BMS controller at a remote location relative to the LTC6804 ICs and the battery pack.

CONFIGURING THE LTC6804-2 IN A MULTI-DROP isoSPI LINK

The addressing feature of the LTC6804-2 allows multiple devices to be connected to a single isoSPI master by multi-dropping them along one twisted pair essentially creating a large parallel SPI network. An example multi-drop system is shown in Figure 43 , the twisted pair should be terminated only at the beginning (master) and

Applications Information

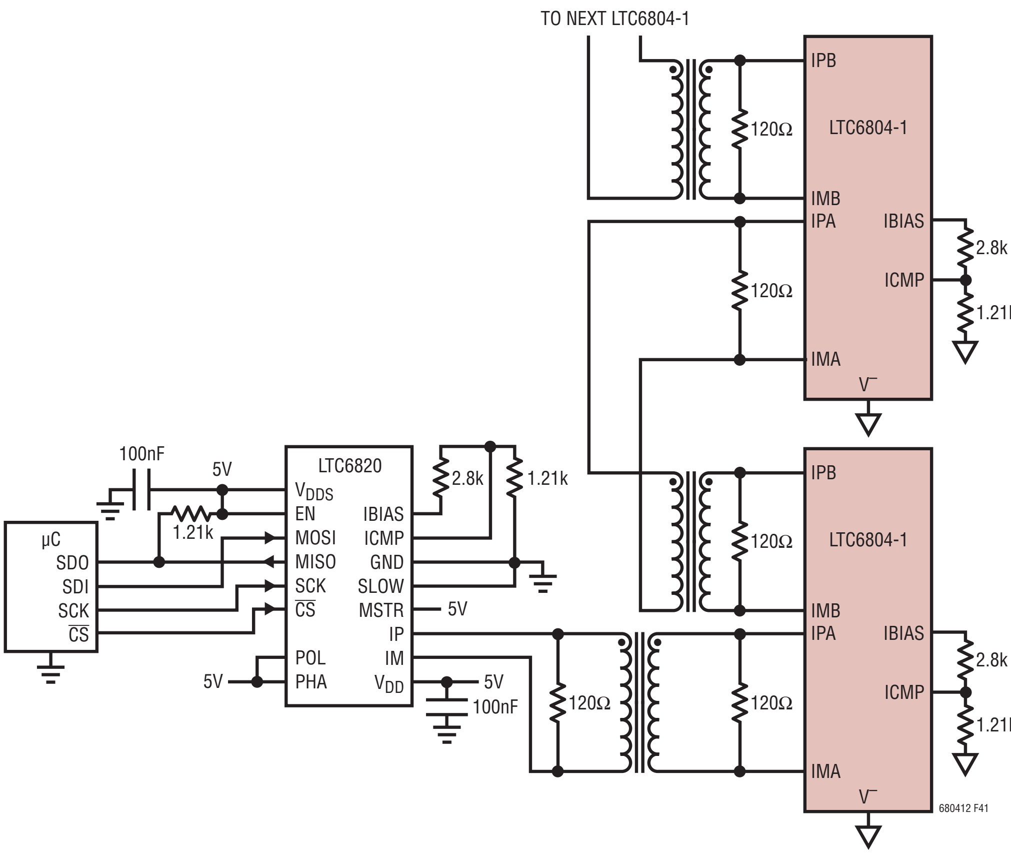


Figure 41. Connecting Multiple LTC6804-1 Devices on the Same PCB

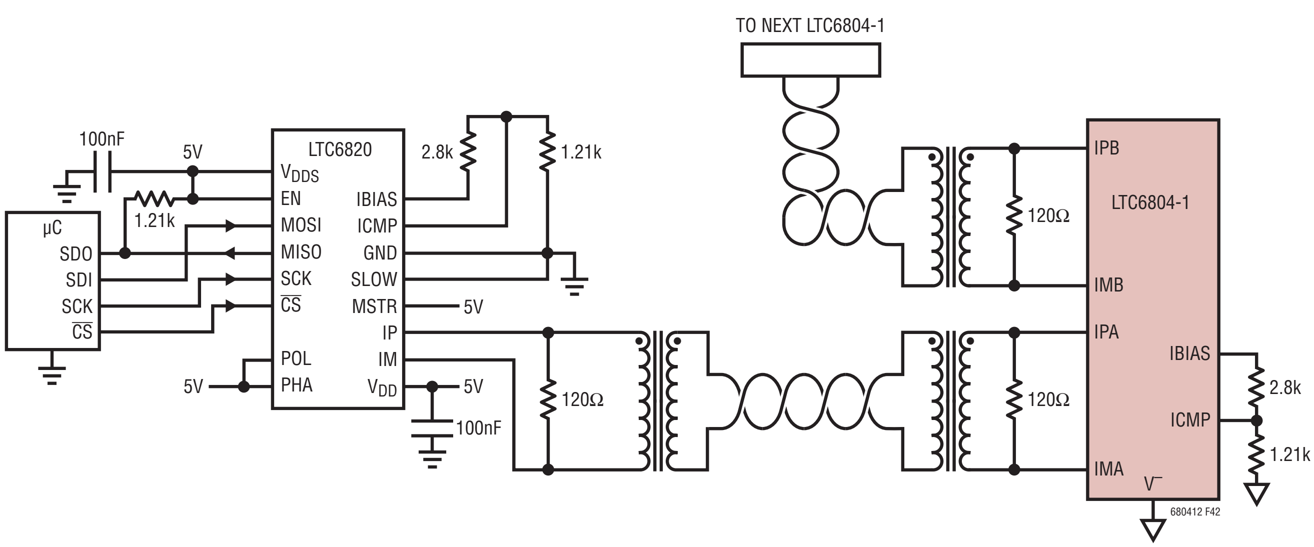


Figure 42. Interfacing an LTC6804-1 with an LTC6820 for Isolated SPI Control

APPLICATIONS INFORMATION

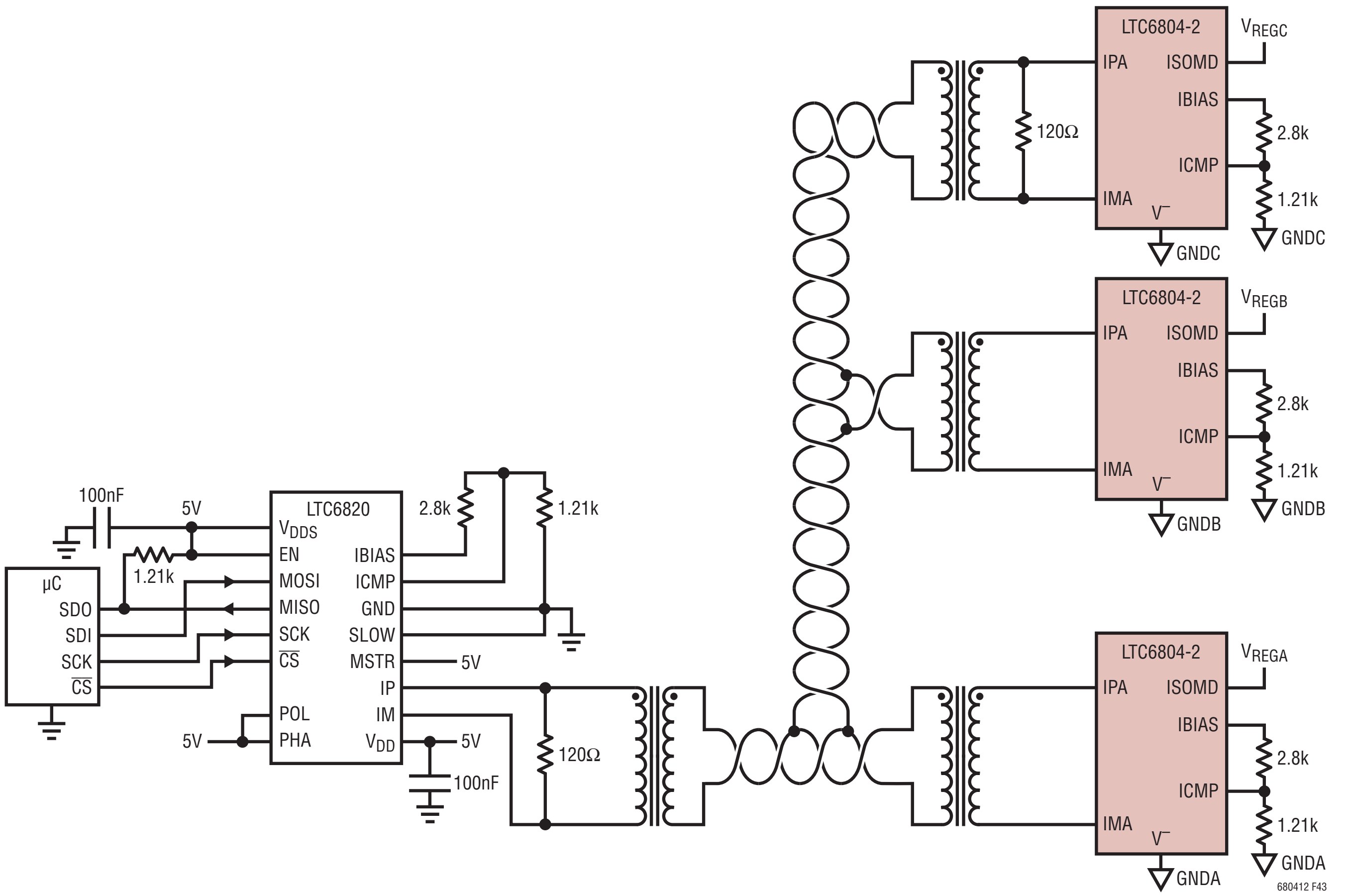


Figure 43. Connecting the LTC6804-2 in a Multi-Drop Configuration

the end. In between, the additional LTC6804-2's will be connected to stubs on the twisted pair. These stubs should be kept short, with as little capacitance as possible, to avoid degrading the termination along the isoSPI wiring. When a LTC6804-2 is not addressed, it will not transmit data pulses. This eliminates the possibility for collisions, as only the addressed device will ever be returning data to the master. The standard filtering circuits and layout guidelines outlined in the EMC section should be followed in multi drop networks.

TRANSFORMER SELECTION GUIDE

As shown in Figure 44, a transformer or a pair of transformers are used to isolate the isoSPI signals between two isoSPI ports. The isoSPI signals have programmable pulse amplitudes up to 1.6V and pulse widths of 50ns and 150ns. To meet these requirements, choose a transformer having a magnetizing inductance ranging from 50µH to 350µH, and a 1:1 turns ratio. Minimizing transformer insertion loss will reduce required transmit power; generally an insertion loss of less than –1.5dB is recommended. To optimize common mode noise rejection, choose a center tapped transformer or a transformer with an integrated common mode choke as show in Figure 45. The center tap should be tied to a 27pF or smaller capacitor (larger will restrict the driver's ability to set the common mode voltage). If the transformer has both a center tap and common mode choke on the primary side, a larger 100pF capacitor may be used. Table 48 shows a recommended list of transformers for use with the LTC6804. 10/100BaseTX Ethernet transformers are inexpensive and work very well in this application. Ethernet transformers have an added benefit in that they normally have common mode chokes built in improving their common mode rejection versus other transformers.

APPLICATIONS INFORMATION

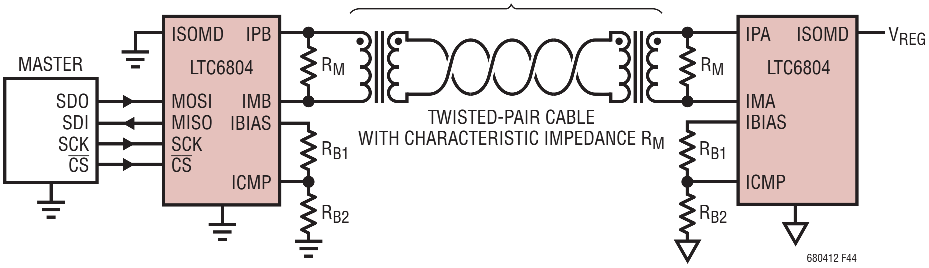


Figure 44. isoSPI Circuit

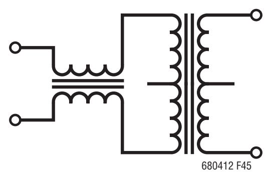


Figure 45. Transformer with Common Mode Choke

Table 47. Recommended Transformers

MANUFACTURER	PART NUMBER	ISOLATION VOLTAGE	TURNS RATIO	TEMPERATURE RANGE	CM CHOKE	CENTER TAP
Halo	TG110-AEX50N5LF	$1500V_{RMS}$	1:1	–45°C to 125°C	Yes	Yes
Halo	TG110-AE050N5LF	$1500V_{RMS}$	1:1	–45°C to 85°C	Yes	Yes
Halo	TGR01-6506V6NL	$3000V_{RMS}$	1:1	–40°C to 105°C	No	No
Pulse	PE-68386NL	1500VDC	1:1	–40°C to 130°C	No	No
Pulse	HX1188NL	$1500V_{RMS}$	1:1	–40°C to 85°C	Yes	Yes
Würth	7490100111	$1500V_{RMS}$	1:1	–40°C to 105°C	Yes	Yes
Würth	750340848	$3750V_{RMS}$	1:1	–40°C to 105°C	No	No

Capacitive Isolation Barrier

In some applications two LTC6804s can be monitoring the same group of batteries for redundancy or two strings of batteries connected in parallel. In these applications both of the LTC6804s will be at the same common mode voltage so the high CMRR of the transformers may not be required. In this situation an alternative to transformers is to use capacitors as the isolation barrier. The use of capacitors is suitable for low cost, isolated signaling over short distances (1 meter or less) that do not require high noise rejection. The capacitors will provide galvanic isolation, but no common mode rejection. This option uses the drivers in a different way, by using pull up resistors to maintain the common mode voltage near V_{REG}, only the sinking drive current has any effect. Figure 46 shows an example circuit using a capacitive isolation barrier capable of driving 1 meter of cable.

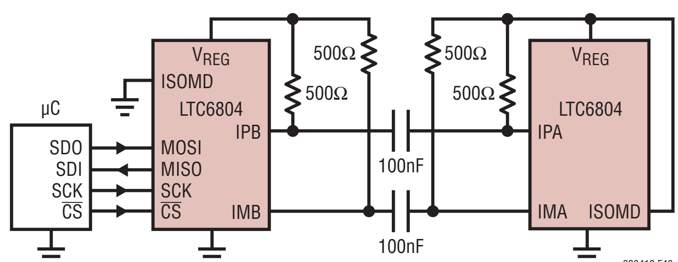


Figure 46. Capacitor Isolation Barrier

isoSPI Setup

The LTC6804 allows the isoSPI link in each application to be optimized for power consumption or for noise immunity. The power and noise immunity of an isoSPI system is determined by the programmed I_B current. The I_B current can range from 100µA to 1mA. A low I_B reduces the isoSPI power consumption in the READY and ACTIVE states, while a high I_B increases the amplitude of the differential signal

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voltage V_A across the matching termination resistor, R_M. I_B is programmed by the sum of the R_{B1} and R_{B2} resistors connected between the IBIAS pin and GND as shown in Figure 44. For most applications setting I_B to 0.5mA is a good compromise between power consumption and noise immunity. Using this I_B setting with a 1:1 transformer and $R_M = 120\Omega$, R_{B1} should be set to 2.8k and R_{B2} set to 1.2k. In a typical CAT5 twisted pair these settings will allow for communication up to 50m. For applications that require cables longer than 50m it is recommended to increase the I_B to 1mA. This compensates for the increased insertion loss in the cable and maintains high noise immunity. So when using cables over 50m and, again, using a transformer with a 1:1 turns ratio and $R_M = 120\Omega$, R_{B1} would be 1.4k and R_{B2} would be 600Ω. Other I_B settings can be used to reduce power consumption or increase the noise immunity as required by the application. In these cases when setting threshold voltage V_{ICMP} and choosing R_{B1} and R_{B2} resistor values the following rules should be used:

For cables under 50m:

$I_B = 0.5mA$

$V_A = (20 \bullet I_B) \bullet (R_M/2)$

$V_{TCMP} = ½ \bullet V_A$

$V_{ICMP} = 2 \bullet V_{TCMP}$

$R_{B2} = V_{ICMP}/I_B$

$R_{B1} = (2/I_B) – R_{B2}$

For cables over 50m:

$I_B = 1mA$

$V_A = (20 \bullet I_B) \bullet (R_M/2)$

$V_{TCMP} = 1/4 \bullet V_A$

$V_{ICMP} = 2 \bullet V_{TCMP}$

$R_{B2} = V_{ICMP}/I_B$

$R_{B1} = (2/I_B) – R_{B2}$

The maximum data rate of an isoSPI link is determined by the length of the cable used. For cables 10 meters or less the maximum 1MHz SPI clock frequency is possible. As the length of the cable increases the maximum possible SPI clock rate decreases. This is a result of the increased propagation delays through the cable creating possible timing violations. Figure 47 shows how the maximum data rate is reduced as the cable length increases when using a CAT 5 twisted pair.

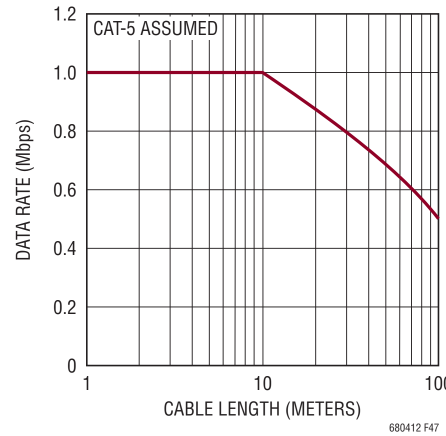

Figure 47. Data Rate vs Cable Length

Cable delay affects three timing specifications, t_{CLK}, t_6 and t_7. In the Electrical Characteristics table, each is derated by 100ns to allow for 50ns of cable delay. For longer cables, the minimum timing parameters may be calculated as shown below:

t_{CLK}, t_6 and $t_7 > 0.9µs + 2 \bullet t_{CABLE}$

EMC

For the best electromagnetic compatibility (EMC) performance, it is recommended to use one of the circuits in Figures 48 and 49. The center tap of the transformer should be bypassed with a 100pF capacitor. The center tap capacitor will help attenuate common mode signals. Large center tap capacitors greater than 100pF should be avoided as they will prevent the isoSPI transmitters common mode voltage from settling. If a transformer without a center tap is used, the termination resistor should be split into two equal halves and connected in series across the IP and DM lines. The center of the two resistors should be bypassed with a capacitor as shown in Figure 49. To improve common mode current rejection a common mode choke should also be placed in series with the IP and IM lines of the LTC6804. The common mode choke will both increase EMI immunity and reduce EMI emission. When choosing a common mode choke, the differential mode impedance should be 20Ω or less for signals 50MHz and below. Common mode chokes similar to what is used in Ethernet applications are recommended.

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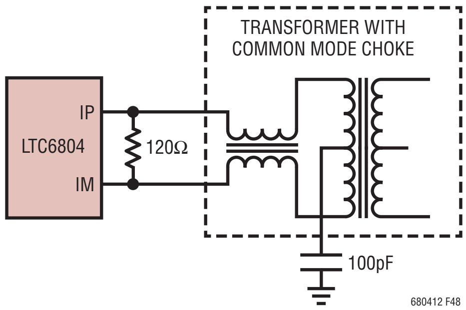


Figure 48. Recommended isoSPI Circuit for Best EMC Performance

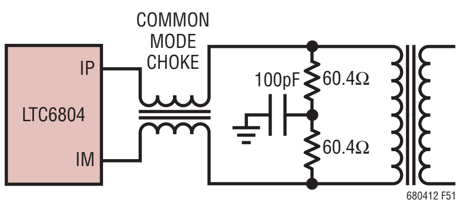


Figure 49. Recommended isoSPI Circuit for Best EMC Performance when Using a Transformer without a Center Tap

Table 49. Recommended Common Mode Chokes

MANUFACTURER	PART NUMBER
TDK	ACT45B-220-2P
Murata	DLW43SH510XK2

Layout of the isoSPI signal lines also plays a significant role in maximizing the immunity of a circuit. The following layout guidelines should be followed:

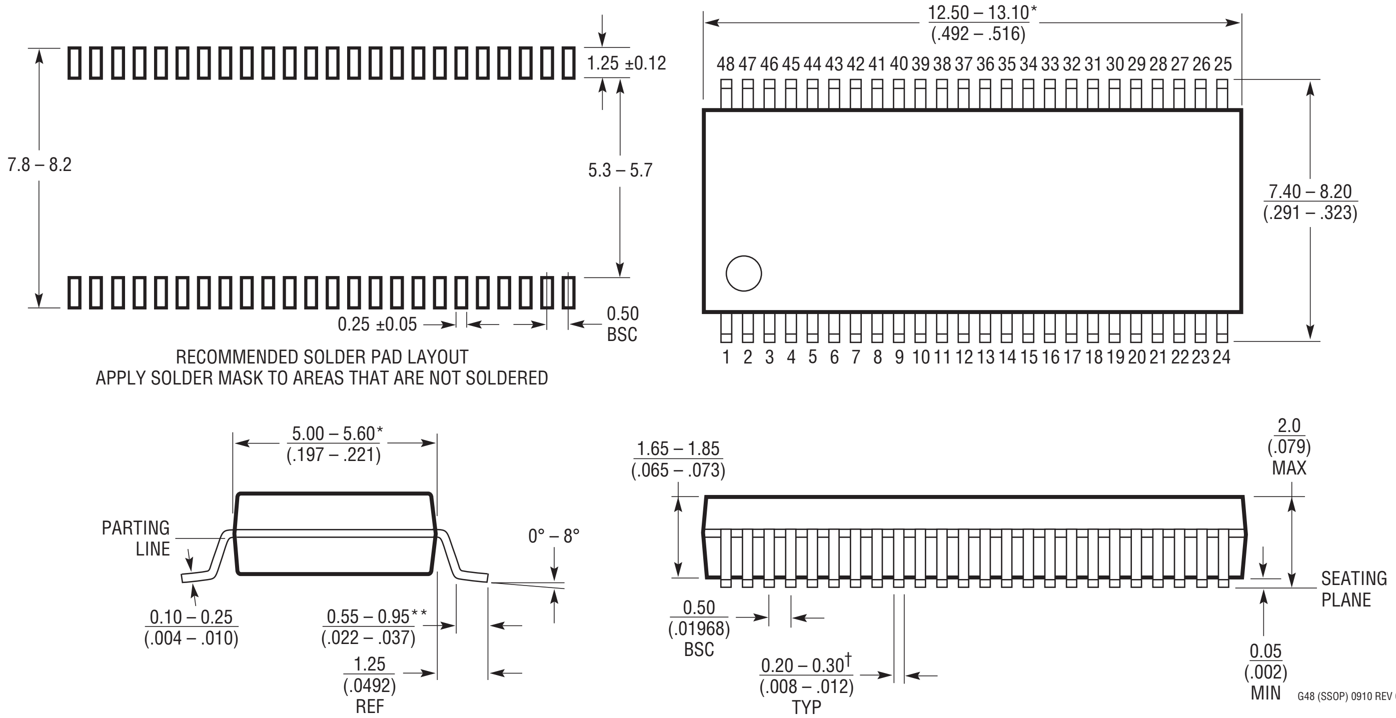
1. The transformer should be placed as close to the isoSPI cable connector as possible. The distance should be kept less than 2cm. The LTC6804 should be placed at least 1cm to 2cm away from the transformer to help isolate the IC from magnetic field coupling.
2. On the top component layer, no ground plane should be placed under the transformer, the isoSPI connector, or in between the transformer and the connector.
3. The isoSPI signal traces should be isolated from surrounding circuits and traces by ground metal or space. No traces should cross the isoSPI signal lines, unless separated by a ground plane on an inner layer.

The isoSPI drive currents are programmable and allow for a trade-off between power consumption and noise immunity. The noise immunity of the LTC6804 has been evaluated using a bulk current injection (BCI) test. The BCI test injects current into the twisted-pair lines at set levels over a frequency range of 1MHz to 400MHz. With the minimum I_B current, 100µA, the isoSPI serial link was capable of passing a 40mA BCI test with no bit errors. A 40mA BCI test level is sufficient for industrial applications. Automotive applications have a much higher BCI requirement so the LTC6804 IB is set to 1mA, the maximum power level. The isoSPI system is capable of passing a 200mA BCI test with no transmitted bit errors. The 200mA test level is typical for automotive requirements.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

G Package
48-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1887 Rev Ø)

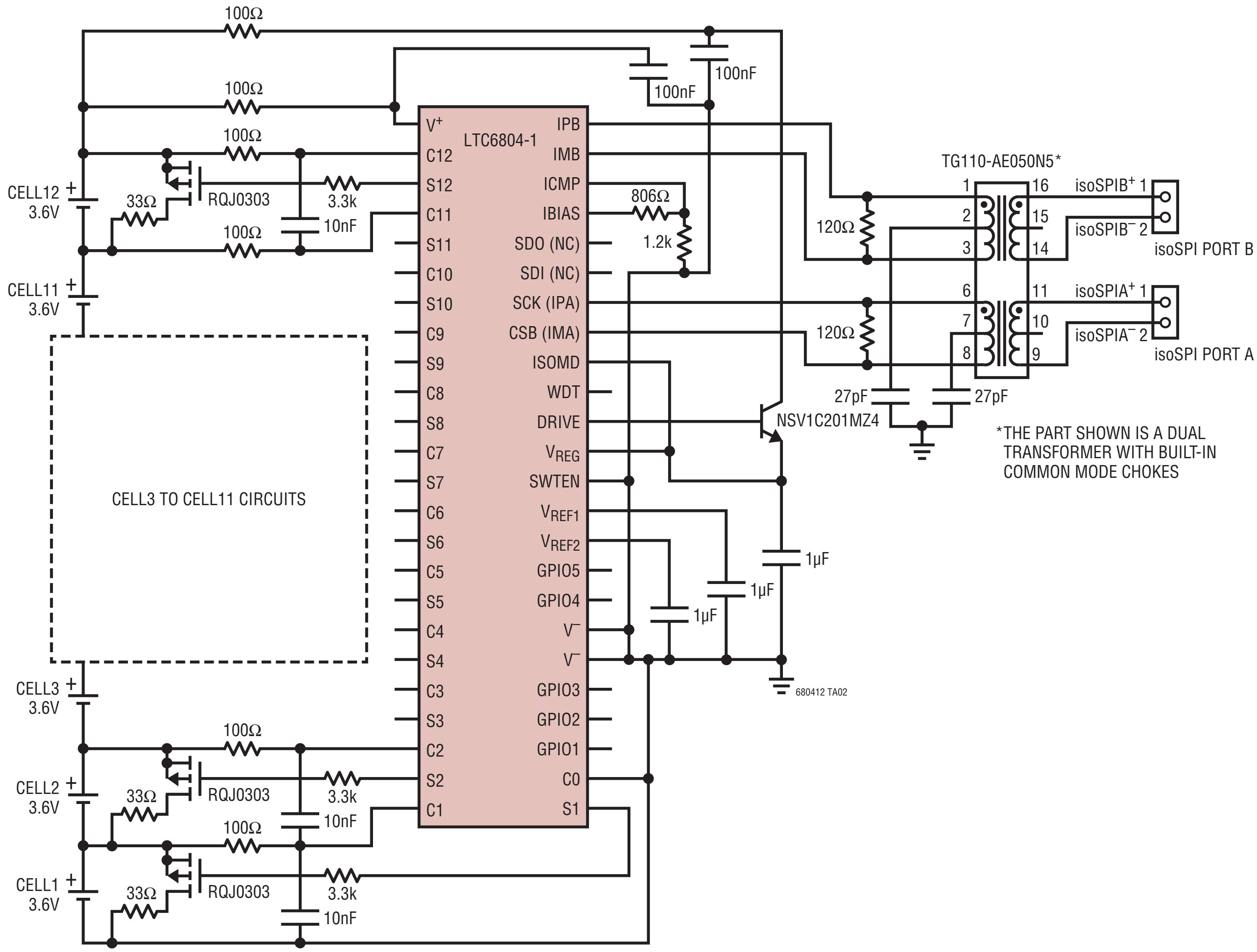


NOTE:
1.DRAWING IS NOT A JEDEC OUTLINE
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE IN MILLIMETERS / (INCHES)
4. DRAWING NOT TO SCALE
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH SHALL NOT EXCEED .15mm PER SIDE
**LENGTH OF LEAD FOR SOLDERRING TO A SUBSTRATE
†THE MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS DO NOT EXCEED 0.13mm PER SIDE

TYPICAL APPLICATION

Basic 12-Cell Monitor with isoSPI Daisy Chain



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6801	Independent Multicell Battery Stack Fault Monitor	Monitors Up to 12 Series-Connected Battery Cells for Undervoltage or Overvoltage. Companion to LTC6802, LTC6803 and LTC6804
LTC6802	Precision Multicell Battery Stack Monitor	1st Generation: Superseded by the LTC6804 and LTC6803 for New Designs
LTC6803	Precision Multicell Battery Stack Monitor	2nd Generation: Functionally Enhanced and Pin Compatible to the LTC6802
LTC6820	Isolated Bidirectional Communications Interface for SPI	Provides an Isolated Interface for SPI Communication Up to 100 Meters, Using a Twisted Pair. Companion to the LTC6804
LTC3300	High Efficiency Bidirectional Multicell Battery Balancer	Bidirectional Synchronous Flyback Balancing of Up to 6 Li-Ion or LiFeP04 Cells in Series. Up to 10A Balancing Current (Set by External Components). Bidirectional Architecture Minimizes Balancing Time and Power Dissipation. Up to 92% Charge Transfer Efficiency. 48-Lead Exposed Pad QFN and LQFP Packages

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