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HMC614LP4 / 614LP4E

RMS & Peak to Average Power Detector 0.1 - 3.9 GHz

Typical Applications

The HMC614LP4(E) is ideal for:

- Log –> Root-Mean-Square (RMS) Conversion
- Received Signal Strength Indication (RSSI)
- Transmitter Signal Strength Indication (TSSI)
- RF Power Amplifier Efficiency Control
- Receiver Automatic Gain Control
- Transmitter Power Control

Features

IPWR Output: Instantaneous Power, Crest Factor Measurement

RF Signal Wave shape & Crest Factor Independent

Supports Controller Mode [1]

±1 dB Detection Accuracy to 3.9 GHz

Input Dynamic Range: -57 dBm to +15 dBm

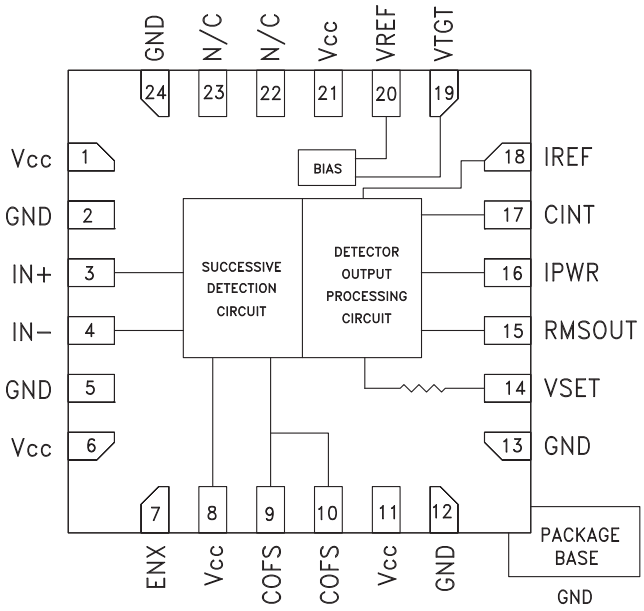
+5V Operation from -40°C to +85°C

Excellent Temperature Stability

Power-Down Mode

24 Lead 4x4mm QFN Package: 9 mm²

Functional Diagram



General Description

The HMC614LP4E RMS Power Detector is designed for RF power measurement, and control applications for frequencies up to 3.9 GHz. The detector provides a “true RMS” representation of any RF/IF input signal. The output is a temperature compensated, monotonic representation of real signal power, measured with a differential input sensing range of 71 dB.

The HMC614LP4E is ideally suited to those wide bandwidth, wide dynamic range applications, requiring repeatable measurement of real signal power; especially where RF/IF wave shape and/or crest factor change with time.

The HMC614LP4E provides an indication of the instantaneous or peak input power level normalized to the average input power level (peak to average power ratio) via the IPWR output. The capability of simultaneously measuring the instantaneous power (envelope power) and the average true RMS power provides crucial information about the RF input signal: Peak Power, Average Power, Peak to average power and RF Wave-Shape.

Electrical Specifications, T_A = +25C, Vcc= 5V, C_{INT} = 0.1 µF [2]

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	100	900	1900	2200	2700	3000	3500	3900	MHz
Dynamic Range (± 1 dB linearity Error) [1]	70	71	70	69	62	62	53	45	dB
Differential Input Configuration Logarithmic Slope									
Logarithmic Slope	37.5	37.5	37.6	38.1	39.6	41.0	44.5	50.2	mV/dB
Logarithmic Intercept	-69.8	-69.4	-68.8	-67.4	-63.6	-60.8	-54.8	-49.2	dBm
Max. input Power at ±1 dB Error	13	15	>15	>15	12	14	10	5	dBm
Min. input Power at ±1 dB Error	-57	-56	-55	-54	-50	-48	-43	-40	dBm
Deviation vs. Temperature: Deviation is measured from reference, which is the same CW Input @ 25° C									
Differential Input Interface with 1:1 Balun Transformer (Over Full Input Frequency Range)					±0.5				dB

[1] For more information regarding controller mode operation, please contact your Hittite sales representative or email sales@hittite.com

[2] Differential input drive via 1:1 balun transformer, VTGT = 2V unless otherwise noted.

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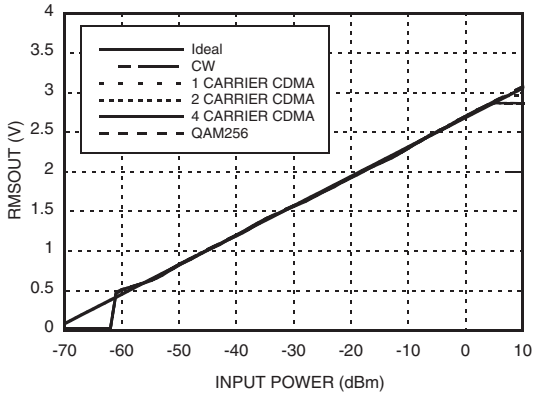
Table 2: Electrical Specifications [1]

Evaluation Kit (Diff. Input Config.) T_A = +25C, Vcc= 5V, C_{INT} = 0.1 µF Unless Otherwise Noted

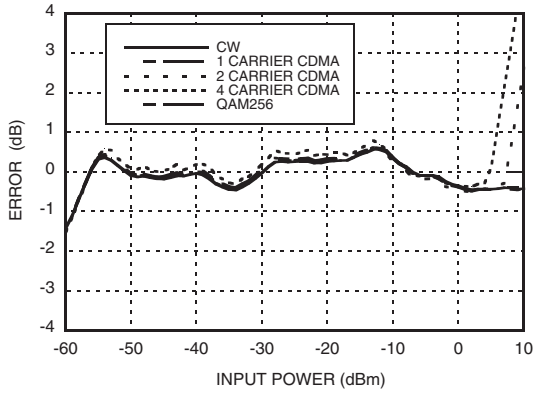
Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	900		1900		2700		3900		MHz
Average Modulation Deviation Error from CW Input [2]									
1 Carrier CDMA	0.02		0.06		0.08		0.03		dB
2 Carrier CDMA	0.02		0.05		0.11		0.02		dB
3 Carrier CDMA	0.15		0.16		0.23		0.16		dB
QAM256	0.01		0.03		0.05		0.01		dB
IPWR/IREF Outputs									
IPWR Output Voltage	with CW Input (average power= instantaneous power)								1.6V
IREF Output Voltage	Same termination resistance as IPWR								1.6V
IPWR Output Slope for Input Power Change Normalized to Average Power [3]	Vtgt = 2V								190 mV
	Vtgt = 1V								95 mV
IPWR Output Slope Variation with Temperature	from -40C to 85C								3%
IPWR Output Modulation BW	for 3 dB voltage drop in Output Swing								35 MHz

[1] Differential input drive via 1:1 balun transformer.
[2] Modulation data taken with VTGT = 1V
[3] IPWR = a(Pin(t)/Pave)+b, a is defined as IPWR Slope for input power change normalized to average power.

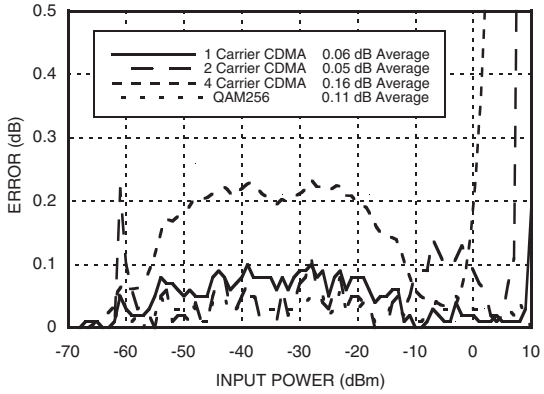
RMSOUT vs. Pin with Different Modulations @ 1900 MHz, VTGT= 1V



RMSOUT Error vs. Pin with Different Modulations @ 1900 MHz, VTGT= 1V



Absolute Error wrt to CW Response @ 1900 MHz for Different Modulation Schemes, VTGT= 1V



Absolute Error wrt to CW Response @ 1900 MHz for Different Modulation Schemes, VTGT= 2V

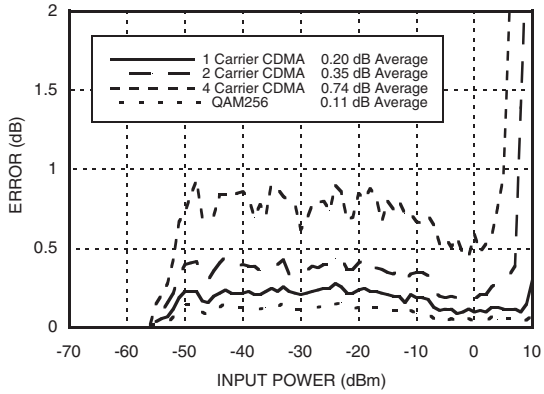


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Table 3: Electrical Specifications [3],

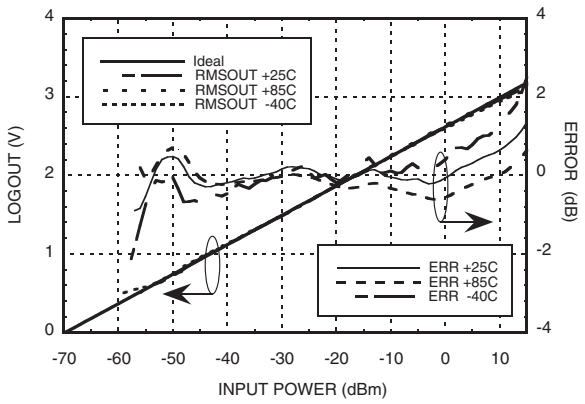
HMC610LP4E Evaluation Kit (Diff. Input Config.), TA = +25C, Vcc= +5V, C_{INT} = 0.1 µF, Unless Otherwise Noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential Input Configuration					
Input Network Return Loss [1]	[1]		>10		dB
Input Resistance between IN+ and IN-	Between pins 3 and 4		200		Ω
Input Voltage Range	$V_{DIFFIN} = V_{IN+} - V_{IN-}$			2.25	V
RMSOUT Output					
Output Voltage Range	RL = 1kΩ, CL = 4.7pF[2]		0.4 - 3.2		V
Source/Sink Current Compliance	RMSOUT held at VCC/2		8 / 0.35		mA
Max. Load Capacitance	With C_{INT} = 0				pF
Output Slew Rate (rise / fall)	With C_{INT} = 0, Cofs = 0		100 / 5		10^6 V/s
V_{SET} Input (Negative Feedback Terminal)					
Input Voltage Range [2]			0.4 - 3.2		V
Input Resistance			1		MΩ
V_{REF} Output (Reference Voltage)					
V_{REF} Output Voltage			2.95		V
V_{REF} Change	Over Full Temperature Range		20		mV
V_{TGT} Input (RMS Target Interface)					
Input Voltage Range				3.65	V
Input Resistance			1		MΩ
ENX Logic Input (Power Down Control)					
Input High Voltage	Standby Mode Active	3.9			V
Input Low Voltage	Normal Operation			1.2	V
Input High Current				1	µA
Input Low Current				1	µA
Input Capacitance			0.5		pF
Power Supply					
Supply Voltage		4.5	5	5.5	V
Supply Current with Pin = -70 dBm	Over Full Temperature Range		65	76	mA
Supply Current with Pin = 0 dBm	Over Full Temperature Range		83	95	mA
Standby Mode Supply Current	ENX = Hi		1		mA

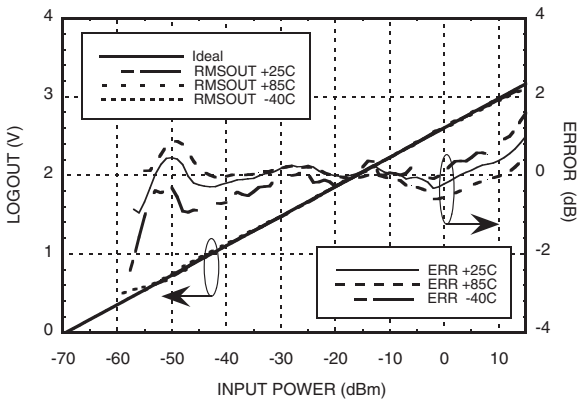
[1] Performance of differential input configuration is limited by balun. Balun used is MACOM ETC1-1-13 good over 4.5 MHz to 3000 MHz

[2] For nominal slope / intercept setting.

RMSOUT & Error vs. Pin @ 100 MHz [1]



RMSOUT & Error vs. Pin @ 900 MHz [1]



[1] CW Input Waveform

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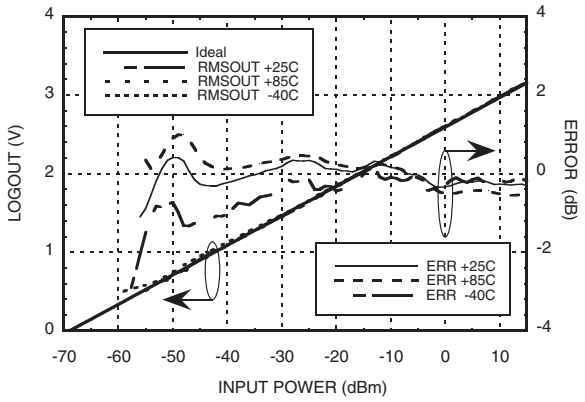
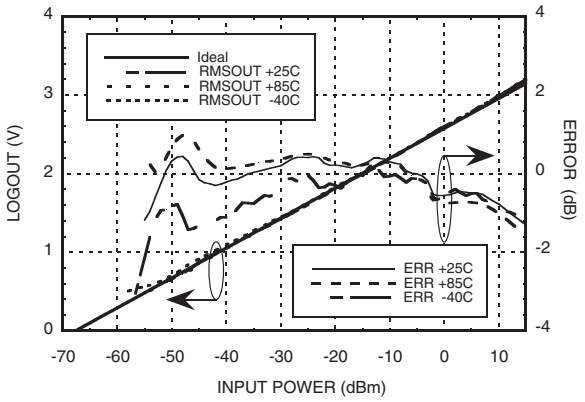
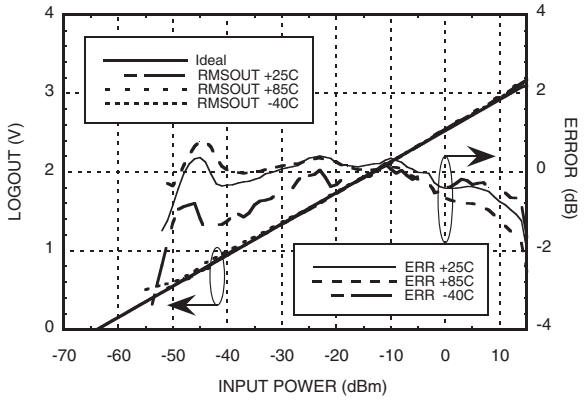
RMSOUT & Error vs. Pin @ 1900 MHz [1]



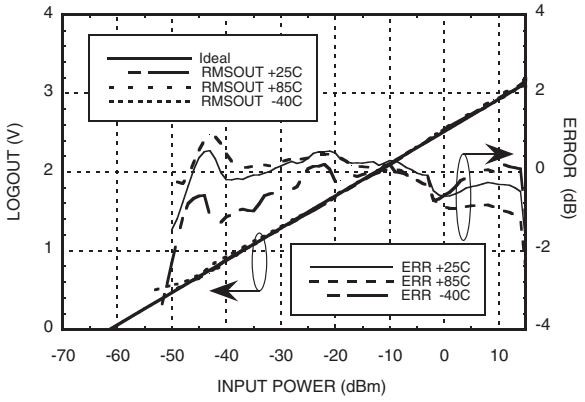
RMSOUT & Error vs. Pin @ 2200 MHz [1]



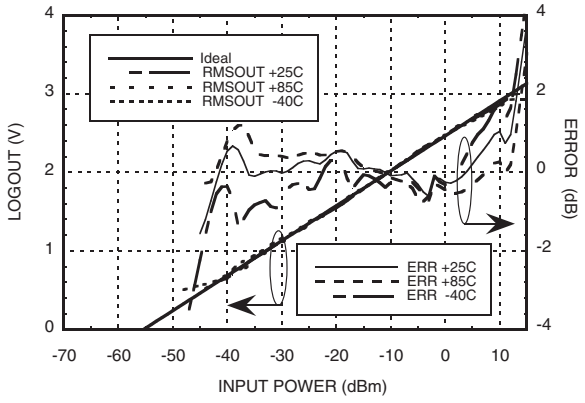
RMSOUT & Error vs. Pin @ 2700 MHz [1]



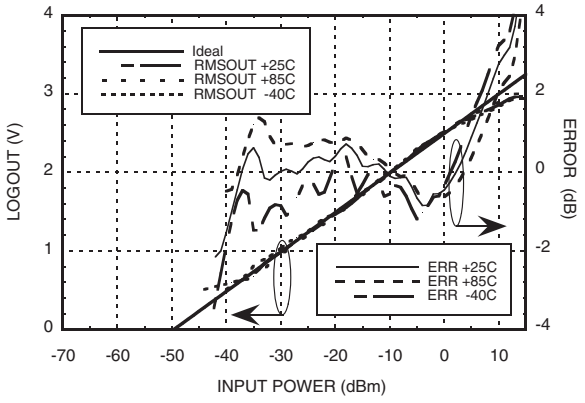
RMSOUT & Error vs. Pin @ 3000 MHz [1]



RMSOUT & Error vs. Pin @ 3500 MHz [1]



RMSOUT & Error vs. Pin @ 3900 MHz [1]



[1] CW Input Waveform

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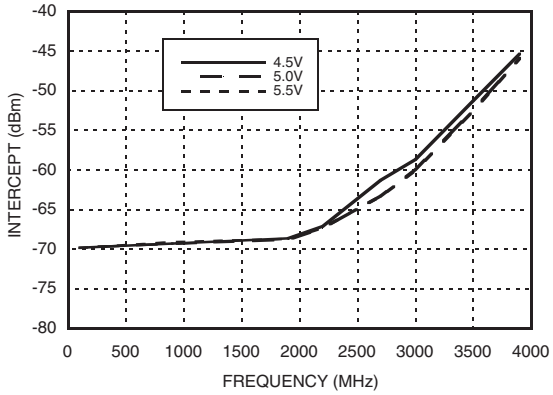
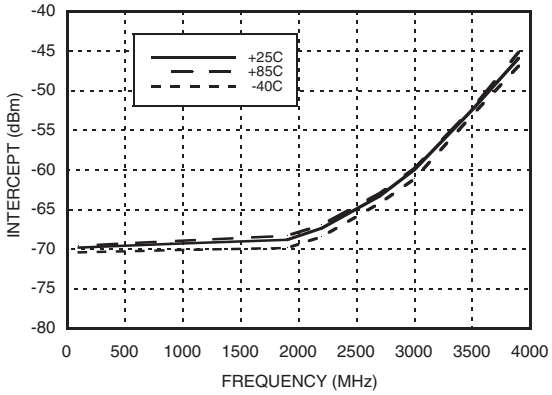
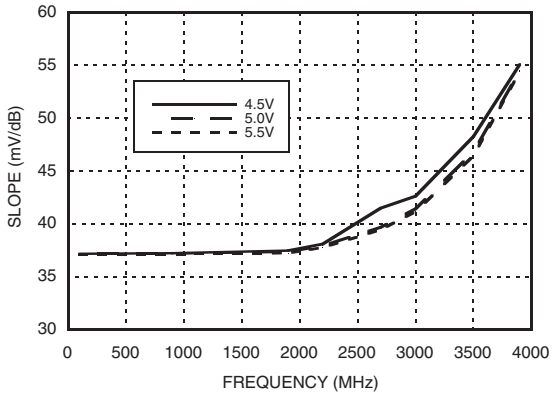
Frequency vs. Intercept Over Supply Voltage [1]



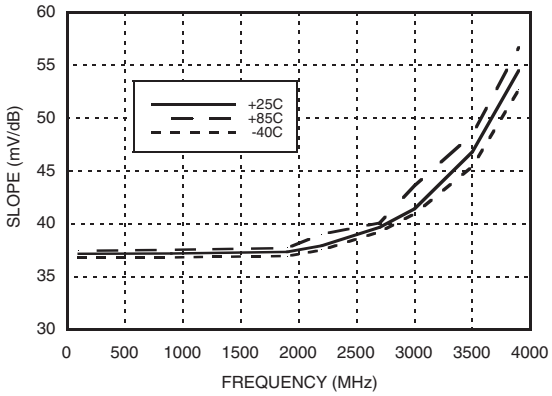
Frequency vs. Intercept Over Temperature [1]



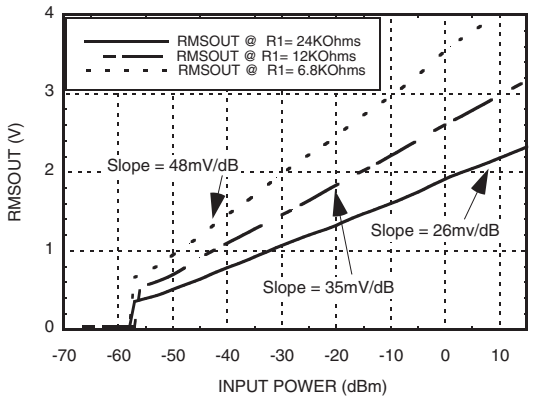
Frequency vs. Slope Over Supply Voltage [1]



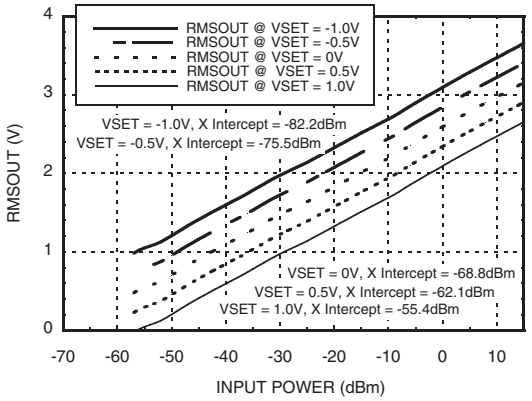
Frequency vs. Slope Over Temperature [1]



RMSOUT vs. Pin, Slope Adjustment [1]



RMSOUT vs. Pin, Intercept Adjustment [2]



[1] See application circuit for location of R1

[2] See application section Log-Slope, R_{FBK} = 12kΩ, R_{SET} = 24KΩ

[3] V_{TGT} 1V, Average Input Power = 0 dBm

[4] V_{TGT} 2V, Average Input Power = 0 dBm

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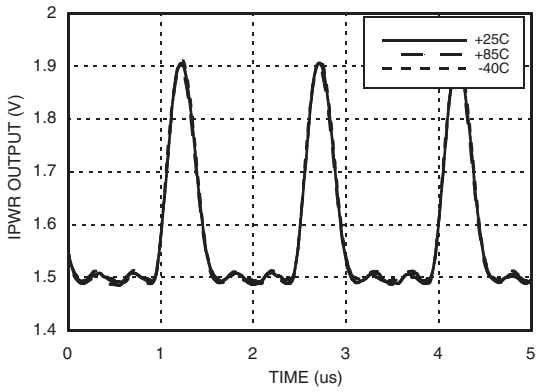
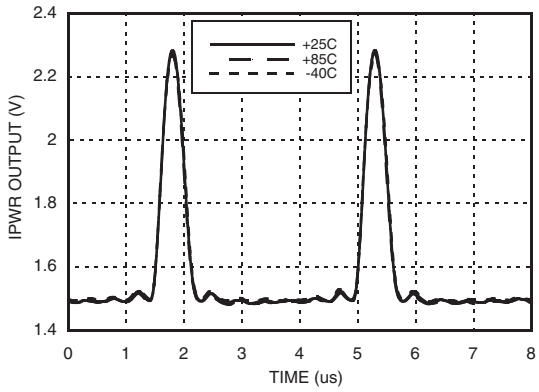
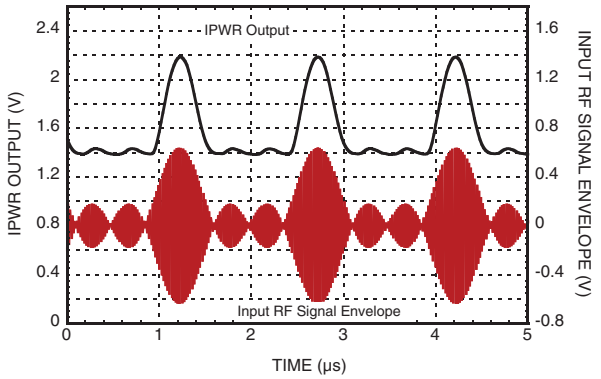
IPWR Output for an Input Crest Factor of 9.03 dB over Temperature vs. Time [3]



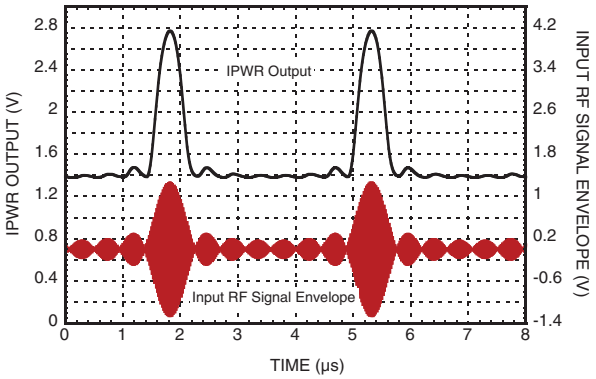
IPWR Output for an Input Crest Factor of 12.04 dB over Temperature vs. Time [3]



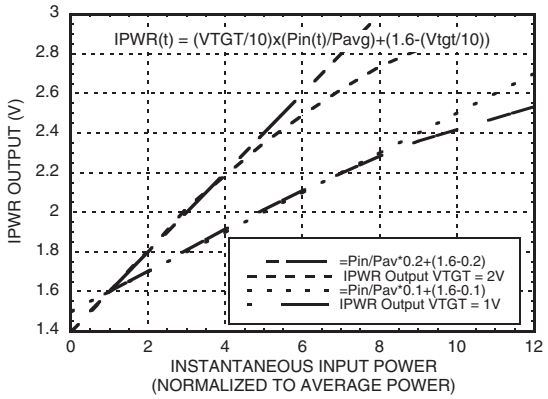
IPWR Output & Input RF Signal Envelope vs. Time For An Input Crest Factor of 9.03 dB [4]



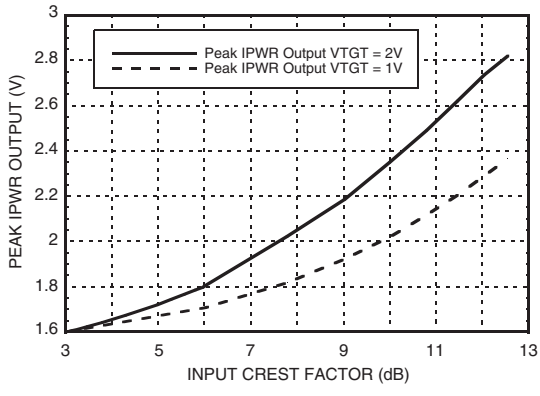
IPWR Output & Input RF Signal Envelope vs. Time For An Input Crest Factor of 12.04 dB [4]



IPWR Output vs. Instantaneous Input Power (Normalized to Average Power) [5]



Peak IPWR vs Input Crest Factor [5]



[1] See application circuit for location of R1

[2] See application section Log-Slope, R_{FBK} = 12kΩ, R_{SET} = 24KΩ

[3] V_{TGT} 1V, Average Input Power = 0 dBm

[4] V_{TGT} 2V, Average Input Power = 0 dBm

[5] P_{IN} = -20 dBm @ 1.9 GHz

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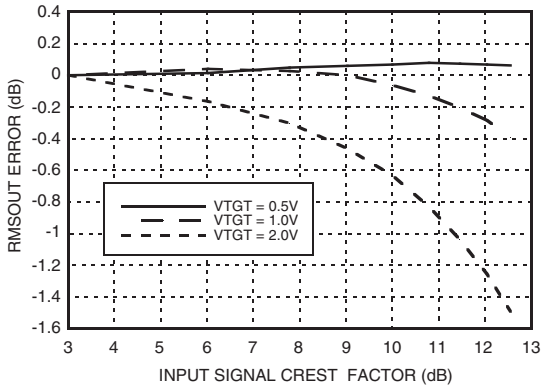
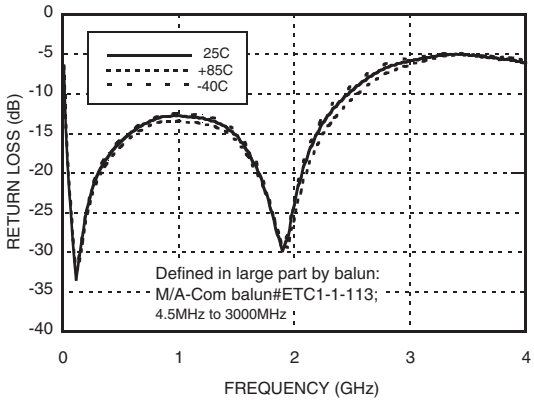
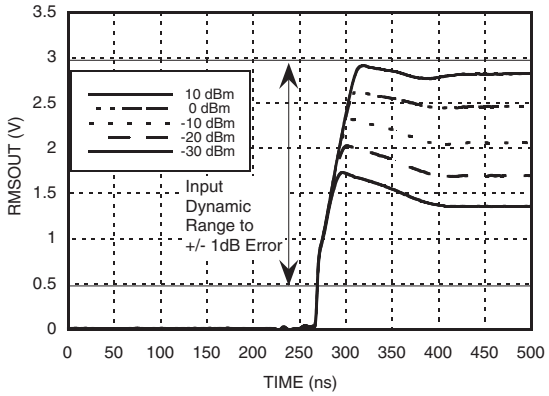
RMS Error vs. Crest Factor Over VTGT [2]



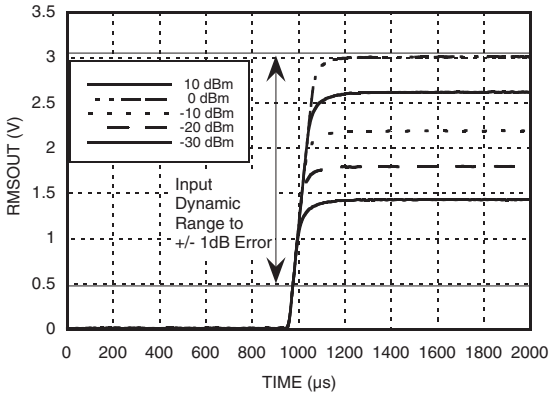
Input Return Loss



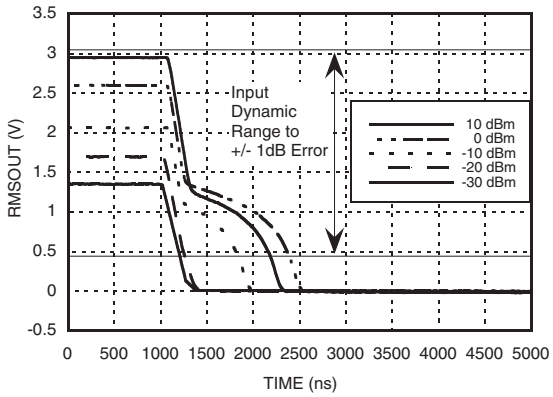
Output Response
Rise Time @ 1900 MHz, C_{INT} = Open



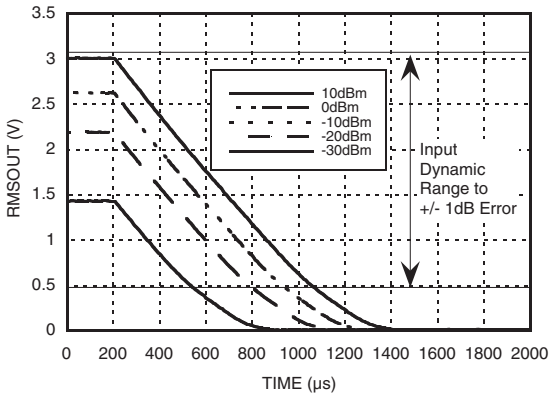
Output Response
Rise Time @ 1900 MHz, C_{INT} = 0.1 µF



Output Response
Fall Time @ 1900 MHz, C_{INT} = Open



Output Response
Fall Time @ 1900 MHz, C_{INT} = 0.1 µF



[1] P_{IN} = -20 dBm @ 1.9 GHz
[2] P_{IN} = -22 dBm @ 1.9 GHz

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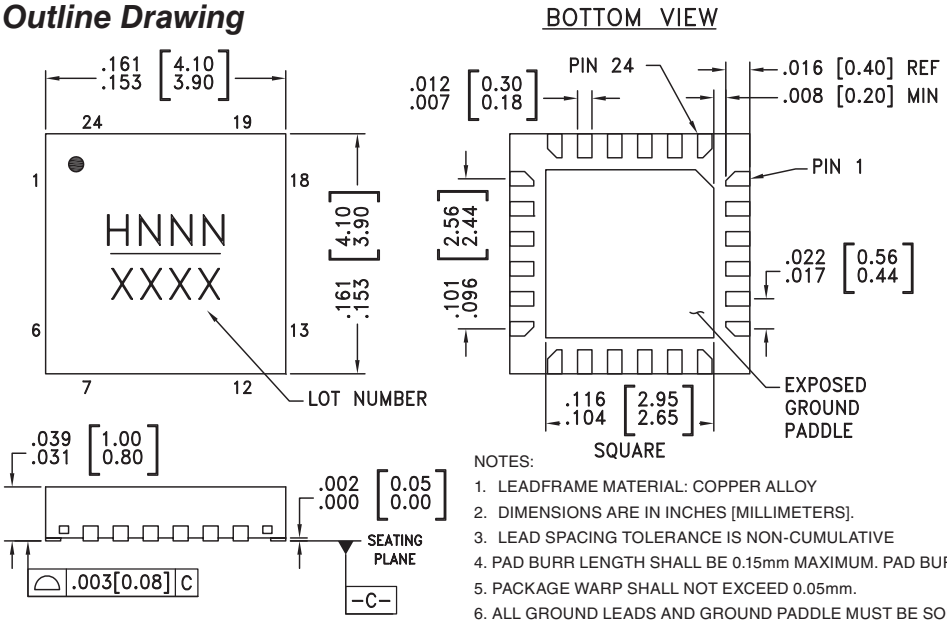
Absolute Maximum Ratings

Supply Voltage	5.6V
RF Input Power	20 dBm
Max. Input Voltage	2.25 Vrms
Channel / Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 22.72 mW/°C above 85°C)	0.91 Watts
Thermal Resistance (R_{th}) (junction to ground paddle)	44.02 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

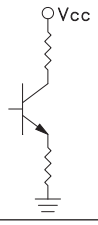
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC614LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H614 XXXX
HMC614LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H614 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 8, 11, 21	Vcc	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	

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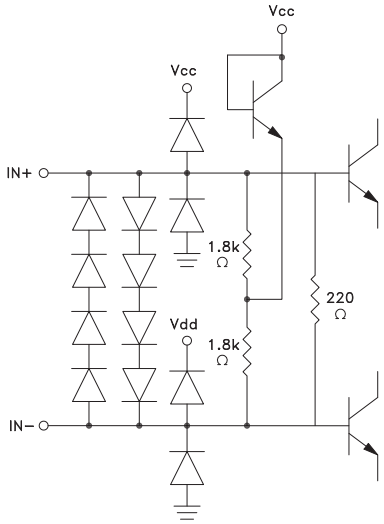
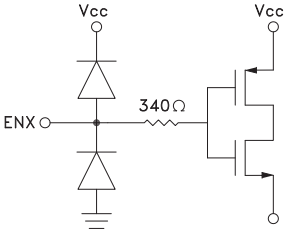
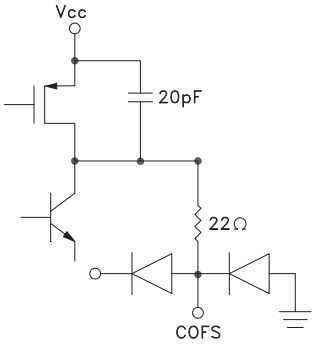
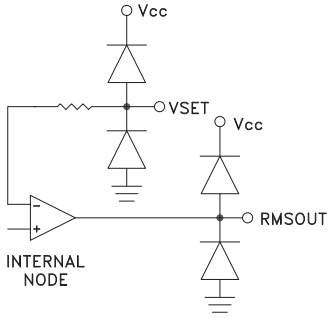
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
2, 5, 13	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	
3, 4	IN+, IN-	RF Input pins. Connect RF to IN+ and IN- through a 1:1 balun.	
7	ENX	Disable pin. Connect to GND for normal operation. Applying voltage V>0.8 Vdd will initiate power saving mode.	
9, 10	COFS	Input high pass filter capacitor. Connect to common via a capacitor to determine 3 dB point of input signal high-pass filter.	
12	N/C	No Connection. These pins maybe be connected to RF/DC ground. Performance will not be affected.	
14	VSET	VSET input. Set point input for controller mode.	
15	RMSOUT	Logarithmic output that converts the input power to a DC level.	

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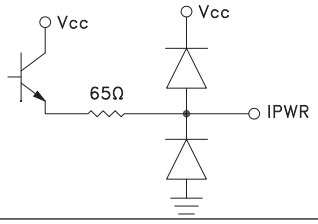
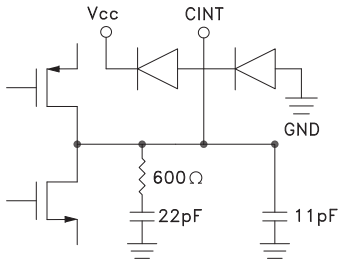
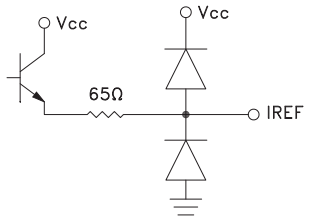
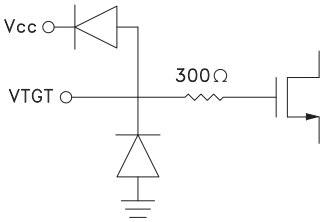
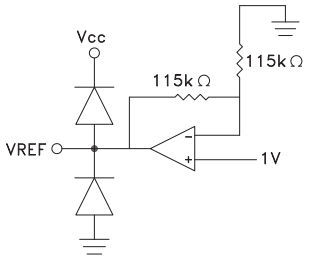
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
16	IPWR	Instantaneous Power Output continuous tracking of Input Power Envelope.	
17	CINT	Connection for ground referenced loop filter integration capacitor. See application schematic.	
18	IREF	Reference DC Voltage for IPWR to replicate voltage at no envelope case.	
19	VTGT	This voltage input changes the logarithmic intercept point. Use of lower target voltage reduces error for complex signals with large crest factors. Normally connected to VREF.	
20	VREF	Reference voltage output.	
22, 23	N/C	The user should not connect to these pins.	

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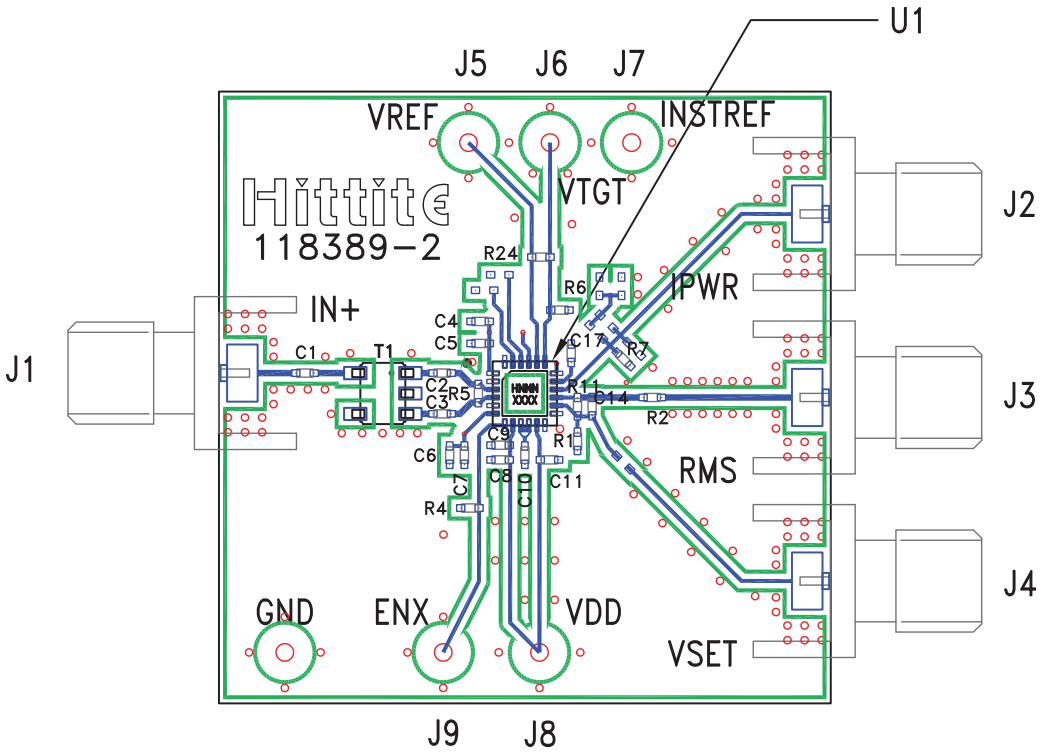
Evaluation PCB



List of Materials for Evaluation PCB 118391 [1]

Item	Description
J1 - J2	PC Mount SMA connector
J3 - J7	DC Pins
C1 - C3	1 nF Capacitor, 0402 Pkg.
C4, C6, C8, C11, C17	0.1 µF Capacitor, 0402 Pkg.
C5, C7, C9	100 PF Capacitor, 0402 Pkg.
C10	1000 PF Capacitor, 0402 Pkg.
R1, R11	12K Ω Resistor, 0402 Pkg.
R2	0 Ω Resistor, 0402 Pkg.
R4	10k Ω Resistor, 0402 Pkg.
R5	68 Ω Resistor, 0402 Pkg.
R6	61.9K Ω Resistor, 0402 Pkg.
R7	3.92K Ω Resistor, 0402 Pkg.
R24	33K Ω Resistor, 0402 Pkg.
T1	1:1 Balun, M/A-COM ETC1-1-13
U1	HMC614LP4 / HMC614LP4E RMS Power Detector
PCB [2]	118389 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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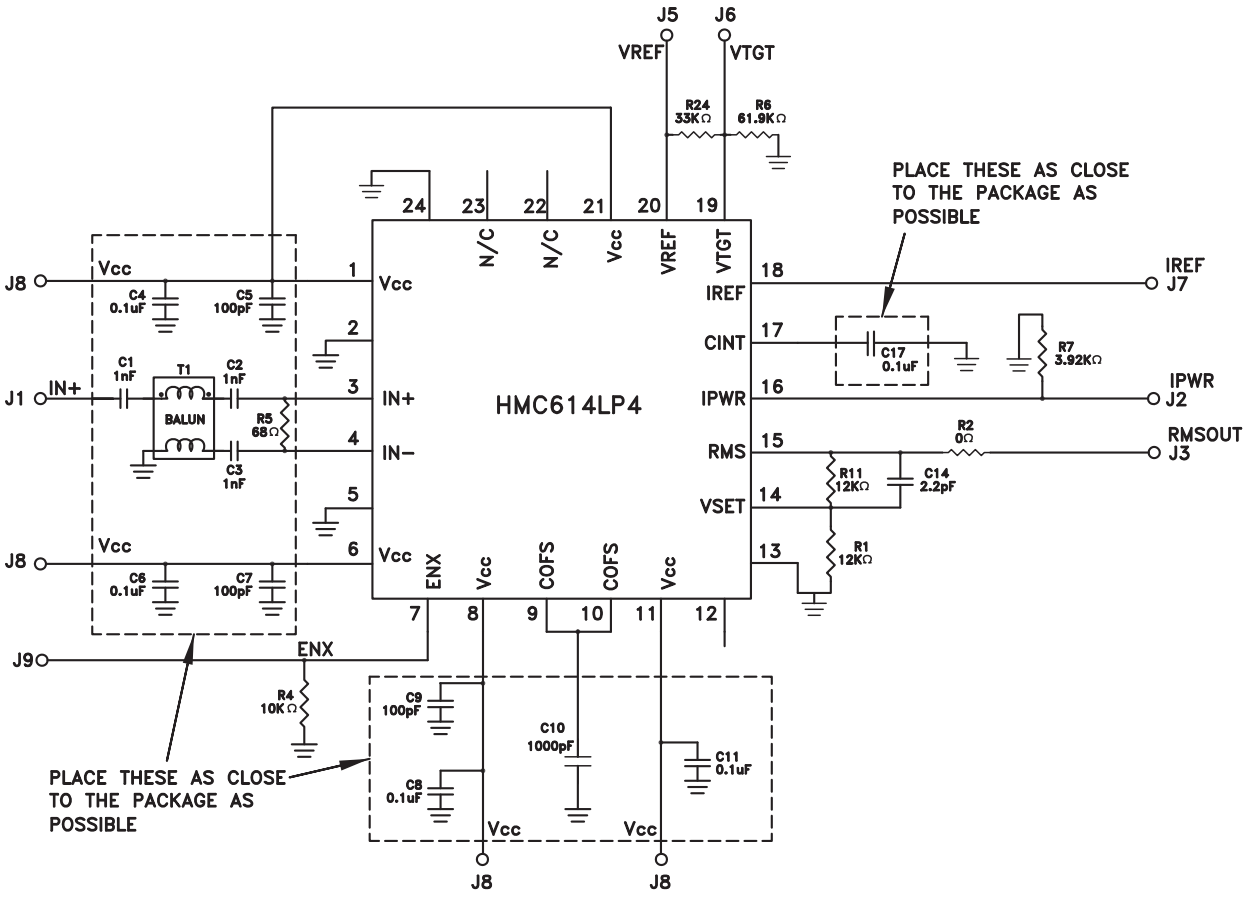
Application Circuit



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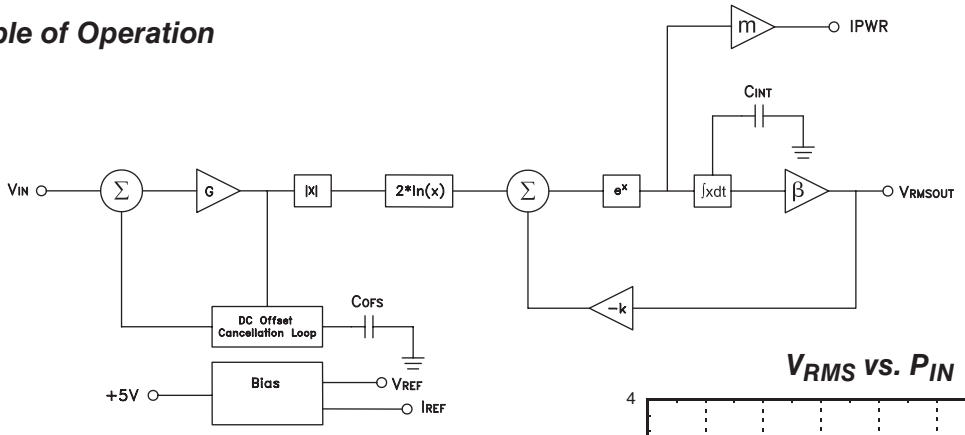
Application Information

Principle of Operation

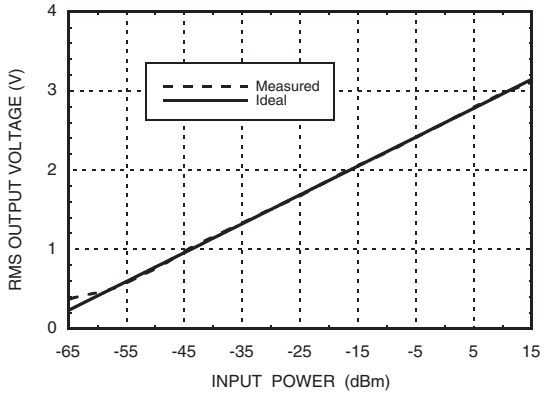


$$V_{RMSOUT} = \frac{1}{k}\ln\left(\beta k G^2 \int V_{IN}^{\,2} dt\right)$$

$$V_{iPWR} = \frac{m V_{IN}^{\,2}}{\beta k \int V_{IN}^{\,2} dt} + \left(iREF - \frac{m}{\beta k}\right)$$

Where ß is op-amp gain set via resistors on the V_{SET} pin.
P_{IN} = V_{RMS}/[log-slope]+[log-intercept], dBm

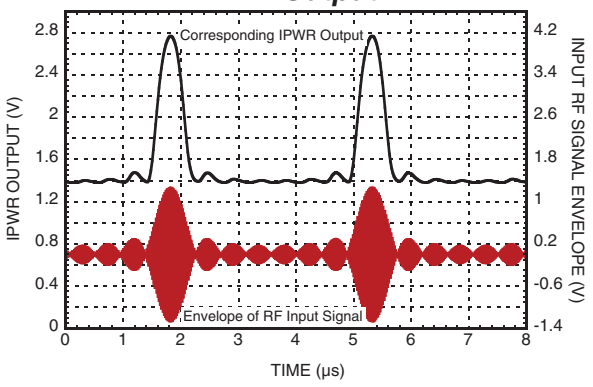
V_{RMS} vs. P_{IN}



Monolithic true-RMS detectors are in-effect analog calculators, calculating the RMS value of the input signal, unlike other types of power detectors which are designed to respond to the RF signal envelope. At the core of an RMS detector is a full-wave rectifier, log/antilog circuit, and an integrator. The RMS output signal is directly proportional to the logarithm of the time-averaged V_{IN}^2. The bias block also contains temperature compensation circuits which stabilize output accuracy over the entire operating temperature range. The DC offset cancellation circuit actively cancels internal offsets so that even very small input signals can be measured accurately.

The iPWR feature tracks the RF envelope and provides a signal which is directly proportional to instantaneous signal power, normalized to average real power calculated by the RMS circuitry. Reading both the iPWR and RMS output voltage signals provides a very informative picture of the RF input signal: peak power, average power, peak-to-average power, and RF wave-shape. Simultaneous measurement of instantaneous signal power and average power is essential for taking full advantage of a receive signal chain's available dynamic range, while avoiding saturation, or to maximize transmitter efficiency.

iPWR Output



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Configuration For The Typical Application

The RF input can be connected in either a differential or single-ended configuration: see "RF Input Interface" section for details on each input configuration.

The RMS output signal is typically connected to V_{SET}, providing a Pin -> V_{RMS} transfer characteristic slope of 36.5mV/dBm, however the RMS output can be re-scaled to "magnify" a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output. Refer to the section under the "log-slope and intercept" heading for details.

The iPWR output voltage signal can be processed directly for measurement of the input RF envelope, or a peak-hold circuit can be applied for measuring crest factor. See the section under "iPWR – Instantaneous Power" for application information.

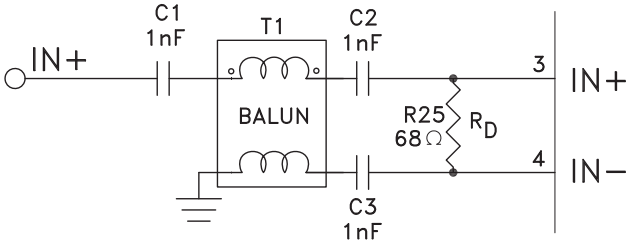
VTGT is also typically connected directly to V_{REF}, however the V_{TGT} voltage can be adjusted to optimize measurement accuracy, especially when measurement at higher crest factors is important: see "Adjusting V_{TGT} for greater precision" section for technical details.

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements: refer to the "System Calibration" section for more details.

RF Input Interface

The IN+ and IN- pins are differential RF inputs, which can be externally configured with differential or single-ended input. Power match components are placed at these input terminals, along with DC blocking capacitors. The coupling capacitor values also set the lower spectral boundary of the input signal bandwidth. The inputs can be reactively matched (refer to input return loss graphs), but a resistor network should be sufficient for good wideband performance.

Differential Input Interface:



The value of RD depends on the balun used; if the balun is 50Ω on both sides of the SE-Diff conversion,

then $R_D = \frac{220 * R_M}{220 - R_M}$, Ω, where

R_M = the desired power match impedance in ohms

For R_M = 50Ω, R_D = 64.7Ω ≈ 68Ω

Single-Ended Input Interface:

Please contact Hittite Customer Support for details on the single-ended input interface.

Choose the input decoupling capacitor values (C2, C3) by first determining the lowest spectral component the power detector is required to sense, f_L.

C2 = C3 = Input decoupling capacitor value $\approx \frac{1}{\pi \times f_L \times 3.2}$ Farads, where f_L is in Hertz.

Example:

If the power detector needs to sense down to 10MHz, the decoupling capacitor value should be 1/(π*10E6*3.2) = 10nF

A DC bias (Vcc-0.7V) is present on the IN+ and IN- pins, and should not be overridden.

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RMS Output Interface and Transient Response

Output transient response is determined by the integration capacitance (C_{INT}), and output load conditions. Using larger values of C_{INT} will narrow the operating bandwidth of the integrator, resulting in a longer averaging time-interval and a more filtered output signal; however it will also slow the power detector's transient response. A larger C_{INT} value favors output accuracy over speed. For the fastest possible transient settling times, leave the C_{INT} pin free of any external capacitance. This configuration will operate the integrator at its widest possible bandwidth, resulting in short averaging time-interval and an output signal with little filtering. Most applications will choose to have some external integration capacitance, maintaining a balance between speed and accuracy. Furthermore, error performance over crest factor is degraded when C_{INT} is very small (for C_{INT}<100pF).

Modulation & Deviation in Electrical Spec Table 2 are given for C_{INT}= 0.1 µF

Start by selecting C_{INT} using the following expression, and then adjust the value as needed, based on the application's preference for faster transient settling or output accuracy.

$$C_{INT} \approx \frac{1500\,\mu F}{2\pi f_{LAM}}$$, in Farads,

where f_{LAM}=lowest amplitude-modulation component frequency in Hertz

Example: when f_{LAM}=10kHz, C_{INT} = 1500µF/(2*π*1E4) = 24E-9 Farads ~ 22nF

Table: Transient Response vs. C_{INT} Capacitance with C_{OFS}= 0

C_{INT}	Rise Time (0 dBm)	Fall Time (-30 dBm)	Fall Time (-10 dBm)	Fall Time (0 dBm)
0	34 nsec	140 nsec	620 nsec	820 nsec
100 pF	120 nsec	550 nsec	920 nsec	1.2 µsec
1 nF	890 nsec	4.1 µsec	6.7 µsec	7.9 µsec
10 nF	9.6 µsec	43 µsec	70 µsec	83 µsec
100 nF	80 µsec	360 µsec	625 µsec	720 µsec

Input signal is 1900 MHz CW-tone switched on and off
RMS is loaded wtih 1kΩ, 4pF, and V_{TGT} = 2V,
D.R. is input dynamic range to ±1 dB error.

Transient response can also be slewed by the RMS output if it is excessively loaded: keep load resistance above 375Ω. An optimal load resistance of approximately 500Ω to 1kΩ will allow the output to change as quickly as it is can. For increased load drive capability, consider a buffer amplifier on the RMS output.

Using an integrating amplifier on the RMS output allows for an alternative treatment for faster settling times. An external amplifier optimized for transient settling can also provide additional RMS filtering, when operating HMC614LP4 with a lower C_{INT} capacitance value.

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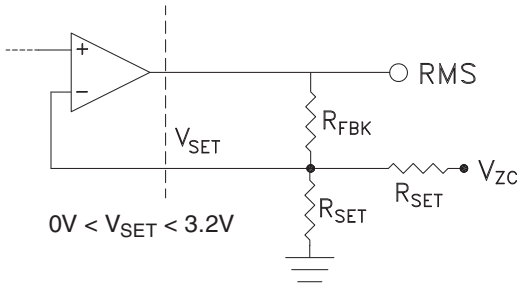
LOG-Slope and Intercept

The HMC614LP4 provides for an adjustment of output scale with the use of an integrated operational amplifier. Log-slope and intercept can be adjusted to "magnify" a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output.

A log-slope of 36.5mV/dBm is set by connecting RMS Output to V_{SET} through resistor network for ß = 1 (see schematic). The log-slope is adjusted by applying the appropriate resistors on the RMS and V_{SET} pins. Log-intercept is adjusted by applying a DC voltage to the V_{SET} pin.



Optimized_slope = (ß + 1) * log_slope / 2

Optimized_intercept = log_intercept – $\frac{ß * V_{ZC}}{2}$

ß = (R_{FBK} / R_{SET}) x 2

When $R_{FBK} = \frac{R_{SET}}{2}$, and VZC = 0V: ß = 1

Note: Apply a capacitor across RFBK for additional stability.

Note: Avoid excessive loading of the RMS output: R_{LOAD} > 375Ω

Example: An application only requires the power detector to measure input signal power levels ranging from -40 dBm to 0 dBm at 900 MHz. To optimize the full output voltage range of RMS, we re-map $P_{IN(MIN)}$ = -40 dBm to $RMS_{(MIN)}$ = 0V and $P_{IN(MAX)}$ = 0dBm to $RMS_{(MAX)}$ =3.2V.

log_slope = 36.5 mV/dB, log_intercept = -72 dBm at 900 MHz (see Electrical Specifications table 3)

Input signal power range = 0 dBm - (-40 dBm) = 40 dB

Output voltage range = 3200 mV

Optimal_slope = 3200 mV/40 dB = 80 mV/dB

Then we should apply VZC to shift RMS down for $P_{IN(MIN)}$ = -40 dBm to map to $RMS_{(MIN)}$ = 0V

$$ß = \frac{optimal\_slope \times 2}{log\_slope} - 1 = \frac{80.0 \times 2}{36.5} - 1 = 3.38 = \frac{2R_{FBK}}{R_{SET}} \sim \frac{51k\Omega}{15k\Omega}, \text{ at 900 MHz}$$

RMS = (PIN – log_intercept) * optimal_slope, with VZC = 0V

And with Pin = -40 dBm: RMS = 2.56V = [(-40 dBm) – (-72 dBm)] * 80 mV/dBm, at 900 MHz

So we must shift RMS down 2.56V by applying VZC =2x (-2.56V) / -ß = 2x (-2.56V) / -3.38 = 1.506

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iPWR – Envelope Power Normalized To Average Power

The iPWR is an envelope detector output which provides a measurement of instantaneous signal power ***normalized*** to average power. The iPWR output makes peak-to-average power comparisons immediately obvious. This simultaneous measurement of envelope power and average power in HMC614LP4 has two fundamental advantages over traditional methods of which employ two different power detectors working in parallel.

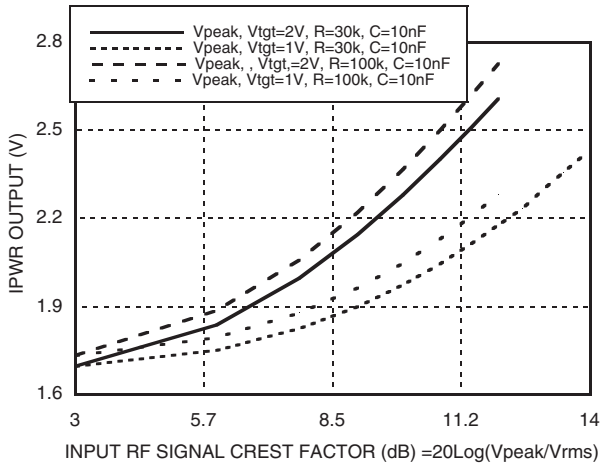
- Both the iPWR and RMS detectors share the same measurement structures, and
- Both the iPWR and RMS detectors share the same temperature compensation mechanisms.

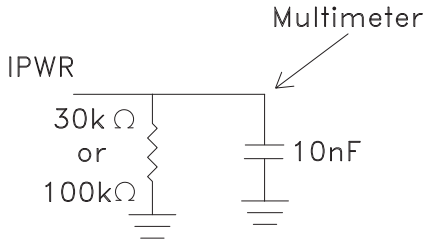
With traditional implementation of peak-to-average power detection, the dominant source of errors is due to the uncorrelated measurement deviations between the two separate detectors. Both detectors in the HMC614LP4 share the same circuits, so any deviations, however small, are fully correlated.

HMC614LP4 provides a reference voltage, iREF (pin 18), which when used with the iPWR output allows cancellation of temperature and supply related variations of the iPWR DC offset. iPWR DC offset is equal to the iREF reference voltage, and this level corresponds to the peak-to-average ratio of an unmodulated carrier (CW-tone crest factor = 3dB). For the best cancellation of the effects of temperature and supply voltage on iPWR DC offset, **load both the iPWR and iREF outputs with an equivalent resistance**.

To measure peak power, a peak-hold mechanism is required at the iPWR output. The peak-hold circuit can be as simple as an RC combination on the iPWR pin. The graph below describes the iPWR peak-hold levels as a function of input crest factor. Note that the voltage applied at VTGT has an effect of the iPWR reading. The VTGT signal optimizes internal bias points for measurement accuracy at higher crest factors: refer to the section under “Adjusting VTGT for greater precision” for a full description on crest factor optimization.

IPWR, Peak Power Output Normalized to Average Power





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Standby Mode

The ENX can be used to force the power detector into a low-power standby mode. In this mode, the entire power detector is powered-down. As ENX is deactivated, power is restored to all of the circuits. There is no memory of previous conditions. Coming-out of stand-by, C_{INT} and C_{OFS} capacitors will require recharging, so if large capacitor values have been chosen, the wake-up time will be lengthened.

DC Offset Compensation Loop

Internal DC offsets, which are input signal dependant, require continuous cancellation. Offset cancellation is a critical function needed for maintenance of measurement accuracy and sensitivity. The DC offset cancellation loop performs this function, and its response is largely defined by the capacitance off the C_{OFS} pin. Setting DC offset cancellation, loop bandwidth strives to strike a balance between offset cancellation accuracy, and loop response time. A larger value of C_{OFS} results in a more precise offset cancellation, but at the expense of a slower offset cancellation response. A smaller value of C_{OFS} tilts the performance trade-off towards a faster offset cancellation response. The optimal loop bandwidth setting will allow internal offsets to be cancelled at a minimally acceptable speed.

$$\text{DC Offset Cancellation Loop} \approx \frac{1}{\pi(5000)(C_{OFS}+20\text{x}10^{-12})} \quad \text{Bandwidth , Hz}$$

For example: loop bandwidth for DC cancellation with C_{OFS} = 1nF, bandwidth is ~62 kHz

Note:
The measurement error produced by internal DC offsets cannot be measured at any single operating point, in terms of input signal frequency and level, with repeatability. Measurement error must be calculated to a best fit line, over the entire operating range (again, in terms of signal level and frequency).

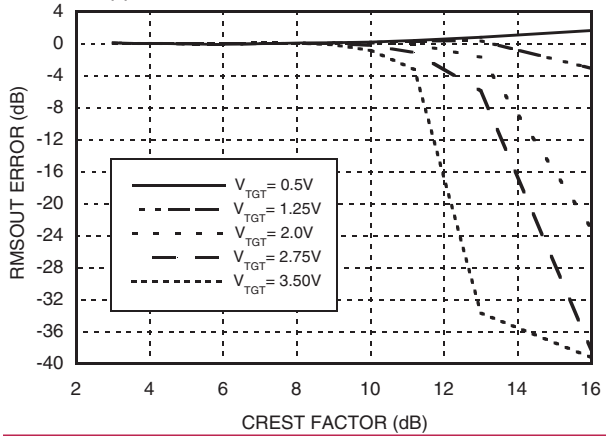
Adjusting V_{TGT} for greater precision

There are two competing aspects of performance, for which V_{TGT} can be used to set a preference. Depending on which aspect of precision is more important to the application, the V_{TGT} pin can be used to find a compromise between two sources of RMS output error: internal DC offset cancellation error and deviation at high crest factors (>10 dB).

- Increasing V_{TGT} input voltage will improve internal DC offset cancellation, but deviation at high crest factors will increase slightly. A 50% increase in V_{TGT} should produce an 18% improvement in RMS precision due to improved DC offset cancellation performance.
- Decreasing V_{TGT} input voltage will reduce errors at high crest factors, but DC offset cancellation performance will be slightly degraded. See “RMS Output Error vs. Crest Factor” graph.
- DC Offsets are observed as a random ripple in the logarithmic characteristics

RMS Output Error vs. Crest Factor

***Worst Case Conditions** using circuit described in “ Application & Evaluation PCB Schematic” section*



V_{TGT} influence on DC offset compensation

V_{TGT}	Logarithmic Linearity Error due to Internal DC Offsets
1.0V	Nominal +0.2 dB
1.5V	Nominal +0.1 dB
2.0V	Nominal
3.0V	Nominal -0.06 dB
3.5V	Nominal -0.1 dB

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Adjusting V_{TGT} for greater precision *(Continued)*

If input signal crest factor is not expected to exceed 10 dB, you can improve RMS precision by increasing V_{TGT} voltage. Keep in mind that changing V_{TGT} also adjusts the log-intercept point, which shifts the "input dynamic range". The best set-point for V_{TGT} will be the lowest voltage that still maintains the "input dynamic range" over the required range of input power. This new V_{TGT} set-point should optimize DC offset correction performance.

If error performance for crest factors >10 dB requires optimization, set V_{TGT} for the maximum tolerable error at the highest expected crest factor. Increasing V_{TGT} beyond that point will unnecessarily compromise internal DC offset cancellation performance. After changing V_{TGT}, re-verify that the "input dynamic range" still covers the required range of input power.

V_{TGT} should be referenced to V_{REF} for best performance. It is recommended to use a temperature stable DC amplifier between V_{TGT} and V_{REF} to create $V_{TGT} > V_{REF}$. The V_{REF} pin is a temperature compensated voltage reference output, only intended for use with V_{TGT}.

System Calibration

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements. When performing this calibration, choose at least two test points: near the top-end and bottom-end of the measurement range. It is best to measure the calibration points in the regions (of frequency and amplitude) where accuracy is most important. Derive the log-slope and log-intercept, and store them in non-volatile memory. Calibrate iPWR scaling by measuring the peak-to-average ratio of a known signal.

For example if the following two calibration points were measured at 2.35 GHz:

With Vrms = 2.34V at Pin= -7 dBm,	Now performing a power measurement:
and Vrms=1.84V at Pin= -16 dBm	Vrms measures 2.13V
slope calibration constant = SCC	[Measured Pin] = [Measured Vrms]*SCC + ICC
SCC = (-16+7)/(1.84-2.34) = 18 dB/V	[Measured Pin] = 2.13*18.0 – 49.12 = -10.78 dBm
intercept calibration constant = ICC	An error of only 0.22 dB
ICC = Pin – SCC*Vrms = -7 – 18.0 * 2.34 = -49.12 dBm	

Factory system calibration measurements should be made using an input signal representative of the application. If the power detector will operate over a wide range of frequencies, choose a central frequency for calibration.

Layout Considerations

- Mount RF input coupling capacitors close to the IN+ and IN- pins.
- Solder the heat slug on the package underside to a grounded island which can draw heat away from the die with low thermal impedance. The grounded island should be at RF ground potential.
- Connect power detector ground to the RF ground plane, and mount the supply decoupling capacitors close to the supply pins.

Definitions:

- Log-slope: slope of P_{IN} –> V_{RMS} best-fit line, when RMS is connected directly to V_{SET} in units of mV/dB
- Log-intercept: x-axis intercept of P_{IN} –> V_{RMS} transfer characteristic. In units of dBm.
- RMS Output Error: The difference between the measured PIN and the best-fit line.

  [measured_P_{IN}] = [measured_V_{RMS}] / [best-fit-slope] + [best-fit-intercept], dBm
- Input Dynamic Range: the range of average input power for which there is a corresponding RMS output voltage with "RMS Output Error" falling within a specific error tolerance.
- Crest Factor: Peak power to average power ratio for time-varying signals.

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Notes:

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