EPSON

S1D13503 Series

Dot Matrix Graphics LCD Controller

■ DESCRIPTION

This device is designed for products where low cost, low power consumption, and low component count are the major design considerations. This chip operates from 2.7 Volts to 5.5 Volts and up to 25 MHz to suit different power consumption, speed and cost requirements. The S1D13503 offers a flexible microprocessor interface and is pin compatible with the SED1352.

The S1D13503 is capable of displaying a maximum of 16 levels of gray shade or 256 simultaneous colors. In gray shade modes, a 16 x 4 Look-Up Table is provided to allow remapping of the 16 possible gray shades displayed on the LCD panel. In color modes, three 16 x 4 Look-Up Tables are provided to allow remapping of the 4096 possible colors displayed on the LCD panel. The S1D13503 can interface to an MC68000 family microprocessor or an 8/16-bit MPU/Bus with minimum external "glue" logic. This device can directly control up to 128K bytes of static RAM with a 16-bit data path, or up to 64K bytes with an 8-bit data path.

■ FEATURES

◆ Technology

- low power CMOS
- 2.7 to 5.5 volt operation
- S1D13503F00A is 100 pin QFP5-S2 surface mount package
- S1D13503F01A is 100 pin QFP15-STD surface mount package
- S1D13503D00A is Die form

◆ System

- maximum 25 MHz input clock (or pixel clock)
- 2-terminal crystal input for internal oscillator or direct connection to external clock source
- maximum 16 MHz, 16-bit MC68000 MPU interface
- 8-bit or 16-bit MPU/Bus interface with memory accesses controlled by a READY (or WAIT#) signal
- option to use built-in index register or direct-mapping to access one of sixteen internal registers
- 8-bit or 16-bit SRAM data bus interface configurations
- display memory configurations:
  - 128K bytes using one 64K x 16 SRAM
  - 128K bytes using two 64K x 8 SRAMs
  - 64K bytes using two 32K x 8 SRAMs
  - 40K bytes using one 8K x 8 and one 32K x 8 SRAM
  - 32K bytes using one 32K x 8 SRAM
  - 16K bytes using two 8K x 8 SRAMs
  - 8K bytes using one 8K x 8 SRAM

◆ Display Modes

- 1 bit-per-pixel, black-and-white display mode
- 2/4 bits-per-pixel, 4/16 level gray shade display modes
- 2/4/8 bits-per-pixel, 4/16/256 level color display modes
- one 16 x 4 Look-Up Table provided for gray shade display modes
- three 16 x 4 Look-Up Tables provided for color display modes
- maximum 16 shades of gray
- maximum 256 simultaneous colors from a possible 4096 colors
- split screen display mode (see AUX[0A])
- virtual display mode (see AUX[0D])

Note: 256 color display mode support requires a 16-bit display memory interface.

◆ Display Support

- example resolutions:
  - 1024 x 768 black-and-white
  - 640 x 480 with 4 colors/grays
  - 640 x 400 with 16 colors/grays
  - 320 x 240 with 256 colors
- passive monochrome LCD panels:
  - 4-bit single (4-bit data transfer)
  - 8-bit single (8-bit data transfer)
  - 8-bit dual (4-bit data transfer for each half panel)
- passive color LCD panels:
  - 4-bit single (4-bit data transfer)
  - 8-bit single (8-bit data transfer)
  - 8-bit dual (4-bit data transfer for each half panel)
  - 16-bit single (8-bit data transfer with external circuit)
  - 16-bit dual (8-bit data transfer with external circuit)

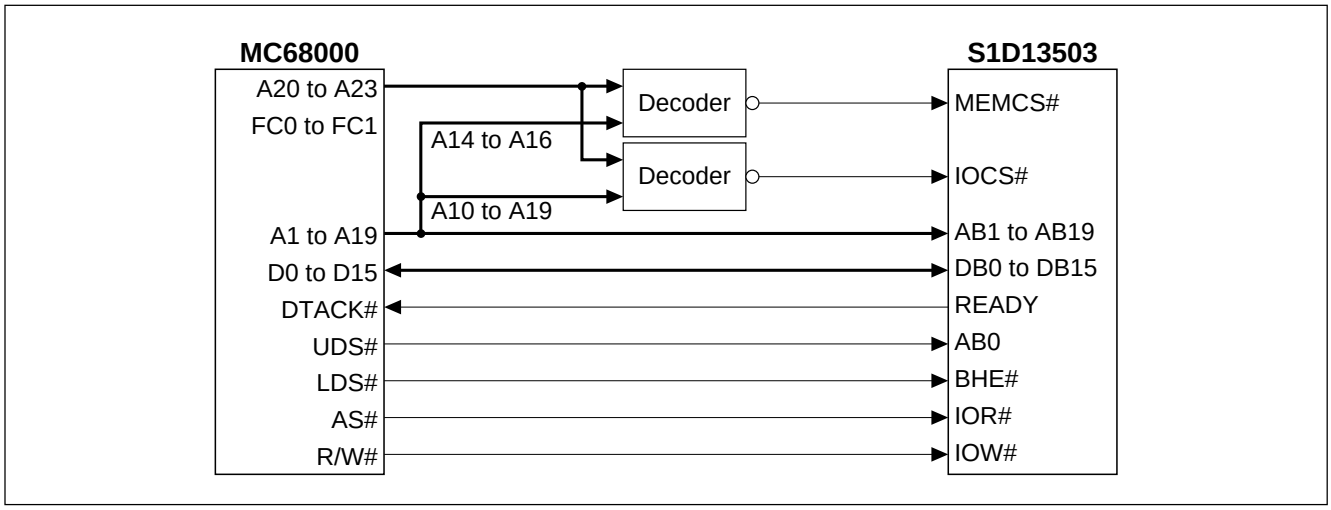
◆ Power Management

- two software power-save modes
- low power consumption
- panel power control switch (see AUX[01] bit 4)

■ TYPICAL SYSTEM BLOCK DIAGRAMS

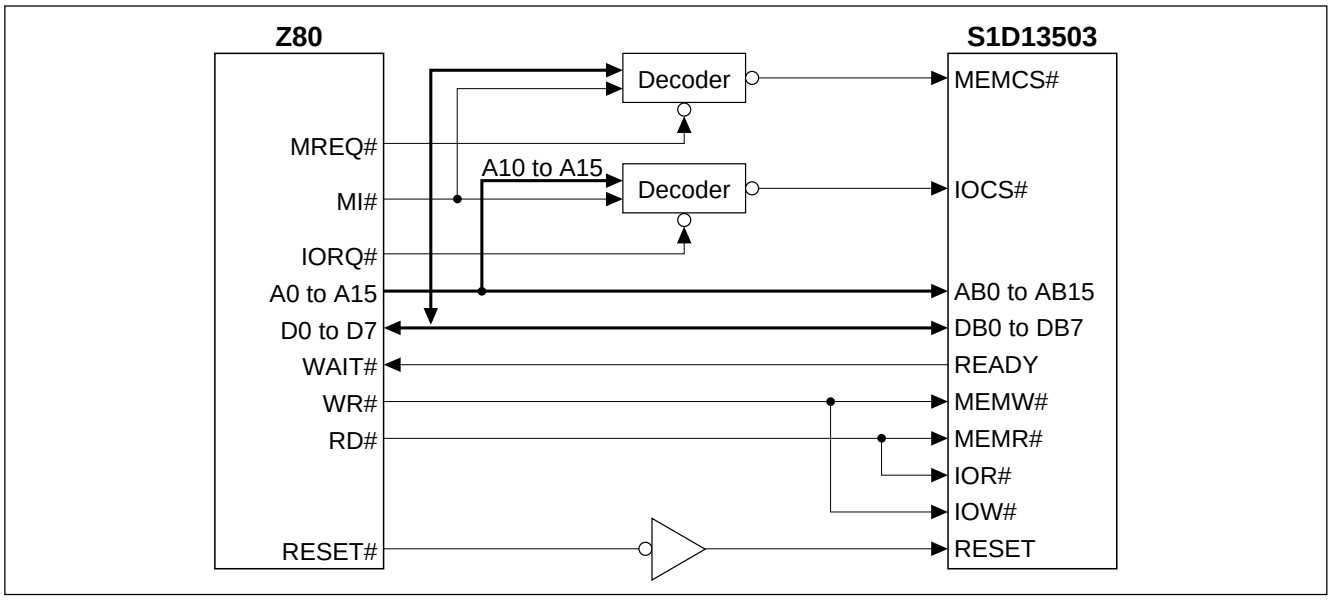
The following figures show typical system implementations of the S1D13503. All of the following block diagrams are shown without SRAM or LCD display. Refer to the interface specific Application Notes for complete details.

16-Bit MC68000 MPU

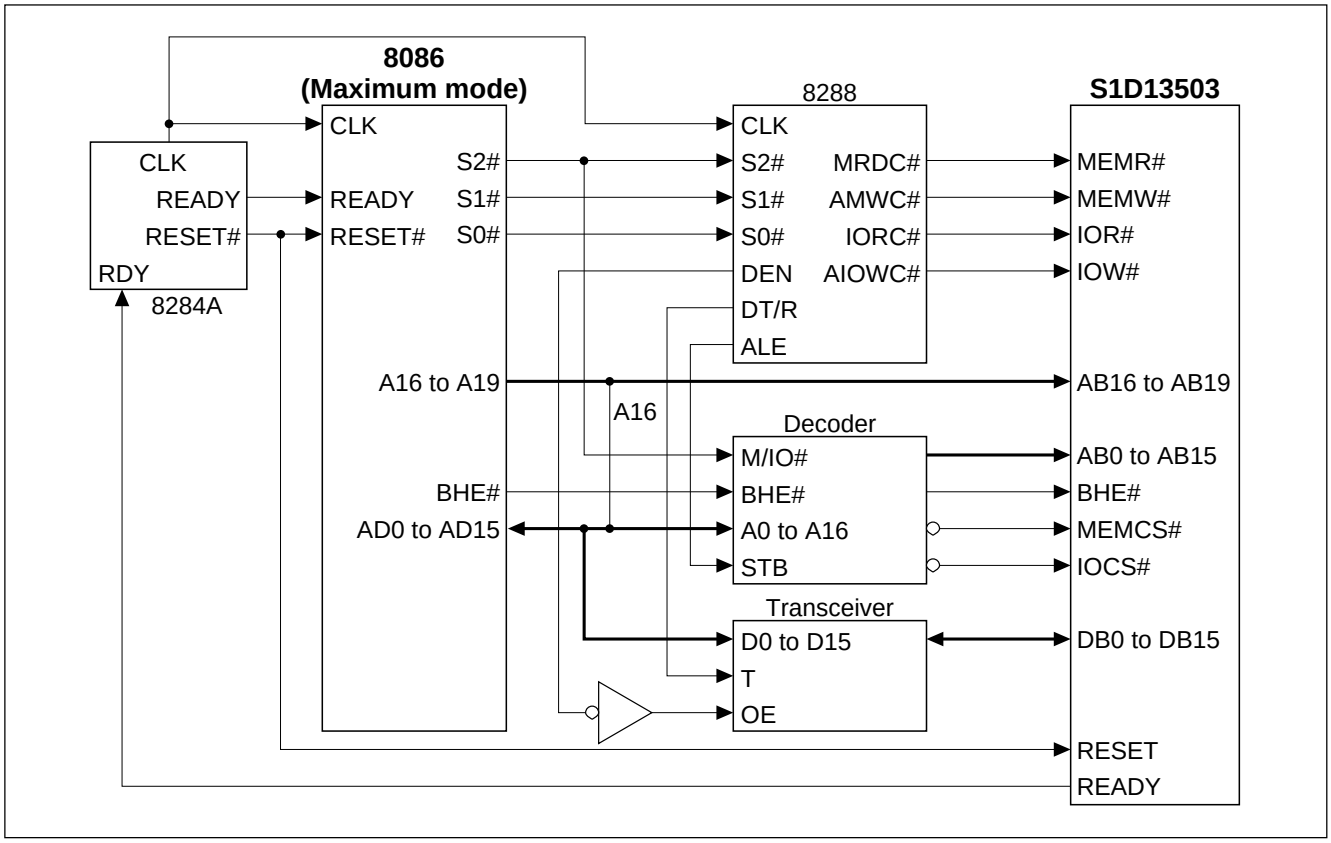


16-Bit 68000 Series
(example implementation only - actual may vary)

MPU with READY (or WAIT#) Signal

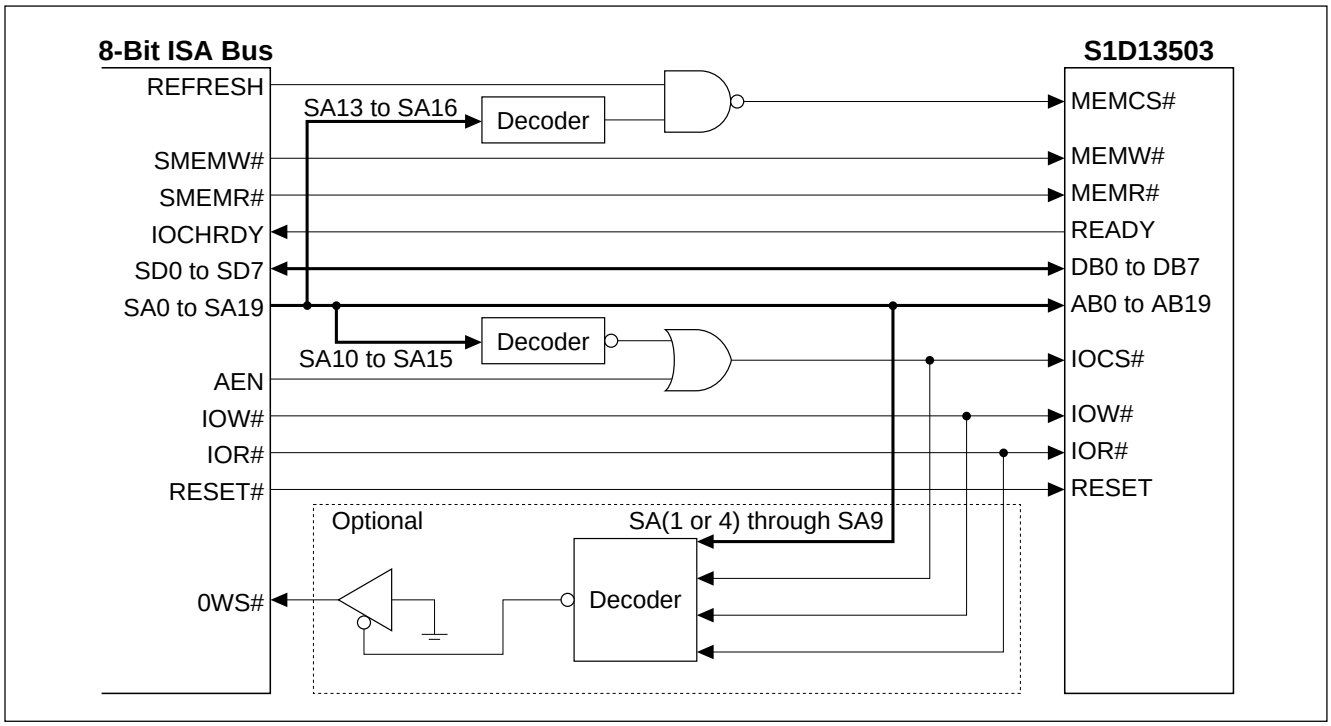


8-Bit Mode, Example: Z80
(example implementation only - actual may vary)

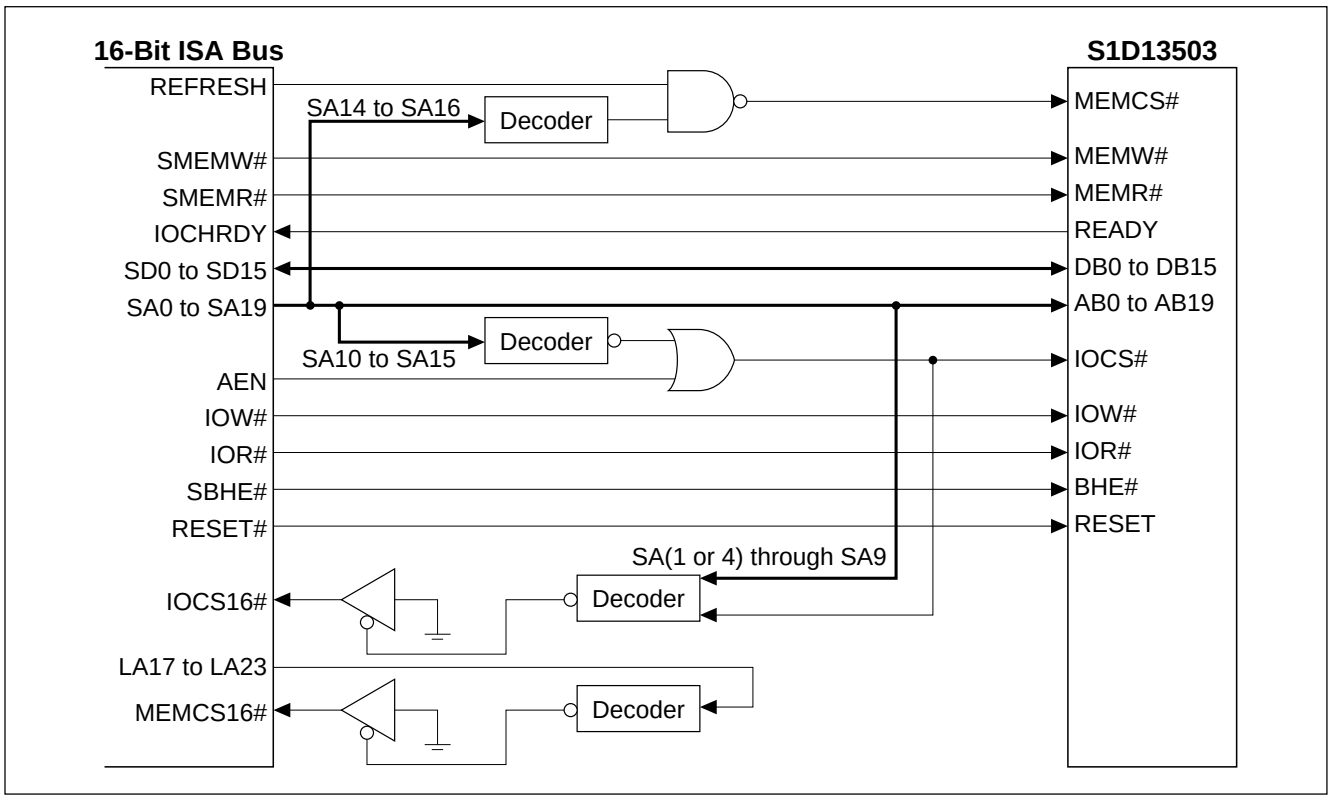


16-Bit Mode, Example: i8086 (maximum mode)
(example implementation only - actual may vary)

ISA Bus

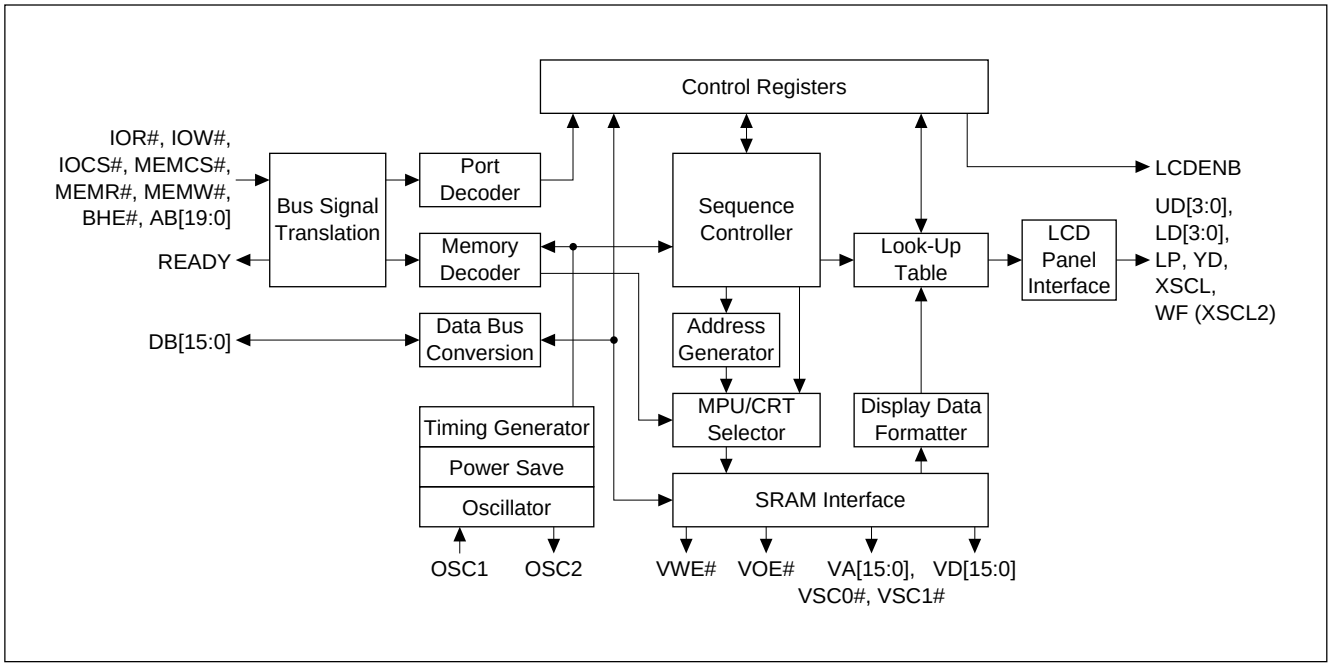


8-Bit Mode (ISA)
(example implementation only - actual may vary)



16-Bit Mode (ISA)
(example implementation only - actual may vary)

◆ Internal Block Diagram



Internal Block Diagram

◆ Functional Block Descriptions

Bus Signal Translation

According to configuration setting VD2, the Bus Signal Translation block translates either MC68000 type MPU signals or MPU controlled by a READY type signals to internal bus interface signals.

Control Registers

The register block contains the 16 internal control and configuration registers. These registers can be accessed by either direct-mapping or using the built-in internal index register.

Sequence Controller

The Sequence Controller block generates horizontal and vertical display timings according to the configuration registers settings.

LCD Panel Interface

The LCD Interface block performs frame rate modulation and output data pattern formatting for both passive monochrome and passive color LCD panels.

Look-Up Table

The Look-Up Table block contains three 16 x 4-bit wide palettes. In gray shade modes, the "green" palette can be configured for the re-mapping of 16 possible shades of gray. In color modes, all three palettes can be configured for the re-mapping of 4096 possible colors. See Look-Up Table Architecture for details.

Port Decoder

According to configuration settings VD1, VD12-VD4, IOCS# and address lines AB9-1, the Port Decoder validates a given I/O cycle.

Memory Decoder

According to configuration settings VD15-VD13, MEMCS# and address lines AB19-17, the Memory Decoder validates a given memory cycle.

Data Bus Conversion

According to configuration setting VD0, the Data Bus Conversion Block maps the external data bus, either 8-bit or 16-bit, into the internal odd and even data bus.

Address Generator

The Address Generator generates display refresh addresses to be used to access display memory.

MPU / CRT Selector

This block grants access to the display memory from either the MPU or the display refresh circuitry.

Display Data Formatter

The Display Data Formatter reads in the display data from the display memory and outputs the correct format for all supported gray shade and color selections.

Clock Inputs / Timing

The Timing block generates the internal master clock (MCLK) according to gray-level/color selected and display memory interface. The master clock (MCLK) can be;

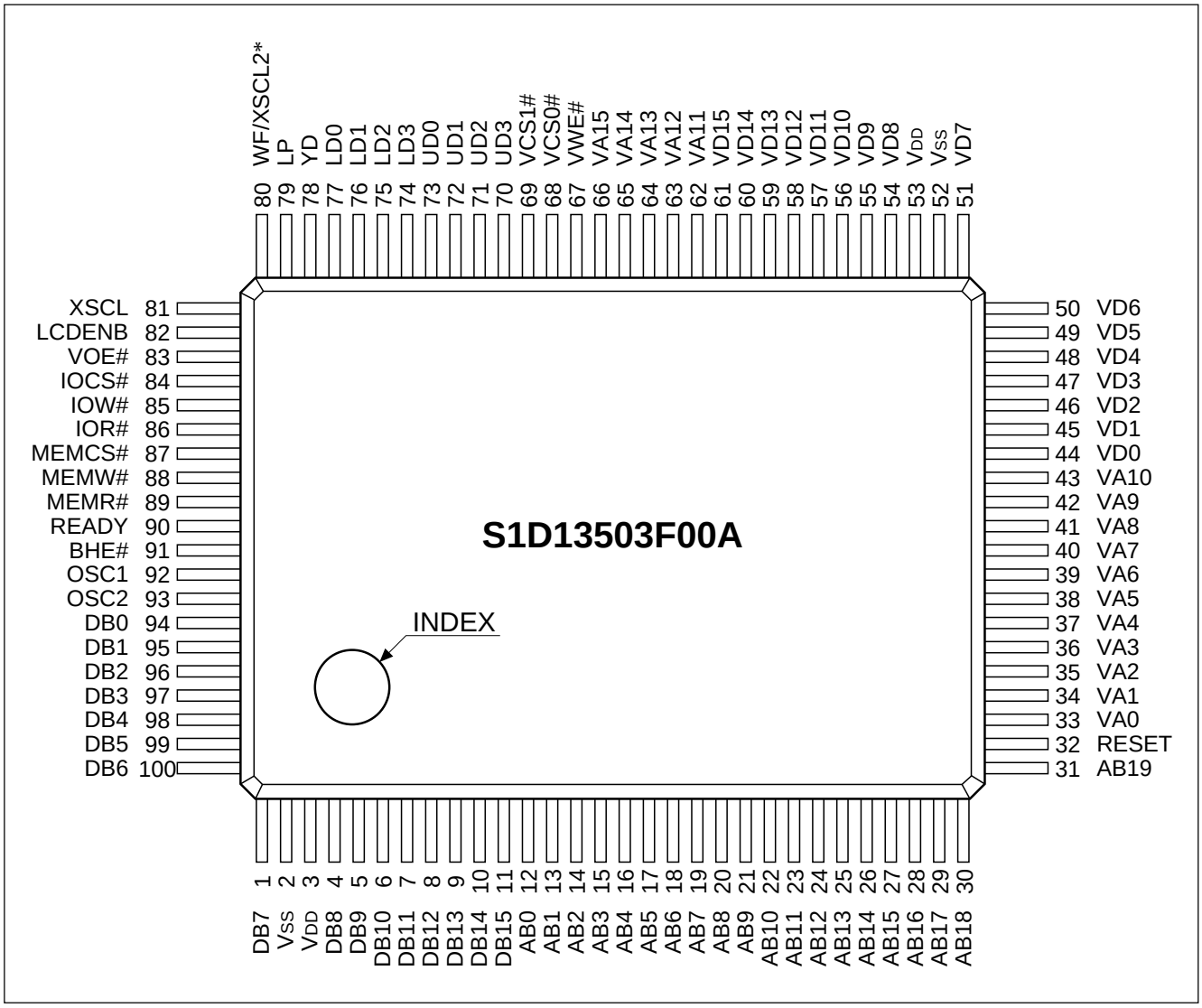
- MCLK = input clock
- MCLK = 1/2 input clock
- MCLK = 1/4 input clock

Pixel clock = input clock (f_{OSC})

SRAM Interface

This block generates the necessary signals to interface to the Display Memory (SRAM).

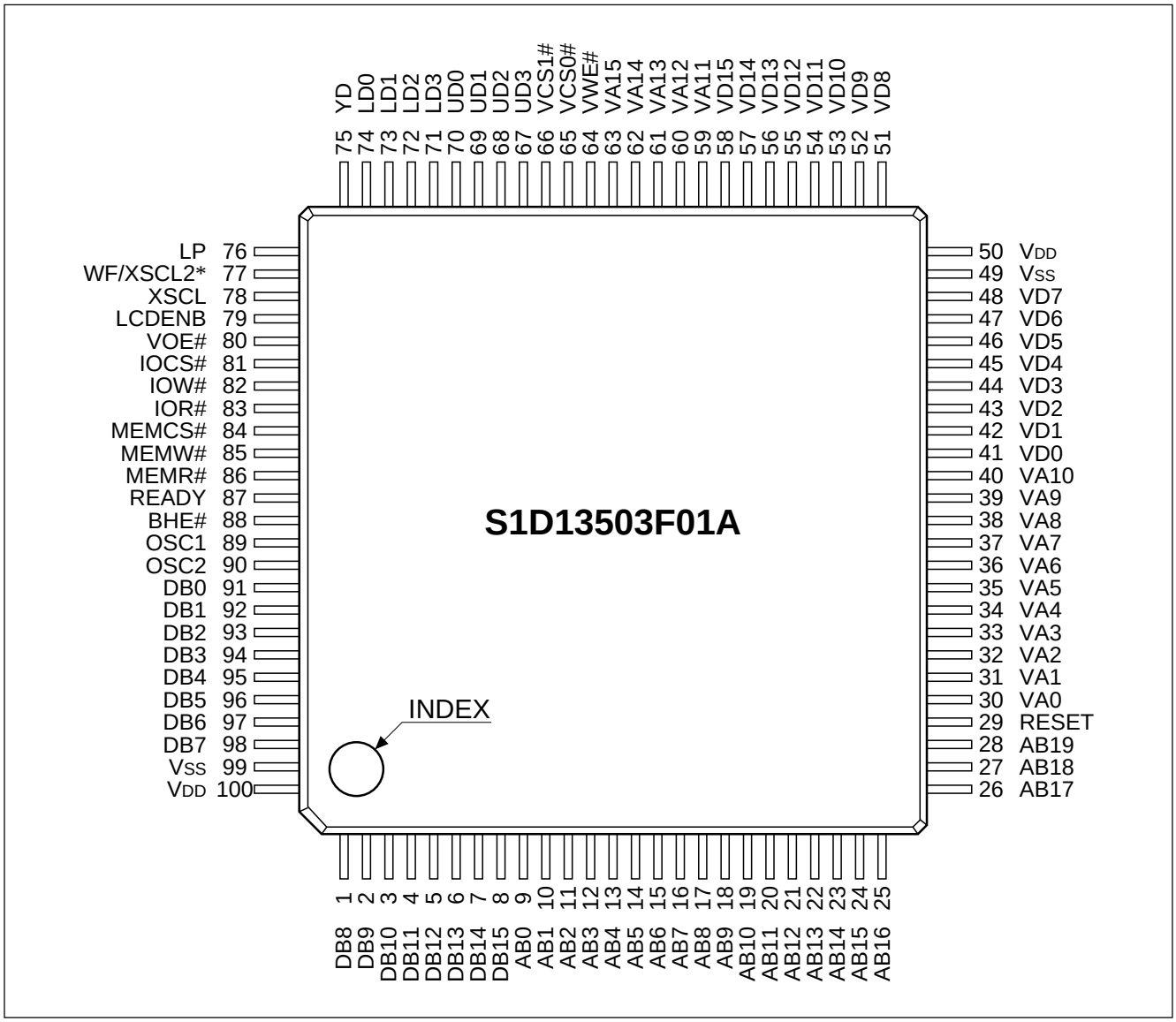
■ PINOUT DIAGRAM



S1D13503F00A Pinout Diagram

Note: Package type: 100 pin surface mount QFP5-S2

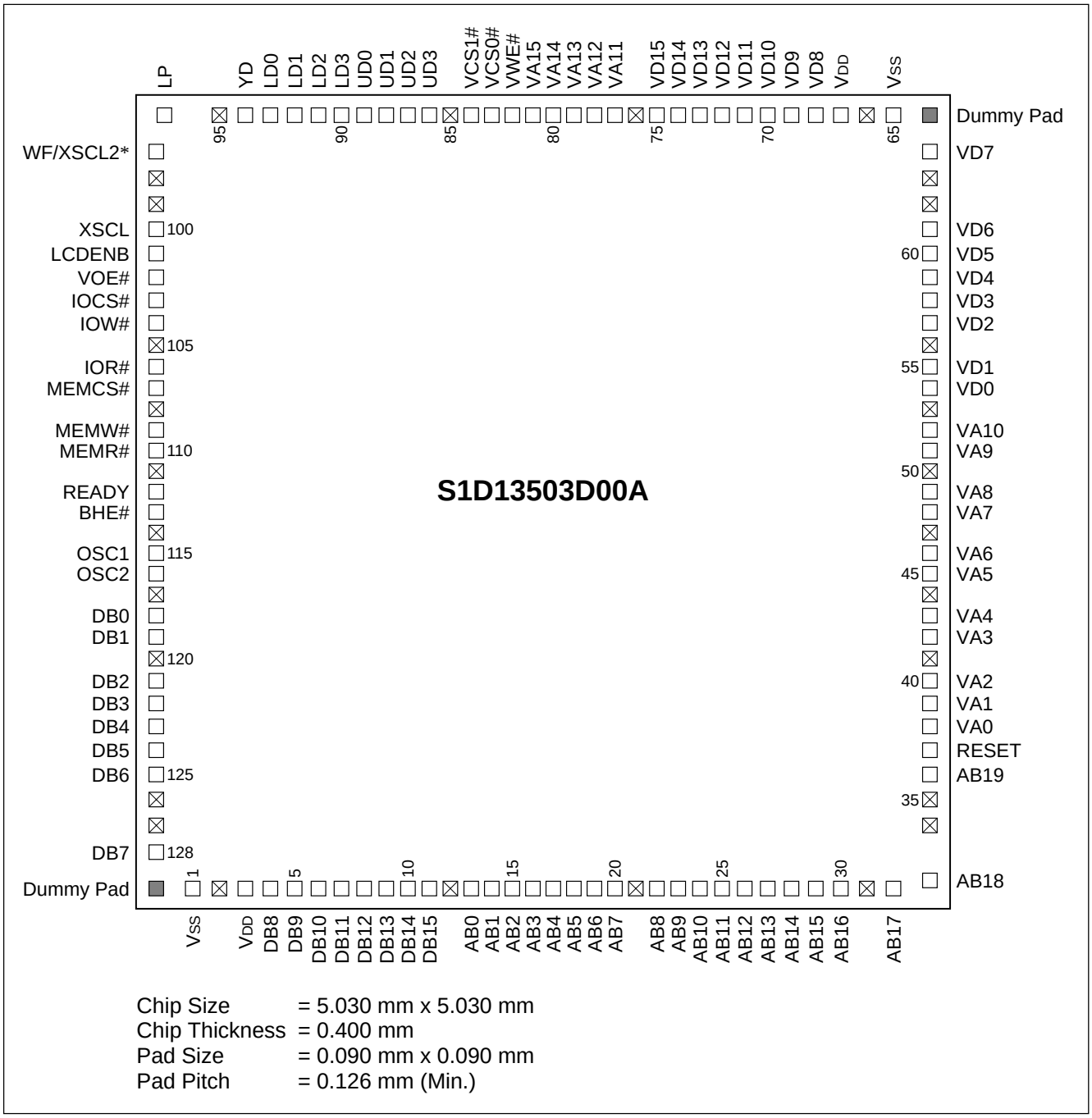
∗ Pin 80 = WF in all display modes except format 1 for 8-bit single color panel.
∗ Pin 80 = XSCL2 in format 1 for 8-bit single color panel.



S1D13503F01A Pinout Diagram

Note: Package type: 100 pin surface mount QFP15-STD

∗ Pin 77 = WF in all display modes except format 1 for 8-bit single color panel.
∗ Pin 77 = XSCL2 in format 1 for 8-bit single color panel.



S1D13503D00A Pad Diagram

∗ Pad 97 = WF in all display modes except format 1 for 8-bit single color panel.
∗ Pad 97 = XSCL2 in format 1 for 8-bit single color panel.

PAD Coordinates

(Unit: mm)

Pad No.	Pad Name	Pad Center Coordinate	
		X	Y
1	V_{SS}	-2.165	-2.390
2	–	-2.000	-2.390
3	V_{DD}	-1.840	-2.390
4	DB8	-1.685	-2.390
5	DB9	-1.535	-2.390
6	DB10	-1.388	-2.390
7	DB11	-1.246	-2.390
8	DB12	-1.106	-2.390
9	DB13	-0.969	-2.390
10	DB14	-0.835	-2.390
11	DB15	-0.703	-2.390
12	–	-0.573	-2.390
13	AB0	-0.444	-2.390
14	AB1	-0.317	-2.390
15	AB2	-0.190	-2.390
16	AB3	-0.063	-2.390
17	AB4	0.063	-2.390
18	AB5	0.190	-2.390
19	AB6	0.317	-2.390
20	AB7	0.444	-2.390
21	–	0.573	-2.390
22	AB8	0.703	-2.390
23	AB9	0.835	-2.390
24	AB10	0.969	-2.390
25	AB11	1.106	-2.390
26	AB12	1.246	-2.390
27	AB13	1.388	-2.390
28	AB14	1.535	-2.390
29	AB15	1.685	-2.390
30	AB16	1.840	-2.390
31	–	2.000	-2.390
32	AB17	2.165	-2.390
33	AB18	2.390	-2.340
34	–	2.390	-2.000
35	–	2.390	-1.840
36	AB19	2.390	-1.685
37	RESET	2.390	-1.535
38	VA 0	2.390	-1.388
39	VA 1	2.390	-1.246
40	VA 2	2.390	-1.106
41	–	2.390	-0.969
42	VA 3	2.390	-0.835
43	VA 4	2.390	-0.703
44	–	2.390	-0.573
45	VA 5	2.390	-0.444
46	VA 6	2.390	-0.317
47	–	2.390	-0.190
48	VA 7	2.390	-0.063
49	VA 8	2.390	0.063
50	–	2.390	0.190
51	VA 9	2.390	0.317
52	VA10	2.390	0.444
53	–	2.390	0.573
54	VD0	2.390	0.703
55	VD1	2.390	0.835
56	–	2.390	0.969
57	VD2	2.390	1.106
58	VD3	2.390	1.246
59	VD4	2.390	1.388
60	VD5	2.390	1.535
61	VD6	2.390	1.685
62	–	2.390	1.840
63	–	2.390	2.000
64	VD7	2.390	2.165
65	V_{SS}	2.165	2.390

Pad No.	Pad Name	Pad Center Coordinate	
		X	Y
66	–	2.000	2.390
67	V_{DD}	1.840	2.390
68	VD8	1.685	2.390
69	VD9	1.535	2.390
70	VD10	1.388	2.390
71	VD11	1.246	2.390
72	VD12	1.106	2.390
73	VD13	0.969	2.390
74	VD14	0.835	2.390
75	VD15	0.703	2.390
76	–	0.573	2.390
77	VA 11	0.444	2.390
78	VA 12	0.317	2.390
79	VA 13	0.190	2.390
80	VA 14	0.063	2.390
81	VA 15	-0.063	2.390
82	VWE#	-0.190	2.390
83	VCS0#	-0.317	2.390
84	VCS1#	-0.444	2.390
85	–	-0.573	2.390
86	UD3	-0.703	2.390
87	UD2	-0.835	2.390
88	UD1	-0.969	2.390
89	UD0	-1.106	2.390
90	LD3	-1.246	2.390
91	LD2	-1.388	2.390
92	LD1	-1.535	2.390
93	LD0	-1.685	2.390
94	YD	-1.840	2.390
95	–	-2.000	2.390
96	LP	-2.340	2.390
97	WF/XSCL2	-2.390	2.165
98	–	-2.390	2.000
99	–	-2.390	1.840
100	XSCL	-2.390	1.685
101	LCDENB	-2.390	1.535
102	VOE#	-2.390	1.388
103	IOCS#	-2.390	1.246
104	IOW#	-2.390	1.106
105	–	-2.390	0.969
106	IOR#	-2.390	0.835
107	MEMCS#	-2.390	0.703
108	–	-2.390	0.573
109	MEMW#	-2.390	0.444
110	MEMR#	-2.390	0.317
111	–	-2.390	0.190
112	READY	-2.390	0.063
113	BHE#	-2.390	-0.063
114	–	-2.390	-0.190
115	OSC1	-2.390	-0.317
116	OSC2	-2.390	-0.444
117	–	-2.390	-0.573
118	DB0	-2.390	-0.703
119	DB1	-2.390	-0.835
120	–	-2.390	-0.969
121	DB2	-2.390	-1.106
122	DB3	-2.390	-1.246
123	DB4	-2.390	-1.388
124	DB5	-2.390	-1.535
125	DB6	-2.390	-1.685
126	–	-2.390	-1.840
127	–	-2.390	-2.000
128	DB7	-2.390	-2.165
129	Dummy Pad	2.390	2.390
130	Dummy Pad	-2.390	-2.390

■ PIN DESCRIPTION

◆ Description

Key:

I = Input
O = Output
I/O = Bidirectional (Input/Output)
P = Power pin
COx = CMOS level output driver, x denotes driver type (see Table “Output Specifications” on page 15)
COxS = CMOS level output driver with slew rate control for noise reduction, x denotes driver type (see Table “Output Specifications” on page 15)
TSx = Tri-state CMOS level output driver, x denotes driver type (see Table “Output Specifications” on page 15)
TSxD2 = Tri-state CMOS level output driver with pull down resistor (typical values of 100 kΩ/200 kΩ at 5 V/3.0 V respectively), x denotes driver type (see Table “Output Specifications” on page 15)
TTL = TTL level input
TTLS = TTL level input with hysteresis

Bus Interface

Pin Name	Type	F00A Pin No.	F01A Pin No.	D00A Pad No.	Driver	Description
DB0–DB15	I/O	94–100, 1, 4 –11	91–98, 1–8	118–119, 121–125, 128, 4–11	TS2	These pins are connected to the system data bus. In 8-bit bus mode, DB8–DB15 must be tied to V_{DD}.
AB0	I	12	9	13	TTLS	In MC68000 MPU interface, this pin is connected to the Upper Data Strobe (UDS#) pin of MC68000. In other MPU/Bus interfaces, this pin is connected to the system address bus.
AB1–AB19	I	13–31	10–28	14–20, 22–30, 32–33, 36	TTL	These pins are connected to the system address bus.
BHE#	I	91	88	113	TTLS	In MC68000 MPU interface, this pin is connected to the Lower Data Strobe (LDS#) pin of MC68000. In other MPU/Bus interfaces, this pin is the Byte High Enable input for use with 16-bit system. In 8-bit bus mode tie the BHE# input to V_{DD}.
IOCS#	I	84	81	103	TTLS	Active low input to select one of sixteen internal registers.
IOW#	I	85	82	104	TTLS	In MC68000 MPU interface, this pin is connected to the R/W# pin of MC68000. This input pin defines whether the data transfer is a read (active high) or write (active low) cycle. In other MPU/Bus interfaces, this is the active low input to write data into an internal register.
IOR#	I	86	83	106	TTLS	In MC68000 MPU interface, this pin is connected to the AS# pin of MC68000. This input pin indicates a valid address is available on the address bus. In other MPU/Bus interfaces, this is the active low input to read data from an internal register.
MEMCS#	I	87	84	107	TTLS	Active low input to indicate a memory cycle.
MEMW#	I	88	85	109	TTLS	Active low input to indicate a memory write cycle. This pin should be tied to V_{DD} in an MC68000 MPU interface.
MEMR#	I	89	86	110	TTLS	Active low input to indicate a memory read cycle. This pin should be tied to V_{DD} in an MC68000 MPU interface.
READY	O	90	87	112	TS3	For MC68000 MPU interface, this pin is connected to the DTACK# pin of MC68000 and is driven low when the data transfer is complete. In other MPU/Bus interfaces, this output is driven low to force the system to insert wait states when needed. READY is placed in a high impedance (Hi-Z) state after the transfer is completed.
RESET	I	32	29	37	TTLS	Active high input to force all signals to their inactive states.

Display Memory Interface

Pin Name	Type	F00A Pin No.	F01A Pin No.	D00A Pad No.	Driver	Description
VD0–VD15	I/O	44–51, 54–61	41–48, 51–58	54–55, 57–61, 64, 68–75	TS1D2	These pins are connected to the display memory data bus. For 16-bit interface, VD0–VD7 are connected to the display memory data bus of even byte addresses and VD8–VD15 are connected to the display memory data bus of odd byte addresses. The output drivers of these pins are placed in a high impedance state when RESET is high. On the falling edge of RESET, the values of VD0–VD15 are latched into the chip to configure various hardware options(see Table “Summary of Power On/Reset Options” on page 13).
VA0–VA15	O	33–43, 62–66	30–40, 59–63	38–40, 42–43, 45–46, 48–49, 51–52, 77–81	CO1	These pins are connected to the display memory address bus.
VCS1#	O	69	66	84	CO1	Active low chip-select output to the second or odd byte address SRAM. See Display Memory Interface section for details.
VCS0#	O	68	65	83	CO1	Active low chip-select output to the first or even byte address SRAM. See Display Memory Interface section for details.
VWE#	O	67	64	82	CO1	Active low output used for writing data to the display memory. This pin is connected to the WE# input of the SRAMs.
VOE#	O	83	80	102	CO1	Active low output to enable reading of data from the display memory. This pin is connected to the OE# input of the SRAMs.

LCD Interface

Pin Name	FPDI-1™ Pin Name #1	Type	F00A Pin No.	F01A Pin No.	D00A Pad No.	Driver	Description
UD3–UD0 LD3–LD0	UD3–UD0 LD3–LD0	O	70–73, 74–77	67–70, 71–74	86–89, 90–93	CO3S	Panel display data bus. The data format depends on the specific panel connected. For 4-bit single panels, LD3–LD0 are driven low (0 state).
XSCL	FPSHIFT	O	81	78	100	CO3	Display data shift clock. Data is shifted into the LCD X-drivers on the falling edge of this signal.
LP	FPLINE	O	79	76	96	CO3	Display data latch clock. The falling edge of this signal is used to latch a row of display data in the LCD X-drivers and to turn on the Y driver (row driver).
WF/ XSCL2	MOD FPSHIFT2	O	80	77	97	CO3	For format 1 of 8-bit single color panels this is the second shift clock. For all other modes, this is the LCD backplane BIAS signal. This output toggles once every frame, or as programmed in AUX[05] bits 7–2.
YD	FPFRAME	O	78	75	94	CO3	Vertical scanning start pulse. A logic ‘1’ on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel Y driver (row driver) to indicate the start of the vertical frame.
LCDENB		O	82	79	101	CO2	LCD enable signal output. It can be used externally to turn off the panel supply voltage and backlight.

#1: VESA Flat Panel Display Interface Standard (FPDI-1TM)

Clock Inputs

Pin Name	Type	F00A Pin No.	F01A Pin No.	D00A Pad No.	Driver	Description
OSC1	I	92	92	115	*	This pin, along with OSC2, is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
OSC2	O	93	93	116	*	This pin, along with OSC1, is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source this pin should be left unconnected.

Power Supply

Pin Name	Type	F00A Pin No.	F01A Pin No.	D00A Pad No.	Driver	Description
V_{DD}	P	3, 53	50, 100	3, 67	P	Voltage supply.
V_{SS}	P	2, 52	49, 99	1, 65	P	Voltage ground.

◆ Summary of Configuration Options

The S1D13503 requires some configuration information on power-up. This information is provided through the SRAM data lines VD[0...15]. The state of these pins are read on the falling edge of RESET and used to configure the following options:

Summary of Power On / Reset Options

Pin Name	Value on this pin at falling edge of RESET is used to configure: (1/0)	
	1	0
VD0	16-bit host bus interface	8-bit host bus interface
VD1	Use direct-mapping for I/O accesses	Use internal index register for I/O accesses
VD2	MC68000 MPU interface	MPU / Bus interface with memory accesses controlled by a READY (WAIT#) signal
VD3	Swap of high and low data bytes in 16-bit bus inter-face	No byte swap of high and low data bytes in 16-bit bus interface
VD12–VD4	Select I/O mapping address bits [9:1]. These nine bits are latched on power-up and are compared to the MPU address bits [9–1]. A valid I/O cycle combined with a valid address will enable the internal I/O decoder. Therefore, both types of I/O mapping are limited to even address boundaries to determine either the absolute or indexed I/O address of the first register. Note that a “valid I/O cycle” includes IOCS# being toggled low.	
VD15–VD13	Select memory mapping address bits [3:1] These three bits are latched on power-up and are compared to the MPU address bits [19–17]. A valid memory cycle combined with a valid address will enable the internal memory decoder. As only the three most significant bits of the address are compared, the maximum amount of memory supported is 128K bytes. Note that a “valid memory cycle” includes MEMCS# being toggled low. When using 128K-byte memory it must be mapped at an even address such that all 128K bytes is available without a change in state on A17, as this would invalidate the internal compare logic.	

Note : The S1D13503 has internal pull down resistors on these pins and therefore will be pulled down and read on a logic “0” after RESET. If pull up resistors are required refer to Table “Input Specifications” on page 16 for pull down resistor values.

Example: If an ISA bus (no byte swap) with memory segment “A” and I/O location 300h are used, the corresponding settings of VD15-VD0 would be:

I/O and Memory Addressing Example

Pin Name	8-Bit ISA Bus		16-Bit ISA Bus	
	Index Register	Direct Mapping	Index Register	Direct Mapping
VD0	0	0	1	1
VD1	0	1	0	1
VD2	0	0	0	0
VD3	0	0	0	0
VD12–VD4	11 0000 000	11 0000 xxx	11 0000 000	11 0000 xxx
VD15–VD13	101	101	101	101

Where x = don't care; 1 = connected to pull-up resistor; 0 = no pull-up resistor

■ D.C. CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	-0.3 to +6.0	V
V_{IN}	Input Voltage	-0.3 to V_{DD} + 0.5	V
V_{OUT}	Output Voltage	-0.3 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. Max. at lead	°C

Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	V_{SS} = 0V	2.7	3.0/3.3/5.0	5.5	V
V_{IN}	Input Voltage	–	V_{SS}	–	V_{DD}	V
I_{OPR}	Operating Current	f_{OSC} = 6MHz 256 colors	–	4.5/5.0/11	–	mA
T_{OPR}	OperatingTemperature	–	-40	25	85	°C

Input Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Low Level Input Voltage	V_{DD} = 4.5V	–	–	0.8	V
		V_{DD} = 3.0V	–	–	0.4	
		V_{DD} = 2.7V	–	–	0.3	
V_{IH}	High Level Input Voltage	V_{DD} = 5.5V	2.0	–	–	V
		V_{DD} = 3.6V	1.3	–	–	
		V_{DD} = 3.3V	1.2	–	–	
V_{T+}	Positive-going Threshold	V_{DD} = 5.0V	–	–	2.4	V
		V_{DD} = 3.3V	–	–	1.4	
		V_{DD} = 3.0V	–	–	1.3	
V_{T-}	Negative-going Threshold	V_{DD} = 5.0V	0.6	–	–	V
		V_{DD} = 3.3V	0.5	–	–	
		V_{DD} = 3.0V	0.4	–	–	
V_H	Hysteresis Voltage	V_{DD} = 5.0V	0.1	–	–	V
		V_{DD} = 3.3V	0.1	–	–	
		V_{DD} = 3.0V	0.1	–	–	
I_{IZ}	Input Leakage Current	–	-1	–	1	µA
C_{IN}	Input Pin Capacitance	f = 1MHz V_{DD} = 0V	–	–	12	pF
R_{PD}	Pull Down Resistance	V_{DD} = 5.0V V_I = V_{DD}	50	100	200	kΩ
		V_{DD} = 3.3V V_I = V_{DD}	90	180	360	
		V_{DD} = 3.0V V_I = V_{DD}	100	200	400	

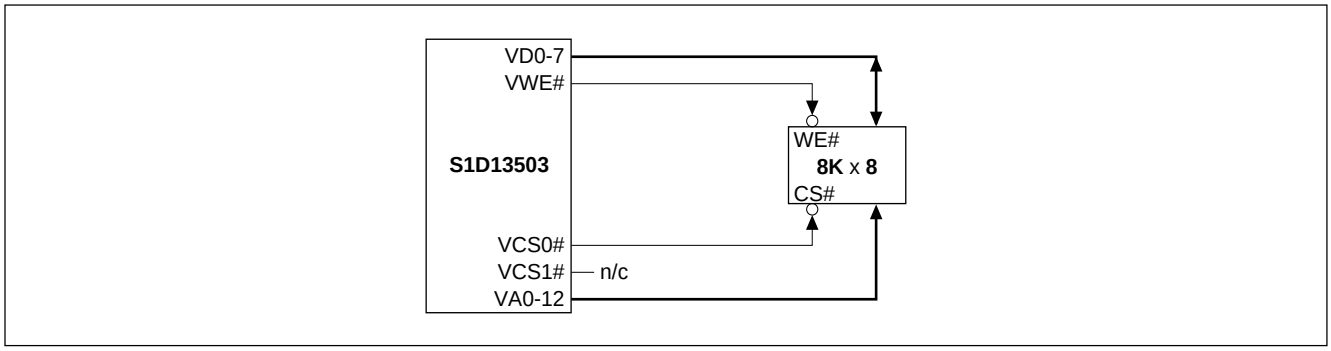
Output Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OL} (5.0V)	Low Level Output Voltage Type 1 -TS1D2, CO1 Type 2 -TS2 Type 3 -TS3, CO3, CO3S	V_{DD} = Min. I_{OL} = 4mA I_{OL} = 8mA I_{OL} = 12mA	–	–	0.4	V
V_{OL} (3.3V)	Low Level Output Voltage Type 1 -TS1D2, CO1 Type 2 -TS2 Type 3 -TS3, CO3, CO3S	V_{DD} = Min. I_{OL} = 2mA I_{OL} = 4mA I_{OL} = 6mA	–	–	0.3	V
V_{OL} (3.0V)	Low Level Output Voltage Type 1 -TS1D2, CO1 Type 2 -TS2 Type 3 -TS3, CO3, CO3S	V_{DD} = Min. I_{OL} = 1.8mA I_{OL} = 3.5mA I_{OL} = 5mA	–	–	0.3	V
V_{OH} (5.0V)	High Level Output Voltage Type 1 -TS1D2, CO1 Type 2 -TS2 Type 3 -TS3, CO3, CO3S	V_{DD} = Min. I_{OH} = -4mA I_{OH} = -8mA I_{OH} = -12mA	V_{DD}-0.4	–	–	V
V_{OH} (3.3V)	High Level Output Voltage Type 1 -TS1D2, CO1 Type 2 -TS2 Type 3 -TS3, CO3, CO3S	V_{DD} = Min. I_{OH} = -2mA I_{OH} = -4mA I_{OH} = -6mA	V_{DD}-0.3	–	–	V
V_{OH} (3.0V)	High Level Output Voltage Type 1 -TS1D2, CO1 Type 2 -TS2 Type 3 -TS3, CO3, CO3S	V_{DD} = Min. I_{OH} = -1.8mA I_{OH} = -3.5mA I_{OH} = -5mA	V_{DD}-0.3	–	–	V
I_{OZ}	Output Leakage Current	–	-1	–	1	µA
C_{OUT}	Output Pin Capacitance	f = 1MHz V_{DD} = 0V	–	–	12	pF
C_{BID}	Bidirectional Pin Capacitance	f = 1MHz V_{DD} = 0V	–	–	12	pF

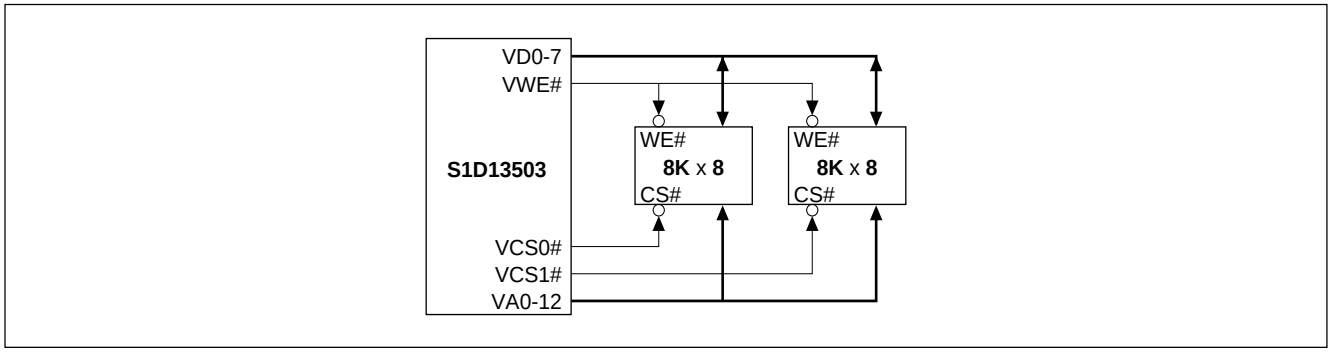
■ DISPLAY MEMORY INTERFACE

◆ SRAM Configurations Supported

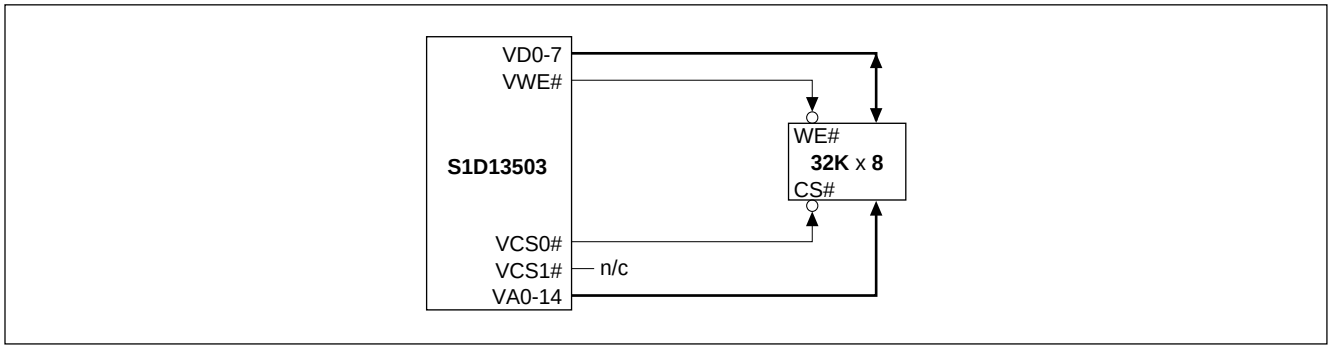
8-Bit Mode



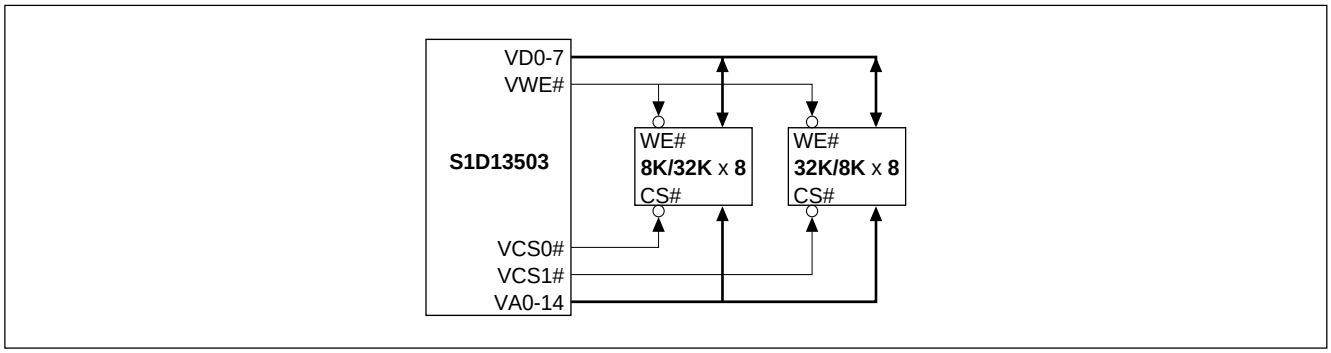
8-Bit Mode - 8K bytes SRAM
(Requires AUX[01] bit 0 = 0)



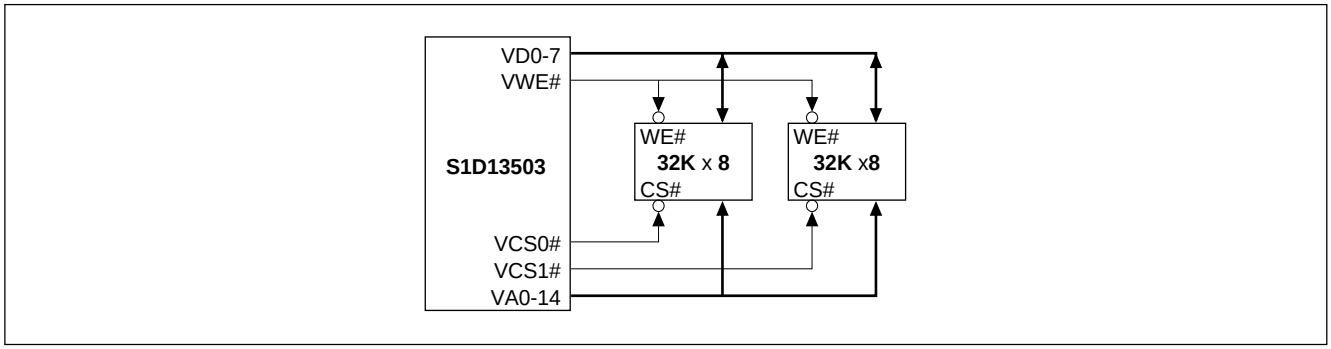
8-Bit Mode - 16K bytes SRAM
(Requires AUX[01] bit 0 = 0)



8-Bit Mode - 32K bytes SRAM
(Requires AUX[01] bit 0 = 1)

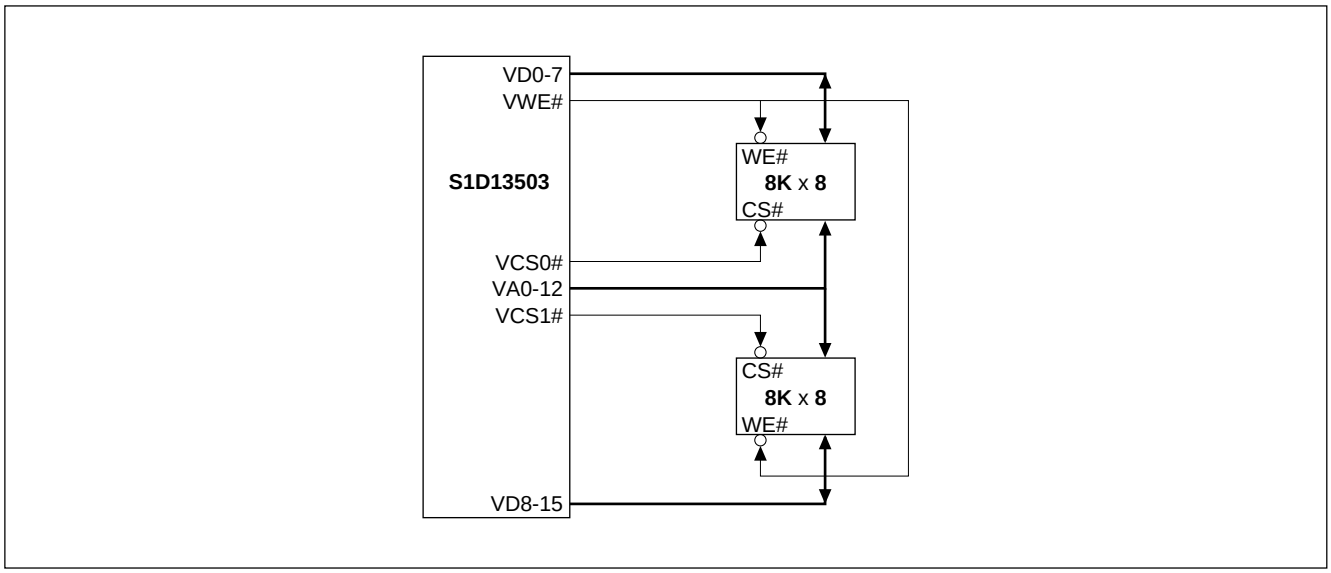


8-Bit Mode - 40K bytes SRAM
[Either (8K x 8 + 32K x 8) requiring AUX[01] bit 0 = 0 or (32K x 8 + 8K x 8) requiring AUX[01] bit 0 = 1]

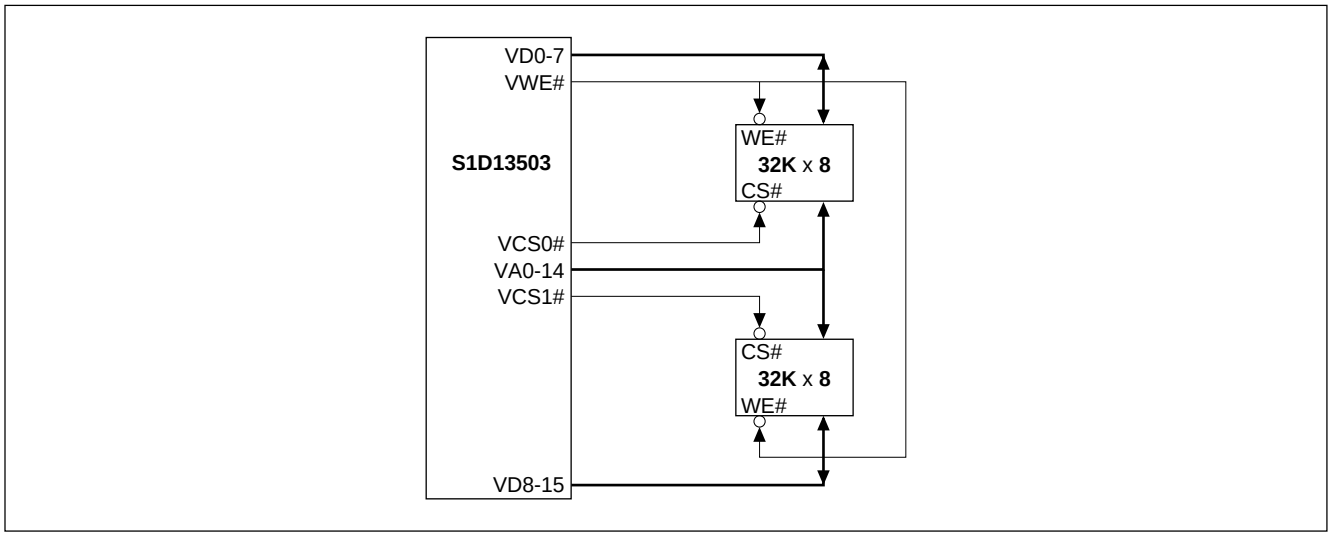


8-Bit Mode - 64K bytes SRAM
(Requires AUX[01] bit 0 = 1)

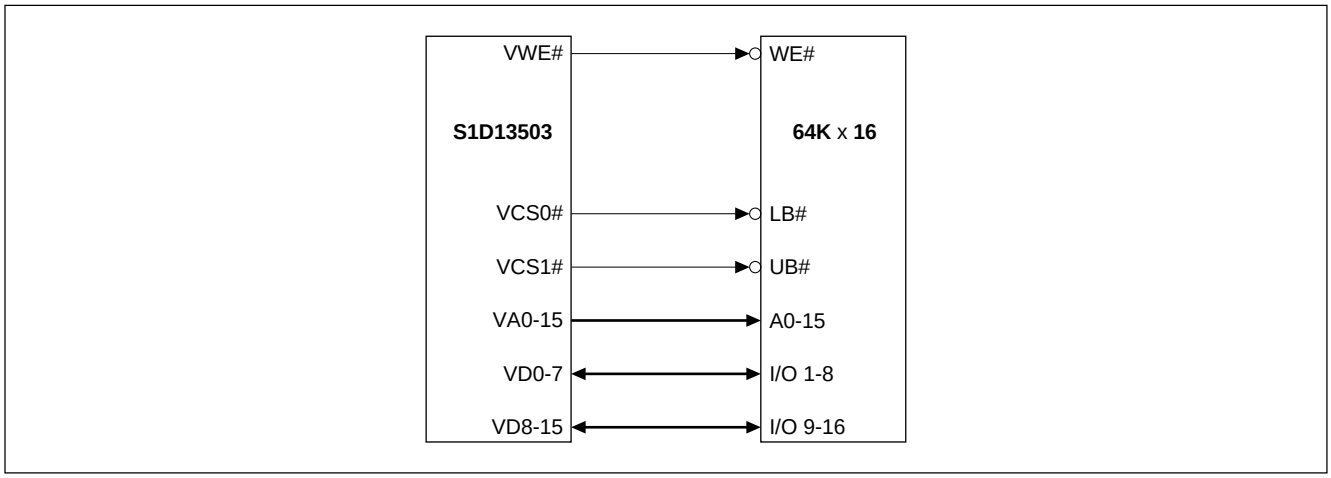
16-Bit Mode



16-Bit Mode - 16K bytes SRAM



16-Bit Mode - 64K bytes SRAM

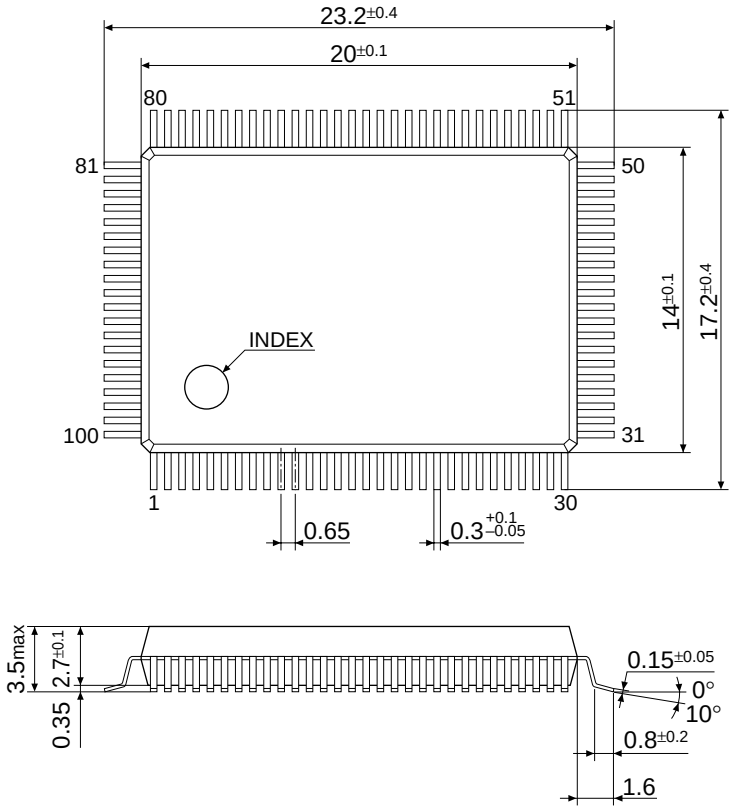


16-Bit Mode - 128K bytes SRAM

■ MECHANICAL DATA

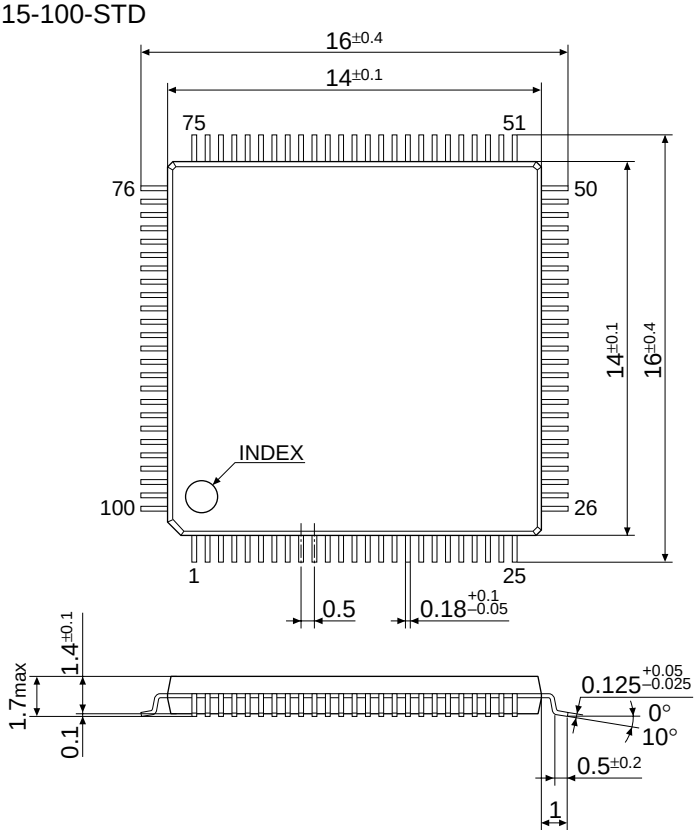
Mechanical Drawing QFP5-100-S2

Unit: mm



Mechanical Drawing QFP15-100-STD

Unit: mm



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