RAiO

# RA8816N

## 144x65 Character / Graphic LCD Driver Specification

Version 1.0

February 19, 2013

RAiO Technology Inc.

# 1. General Description

The RA8816N is a Dot-Matrix LCD Driver that supports both character and graphic modes. It has a built-in 256K bytes character ROM and 1170 bytes display RAM. The embedded ROM consists of Chinese (or Japanese for –J product), English and ASCII fonts, and the embedded display RAM supports up to 144x65 dots LCD panel. The RA8816N also provides a scrolling buffer memory for scrolling functions. It supports vertical and horizontal scrolling features, and all of these functions are executed by hardware.

In character mode, the RA8816N supports Traditional Chinese (BIG5), Simplified Chinese (GB) and Japanese (S-JIS) code. The system (MPU) does not need to take a lot of time to show the Chinese or Japanese font in this mode. It also provides small ASCII (8x8) and big ASCII (8x16) fonts for English, Japanese, European and Latin character. The RA8816N also integrates much powerful hardware that includes contrast adjustment, 4x5 Key-Scan and eight General Purpose I/Os.

The RA8816N is a highly integrated chip of LCD controller and driver. It reduces a lot of time for system development, and saves much cost for hardware system that due to it provides many features for related LCD display applications.

# 2. Feature

- Support both Character and Graphic Mode
- Support 8080 / 6800, 8 / 4-bit Parallel Interface, 3-Wire / 4-Wire Serial Interface
- Built-in 256KB Font ROM: Chinese, S-JIS, English, ASCII, Japanese, Latin, Latin-ext A, Latin-ext B
- Support ASCII 8x8 / 8x16 Half Size Font, 16x16 Full Size Chinese Font
- Support Maximum 144 SEG x 65 COM LCD Panel. 4 x 9 Chinese Fonts (16x16), or 8 x 18 English Fonts (8x8)
- Built-in 256 bytes SRAM for Create Font
- Built-in 1170 bytes Display RAM and 450 bytes Scrolling Buffer
- Support 1/65 Duty, 1/9~1/5 Bias Panel
- Built-in 2X~4X (Voltage Booster), Voltage Regulator, Voltage Follower
- Eight General Purpose I/Os (GPIO)
- Built-in 4x5 Key-scan Circuit
- Support Horizontal / Vertical Scrolling Functions
- Provide 32-Steps Contrast Adjuster
- Build-in RC Oscillator
- Voltage Operation: VDD → 2.7~3.6V
- Package: Gold Bump Die

**Table 2-1 : Ordering Information**

| Parts Number | Package and Font Type |
|---|---|
| RA8816N-T | Au-Bump Die, Traditional Chinese (BIG5) |
| RA8816N-S | Au-Bump Die, Simplified Chinese (GB2312) |
| RA8816N-J | Au-Bump Die, Japanese (S-JIS) |

## 3. Block Diagram

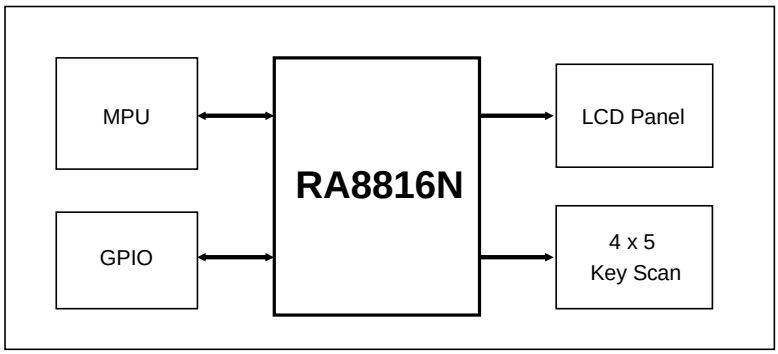


**Figure 3-1 : System Block**

The RA8816N is consisted of Display RAM, 256KB Font ROM, Command Registers, LCD Controller, LCD Driver, Voltage Booster, Voltage Regulator, MPU Interface and Key-Scan circuit.

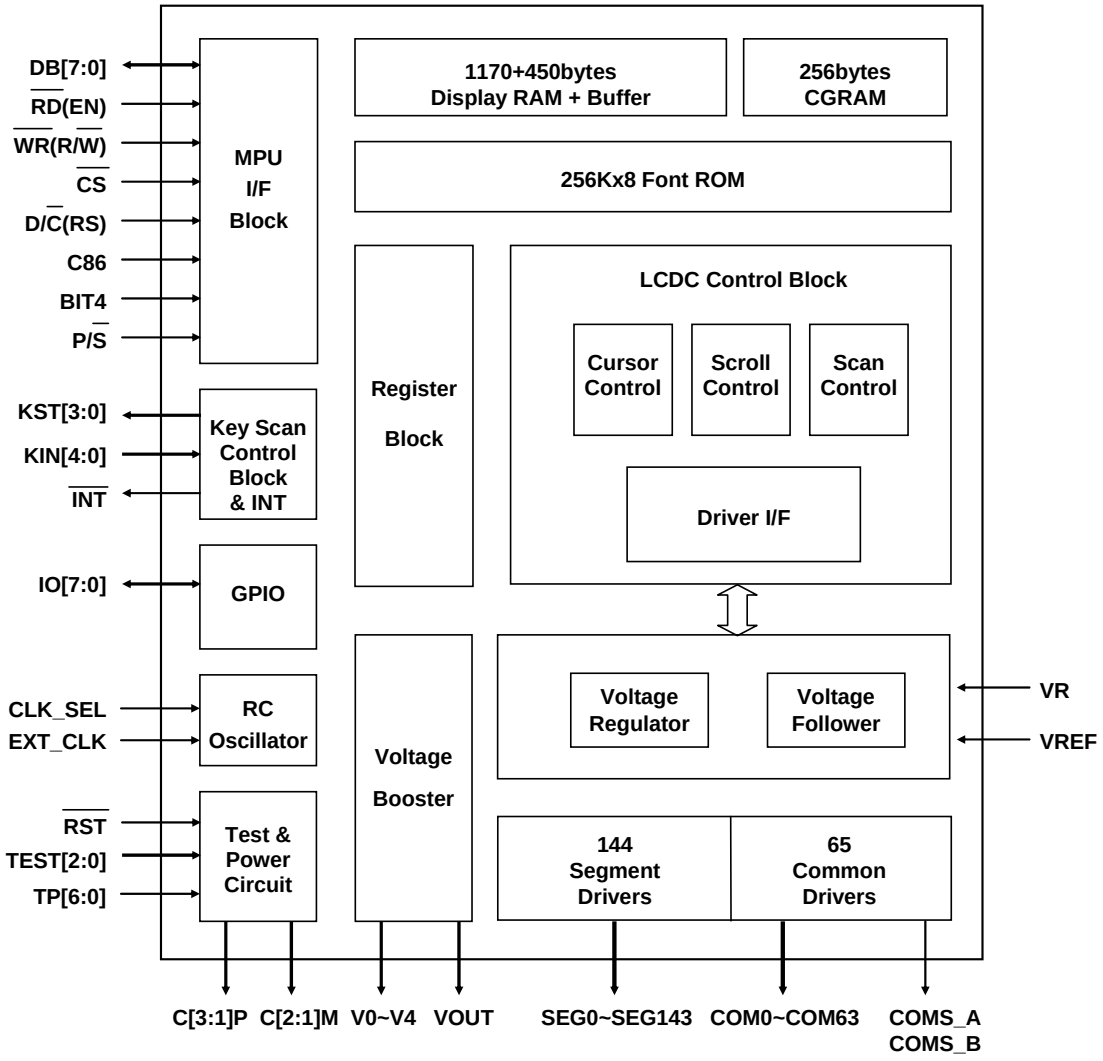


**Figure 3-2 : Internal Block**

# 4. Pin Definition

## 4-1 MPU Interface

**Table 4-1**

| Pin Name | I/O | Description |
|---|---|---|
| DB[7:0]<br><br>DB0: SCK<br>DB1: SDA/SDO<br>DB2: RS/SDI<br>DB3: $\overline{CS}$<br>DB[7:6]: SMOD | I/O | **Data Bus**<br>When MPU uses parallel mode and 8-bit interface then all of the DB[7:0] are valid. When uses 4-bit interface then only DB[3:0] are valid, and DB[7:4] have to be kept floating.<br>When P/$\overline{S}$ is "0", then the interface between MPU and RA8816N is Serial Mode. The pins DB[7:6] (SMOD[1:0]) are used to select which serial mode:<br>**SMOD : Serial Mode**<br>0 0 : Reserved.<br>0 1 : 3-Wire, SCK, SDA, $\overline{CS}$ are used.<br>1 0 : 4-Wire, SCK, SDA, RS, $\overline{CS}$ are used.<br>1 1 : 4-Wire, SCK, SDO, SDI, $\overline{CS}$ are used.<br>In serial mode, all of the related signals are defined by DB[3:0]:<br>SCK (DB0) : Serial Clock.<br>SDA (DB1) : Bi-direction Mode Serial Data.<br>SDO (DB1) : Data Out.<br>RS (DB2) : Memory/Register Cycle Select.<br>SDI (DB2) : Serial Data In.<br>$\overline{CS}$ (DB3) : Chip Select, active low. |
| $\overline{RD}$<br>EN | I | **Read Control or Enable**<br>When use 8080 series interface, $\overline{RD}$ is the read signal and active low.<br>When use 6800 series interface, EN is the Enable signal and active high.<br>This pin must be kept high for 3 or 4-wires serial mode. |
| $\overline{WR}$<br>R/$\overline{W}$ | I | **Write Control or Read-Write Control**<br>When use 8080 series interface, $\overline{WR}$ is the write signal and active low.<br>When use 6800 series interface, this pin is R/$\overline{W}$, active high for read cycle and active low for write cycle.<br>This pin must be kept high for 3 or 4-wires serial mode. |
| D/$\overline{C}$<br>RS | I | **Data/Command Select or Register Select**<br>When use 8080 series interface, this is Data or Command signal. When D/$\overline{C}$ is "0", means Register Cycle (or Command Cycle). When D/$\overline{C}$ is "1", means Data Access Cycle (Data Cycle).<br>When use 6800 series interface, this is the RS signal. When RS is "0", means Register Cycle and "1" means Data Access Cycle.<br>This pin must be kept high for serial mode. |
| $\overline{CS}$ | I | **Chip Select**<br>This is chip enable for RA8816N.<br>This pin must be kept high for serial mode. |
| $\overline{INT}$ | O | **Interrupt Signal**<br>This is an interrupt output for MPU. Active low。 |
| C86 | I | **MPU Select**<br>C86 = 0 ➔ The MPU interface is 8080 series.<br>C86 = 1 ➔ The MPU interface is 6800 series (Default).<br>This pin must be kept high for serial mode. |

| Pin Name | I/O | Description |
|---|---|---|
| BIT4 | I | **Data Bit Select**<br>BIT4 = 0➔ The parallel mode is use 8-bit data bus.<br>BIT4 = 1➔ The parallel mode is use 4-bit data bus (Default).<br>This pin must be kept high for serial mode. |
| P/$\overline{S}$ | I | **Parallel/Serial Select**<br>P/$\overline{S}$ = 0 ➔ The MPU interface is serial mode (Default). See the setting of DB[7:6].<br>P/$\overline{S}$ = 1 ➔ The MPU interface is parallel mode. |

## 4-2 Clock and Power

**Table 4-2**

| Pin Name | I/O | Description |
|---|---|---|
| V0~V4 | O | **Voltage Source of LCD Driver**<br>The relationship of the power is VOUT>V0≧V1≧V2≧V3≧V4≧VSS |
| C[3:1]P, C[2:1]N | I | **Capacitor Input**<br>These are used to connect capacitors for internal Booster. |
| VOUT | O | **Booster Output** |
| VREF | I | **Reference Voltage Input**<br>This is the external reference voltage input when the internal one is disabled. |
| VR | I | **Voltage Adjustment**<br>Applies voltage between V0 and VSS by connecting a resistor divider. |
| CLK_SEL | I | **Clock Select**<br>This pin is used to select the clock source. When CLK_SEL is “1”, the clock is generated by internal RC oscillator. When CLK_SEL is “0”, the system clock is driven by external pin - EXT_CLK. |
| EXT_CLK | I | **External Clock**<br>When CLK_SEL is “0”, this pin is the external clock input. When CLK_SEL is “1”, this pin is not used and has to be connected to VDD or GND. |
| VDD<br>VDDP | P | **Power** |
| GND<br>GNDP | P | **Ground** |

## 4-3 LCD Panel Interface

**Table 4-3**

| Pin Name | I/O | Description |
|---|---|---|
| SEG0 ~ SEG143 | O | **Segment Signals for Panel** |
| COM0 ~ COM63 | O | **Common Signals for Panel** |
| COMS_A<br>COMS_B | O | **Icon Common Signals for Panel** |
| DUMY[5:0] | O | **Dummy PAD** |

## 4-4 Misc.

**Table 4-4**

| Pin Name | I/O | Description |
|---|---|---|
| KST[3:0] | O | **Key Strobe Output** |
| KIN[4:0] | I | **Key Data Input**<br>For pins that are not used, please connect them to VDD. |
| IO[7:0] | I/O | **General Purpose I/O** |
| $\overline{RST}$ | I | **Reset**<br>RST=0, RA8816N will be reset.<br>RST=1, Normal condition. |
| TEST[2:0] | I | **Test Pins**<br>These pins must be connected to GND in normal mode. |
| TP[6:0] | I | **Test Pins**<br>These pins must be kept NC for normal mode. |

**Table 4-5 : Pin Definition of Parallel / Serial Mode of MPU**

| Pin Name | I/O | Parallel Mode | | | | Serial Mode | | |
|---|---|---|---|---|---|---|---|---|
| | | 8080 | | 6800 | | 3-Wire | 4-Wire (A-Type) | 4-Wire (B-Type) |
| | | 8Bit | 4Bit | 8Bit | 4Bit | | | |
| DB7 | I/O | DB7 | --*1 | 0 | -- | 0 | 1 | 1 |
| DB6 | I/O | DB6 | -- | 1 | -- | 2 | 0 | 1 |
| DB5 | I/O | DB5 | -- | -- | -- | -- | -- | -- |
| DB4 | I/O | DB4 | -- | -- | -- | -- | -- | -- |
| DB3 | I/O | DB3 | DB3 | DB3 | DB3 | $\overline{CS}$ | $\overline{CS}$ | $\overline{CS}$ |
| DB2 | I/O | DB2 | DB2 | DB2 | DB2 | -- | RS | SDI |
| DB1 | I/O | DB1 | DB1 | DB1 | DB1 | SDA | SDA | SDO |
| DB0 | I/O | DB0 | DB0 | DB0 | DB0 | SCK | SCK | SCK |
| $\overline{RD}$ , EN | I | $\overline{RD}$ | $\overline{RD}$ | EN | EN | 1*2 | 1*2 | 1*2 |
| $\overline{WR}$ , R/$\overline{W}$ | I | $\overline{WR}$ | $\overline{WR}$ | R/$\overline{W}$ | R/$\overline{W}$ | 1*2 | 1*2 | 1*2 |
| D/$\overline{C}$ , RS | I | D/$\overline{C}$ | D/$\overline{C}$ | RS | RS | 1*2 | 1*2 | 1*2 |
| $\overline{CS}$ | I | $\overline{CS}$ | $\overline{CS}$ | $\overline{CS}$ | $\overline{CS}$ | 1 | 1 | 1 |
| C86 | I | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| BIT4 | I | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| P/$\overline{S}$ | I | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

Note1 : "--" means the pin is not used and kept floating (NC).

Note2 : In serial mode, the unused parallel pins have to be connected to high (VDD).

# 5. Pin Diagram

## 5-1 COG Pad

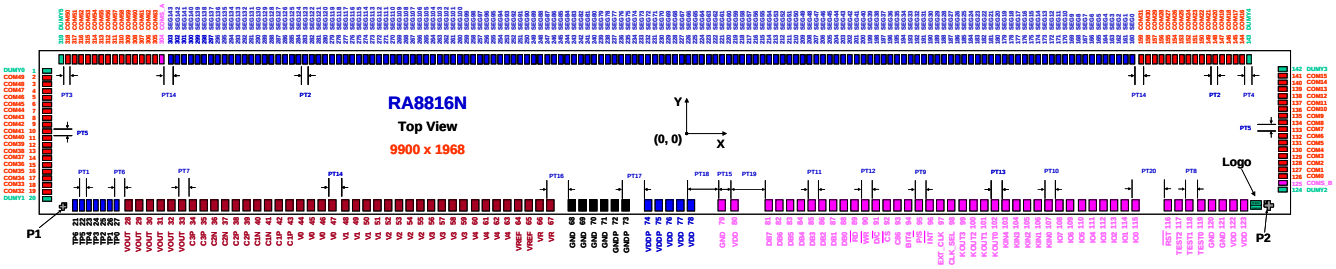


**Figure 5-1：Pin Diagram**

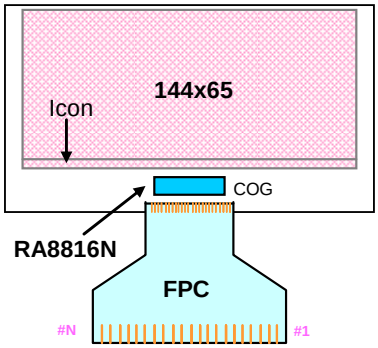


**Figure 5-2 : COG Module**