MICRO NETWORKS

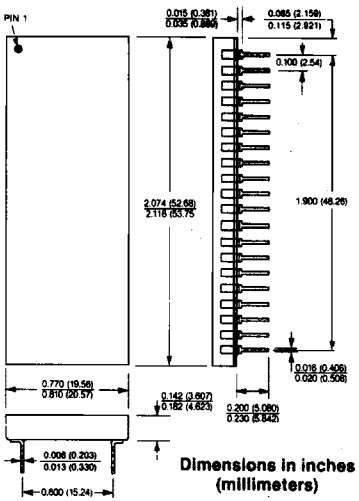
MN5245
MN5246

1.1 MHz, 12-Bit
A/D CONVERTERS

FEATURES

- 850nsec Maximum Conversion Time
- Guaranteed 1.1MHz Conversion Rate
- 1MHz Sampling Rate When used with MN376 T/H Amplifier
- Multisourced
- Small 40-Pin DIP
- No Missing Codes Guaranteed Over Temperature
- TTL Compatible
- 3-State Output Buffer (MN5245A, MN5246A)
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

40 PIN DIP



Dimensions in inches (millimeters)

DESCRIPTION

MN5245, MN5245A, MN5246 and MN5246A are 850nsec, 12-bit, A/D converters that guarantee 1.1MHz conversion rates. When used with MN376 High-Speed T/H Amplifiers, these A/D's can be configured to form bonafide, 1MHz, sample-and-convert systems that can digitize full-scale (5V) input signals with bandwidths up to 500kHz. These systems typically achieve signal-to-noise ratios of 70dB with harmonics down more than −80dB while digitizing 500kHz signals at the Nyquist rate.

Packaged in standard, 40-pin, hermetically sealed, ceramic dual-in-lines, MN5245 and MN5246 A/D converters offer an outstanding combination of resolution, speed, size and cost. These TTL compatible devices achieve their sub-1usec conversion speed using the digitally corrected subranging (serial-parallel) A/D conversion technique. Recent advances in monolithic flash A/D converters and improvements in digital error correcting techniques have enabled us to reduce chip count over previous designs while improving performance.

MN5245 has a 0 to +5V analog input range; while MN5246 has a ±2.5V analog input range. "A" versions of each device contain internal 3-state output buffers to facilitate microprocessor interfacing. All models guarantee ±0.024% FSR integral linearity and "no missing codes" for 12 bits over their entire specified temperature ranges.

MN5245 and MN5246 are ideal design solutions for high-speed digitizing applications in which speed, accuracy, size and reliability are paramount considerations. Typical applications include spectrum, vibration, waveform and transient analyzers; radar, sonar and video digitizers; medical imaging equipment; digital filters; and multiplexed or simultaneous-sampling data-acquisition systems.

MN5245 and MN5246 are manufactured in Micro Networks MIL-STD-1772 qualified hybrid facility, and for military/aerospace and harsh-environment industrial applications, they are available 100% screened to MIL-H-38534.

MN5245/46

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN5245 MN5246 1MHz 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125° C (case)
Specified Temperature Range:	
MN5245, 45A, 46, 46A	0°C to +70°C (case)
MN5245E, 45AE, 46E, 46AE	−25°C to +85°C (case)
MN5245H, 45AH, 46H, 46AH	−55°C to +125°C (case)
MN5245H/B, 45AH/B, 46H/B, 46AH/B	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 9)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 3)	+0.5 to −18 Volts
+5V Supply (+V_{dd}, Pins 15, 22, 39)	−0.5 to +7 Volts
Digital Inputs (Pins 36 and 37)	−0.5 to +5.5 Volts
Analog Input (Pin 1): MN5245, MN5245A	−1 to +6 Volts
MN5246, MN5246A	−3.5 to +3.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5245A H/B CH

- Select MN5245 or MN5246
- Add "A" suffix for optional 3-state output buffer.
- Standard Part is specified for 0°C to +70°C operation.
- Add "E" suffix for specified −25°C to +85°C (case) operation.
- Add "H" suffix for specified −55°C to +125°C (case) operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range: MN5245, MN5245A		0 to +5		Volts
MN5246, MN5246A		−2.5 to +2.5		Volts
Input Impedance (Note 11)		2/10		kΩ/pF
DIGITAL INPUTS				
Logic Levels: Logic "1"	+2.0		+5.0	Volts
Logic "0"	0		+0.8	Volts
Loading (Note 2): Start Convert Input			1	LS TTL Load
Data Enable Input (MN5245A, MN5246A)			1	LS TTL Load
TRANSFER CHARACTERISTICS (Note 3)				
Integral Linearity Error: Initial (+25°C)		±½	±1	LSB
Over Temperature		±½	±1	LSB
12-Bit No Missing Codes		Guaranteed Over Temperature		
Full Scale Absolute Accuracy Error (Note 4): Initial (+25°C)		±0.05	±0.15	%FSR
Over Temperature		±0.1	±0.3	%FSR
Unipolar Offset Error (MN5245, MN5245A; Note 5): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature		±0.1	±0.15	%FSR
Drift		±10	±20	ppm of FSR/°C
Bipolar Zero Error (MN5246, MN5246A; Note 6): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature		±0.1	±0.2	%FSR
Drift		±10	±25	ppm of FSR/°C
Gain Error (Note 7): Initial (+25°C)		±0.05	±0.1	%
Over Temperature		±0.1	±0.3	%
Drift		±15	±40	ppm/°C
DIGITAL OUTPUTS				
Output Coding (Note 8): MN5245, MN5245A		Straight Binary		
MN5246, MN5246A		Offset Binary		
Output Logic Levels (Note 12): Logic "1" ($I_{SOURCE} \leq 100\mu A$)	+2.7			Volts
Logic "0" ($I_{SINK} \leq 2mA$)			+0.5	Volts
Leakage (Bit 1-Bit 12) in High-Z State (MN5245A, MN5246A):				
Logic "1" (V_{OH} = +2.7V)			+10	μA
Logic "0" (V_{OL} = +0.4V)			−10	μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 9)		825	850	nsec
Conversion Rate (Note 9)	1.1			MHz
Start Convert Pulse Width (Notes 10, 11)	50			nsec
Delay Falling Edge of Start to Status = "1" (Note 11)		45		nsec
Delay Falling Edge of Start to Previous Output Data Invalid (Note 11)		750		nsec
Delay Falling Edge of Start to Falling Edge of T/H Control		750	780	nsec
Delay Falling Edge of Status to Output Data Valid (Note 11)			0	nsec
Delay Falling Edge of Enable to Output Data Valid (Note 11)			50	nsec
REFERENCE OUTPUT				
Internal Reference (Note 11): Voltage		+5.000		Volts
Accuracy		±2		%
Drift		±10		ppm/°C
External Current		5		μA

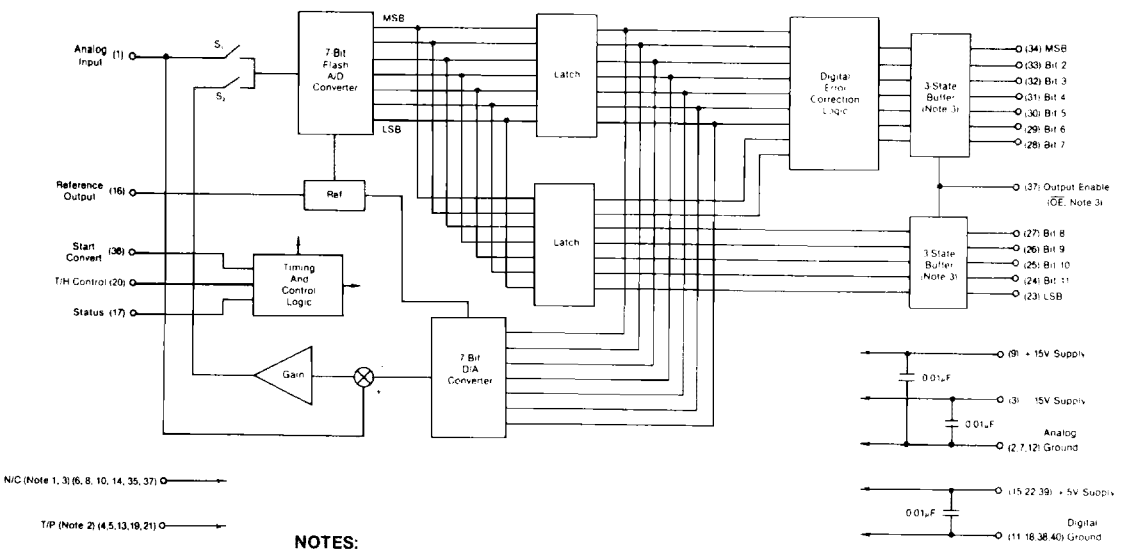
POWER SUPPLY REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Power Supply Range: +15V Supply	+14.55	+15	+15.43	Volts
−15V Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection (Note 13): +15V Supply	−50			dB
−15V Supply	−50			dB
+5V Supply	−50			dB
Current Drain: +15V Supply		+41	+50	mA
−15V Supply		−83	−90	mA
+5V Supply		+150	+165	mA
Power Consumption		2635	2925	mW

SPECIFICATION NOTES:

1. Unless otherwise indicated, listed specifications apply for all MN5245, MN5245A, MN5246 and MN5246A models. Drift specifications apply over each device's specified temperature range as selected by part number suffix.
2. One LS TTL load is defined as sinking 20μA with a logic "1" applied and sourcing 0.4mA with a logic "0" applied.
3. FSR = Full Scale Range. For both the MN5245 and MN5246, FSR = 5 volts. For a 12-bit converter, 1LSB = 0.024% FSR.
4. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 to 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
5. Unipolar offset error is defined for the MN5245 and MN5245A as the difference between the actual and ideal input voltage at which the 0000 0000 0000 to 0000 0000 0001 transition occurs. The ideal value at which this transition should occur is + ½LSB. See Digital Output Coding.
6. Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 0111 1111 1111 to 1000 0000 0000 transition occurs for the MN5246 and MN5246A. The ideal value at which this transition should occur is − ½LSB. See Digital Output Coding.
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000. Initial gain error is adjustable to zero with an external potentiometer.
8. See Output Coding table for details.
9. Conversion time is defined as the width of the converter's Status output pulse. The combination of 50nsec Start Convert pulses and 850nsec Status pulses permits minimum 1.1MHz conversion rates. See Timing Diagram.
10. Actual conversion process is initiated on the falling edge of the Start Convert signal. See Timing diagram.
11. These parameters are listed for reference only and are not tested.
12. Digital outputs include Data Bits (pins 23-34), Status (pin 17), and T/H control (pin 20). Specified drive capability is the equivalent of 5 LS TTL loads minimum.
13. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

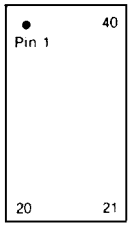
BLOCK DIAGRAM



NOTES:

1. "No Connects" (N/C) are not connected to internal circuitry.
2. "Test Points" (T/P) are connected to internal circuitry and should not be connected to externally.
3. 3-state output buffers included only in "A" models. For standard MN5245 and MN5246, pin 37 is a N/C.

PIN DESIGNATIONS



1	Analog Input	40	Digital Ground
2	Analog Ground	39	+ 5V Supply
3	− 15V Supply	38	Digital Ground
4	Test Point	37	N/C ($\overline{OE}$)
5	Test Point	36	Start Convert
6	N/C	35	N/C
7	Analog Ground	34	Bit 1 (MSB)
8	N/C	33	Bit 2
9	+ 15V Supply	32	Bit 3
10	N/C	31	Bit 4
11	Digital Ground	30	Bit 5
12	Analog Ground	29	Bit 6
13	Test Point	28	Bit 7
14	N/C	27	Bit 8
15	+ 5V Supply	26	Bit 9
16	Reference Output	25	Bit 10
17	Status (E.O.C.)	24	Bit 11
18	Digital Ground	23	Bit 12 (LSB)
19	Test Point	22	+ 5V Supply
20	T/H Control	21	Test Point

NOTES:

1. "No Connects" (N/C) are not connected to internal circuitry.
2. "Test Points" (T/P) are connected to internal circuitry and should not be connected to externally.
3. 3-state output buffers included only in "A" models. For standard MN5245 and MN5246, pin 37 is a N/C.

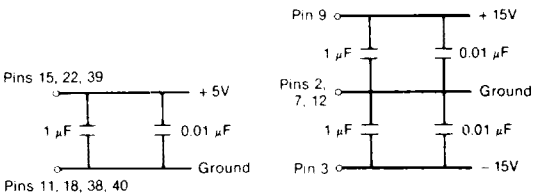
APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and performance from the MN5245 and MN5246. Analog Ground pins (pins 2, 7, and 12) are not connected internally to Digital Ground pins (pins 11, 18, 38 and 40). All ground pins should be tied together as close to the unit as possible and connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

A 0.1μF capacitor should be connected from Reference Output (pin 16) to system analog ground.

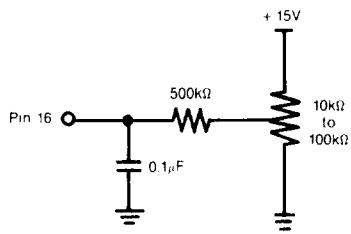


POWER SUPPLY DECOUPLING

STATUS OUTPUT/DATA VALID — The Status or End of Conversion (E.O.C.) output is set to logic "1" by the falling edge of the Start Convert; remains high during the conversion; and is set to a logic "0" by the rising edge of the T/H Control output, signaling that the conversion is complete. Digital output data is valid on the falling edge of Status and remains valid until the next falling edge of T/H Control (approximately 750nsec after Start Convert goes low initiating the next conversion). It is important to note that the falling edge of the T/H Control indicates the end of the "analog-processing" portion of the A/D conversion and the beginning of the "digital-processing" portion. Output data becomes **invalid** on the falling edge of the T/H Control signal, and it is not recommended that this edge be used to clock data away from the MN5245/46. When making successive conversions, any of the edges occuring during the beginning of the data-valid period (fall of Status, falling edge of the next Start Convert, rising edge of Status, etc.) are better suited for this purpose. Also, output data can be enabled (MN5245A/MN5246A) during this data-valid period by bringing Output Enable ($\overline{OE}$, pin 37) low. The delay from the falling edge of Output Enable to output data valid is 50nsec maximum.

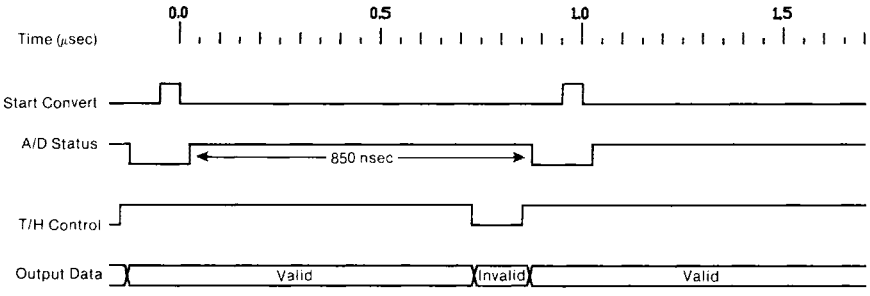
REFERENCE IN/OUT, GAIN ADJUST—Pin 16 on MN5245/MN5246 type A/D converters serves a unique function. The devices' internal + 5V ± 2% reference is brought out at this point and can be used to drive external loads. If used for this purpose, pin 16 should be buffered with a FET-input device as drawing more than 5μA from the internal reference will affect MN5245/MN5246 accuracy and linearity. Pin 16 can also be used as a Reference In Point if it is necessary to operate MN5245/MN5246 from an external reference. An application requiring an external reference might be one in which it is necessary to have a number of devices operate from the same reference to track each other in changing temperatures. The applied reference should be + 5V ± 250mV.

Pin 16 also functions as the gain-adjust point for MN5245/MN5246 A/D converters. Gain adjustment is accomplished using a 10kΩ to 100kΩ trimming potentiometer and a 500kΩ series resistor as shown below. The series resistor can be ± 20% carbon composition or better. The multiturn potentiometer should have a TCR of 100ppm/°C or less to minimize drift with temperature. Gain adjusting is normally accomplished by applying the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 digital-output transition is ideally supposed to take place and adjusting the pot until the transition is observed.



Gain Adjust Range = ± 0.2% FSR

TIMING DIAGRAM



TIMING DIAGRAM NOTES

1. Minimum Start Convert pulse width is 50nsec, and Start Convert must remain low during conversion.
2. Status rises to a "1" typically 45nsec after the falling edge of Start Convert.
3. Digital output data from the previous conversion is valid typically 750nsec after the falling edge of Start and 705nsec after the rising edge of Status.
4. Digital output data is valid on the falling edge of Status.
5. For MN5245A or MN5246A, output data becomes valid a maximum of 50nsec after Output Enable (pin 37) is brought low.
6. The falling edge of T/H Control occurs 780nsec maximum after the falling edge of Start Convert.

DIGITAL OUTPUT CODING

Analog Input		Digital Output
MN5245, MN5245A	MN5246, MN5246A	MSB LSB
+5.0000	+2.5000	1111 1111 1111
+4.9982	+2.4982	1111 1111 111Ø*
+2.5006	+0.0006	1000 0000 000Ø*
+2.4994	−0.0006	ØØØØ ØØØØ ØØØØ*
+2.4982	−0.0018	0111 1111 111Ø*
+0.0006	−2.4994	0000 0000 000Ø*
0.0000	−2.5000	0000 0000 0000

NOTES

1. For a 12-bit converter with a 5 volt FSR, 1LSB = 1.22mV.
2. Coding is straight binary for the unipolar 5V range and offset binary for the bipolar 2.5V range.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For the MN5245 or MN5245A, the transition from output code 1111 1111 1111 to output code 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of +4.9982V (+F.S. − 1½LSB). Subsequently, any voltage greater than +4.9982V will give a digital output of all "1's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 (or vice versa) will ideally occur at an input of +2.4994V. The 0000 0000 0000 to 0000 0000 0001 transition will occur at +0.0006V. An input more negative than this level will give all "0's".

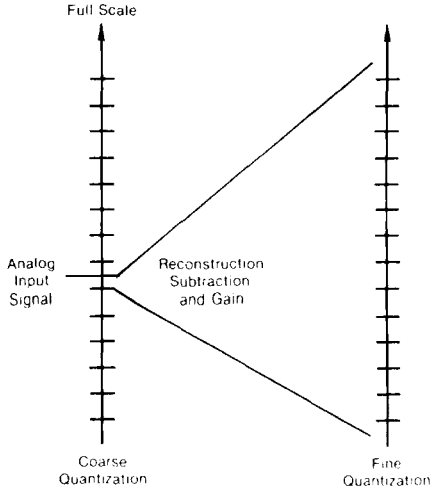
DESCRIPTION OF OPERATION — MN5245 and MN5246 are multi-stage (two-step) A/D converters. They employ the Micro Networks Serial-Parallel conversion technique (sometimes referred to as the subranging technique) with digital error correction. The technique uses two 7-bit flash A/D converters (actually a single 7-bit flash coverter is used twice) in a configuration that yields a resolution (12 bits) that is beyond the practical limits of what can be achieved in a single "high-resolution" flash coverter. The technique trades off speed against resolution and, in the case of MN5245/MN5246, against size, as putting the device in a single DIP package necessitates additional considerations.

As shown in the block diagram, the main function blocks in MN5245/MN5246 type A/D's may be partitioned into analog functions (including input switching network (S_1 and S_2); 7-bit, high-speed, flash-type A/D converter; precision, 7-bit, high-speed D/A converter; high-speed difference amplifier with gain; precision reference; and timing circuits) and digital functions (including 2 sets of latches; the digital-error-correction logic; and the 3-state output buffers). The circuit functions in the following manner.

The falling edge of the Start Convert command (50nsec minimum pulse width): drives the Status output to a logic "1" (approximate 45nsec delay) indicating that a conversion is in process; switches S_1 on and S_2 off connecting the analog input signal directly to the 7-bit flash converter; and initiates a series of timing pulses that will control the assorted operations of the converter during the conversion cycle. At this point, digital output data from the previous conversion is still valid, and it remains so until approximately 750nsec after the falling edge of Start.

After a period of time allowing the flash-converter input circuitry to settle, the first internally generated timing pulse initiates a flash conversion and subsequently latches the 7-bit output into the first latch. The input signal has now been coarsely quantized into $2^7 = 128$ levels and the result, after being stored in the first latch, is simultaneously directed to the 7-bit D/A converter which reconstructs the signal into an analog equivalent.

This digitized and subsequently reconstructed signal is subtracted from the original analog input yielding the difference between the first 7-bit conversion and the input signal. As depicted below, the difference signal is then amplified and itself digitized by being fed back into the 7-bit flash converter via the closing of S_2 and the opening of S_1. The result of this conversion is now latched into the second latch.



One of the tradeoffs that enable MN5245 and MN5246 to be built in DIP's was the decision to use a single 7-bit flash converter and cycle through it twice rather than use 2 flash A/D's. Had 2 A/D's been used, the amplified difference signal would be routed to the second A/D at this point, liberating the first A/D to begin a new conversion cycle and eliminating the S_1S_2 switching network and its associated settling times.

Returning to the conversion process, one might conclude that digitizing the amplified difference signal would constitute the end of a conversion as the 5 most significant bits (MSB's) from the second 7-bit conversion could simply be added to the 7 bits from the first conversion to give a full, accurate, 12-bit output. However, the realities of implementing the conversion technique make such an obvious conclusion a wrong one.

The major sources of error in the technique occur in the first 7-bit conversion and result from the fact that such a conversion is only 7, or at most, 8-bits accurate. Twelve-bit accuracy would be required at this point in order for one to simply add output bits together to get an accurate result. Such 7-bit resolution, 12-bit accurate flash converters do not exist, and if they did, would probably be considerably slower than required to make a 850nsec 12-bit conversion. The problem is overcome using the technique of digital error correction. In this technique, the first 7-bit A/D conversion is allowed to have errors (as long as they are within some known bounded range), and these errors are corrected for in the later portion of the conversion cycle. The process proceeds as follows: Recall that if the 7-bit converter had 12-bit accuracy one would only need 5 bits from the second conversion to produce a 12-bit result. By digitizing the difference signal to a level that is four times greater than theoretically required (7 bits compared to 5 bits) and comparing the result to theoretically anticipated limits, one can deduce what the inaccuracies were in the first 7-bit conversion. This is what MN5245/MN5246's digital-error-correction circuity accomplishes. Using combinatorial logic and lookup tables, the error-correction circuitry assesses the 2 most significant bits of the digitized difference signal; decides how accurate the first 7-bit conversion was; and adds or subtracts bits to or from the first 7-bit output as necessary. Once the first 7 bits have been corrected, they are simply added to the 5 remaining bits of the second conversion to produce the full 12-bit output. This is why in the Block Diagram, the two MSB's from the second latch are routed to the digital-error-correction logic and the 5 LSB's are directed to the output.

It should be obvious, following the above discussion, that MN5245/MN5246 A/D's normally require the use of track-hold amplifiers (T/H's) to hold the input signal relatively constant during the first conversion and the subsequent subtraction, gain and second digitization cycles. The output droop rate of the track-hold should be slow enough so the held signal does not change more than $\pm$ ½LSB ($\pm$ 0.61mV) during the conversion period. Micro Networks MN375 and MN376 both do the job well. A consideration that may enable designers to improve throughput when using MN5245 and MN5246 with T/H's is that an accurate input signal is no longer required after the second 7-bit A/D conversion has been made. During the interval between that conversion and the point at which Status drops to a "0" indicating that the conversion is complete, the digital-error-correction logic is performing its function and the analog input circuitry is dormant. This period is called converter "slack time" and is typically 100nsec for MN5245/MN5246 devices. The T/H amplifier can be put back into its tracking (signal acquisition) mode at this point rather than waiting until the falling edge of Status by utilizing the T/H control output (pin 20) described on the following pages.

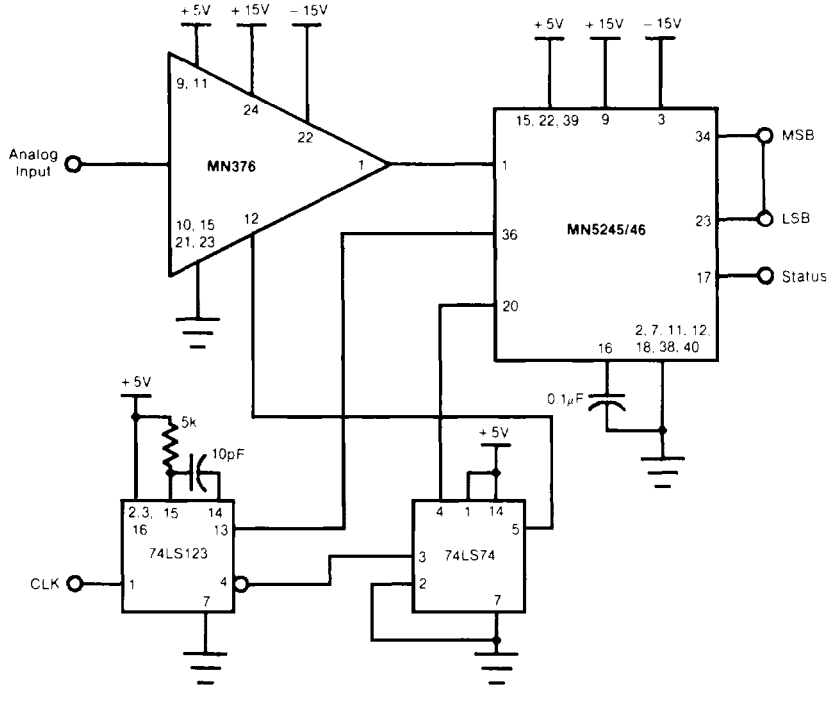
MN5245/5246 — MN376 1MHz Sampling System

A/D converters that utilize the subranging (serial-parallel) conversion architecture may be relatively limited in their ability to accurately convert rapidly changing dynamic input signals. In other words, these high-throughput digitizers often have analog input bandwidth limitations. In situations in which both high-throughput and high-bandwidth digitizing is required, a track-hold (T/H) amplifier can be used to overcome the A/D's inherent limitations. The T/H has the ability to quickly capture rapidly changing analog signals and hold them constant while the A/D performs its conversion. The MN376 High Speed T/H Amplifier (200nsec maximum acquisition time) has been designed specifically for this type of usage with MN5245/46. The following application information describes how to configure MN376 and MN5245/46 to create a T/H-A/D pair that is capable of sampling and digitizing at rates in excess of 1MHz and has a full-power input bandwidth greater than 500kHz. Interconnect and timing diagrams are shown below, and the basics of the application are applicable to most high-speed T/H-A/D combinations.

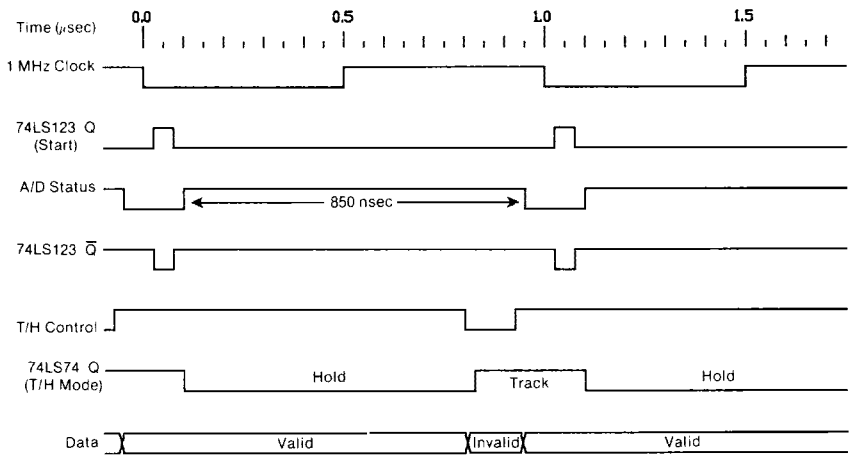
The T/H Control pulse provided on pin 20 of the MN5245/46 is the key to this application. The falling edge of this output signals the end of the "analog-processing" portion of the A/D conversion and consequently, the end of the requirement for a constant-value analog input signal. Immediately thereafter, the T/H can be removed from its "hold" state and permitted to acquire a new input sample, i.e., the T/H can be put into the acquisition (track) mode. The T/H Control line remains low for approximately 100nsec (during the "digital-processing" portion of the conversion) and then returns high triggering the fall of the A/D's Status output. The falling edge of Status signals the end of the conversion and the validity of digital output data (see Description of Operation if necessary). At the beginning of the next conversion, the T/H is driven from the track (signal-acquisition) mode to the hold mode "freezing" the input signal permitting an accurate conversion to proceed.

Maximum throughput is achieved in this application because the T/H is driven into the acquisition mode for its next sample prior to the completion of the ongoing A/D conversion and remains in the acquisition mode while the A/D is being "set up" for its next conversion. This "overlapping" allows every nanosecond to be utilized.

APPLICATION SCHEMATIC



APPLICATION TIMING DIAGRAM



As previously stated, the MN376-MN5245/46 T/H-A/D combination is capable of sampling and digitizing at rates in excess of 1MHz, with the actual rate determined by the frequency of the externally applied clock. See interconnect and timing diagrams. The falling edge of the external clock triggers the 74LS123 one-shot, and the clock can have any duty cycle as long as it has a minimum positive pulse width of 50nsec to accommodate the setup-time requirement of the one-shot. The Q output of the one shot provides a 50nsec start-convert signal to the MN5245/46; while the rising edge of the $\overline{Q}$ output simultaneously resets the 74LS74 flip-flop. The Q output of the flip-flop controls the operational mode of the T/H (utilizing the T/H's $\overline{\text{hold}}$ input), and at the beginning of a sample/convert cycle, the flip-flop output going to a logic "0" drives the T/H into the hold mode. This "freezes" (holds) the input signal that the T/H has been acquiring/tracking up until this time.

It is unnecessary to have the 74LS123 one-shot in this application if the externally applied clock can be made to be a series of 50nsec-wide positive pulses occurring at a 1MHz rate. In other words, if the clock can be made to look like the output of the one-shot in our timing diagram, it is unnecessary to have the one-shot. The clock can drive the MN5245/46 directly, and it can be inverted to drive the 74LS74.

The falling edge of the MN5245/46's applied start-convert signal (the Q output of the one-shot) initiates the A/D conversion process and drives the converter's status line high. The "first-pass" conversion of MN5245/46's internal 7-bit flash A/D does not occur until approximately 190nsec after the falling edge of the start-convert signal. This delay allows time for the T/H's track-to-hold output transient to fully settle before the 7-bit flash makes it first conversion. The MN376 specifies a maximum transient settling time (to ± 1mV) of 100nsec. The T/H remains in the hold mode while the A/D conversion continues, and the T/H's excellent output-droop performance guarantees that the A/D's input will not change more than 5μV during the conversion window. At approximately 700nsec into the conversion, the T/H Control line (pin 20) goes low signaling the end of the analog-processing portion of the conversion. This action asynchronously sets the flip-flop output to a logic "1", which in turn drives the MN376 T/H back into the signal-acquisition (track) mode. Approximately 100nsec later, the rising edge of the pin 20 signal triggers the fall of the Status line indicating that the conversion is complete and that output data is now valid. The Status pulse is guaranteed not be wider than 850nsec, and neither the rising edge of the T/H Control signal (pin 20) nor the falling edge of the Status signal (pin 17) will affect the operational mode of the T/H. It remains in the track mode through both events.

When making repetitive conversions, the T/H Control signal permits the MN376 to acquire and track new samples of the input signal during the "slack time" of the present conversion. When the T/H Control signal is used in this manner in a 1MHz application, a minimum of 240nsec is allocated for the MN376 acquisition-time requirements. This more than accommodates the MN376's maximum acquisition time of 200nsec (10V step acquired to ± 1mV or 5V step acquired to ± ½mV).

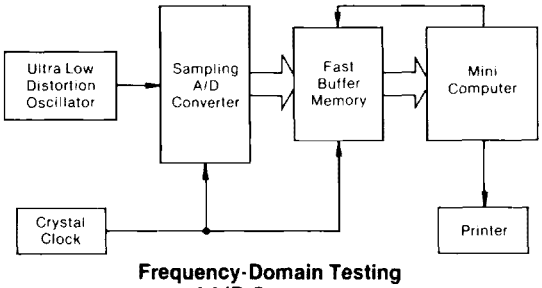
MN5245/5246 has a latched output, and output data from a conversion typically remains valid into the next conversion for 750nsec beyond the falling edge of the next start-convert signal. Output data becomes **invalid** on the falling edge of the T/H Control signal, and it is not recommended that this edge be used to clock data away from MN5245/46. Any of the edges occurring during the beginning of the data-valid period (clock edge, one-shot outputs, rising edge of Status, etc.) are better suited for this purpose.

This T/H-A/D pair is guaranteed to meet all its performance specs while running at a 1MHz sampling rate. The slew rate (300V/μsec), full-power bandwidth and aperture jitter ($\pm$ 25psec) of the T/H are good enough to accurately track and sample full-scale (5V), 500kHz, input signals. Consequently, this T/H-A/D pair can accurately sample and digitize (at a 1MHz rate) full-scale input signals with frequency content (bandwidths) up to 500kHz.

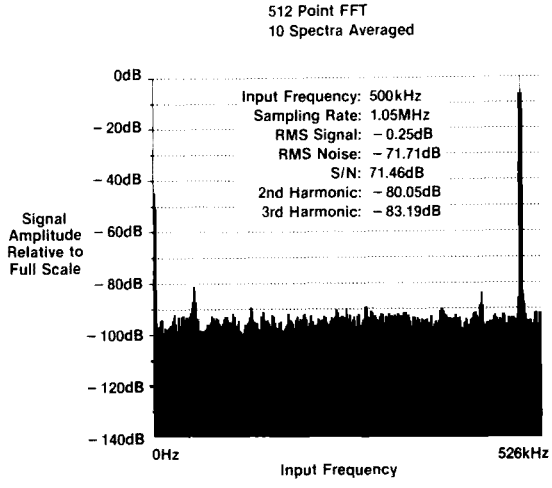
This means that the Nyquist criterion of sampling 2 times per peroid (sample/digitizing rate equal to at least 2 times the signal frequency) is satisfied, and the MN5245/46 pair is truly a Nyquist A/D converter. Evaluating it as such is no longer a difficult task.

The availability of low-cost, p.c. based, digital-signal-processing (D.S.P.) technology has made it relatively easy to now perform dynamic, frequency-domain evaluations of sampling A/D converters. Prior to this, it was virtually impossible to review the listed specifications for A/D converters and/or T/H amplifiers and make a valid determination of the true dynamic capabilities of either device. This inconclusiveness was due primarily to the fact that virtually all traditional A/D converter specs (integral linearity, differential linearity, accuracy, gain, etc.) are tested statically and cannot necessarily be extrapolated to dynamic situations. It was also due to the fact that appropriate dynamic T/H specs either were similarly static (linearity); did not exist (harmonic distortion); or were too difficult to understand (aperture jitter).

In the dynamic tests that we now perform at Micro Networks, the MN376-MN5256/46 T/H-A/D combination is operated in a manner that resembles an application as a digital spectrum analyzer. A very low distortion signal generator (harmonics $-$90dB) is used to generate a pure, full-scale, 500kHz sine wave that MN376-MN5245/46 samples and digitizes at a 1MHz rate. These conditions (signal period = 2μsec, sampling interval = 1μsec) achieve the Nyquist sampling criterion (at least 2 samples per signal cycle). A total of 512 sample-and-convert operations are performed, and the digital-output data is stored in a high-speed, FIFO, buffer-memory box. The 512 data points are then accessed by a microcomputer which executes a 512-point Fast Fourier Transform (FFT) after applying a Hanning (raised cosine) window function to the data. The resulting spectrum shows the amplitude and frequency content of the converted signal along with any errors (noise, harmonic distortion, spurious signals, etc.) introduced by the A/D converter. Subsequently, signal-to-noise ratio (SNR) and harmonic distortion measurements are made from the spectrum. A functional block diagram of the test setup and a sample spectrum appear below.



Frequency-Domain Testing of A/D Converters



The spectrum above is the real portion (imaginary portions of spectra are discarded) of a 512-point FFT. The horizontal axis is the frequency axis, and its rightmost end is equal to ½ the sampling rate (526kHz in this case). The horizontal axis is divided into 256 frequency bins, each with a width of 2.05kHz. Recall that the highest frequency on the frequency axis of the spectrum of a sampled signal is equal to one-half the sampling rate and that input signals with frequencies higher than ½ the sampling rate are effectively "undersampled" and aliased back into the spectrum.

The vertical axis of the spectrum corresponds to signal amplitude in rms volts relative to a full-scale sinusoidal input signal (0dB). The sample spectrum above is the result of averaging 10 512-point FFT's run on data taken from an MN376-MN5246 operating on its $\pm$2.5V bipolar input range with a full scale input sine wave (v(t) = 2.5sinwt) at a frequency of 500kHz. In the spectrum, the full-scale input signal appears at 500kHz at a level of $-$0.25dB. Full-scale r.m.s. signals do not appear at $-$3dB levels because our FFT program has been normalized to bring them to zero. The d.c. component in the spectrum is effectively the offset error of the MN376-MN5246 combined with that of the signal generator and test fixture. A second harmonic distortion component is aliased back into the spectrum and appears at 52kHz at a level of $-$80.30dB ($-$80.05dB relative to the signal level). The third harmonic is also aliased into the spectrum and appears at 448kHz at a level of $-$83.44dB ($-$83.19dB relative to the signal level). The fourth and fifth harmonics, if they were present, would occur at 104kHz and 396kHz respectively, however, due to their small amplitudes they are buried in the broadband noise.

Harmonic distortion and spurious noise levels are calculated as the ratio (in dB) of the signal level ot the strongest harmonic or spurious (nonharmonic) signal in the spectrum. In the sample spectrum above, the strongest harmonic is the second. It appears at a level of $-$80.30dB, and the signal to harmonics ratio is equal to $-$80.05dB. Rms noise is calculated as the rms summation of all nonfundamental and nonharmonic components in the output spectrum, and SNR is calculated as the ratio of the rms signal to rms noise. For the above spectrum, the normalized rms signal level is $-$0.25dB; the rms noise level is $-$71.71dB; and the SNR is 71.46dB.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