Integrated Device Technology, Inc.

512K (64K x 8) SYNCHRONOUS STATIC RAM PLASTIC SIP MODULE

IDT 7MP6025

FEATURES:

- 64K x 8 fully synchronous memory
- High-speed—20MHz read cycle time
- 16-bit synchronous address input
- 8-bit synchronous data input
- Synchronous chip select and write enable
- Separate clock enable for each register
- Low standby power
- Onboard decoupling capacitors
- Available in 43-pin SIP (single in-line package) configuration
- 2 Ground and 2 V_{CC} pins

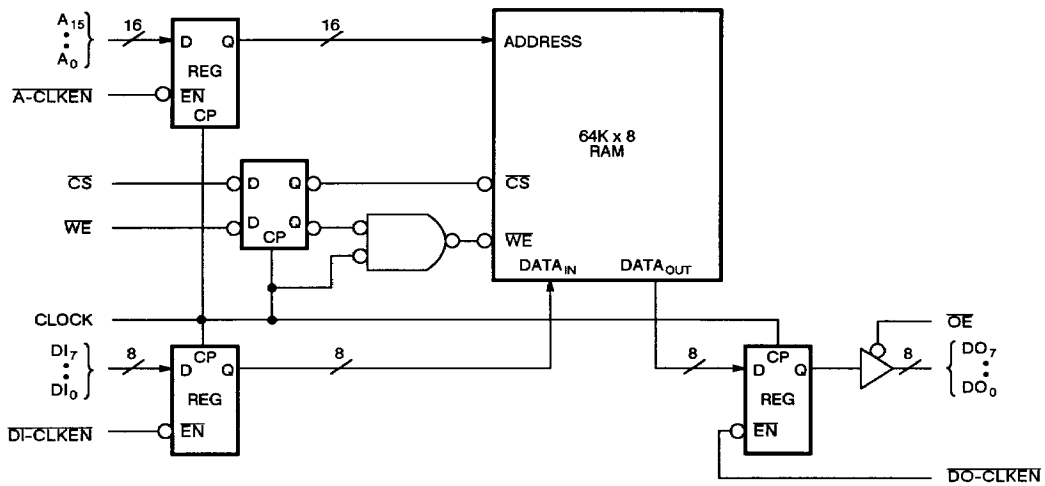
DESCRIPTION:

The IDT7MP6025 is a 64K x 8 synchronous RAM with edge triggered registers on the address lines, data-in bus, data-out bus, chip select and write enable. The edge triggered register of the 16 address lines features an independent clock enable that allows the address register to be selectively loaded. The address register will be loaded on the low-to-high transition of the clock when the clock enable line is low and will hold its current contents on the low-to-high transition of the clock when the clock enable is high. Similarly, the 8-bit data-in register will be loaded with new data on the low-to-high transition of the clock when the data-in clock enable is low and will hold its contents when the data-in clock enable is high. The data-out register will receive new data from the 64K x 8 RAM when the clock enable line is low and will hold its data when the clock enable line is high at the low-to-high transition of the clock. All clock enables, as well as address and data inputs, must meet the appropriate set-up and hold times with respect to the clock.

The eight data output bits are enabled when the output enable is low and are in the high-impedance state when the output enable is high. The chip select and write enable signals are also registered in D flip-flops. These two flip-flops are loaded with new data on each low-to-high transition of the clock. The chip select is passed directly from the Q output of the D-type flip-flop to the 64K x 8 RAM. The write enable signal is gated with the clock signal to generate a delayed write enable pulse. In essence, this gives the output of the address register time to settle and internally select the appropriate byte of RAM before the write enable goes low to write new data into the RAM. Thus, the low-to-high transition of the clock causes the chip select and write enable flip-flops to be loaded with new data and immediately deselects a previous write by means of the clock going high. The data lines to the RAM and the address lines to the RAM may indeed change to new values based on the low-to-high transition of the clock. When the clock goes from high-to-low, if the chip select is low and the write enable is low, a write cycle is begun and the data at the RAM data inputs will be written into the selected address. If the write enable is high or the chip enable is high, data will not be written into the memory.

One of the features of this configuration of memory that has registers on all of the address lines, data input lines and data output lines as well as the control lines, is to provide the highest possible clock rate in the system. All that is necessary is that the data, address, chip select, write enable and clock enables signals meet the required set-up and hold time with respect to the clock. In this manner, fully asynchronous operation is achieved. The IDT7MP6025 is offered as a compact, cost-effective 43-pin plastic SIP module.

FUNCTIONAL BLOCK DIAGRAM



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COMMERCIAL TEMPERATURE RANGE **JANUARY 1989**

DSC-7031/-

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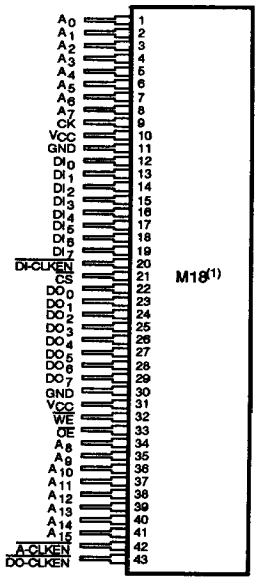
PIN CONFIGURATION



SIP
SIDE VIEW

NOTE:

1. For module dimension, please refer to module drawing M18 in the packaging section.

PIN NAMES

A_{0-15}	Addresses
CK	Clock
DI_{0-7}	Data Input
DO_{0-7}	Data Output
$\overline{DI\text{-}CLKEN}$	Data Input Clock Enable
$\overline{A\text{-}CLKEN}$	Address Clock Enable
$\overline{DO\text{-}CLKEN}$	Data Output Clock Enable
V_{CC}	Power
GND	Ground
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	COMMERCIAL	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	5	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{OUT}, V_{OUT} = GND to V_{CC}	–	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	MAX.	UNIT
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max.; Output Open	725	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; f = f_{MAX}, Output Open	950	mA
I_{SB1}	Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} > V_{CC}$ - 0.2V or < 0.2V	125	mA

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	22	pF

NOTE:

1. This parameter is sampled and not 100% tested.

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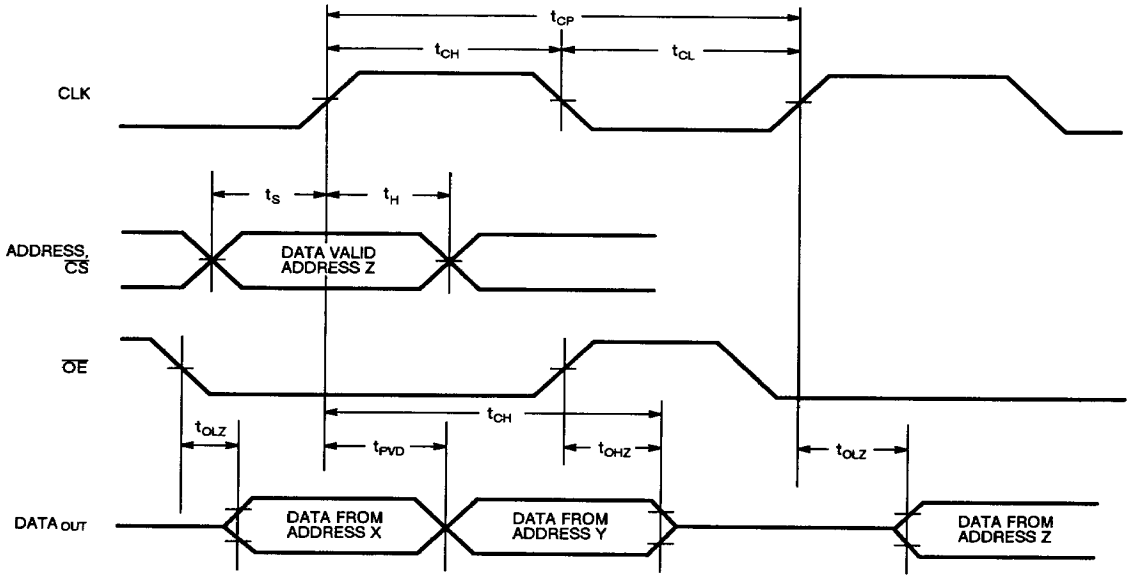
AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	7MP6025S35		7MP6025S45		7MP6025S55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
t_{CP}	Read Cycle Time	35	–	45	–	55	–	ns
t_{CH}	Clock High Time	10	–	10	–	10	–	ns
t_{CL}	Clock Low Time	10	–	10	–	10	–	ns
t_S	Address, $\overline{WE}$, $\overline{CS}$, $\overline{CE}$ Set Up Time	4	–	5	–	5	–	ns
t_H	Address, $\overline{WE}$, $\overline{CS}$, $\overline{CE}$ Hold Time	4	–	6	–	6	–	ns
t_{OLZ} (1)	Output Low Z Time	–	10	–	15	–	15	ns
t_{OHZ} (1)	Output High Z Time	–	8	–	11	–	11	ns
t_{PVD}	Prop Delay to Valid Data Out	–	10	–	15	–	15	ns
WRITE CYCLE								
t_{CP}	Write Cycle Time	35	–	45	–	55	–	ns
t_{CH}	Clock High Time	10	–	10	–	10	–	ns
t_{CL}	Clock Low Time	23	–	30	–	37	–	ns
t_S	Data, Addr, $\overline{WE}$, $\overline{CS}$, $\overline{CE}$ Set Up Time	4	–	5	–	5	–	ns
t_H	Data, Addr, $\overline{WE}$, $\overline{CS}$, $\overline{CE}$ Hold Time	4	–	6	–	6	–	ns

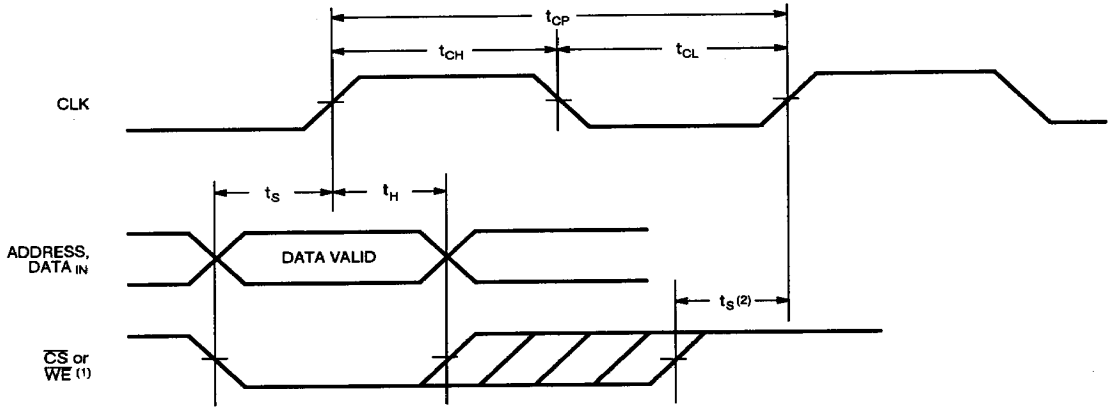
NOTE:
1. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE (1)



NOTE:
1. The device must be selected by a $\overline{CS}$ level for the conditions above to take place.

TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. Either $\overline{CS}$ or $\overline{WE}$ can be used to trigger a write cycle, provided that the other signal is low at the same time.
2. When a write is terminated, either $\overline{CS}$ or $\overline{WE}$ must become high at least one t_S before the next rising edge of CLK.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	CK	$\overline{DO}$-CLKEN	$\overline{DI}$-CLKEN	$\overline{A}$-CLKEN	$\overline{WE}$	OUTPUT	POWER
Standby	H	H	↑	H	H	H	X	High Z	Standby
Read	L	L	↑	L	X	L	H	Low Z	Active
Read	L	H	↑	L	X	L	H	High Z	Active
Write	L	H	↑	H	L	L	L	High Z	Active

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

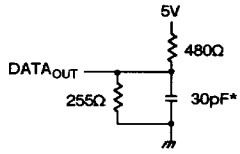

Figure 1. Output Load

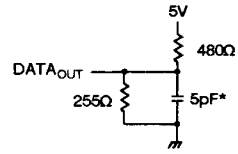

Figure 2. Output Load (for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW})

* Including scope and jig.

ORDERING INFORMATION