ELPIDA

PRELIMINARY DATA SHEET

256M bits DDR Mobile RAM

EDK2516CBBH (16M words × 16 bits)

Description

The EDK2516CB is a 256M bits DDR Mobile RAM organized as 4,194,304 words×16 bits×4 banks. The DDR Mobile RAM achieved low power consumption and high-speed data transfer using the 2bits prefetch-pipeline architecture. Command and address inputs are synchronized with the positive edge of the clock. Data inputs and outputs are synchronized with both edges of DQS(Data Strobe). DLL is not implemented. This product is packaged in 60-ball FBGA.

Features

- Low voltage power supply
  - VDD: 1.8V ± 0.15V
  - VDDQ: 1.8V ± 0.15V
- Wide temperature range (–25°C to 85°C)
- Programmable partial self refresh
- Programmable driver strength
- Programmable temperature compensated self refresh
- Deep power down mode
- Small package (60-ball FBGA)
- FBGA package is lead free solder (Sn-Ag-Cu)
- Data rate: 200Mbps/IO(max)
- Doule Data Rate architecture: two data transfers per one clock cycle
- Bi-directional, data strobe (DQS) is transmitted /received with data, to be used in capturing data at the receiver.
- 1.8V LVCMOS interface
- Command and address signals refer to a positive clock edge
- Quad internal banks controlled by BA0 and BA1
- Data mask (DM) for write data
- Wrap sequence = Sequential/ Interleave
- Programmable burst length (BL) = 2, 4, 8
- Automatic precharge and controlled precharge
- Auto refresh and self refresh
- 8,192 refresh cycles/64ms

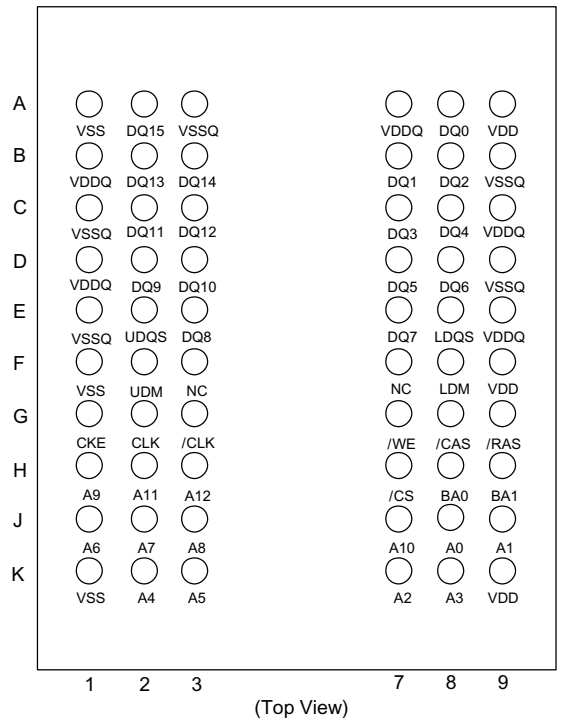
(7.8μs maximum average periodic refresh interval)

- Burst termination by Burst stop command and Precharge command

Pin Configurations

/xxx indicates active low signal.

60-ball FBGA



(Top View)

A0 to A12	Address input
BA0, BA1	Bank select address
DQ0 to DQ15	Data-input/output
UDQS, LDQS	Input and output data strobe
/CS	Chip select
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
UDM, LDM	Write data mask
CK	Clock input
/CK	Differential clock input
CKE	Clock enable
VDD	Power for internal circuit
VSS	Ground for internal circuit
VDDQ	Power for DQ circuit
VSSQ	Ground for DQ circuit
NC	No connection

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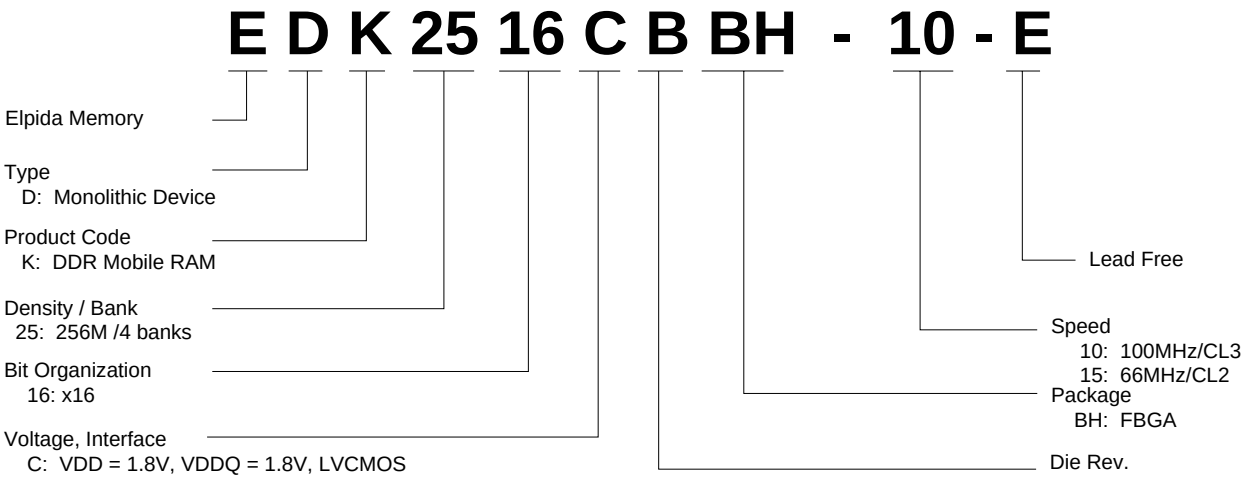
Ordering Information

Part number	Organization (words × bits)	Internal banks	Clock frequency MHz (max.)	/CAS latency	Package
EDK2516CBBH-15-E	16M × 16	4	66	2	60-ball FBGA
EDK2516CBBH-10-E			100	3	

Part Number



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Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power up, wait more than 200 µs and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Voltage on any pin relative to VSS	VT	–1.0 to +2.6	V	
Supply voltage relative to VSS	VDD	–1.0 to +2.6	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	1.0	W	
Operating temperature	TA	-25 to +85	°C	
Storage temperature	Tstg	–55 to +125	°C	

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (TA = -25 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	VDD, VDDQ	1.65	1.8	1.95	V	1
	VSS, VSSQ	0	0	0	V	
Input high voltage	VIH (DC)	0.8 × VDDQ	—	VDDQ + 0.3	V	2
Input low voltage	VIL (DC)	–0.3	—	0.3	V	3
Input voltage level, CK and /CK inputs	VIN (DC)	–0.3	—	VDDQ + 0.3	V	
Input differential cross point voltage, CK and /CK inputs	VIX (DC)	0.5 × VDDQ – 0.2V	0.5 × VDDQ	0.5 × VDDQ + 0.2V	V	
Input differential voltage, CK and /CK inputs	VID (DC)	1.0	—	VDDQ + 0.6	V	

Notes: 1. VDDQ must be lower than or equal to VDD.
2. VIH is allowed to exceed VDD up to 2.6V for the period shorter than or equal to 5ns.
3. VIL is allowed to outreach below VSS down to –1.0V for the period shorter than or equal to 5ns.

DC Characteristics 1 (TA = –25 to +85ºC, VDD, VDDQ = 1.8V ± 0.15V, VSS, VSSQ = 0V)

Parameter / Grade / /CAS latency	Symbol	-10 max.	-15 max.	Unit	Test condition	Notes
Operating current (CL = 2)	IDD1	—	45	mA	Burst length = 1 tRC ≥ tRC min., IO = 0mA, One bank active	1
(CL = 3)	IDD1	45	—	mA		
Standby current in power down	IDD2P	TBD	TBD	mA	CKE ≤ VIL max., tCK = 15ns	
Standby current in power down (input signal stable)	IDD2PS	TBD	TBD	mA	CKE ≤ VIL max., tCK = ∞	
Standby current in non power down	IDD2N	3.0	3.0	mA	CKE ≥ VIH min., tCK = 15ns, /CS ≥ VIH min., Input signals are changed one time during 30ns.	
Standby current in non power down (input signal stable)	IDD2NS	2.0	2.0	mA	CKE ≥ VIH min., tCK = ∞, Input signals are stable.	
Active standby current in power down	IDD3P	TBD	TBD	mA	CKE ≤ VIL max., tCK = 15ns	
Active standby current in power down (input signal stable)	IDD3PS	TBD	TBD	mA	CKE ≤ VIL max., tCK = ∞	
Active standby current in non power down	IDD3N	TBD	TBD	mA	CKE ≥ VIH min., tCK = 15 ns, /CS ≥ VIH min., Input signals are changed one time during 30ns.	
Active standby current in non power down (input signal stable)	IDD3NS	TBD	TBD	mA	CKE ≥ VIH min., tCK = ∞, Input signals are stable.	
Burst operating current (CL = 2)	IDD4	—	30	mA	tCK ≥ tCK min., IOUT = 0mA, All banks active	2
(CL = 3)	IDD4	45	—	mA		
Refresh current (CL = 2)	IDD5	50	50	mA	tRC ≥ tRC min.	3
Self refresh current PASR="000" (Full)	IDD6	150	150	µA	TCSR="00" (Ts*4 ≤ 70°C)	
PASR="001" (2BK)		TBD	TBD	µA	CKE ≤ 0.2V	
PASR="010" (1BK)		TBD	TBD	µA		
PASR="101" (1/2 BK)		TBD	TBD	µA		
PASR="110" (1/4 BK)		TBD	TBD	µA		
PASR="000" (Full)	IDD6	100	100	µA	TCSR="01" (Ts*4 ≤ 45°C)	
PASR="001" (2BK)		TBD	TBD	µA	CKE ≤ 0.2V	
PASR="010" (1BK)		TBD	TBD	µA		
PASR="101" (1/2 BK)		TBD	TBD	µA		
PASR="110" (1/4 BK)		TBD	TBD	µA		
PASR="000" (Full)	IDD6	250	250	µA	TCSR="11" (Ts*4 ≤ 85°C)	
PASR="001" (2BK)		TBD	TBD	µA	CKE ≤ 0.2V	
PASR="010" (1BK)		TBD	TBD	µA		
PASR="101" (1/2 BK)		TBD	TBD	µA		
PASR="110" (1/4 BK)		TBD	TBD	µA		
Standby current in deep power down mode	IDD7	10	10	µA	CKE ≤ 0.2V	

Notes: 1. IDD1 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, IDD1 is measured condition that addresses are changed only one time during tCK (min.).
2. IDD4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, IDD4 is measured condition that addresses are changed only one time during tCK (min.).
3. IDD5 is measured on condition that addresses are changed only one time during tCK (min.).
4. Ts is surface temperature.

DC Characteristics 2 (TA = -25 to +85°C, VDD, VDDQ = 1.8V ± 0.15V, VSS, VSSQ = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–1.0	1.0	µA	0 ≤ VIN ≤ VDDQ	
Output leakage current	ILO	–1.5	1.5	µA	0 ≤ VOUT ≤ VDDQ, DQ = disable	
Output high voltage	VOH	VDDQ – 0.2	—	V	IOH = – 0.1mA	
Output low voltage	VOL	—	0.2	V	IOL = 0.1 mA	

Pin Capacitance (TA = +25°C, VDD, VDDQ = 2.5V ± 0.2V)

Parameter	Symbol	Pins	min.	Typ	max.	Unit	Notes
Input capacitance	CI1	CK, /CK	2.0	—	3.0	pF	1
	CI2	All other input pins	2.0	—	3.0	pF	1
Data input/output capacitance	CI/O	DQ, DM, DQS	4.0	—	5	pF	1, 2,

Notes: 1. These parameters are measured on conditions: f = 100MHz, VOUT = VDDQ/2, ΔVOUT = 0.2V, TA = +25°C.
2. DOUT circuits are disabled.

AC Characteristics (TA = -25 to +85ºC, VDD, VDDQ = 1.8V ± 0.15V, VSS, VSSQ = 0V)

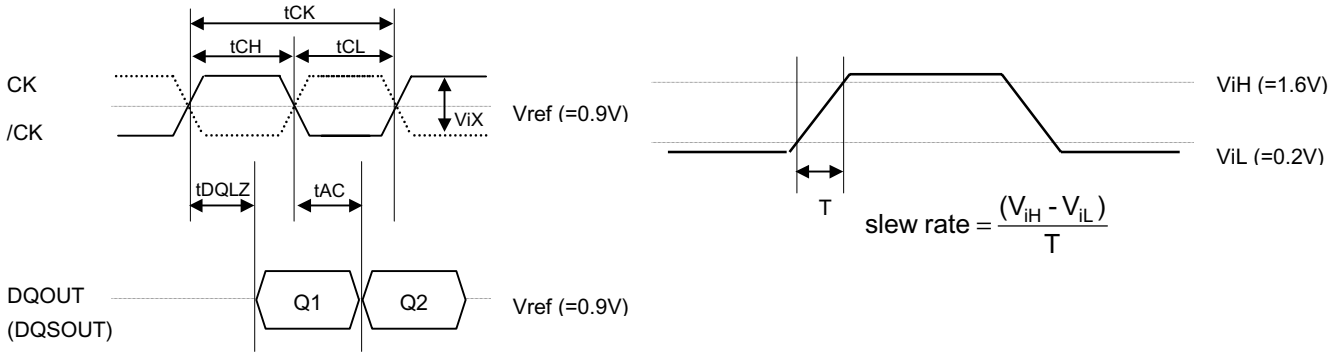
		-10		-15			
Parameter	Symbol	min.	max.	min.	max	Unit	Notes
Clock cycle time (CL =2)	tCK	—	—	15	—	ns	
(CL =3)	tCK	10	—	—	—	ns	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
DQ output access time from CK, /CK	tAC	2.0	7.0	2.0	9.0	ns	2
DQS output access time from CK, /CK	tDQSCK	2.0	7.0	2.0	9.0	ns	2
DQ-out high-impedance time from CK, /CK	tHZ	2.0	7.0	2.0	9.0	ns	5
DQ-out low-impedance time from CK, /CK	tLZ	2.0	7.0	2.0	9.0	ns	6
DQS-out high-impedance time from CK, /CK	tDQSHZ	2.0	7.0	2.0	9.0	ns	5
DQS-out low-impedance time from CK, /CK	tDQSLZ	2.0	7.0	2.0	9.0	ns	6
DQS to DQ skew	tDQSQ	—	0.75	—	1.0	ns	3
Dout valid window	tDV	3.0	—	4.0	—		4
DQ and DM input setup time	tDS	1.0	—	1.5	—	ns	3
DQ and DM input hold time	tDH	1.0	—	1.5	—	ns	3
Write preamble setup time	tWPRES	0	—	0	—	ns	
Write preamble	tWPRE	0.25	—	0.25	—	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	7
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	—	0.2	—	tCK	
DQS falling edge hold time from CK	tDSH	0.2	—	0.2	—	tCK	
DQS input high pulse width	tDQSH	0.35	—	0.35	—	tCK	
DQS input low pulse width	tDQSL	0.35	—	0.35	—	tCK	
Address and control input setup time	tIS	1.5	—	2.0	—	ns	3
Address and control input hold time	tIH	1.5	—	2.0	—	ns	3
Mode register set command cycle time	tMRD	2	—	2	—	tCK	
Active to Precharge command period	tRAS	60	120000	60	120000	ns	
Active to Active/Auto refresh command period	tRC	90	—	90	—	ns	
Auto refresh to Active/Auto refresh command period	tRFC	110	—	110	—	ns	
Active to Read/Write delay	tRCD	30	—	30	—	ns	
Precharge to active command period	tRP	30	—	30	—	ns	
Active to active command period	tRRD	20	—	20	—	ns	
Write recovery time	tWR	20	—	30	—	ns	
Self Refresh Exit Period	tSREX	120	—	120	—	ns	
Average periodic refresh interval	tREF	—	7.8	—	7.8	µs	

Notes:

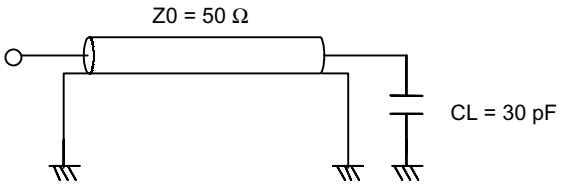
1. On all AC measurements, we assume the test conditions shown in the next page. Full driver strength is assumed for the output load seen in “Test conditions”, that is both A6 and A5 of EMRS is set to be “L”.
2. This parameter defines the signal transition delay from the cross point of CK and /CK. The signal transition is defined to occur when the signal level crossing VREF.
3. The timing reference level is VREF.
4. Output valid window is defined to be the period between two successive transition of data out signals. The signal transition is defined to occur when the signal level crossing VREF.
5. tHZ, tDQSHZ is defined as DOUT transition delay from Low-Z to High-Z at the end of read burst operation. The timing reference is cross point of CK and /CK. This parameter is not referred to a specific DOUT voltage level, but specify when the device output stops driving.
6. tLZ, tDQSLZ is defined as DOUT transition delay from High-Z to Low-Z at the beginning of read operation. This parameter is not referred to a specific DOUT voltage level, but specify when the device output begins driving.
7. The transition from Low-Z to High-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.

Test Conditions

Parameter	Symbol	Value	Unit
Input reference voltage	VREF	0.9	V
Input high voltage	VIH (AC)	1.6	V
Input low voltage	VIL (AC)	0.2	V
Input differential voltage, CK and /CK inputs	VID (AC)	1.4	V
Input differential cross point voltage, CK and /CK inputs	VIX (AC)	0.9	V
Input signal slew rate	SLEW	1	V/ns



Test condition (Wave form and Timing Reference)

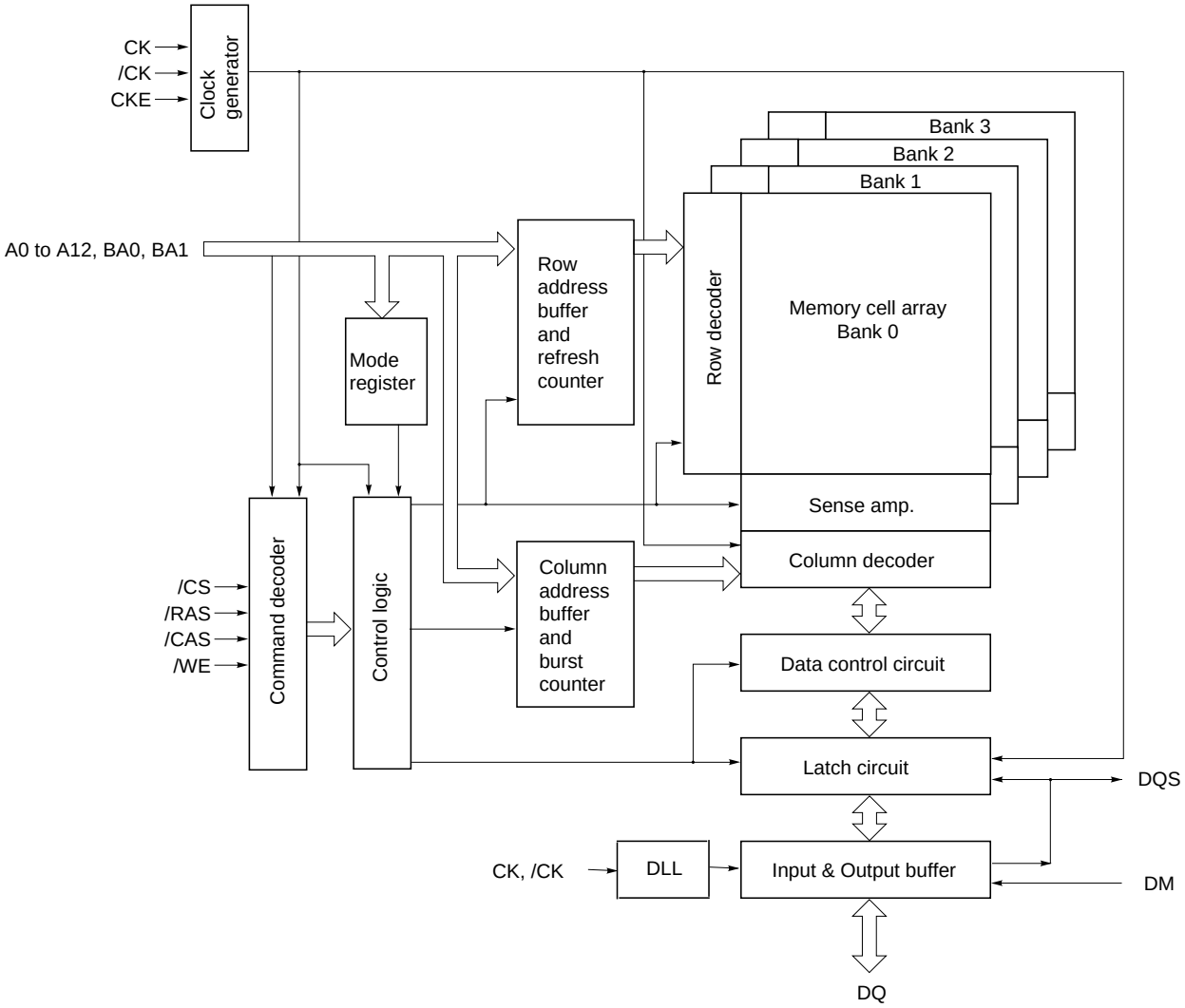


Output Load

Timing Parameter Measured in Clock Cycle

		Number of clock cycle			
tCK		10ns		15ns	
Parameter	Symbol	min.	max.	min.	max.
Write to pre-charge command delay (same bank)	tWPD	3 + BL/2		3 + BL/2	
Read to pre-charge command delay (same bank)	tRPD	BL/2		BL/2	
Write to read command delay (to input all data)	tWRD	2 + BL/2		2 + BL/2	
Burst stop command to write command delay (CL = 2)	tBSTW	—		2	
(CL = 3)	tBSTW	3		—	
Burst stop command to DQ High-Z (CL = 2)	tBSTZ	—		2	
(CL = 3)	tBSTZ	3		—	
Read command to write command delay (to output all data) (CL = 2)	tRWD	—		2 + BL/2	
(CL = 3)	tRWD	3 + BL/2		—	
Pre-charge command to High-Z (CL = 2)	tHZP	—		2	
(CL = 3)	tHZP	3		—	
Write command to data in latency	tWCD	1		1	
Write recovery	tWR	2		2	
DM to data in latency	tDMD	0		0	
Mode register set command cycle time	tMRD	2		2	
Self refresh exit to non-column command	tSNR	12		8	
Auto refersh period	tRFC	11		8	
Power down entry	tPDEN	1		1	
Power down exit to command input	tPDEX	1		1	

Block Diagram



Pin Function

CK, /CK (input pins)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the /CK falling edge. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CK and the /CK. CK is the master clock input to this pin. The other input signals are referred at CK rising edge.

/CS (input pin)

When /CS is Low, commands and data can be input. When /CS is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 toA12 (input pins)

Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the /CK falling edge in a bank active command cycle. Column address (See “Address Pins Table”) is loaded via the A0 to the A8 at the cross point of the CK rising edge and the /CK falling edge in a read or a write command cycle. This column address becomes the starting address of a burst operation.

[Address Pins Table]

	Address (A0 to A12)	
Part number	Row address	Column address
EDK2516CBBH	AX0 to AX12	AY0 to AY8

A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = High when a precharge command is issued, all banks are precharged. If A10 = Low when a precharge command is issued, only the bank that is selected by BA1/BA0 is precharged. If A10 = High when read or write command, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

BA0 and BA1 (input pins)

BA0, BA1 are bank select signals (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low. CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High. CKE must be maintained high throughout read or write access.

The CKE level must be kept for 1 CK cycle at least, that is, if CKE changes at the cross point of the CK rising edge and the /CK falling edge with proper setup time tIS, by the next CK rising edge CKE level must be kept with proper hold time tIH.

DQ0 toDQ15 (input/output pins)

Data is input to and output from these pins.

UDQS, LDQS (input and output pin): DQS provides the read data strobes (as output) and the write data strobes (as input). LDQS is the strobe signals specific for the lower DQ signls (DQ0-DQ7). UDQS is the strobe signals specific for the upper DQ signls (DQ8-DQ15).

UDM, LDM (input pin)

DM are the reference signals of the data input mask function. DMs are sampled at the cross point of DQS and VREF. LDM controls the lower DQ signals (DQ0-DQ7). UDM controls the upper DQ signals (DQ7-DQ15).

VDD, VSS, VDDQ, VSSQ (Power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

Command Operation

Command Truth Table

DDR Mobile RAM recognize the following commands specified by the /CS, /RAS, /CAS, /WE and address pins. All other combinations than those in the table below are illegal.

		CKE									
Command	Symbol	n – 1	n	/CS	/RAS	/CAS	/WE	BA1	BA0	AP	Address
Ignore command	DESL	H	H	H	×	×	×	×	×	×	×
No operation	NOP	H	H	L	H	H	H	×	×	×	×
Burst stop in read command	BST	H	H	L	H	H	L	×	×	×	×
Column address and read command	READ	H	H	L	H	L	H	V	V	L	V
Read with auto-precharge	READA	H	H	L	H	L	H	V	V	H	V
Column address and write command	WRIT	H	H	L	H	L	L	V	V	L	V
Write with auto-precharge	WRITA	H	H	L	H	L	L	V	V	H	V
Row address strobe and bank active	ACT	H	H	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	H	L	L	H	L	V	V	L	×
Precharge all bank	PALL	H	H	L	L	H	L	×	×	H	×
Refresh	REF	H	H	L	L	L	H	×	×	×	×
	SELF	H	L	L	L	L	H	×	×	×	×
Mode register set	MRS	H	H	L	L	L	L	L	L	L	V
	EMRS	H	H	L	L	L	L	L	H	L	V

Remark: H: VIH. L: VIL. ×: VIH or VIL V: Valid address input

Note: The CKE level must be kept for 1 CK cycle at least.

Ignore command [DESL]

When /CS is High at the cross point of the CK rising edge and the VREF level, every input are neglected and internal status is held.

No operation [NOP]

As long as this command is input at the cross point of the CK rising edge and the VREF level, address and data input are neglected and internal status is held.

Burst stop in read operation [BST]

This command stops a burst read operation, which is not applicable for a burst write operation.

Column address strobe and read command [READ]

This command starts a read operation. The start address of the burst read is determined by the column address (See “Address Pins Table” in Pin Function) and the bank select address. After the completion of the read operation, the output buffer becomes High-Z.

Read with auto-precharge [READA]

This command starts a read operation. After completion of the read operation, precharge is automatically executed.

Column address strobe and write command [WRIT]

This command starts a write operation. The start address of the burst write is determined by the column address (See “Address Pins Table” in Pin Function) and the bank select address.

Write with auto-precharge [WRITA]

This command starts a write operation. After completion of the write operation, precharge is automatically executed.

Row address strobe and bank activate [ACT]

This command activates the bank that is selected by BA0, BA1 and determines the row address (AX0 to AX12). (See Bank Select Signal Table)

Precharge selected bank [PRE]

This command starts precharge operation for the bank selected by BA0, BA1. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

Precharge all banks [PALL]

This command starts a precharge operation for all banks.

Refresh [REF/SELF]

This command starts a refresh operation. There are two types of refresh operation, one is auto-refresh, and another is self-refresh. For details, refer to the CKE truth table section.

Mode register set/Extended mode register set [MRS/EMRS]

The DDR mobile RAM has the two mode registers, the mode register and the extended mode register, to defines how it works. The both mode registers are set through the address pins (the A0 to the A12, BA0 to BA1) in the mode register set cycle. For details, refer to "Mode register and extended mode register set".

Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR Mobile SDRAM.

Function Truth Table (1)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Precharging*1	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*11	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*11	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*11	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	×	×		ILLEGAL	—
Idle*2	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*11	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*11	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*11	—
	L	L	H	H	BA, RA	ACT	Activating	Active
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	H	×	REF, SELF	Refresh/ Self refresh*12	Idle/ Self refresh
	L	L	L	L	MODE	MRS	Mode register set*12	Idle
Refresh (auto-refresh)*3	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	H	H	H	L	×	BST	ILLEGAL	—
	L	H	L	×	×		ILLEGAL	—
	L	L	×	×	×		ILLEGAL	—

Function Truth Table (2)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Activating*4	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL*11	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*11	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*11	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*11	—
	L	L	L	×	×		ILLEGAL	—
Active*5	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	Active
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation	Read/READA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting write operation	Write recovering/ precharging
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	Pre-charge	Idle
	L	L	L	×	×		ILLEGAL	—
Read*6	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	BST	Active
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst read operation to start new read	Active
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*13	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting burst read operation to start pre-charge	Precharging
	L	L	L	×	×		ILLEGAL	—

Function Truth Table (3)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Read with auto-pre-charge*7	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*11	—
	L	L	L	×	×		ILLEGAL	—
Write*8	H	×	×	×	×	DESL	NOP	Write recovering
	L	H	H	H	×	NOP	NOP	Write recovering
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst write operation to start read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Interrupting burst write operation to start new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting write operation to start pre-charge.	Idle
	L	L	L	×	×		ILLEGAL	—
Write recovering*9	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL*11	—
	L	L	L	×	×		ILLEGAL	—

Function Truth Table (4)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Write with auto-pre-charge*10	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	—
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*11	—
	L	L	L	×	×		ILLEGAL	—

Remark: H: VIH. L: VIL. ×: VIH or VIL

Notes: 1. The DDR mobile RAM is in "Precharging" state for tRP after precharge command is issued.
2. The DDR mobile RAM reaches "IDLE" state tRP after precharge command is issued.
3. The DDR mobile RAM is in "Refresh" state for tRC after auto-refresh command is issued.
4. The DDR mobile RAM is in "Activating" state for tRCD after ACT command is issued.
5. The DDR mobile RAM is in "Active" state after "Activating" is completed.
6. The DDR mobile RAM is in "READ" state until burst data have been output and DQ output circuits are turned off.
7. The DDR mobile RAM is in "READ with auto-precharge" from READA command until burst data has been output and DQ output circuits are turned off.
8. The DDR mobile RAM is in "WRITE" state from WRIT command to the last burst data are input.
9. The DDR mobile RAM is in "Write recovering" for tWR after the last data are input.
10. The DDR miobile RAM is in "Write with auto-precharge" until tWR after the last data has been input.
11. This command may be issued for other banks, depending on the state of the banks.
12. All banks must be in "IDLE".
13. Before executing a write command to stop the preceding burst read operation, BST command must be issued.

CKE Truth Table

Current state	Command	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	Address	Notes
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	×	2
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	×	2
Idle	Power down entry (PDEN)	H	L	L	H	H	H	×	
		H	L	H	×	×	×	×	
Idle	Deep power down entry(DPWDE)	H	L	L	H	H	L	×	
Self refresh	Self refresh exit (SELFX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	
Power down	Power down exit (PDEX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	
Deep power down	Power down exit (DPDEX)	L	H	×	×	×	×	×	

Notes: 1. H : VIH . L : VIL × : VIH or VIL .

2. All the banks must be in IDLE before executing this command.

3. The CKE level must be kept for 1 CLK cycle at least.

Auto-refresh command [REF]

This command executes auto-refresh. The banks and the ROW addresses to be refreshed are internally determined by the internal refresh controller. The average refresh cycle is 7.8 μs. The output buffer becomes High-Z after auto-refresh start. Precharge has been completed automatically after the auto-refresh. The ACT or MRS command can be issued tRFC after the last auto-refresh command.

Self-refresh entry [SELF]

This command starts self-refresh. The self-refresh operation continues as long as CKE is held Low. During the self-refresh operation, all ROW addresses are repeated refreshing by the internal refresh controller. A self-refresh is terminated by a self-refresh exit command.

Power down mode entry [PDEN]

tPDEN (= 1 cycle) after the cycle when [PDEN] is issued. The DDR Mobile RAM enters into power-down mode. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. No internal refresh operation occurs during the power down mode. [PDEN] do not disable DLL.

Deep power down entry [DPDEN]

After the command execution, deep power down mode continues while CKE remains low.

Before executing deep power down, all banks must be precharged or in idle state.

Self-refresh exit [SELFX]

This command is executed to exit from self-refresh mode. tRC + 3tCK after [SELFX], non-read commands can be executed

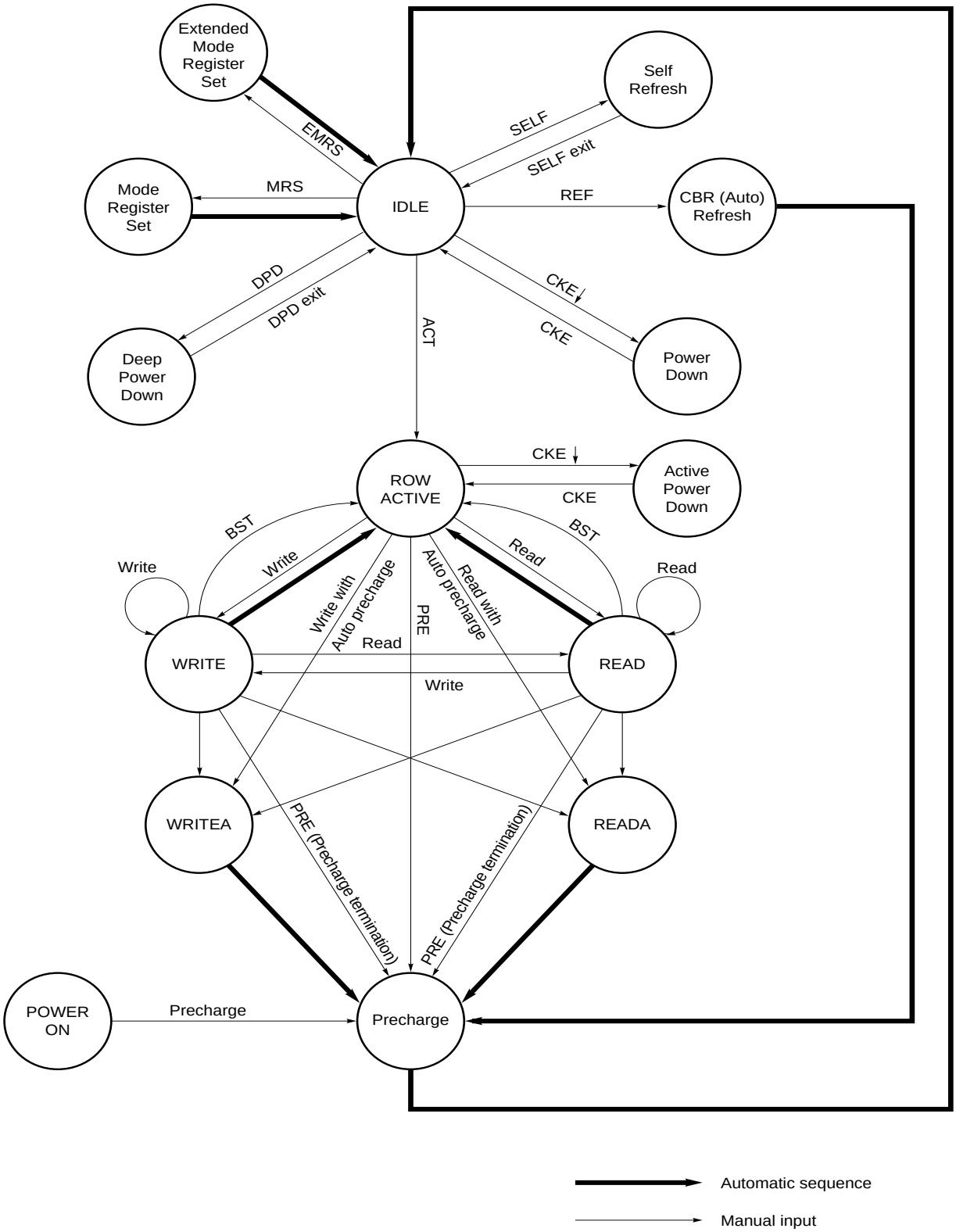
Power down exit [PDEX]

The DDR Mobile SDRAM can exit from power down mode tPDEX (1 cycle min.) after the cycle when [PDEX] is issued.

Deep power down exit [DPDEX]

CKE goes high in the deep power down mode, the DDR Mobile RAM exits the deep power down mode.

Simplified State Diagram



Operation of the DDR Mobile RAM

Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 200 μs or longer pause must precede any signal toggling.

(2) After the pause, all banks must be precharged using the Precharge command (The Precharge all banks command is convenient).

(3) Once the precharge is completed and the minimum tRP is satisfied, two or more Auto refresh must be performed.

(4) Both the mode register and the extended mode register must be programmed. After the mode register set cycle or the extended mode register set cycle, tRSC (2 CLK minimum) pause must be satisfied.

Remarks:

1 The sequence of Auto refresh, mode register programming and extended mode register programming above may be transposed.

2 CKE and DQM must be held high until the Precharge command is issued to ensure data-bus High-Z.

Mode Register and Extended Mode Register Set

There are two mode registers, the mode register and the extended mode register so as to define the operating mode. Parameters are set to both through the A0 to the A12 and BA0, BA1 pins by the mode register set command [MRS] or the extended mode register set command [EMRS]. The mode register and the extended mode register are set by inputting signal via the A0 to the A12 and BA0, BA1 during mode register set cycles. BA0 and BA1 determine which one of the mode register or the extended mode register are set. Prior to a read or a write operation, the mode register must be set.

Remind that no other parameters are shown in the table bellow are allowed to input to the registers.

Mode register

The mode register has three fields;

Options : A12 through A7
/CAS latency : A6 through A4
Wrap type : A3
Burst length : A2 through A0

Following mode register programming, no command can be issued before at least 2 CLK have elapsed.

/CAS Latency

Set /CAS latency as follows.

Part number	/CAS latency
EDK2516CBBH-10-E	3
EDK2516CBBH-15-E	2

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become High-Z. The burst length is programmable as 2, 4, 8.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. “Burst Length Sequence” shows the addressing sequence for each burst length using them. Both sequences support bursts of 2, 4 and 8.

Extended Mode Register

The extended mode register has four fields;

Options	: A12 through A7
Drive Strength	: A6 through A5
Temperature Compensated Self Refresh	: A4 through A3
Partial Array Self Refresh	: A2 through A0

Following extended mode register programming, no command can be issued before at least 2 CLK have elapsed.

Drive Strength

By setting specific parameter on A6 and A5, driving capability of data output drivers is selected.

Temperature Compensated Self Refresh

A4 and A3 bit of EMRS control the internal self refresh timer and self refresh current.

Partial Array Self Refresh

Memory array size to be refreshed during self refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self refresh.

Mode Register Definition

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	LTMODE			WT	BL			Mode Register Set

	Bits6-4	/CAS latency
Latency mode	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

	Bits2-0	WT = 0	WT = 1
Burst length	000	R	R
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	R	R

Wrap type	0	Sequential
	1	Interleave

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	1	0	0	0	0	0	0	DS		TCSR		PASR			Extended Mode Register Set

	Bits6-5	Strength
Drive Strength	00	Normal
	01	1/2 strength
	10	1/4 strength
	11	1/8 strength

	Bits2-0	Refresh Array
Partial Array Self Refresh	000	All banks
	001	Bank A & Bank B (BA1=0)
	010	Bank A (BA0=BA1=0)
	011	R
	100	R
	101	1/2 of Bank A (RA11=0)
	110	1/4 of Bank A (RA11=RA10=0)
	111	R

	Bits4-3	Max Temperature
Temprature Compensated Self Refresh	00	70°C
	01	45°C
	10	15°C
	11	85°C

Remark R : Reserved

Burst Operation

The burst type (BT) and the first three bits of the column address determine the order of a data out.

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

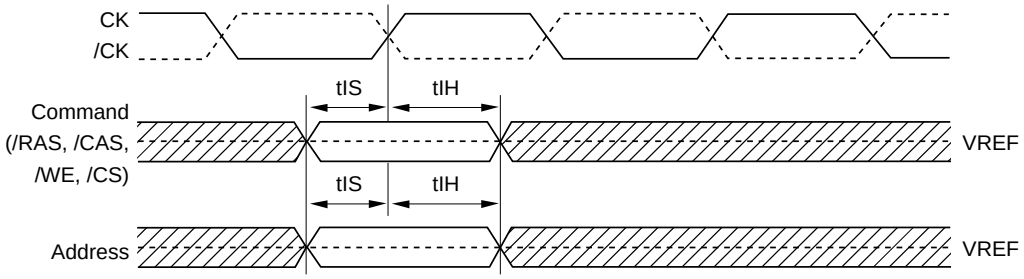
Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

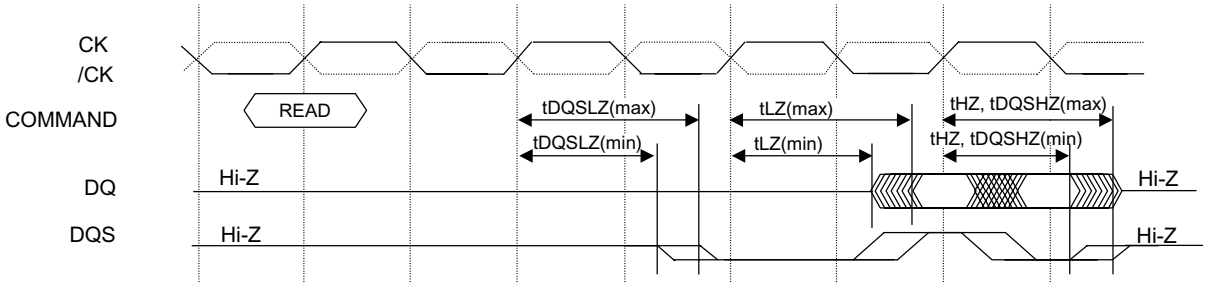
Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

Timing Waveforms

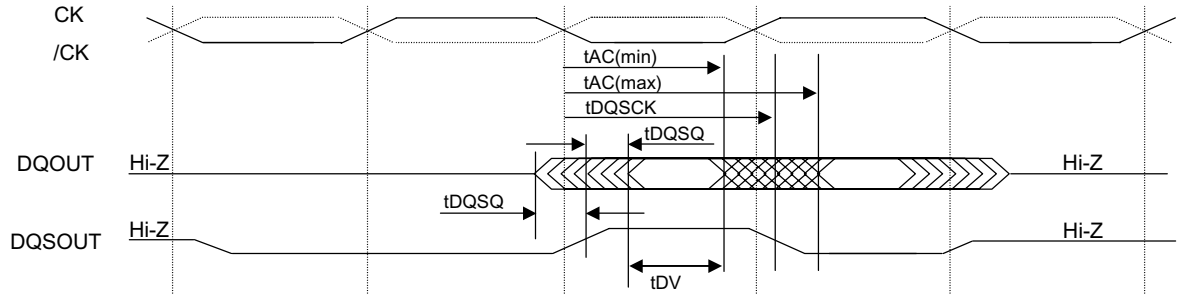
Command and Addresses Input Timing Definition



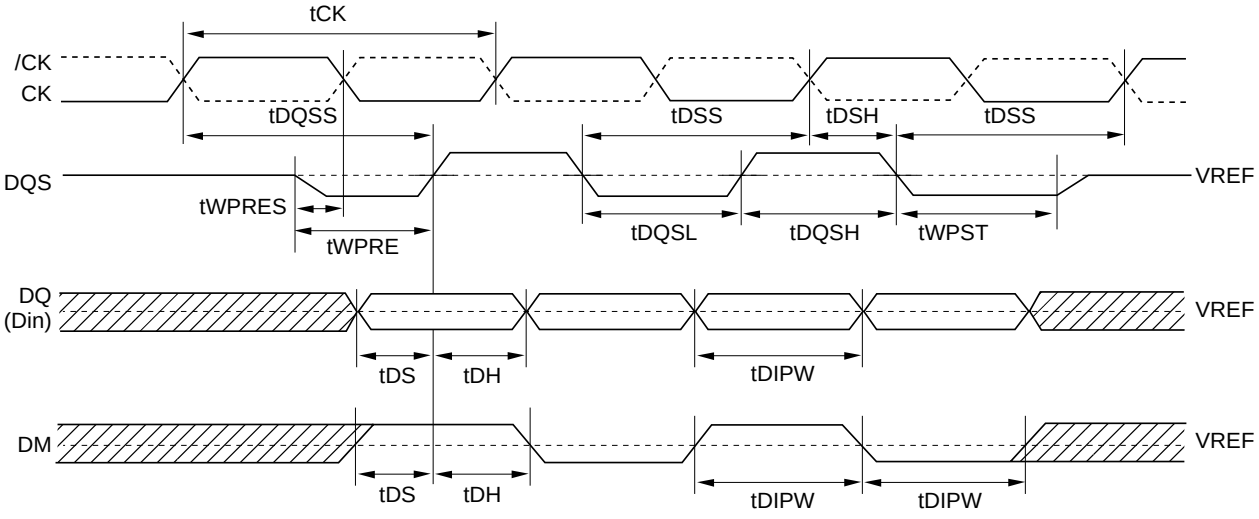
Read Timing Definition(1)



Read Timing Definition(2)



Write Timing Definition

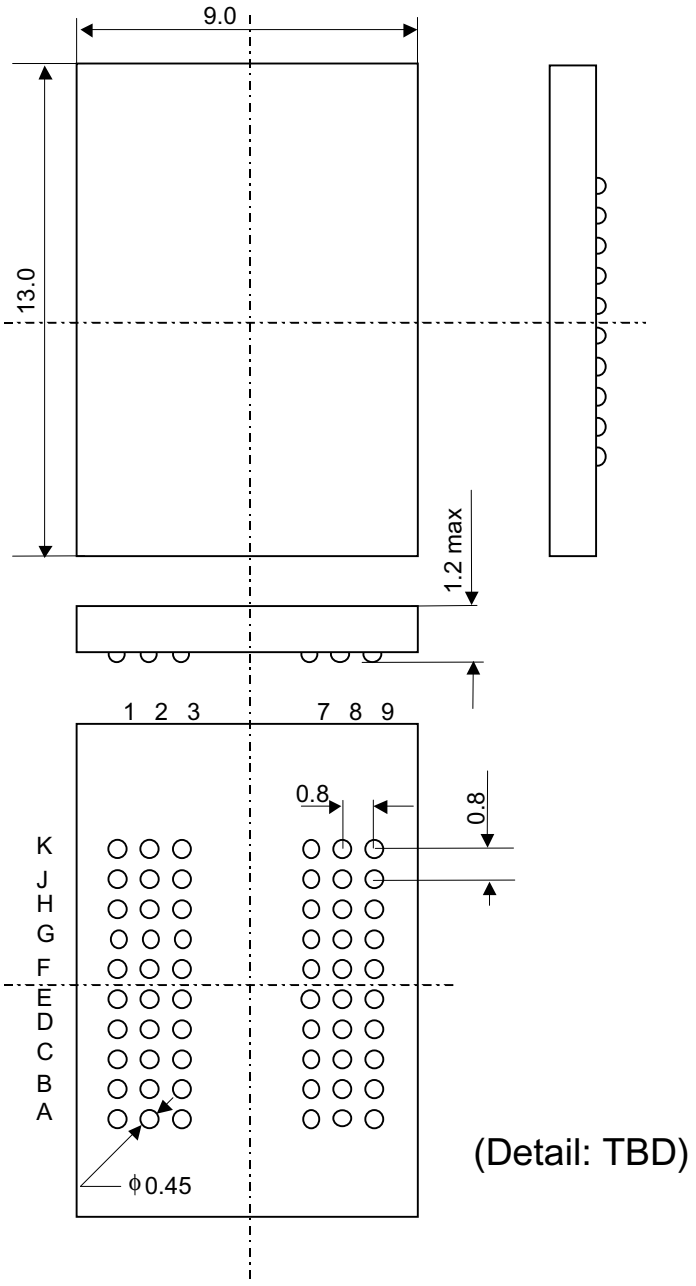


Package Drawing

60-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit : mm



(Detail: TBD)

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the EDK2516CBBH.

Type of Surface Mount Device

EDK2516CBBH: 60-ball FBGA < Lead free (Sn-Ag-Cu) >

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107