Power -Distribution Switches with Soft Start

Features

- **78mΩ High Side MOSFET**
- **2.5A Continuous Current**
- **Soft Start Time Programmable by External Capacitor**
- **Wide Supply Voltage Range: 4.5V to 24V**
- **Current Limit and Short Circuit Protections**
- **Under Voltage Lockout Protection**
- **Over-temperature Protection**
- **Logic Level Enable Input**
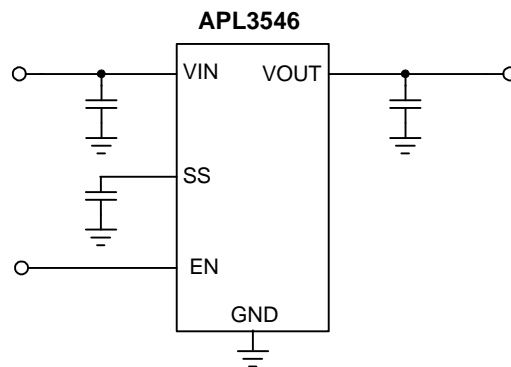- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **TFT LCD Modules**
- **Notebook and Desktop Computers**
- **USB Ports**
- **High-side Power Protection Switches**

General Description

The APL3546 is a power-distribution switch with some protection functions that can deliver current up to 2.5A. The device incorporates a 78mΩ N-channel MOSFET power switch that is controlled by an enable logic pin and has a SS pin dedicated to soft start ramp-up rate control that can be used in application where the inrush current is concerned.
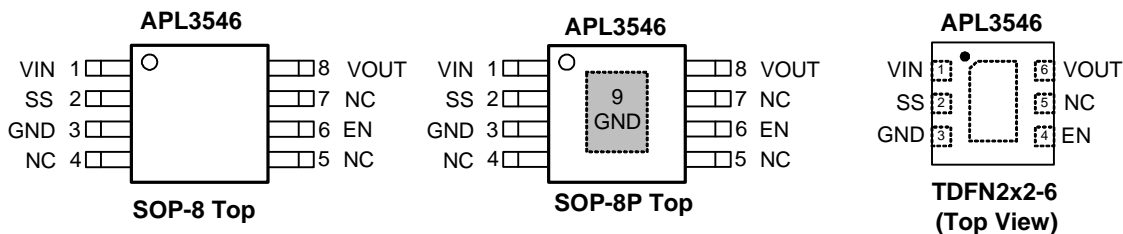
The device integrates some protection features, including current limit protection, short circuit protection, over-temperature protection and UVLO. The current limit and short circuit protection can protect down-stream devices from catastrophic failure by limiting the output current at current limit threshold during over-load or short circuit events. When VOUT drops below V_{IN}-1V the devices limit the current to a lower and safe level. The over-temperature protection function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 150°C and will automatically turns on the power switch when the temperature drops by 20°C. The UVLO function keeps the power switch in off state until there is a valid input voltage present.
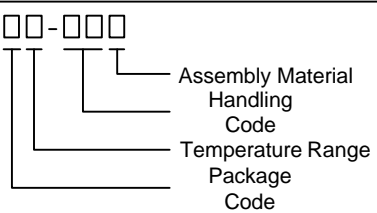
Simplified Application Circuit

Pin Configuration

APL3546

VIN 1 ☐ ☐ 8 VOUT
SS 2 ☐ ☐ 7 NC
GND 3 ☐ ☐ 6 EN
NC 4 ☐ ☐ 5 NC

SOP-8 Top

APL3546

VIN 1 ☐ ☐ 8 VOUT
SS 2 ☐ 9 ☐ 7 NC
GND 3 ☐ GND ☐ 6 EN
NC 4 ☐ ☐ 5 NC

SOP-8P Top

APL3546

VIN 1 ☐ ☐ 6 VOUT
SS 2 ☐ ☐ 5 NC
GND 3 ☐ ☐ 4 EN

**TDFN2x2-6
(Top View)**

Ordering and Marking Information

APL3546 ☐☐-☐☐☐

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
  K : SOP-8   QB : TDFN 2×2-6   KA : SOP-8P
Operating Ambient Temperature Range
  I : -40 to 85°C
Handling Code
  TR : Tape & Reel
Assembly Material
  G : Halogen and Lead Free Device

APL3546 K: APL3546
             XXXXX
             •   X - Date Code

APL3546 QB: L46
              • X   X - Date Code

APL3546 KA: APL3546
              XXXXX
              •   X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND Voltage	-0.3 ~ 26	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 26	V
V_{EN}	EN to GND Voltage	-0.3 ~ 7	V
V_{SS}	SS to GND Voltage	-0.3 ~ 7	V
I_{OUT}	Continuous output current, IOUT	Internally Limited	A
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air	SOP-8	130	^{o}C/W
		SOP-8P	75	
		TDFN2x2-6	130	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	4.5 ~ 24	V
I_{OUT}	VOUT Output Current	0 ~2.5	A
T_A	Ambient Temperature	-40 ~ 85	^{o}C
T_J	Junction Temperature	-40 ~ 125	^{o}C

Note 3: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN} =5V. Typical values are at T_A=25°C.

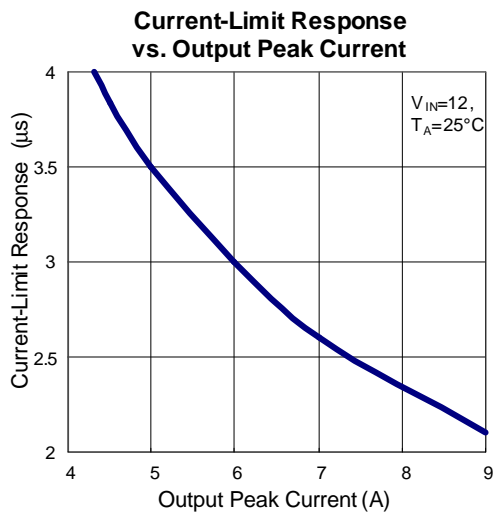| Symbol	Parameter	Test Conditions	APL3546			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VIN Supply Current	No load, V_{EN}=0V	-	30	50	µA
		No load, V_{EN}=5V	-	250	400	µA
	Leakage Current	V_{OUT}=GND , V_{EN}=0V	-	-	1	µA
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	I_{OUT}=2A, T_A= 25 ^{o}C ,V_{IN}=12V	-	78	90	mΩ
		I_{OUT}=2A, V_{IN}=12V	-	78	100	mΩ
UNDER-VOLTAGE LOCKOUT						
	VIN UVLO Threshold Voltage	V_{IN} rising	3.3	-	3.9	V
	VIN UVLO Hysteresis		-	0.2	-	V
CURRENT LIMIT AND SHORT CIRCUIT PROTECTIONS						
I_{LIM}	Current Limit Threshold	V_{IN}=4.5V to 24V	4	5	6	A
I_{SHORT}	Short Circuit Output Current	V_{IN}=4.5V to 24V	-	-	1.2	A
SOFT-START CONTROL PIN						
I_{SS}	SS Current	V_{IN}=12V,	1	2	3	µA
t_{SS}	Soft-Start Time	V_{IN}=12V, No load, C_{OUT}=1uF, C_{SS} =1nF	-	0.5	-	ms
		V_{IN}=12V, No load, C_{OUT}=1uF, C_{SS} =open	1	2	3	ms
	Soft-Star Discharge Resistance	V_{EN}=0V	-	300	-	Ω

Electrical Characteristics(Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN} =5V. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3546			Unit
			Min.	Typ.	Max.	
EN INPUT PIN						
V_{IH}	Input Logic High	V_{IN}=4.5V to 24V	2	-	-	V
V_{IL}	Input Logic Low	V_{IN}=4.5V to 24V	-	-	0.6	V
	Input Current		-	-	1	µA
	VOUT Discharge Resistance	V_{EN}=0V	-	950	-	Ω
$t_{D(ON)}$	Turn on Delay Time		-	300	-	µs
$t_{D(OFF)}$	Turn off Delay Time		-	3	-	µs
OVERT-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Threshold	T_J rising	-	150	-	°C
	Over-Temperature Hysteresis		-	20	-	°C

Pin Description

| NO.			NAME	FUNCTION
SOP-8	SOP-8P	TDFN2x2-6		
1	1	1	VIN	Power Supply Input. Connect this pin to external DC supply.
2	2	2	SS	Soft Start Control Pin. Connect a capacitor to GND to control the soft start rate. If the SS pin is left floating the soft start time is 2ms when V_{IN}=12V.
3	3,9	3	GND	GND
4	4	-	NC	No connection.
5	5	-	NC	No connection.
6	6	4	EN	Enable Input. Pull this pin to high to enable the device and pull this pin to low to disable device. The EN pin cannot be left floating.
7	7	5	NC	No connection.
8	8	6	VOUT	Output Voltage Pin. The output voltage follows the input voltage. When EN is low the output voltage is discharged by an internal resistor.

Typical Operating Characteristics

**Current-Limit Response
vs. Output Peak Current**

V_{IN}=12,
T_A=25°C

Current-Limit Response (µs)

Output Peak Current (A)

Operating Waveforms

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.
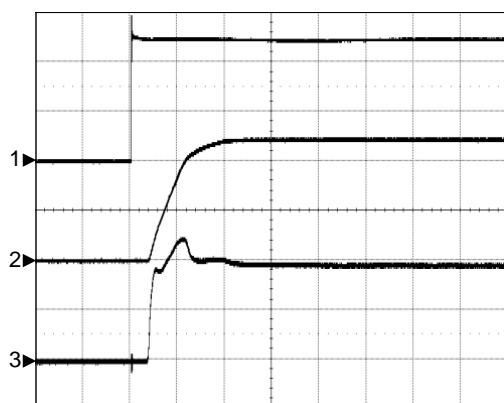
Power On
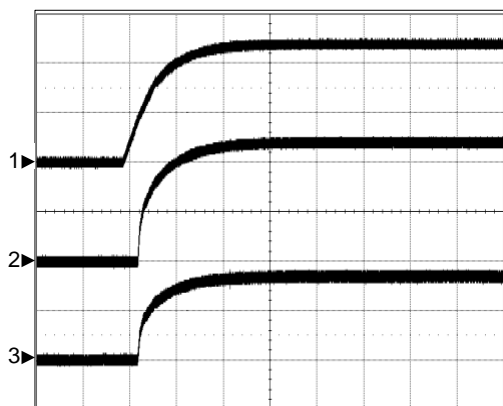
Vin=12V, Cin=1uF, Cout=10uF, Rout=30Ω
CH1: V_{in} (5V/Div)
CH2: V_{out} (5V/Div)
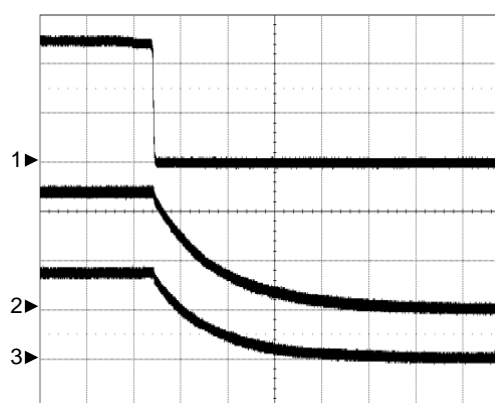CH3: I_{in} (0.2A/Div)
Time: 5ms/Div

Power Off
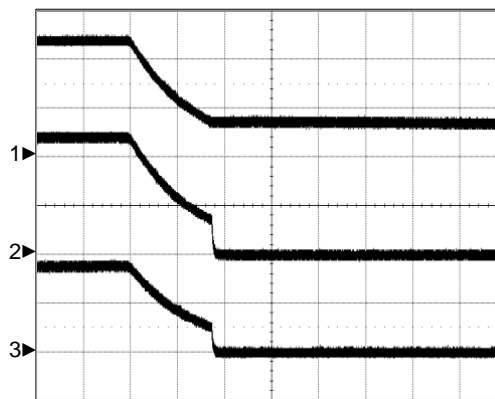
Vin=12V, Cin=1uF, Cout=10uF, Rout=30Ω
CH1: V_{in} (5V/Div)
CH2: V_{out} (5V/Div)
CH3: I_{in} (0.2A/Div)
Time: 10ms/Div

Turn On Response

Vin=12V, Cin=1uF, Cout=10uF, Rout=30Ω
CH1: EN (2V/Div)
CH2: V_{out} (5V/Div)
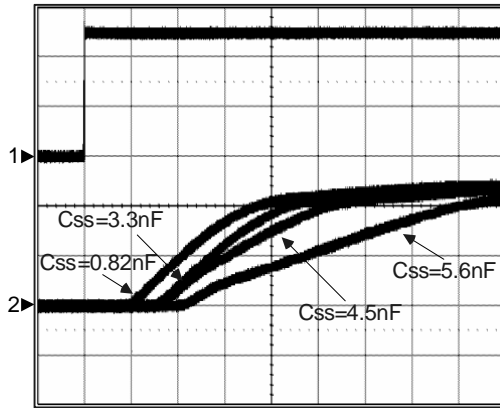CH3: I_{in} (0.2A/Div)
Time: 500us/Div

Turn Off Response

Vin=12V, Cin=1uF, Cout=10uF, Rout=30Ω
CH1: EN (2V/Div)
CH2: V_{out} (5V/Div)
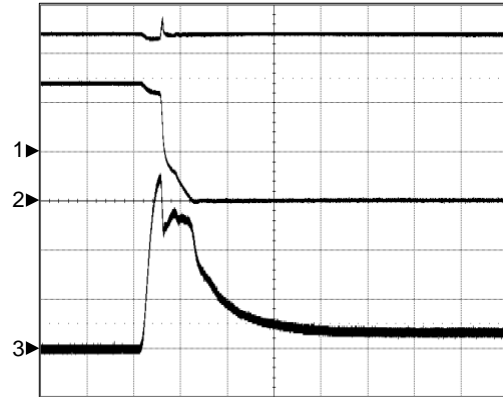CH3: I_{in} (0.2A/Div)
Time: 500us/Div

Operating Waveforms

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.
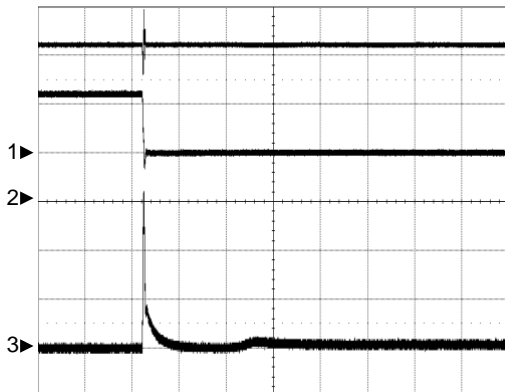
Soft Start Ramp Up Control

Css=3.3nF

Css=0.82nF

Css=5.6nF

Css=4.5nF

Vin=12V, Cin=1uF, Cout=10uF, Rload=30Ω
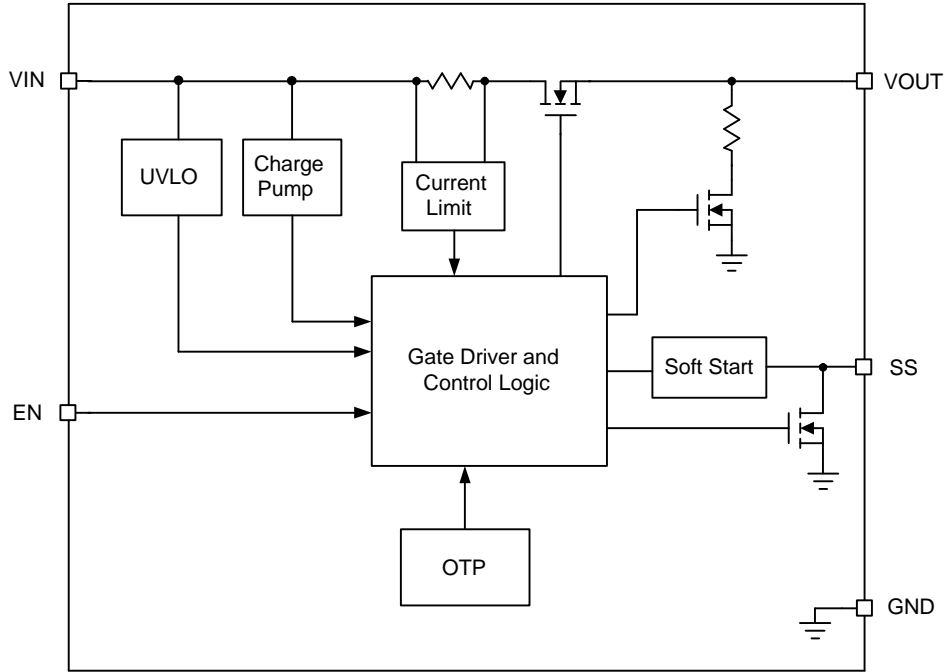CH1: EN (2V/Div)
CH2: V_{out} (5V/Div)
Time: 100us/Div

Current Limit Response

Vin=12V, Cin=1uF, Cout=10uF
CH1: Vin (5V/Div)
CH2: V_{out} (5V/Div)
CH3: I_{out} (2A/Div)
Time: 20us/Div

Short circuit Protection

Vin=12V, Cin=1uF, Cout=10uF,
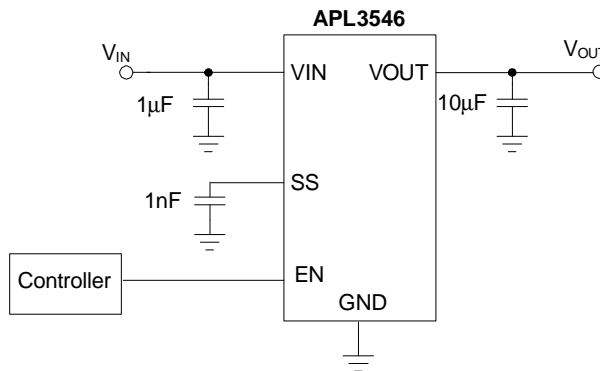Vout short to GND
CH1: Vin (5V/Div)
CH2: V_{out} (5V/Div)
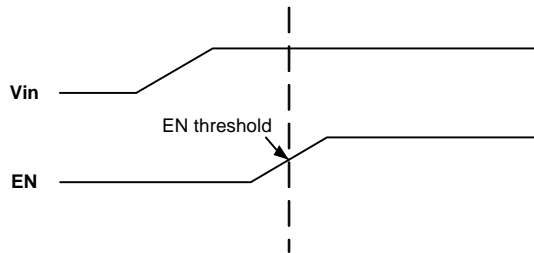CH3: I_{out} (2A/Div)
Time: 20us/Div

Block Diagram

Typical Application Circuit

Function Description

Power Sequencing

At start-up, it is necessary to ensure that the V_{IN} and EN are sequenced correctly.

Under-voltage Lockout (UVLO)

The APL3546 power switch is built-in an under-voltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switch is an N-channel MOSFET with a low RDS(ON). The internal power MOSFET does not have the body diode. When IC is off, the MOSFET prevents a current flowing from the VOUT back to VIN and VIN to VOUT.

Current Limit Protection

The APL3546 power switch provides the current limit protection function. During current limit, the devices limit output current at current limit threshold. For reliable operation, the device should not be operated in current limit for extended period time.

Short-circuit Protection

When the output voltage drops below VIN-1V, which is caused by the over load or short circuit, the devices limit the output current down to a safe level. The short circuit current limit is used to reduce the power dissipation during short circuit condition. If the junction temperature is over the thermal shutdown temperature the device will enter the thermal shutdown.

Soft-Start

The APL3546 provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start ramp-up rate is controlled by a capacitor from SS pin to ground. the soft start time can be calculated by this following equation:

$$t_{ss} = 0.1(C_{SS} \times V_{IN})/ I_{SS}$$

where,

t_{SS} is soft start time of VOUT rising from 0 to 100%, of which unit is second.

C_{SS} is the value of the capacitor connected from SS pin to GND, of which unit is micro-Farad.

V_{IN} is the amplitude of input voltage applied to this device, of which unit is volt.

I_{SS} is the SS pin charge current, typical value is 2μA.

If the C_{SS} is not connected or tied to V_{IN}, the soft start time is 2ms when V_{IN}=12V.

Enable/Disable

Pull the EN below 0.6V to disable the device and pull EN above 2V to enable the device. When the IC is disabled the supply current is reduced to less than 35μA. The enable input is compatible with both TTL and CMOS logic levels. The EN pin cannot be left floating.

Over-temperature Protection

When the junction temperature exceeds 150°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Application Information

Input Capacitor

A 1µF ceramic bypass capacitor from V_{IN} to GND, located near the APL3546, is strongly recommended to suppress the ringing during short-circuit fault event. Without the bypass capacitor, the output short may cause sufficient ringing on the input (from supply lead inductance) to damage internal control circuitry.

Output Capacitor

A low-ESR 10µF MLCC, aluminum electrolytic or tantalum between VOUT and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral. Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1µF ceramic capacitor improves the immunity of the device to short-circuit transients.

During soft-start process, the output bulk capacitor draws inrush current from VIN. If the inrush current reaches fold back current-limit threshold, namely 1A, the output current will be clamped in 1A level. It will take longer to complete the soft-start process since the soft-start rate is controlled neither by internal soft-start nor by external soft-start circuitry. When the C_{OUT} meets the following formula, the soft-start will be controlled by fold back current-limiting:

$$C_{OUT} > (I \times t_{ss}) / V_{IN}$$

where

t_{ss} is 2ms when SS is open or tied to V_{IN}, or obtained by the tss equation, described in the paragraph of Soft-Start in Functional Description section when C_{ss} is used. If the soft-start rate is controlled by the fold back current limiting, the soft-start time can be got by the following equation:

$$t_{ss\_Foldback} = (C_{OUT} \times V_{IN}) / I$$

Current Limit Protection

The APL3546 power switch provides the current limit protection function. During current limit, the devices limit output current at current limit threshold. For reliable operation, the device should not be operated in current limit for extended period time.

Soft-Start Capacitor

The APL3546 has a built-in adjustable soft-start control for user to set an optimum soft-start time for the application. The soft-start time can be calculated by the equation, described in the paragraph of Soft-Start in Functional Description section. Please note that there are minimum and maximum limitations of soft-start capacitor. If the value of soft-start capacitor is less than the minimum limitation or higher than the maximum limitation (please refer to the Recommended Operating Conditions), the soft-start time will become internally controlled as if there is no C_{ss}, t_{ss}=2ms when V_{IN}=12V, for example. If a soft start capacitor is used, please make sure the C_{ss} is in the recommended operating range.

Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VIN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.
3. Locate APL3546 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep V_{IN} and V_{OUT} traces as wide and short as possible.

Package Information

SOP-8

-T- SEATING PLANE < 4 mils

SEE VIEW A

h X 45°

VIEW A

GAUGE PLANE
SEATING PLANE
0.25
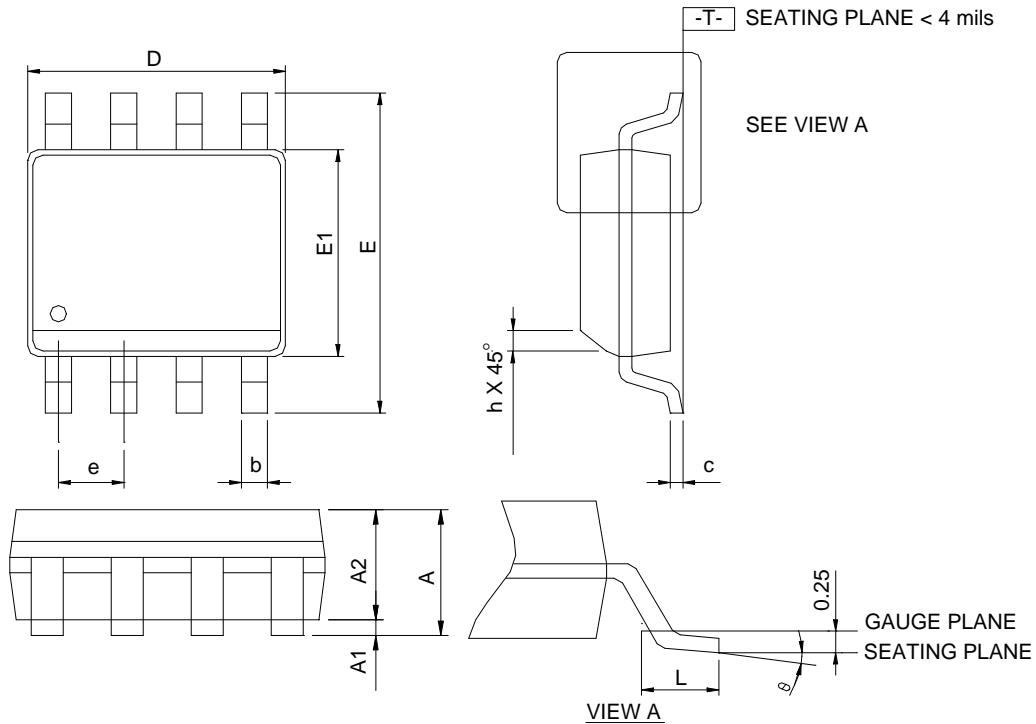
SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
   Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions.
   Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

SOP-8P
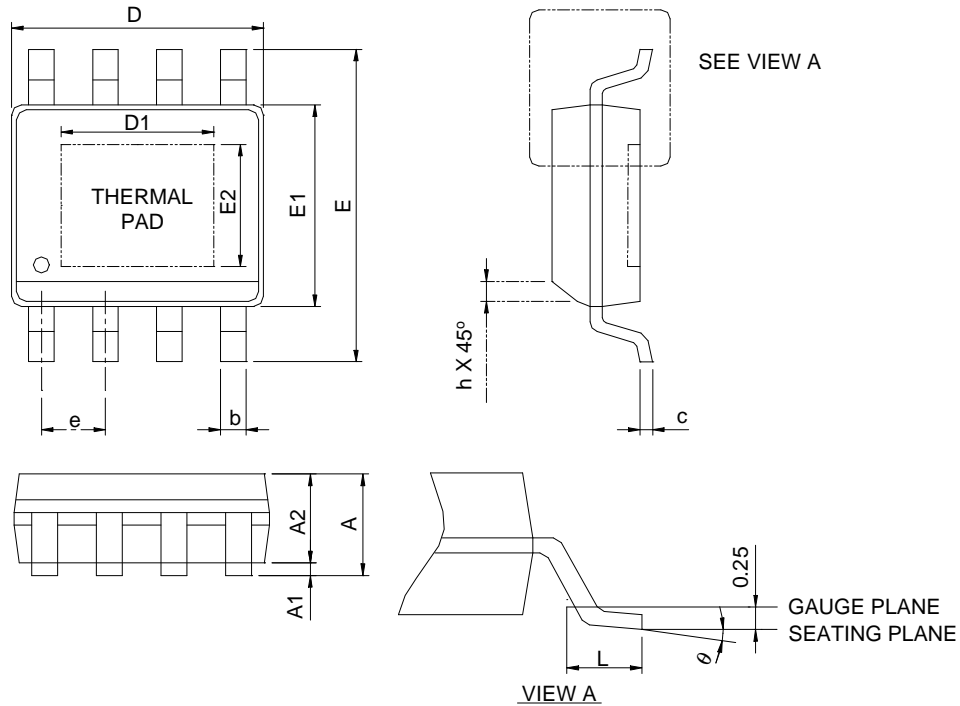
SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0ºC	8ºC	0ºC	8ºC

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

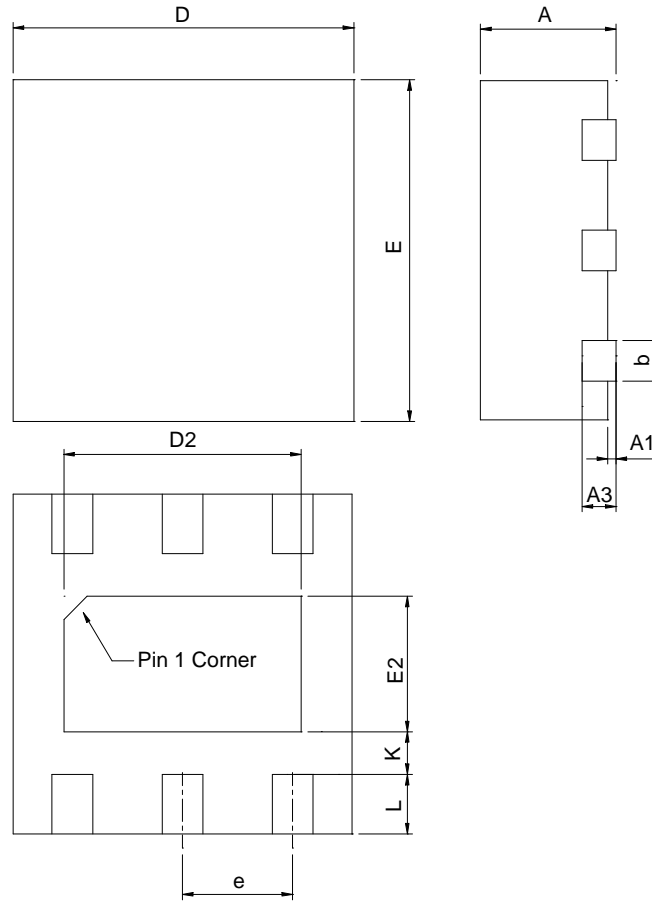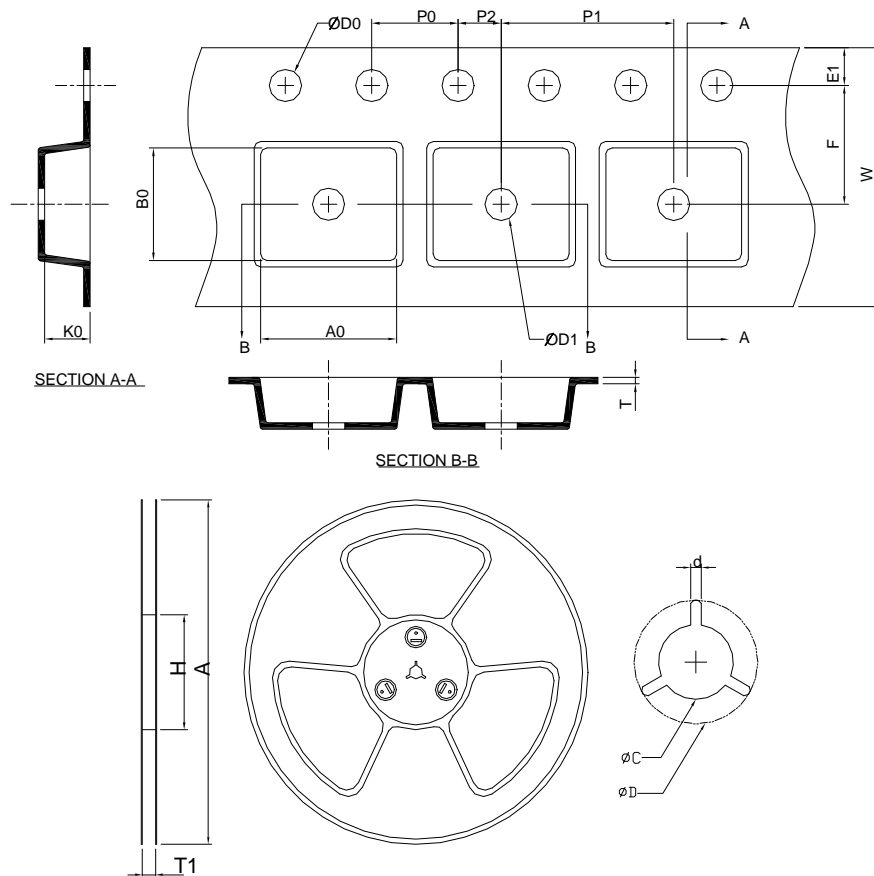**TDFN2x2-6**

SYMBOL	TDFN2x2-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.65 BSC		0.026 BSC	
L	0.30	0.45	0.012	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 WCCC.

Carrier Tape & Reel Dimensions

SECTION A-A

SECTION B-B

Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35 MIN	2.35 MIN	1.30±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500
SOP-8P	Tape & Reel	2500
TDFN2x2-6	Tape & Reel	3000

Taping Direction Information

SOP-8/SOP-8P

USER DIRECTION OF FEED

TDFN2x2-6

USER DIRECTION OF FEED
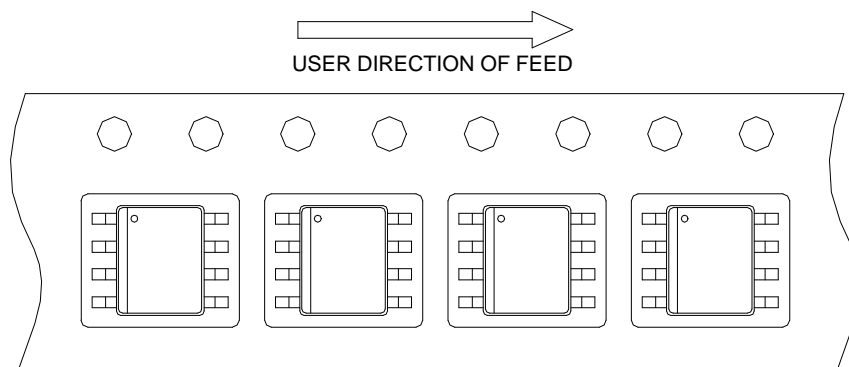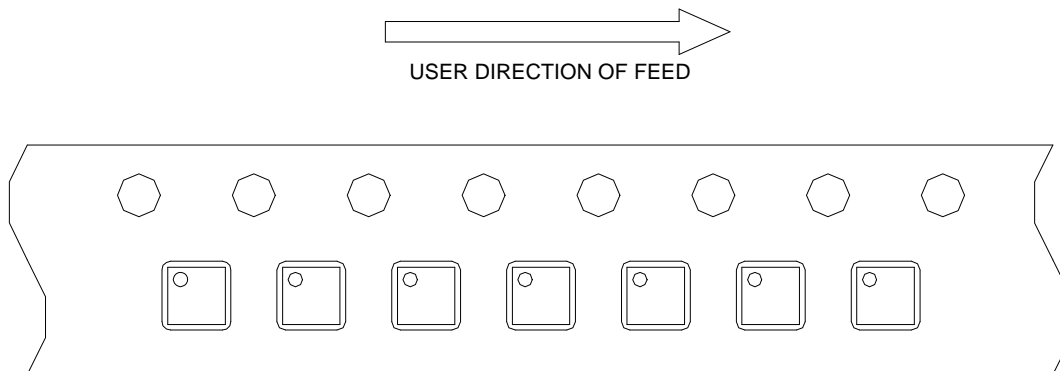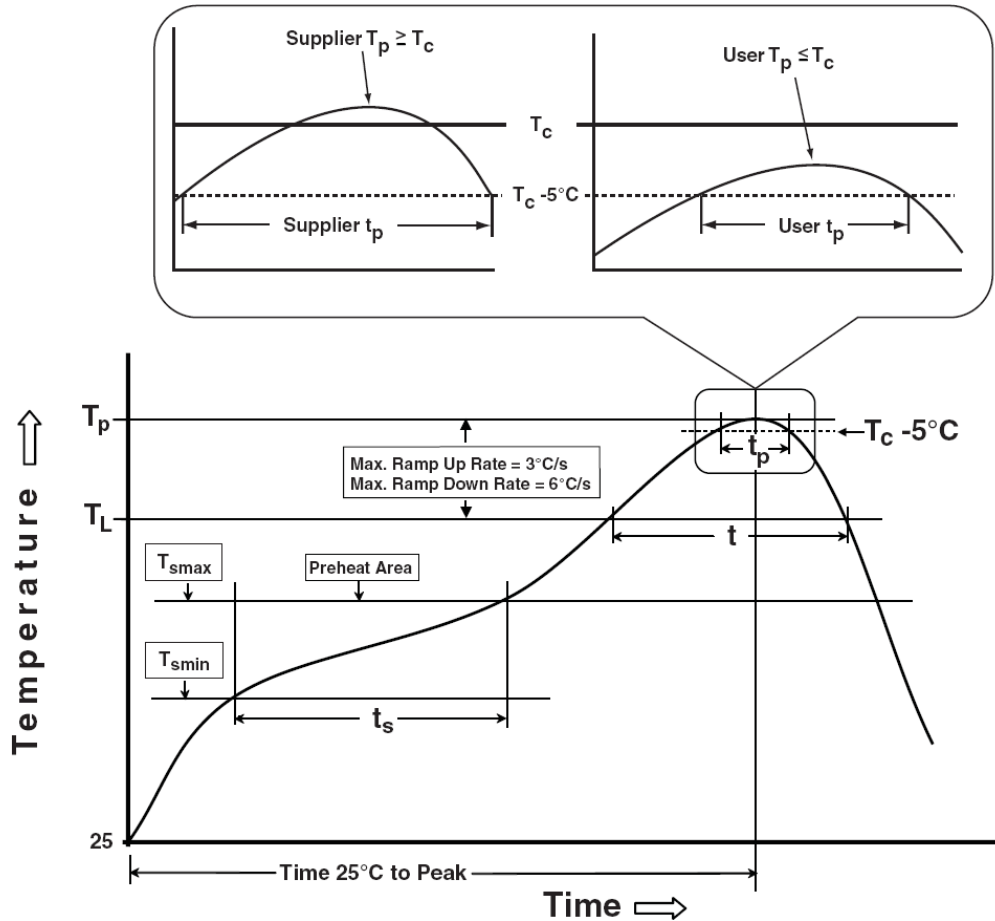
Classification Profile

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1_{tr} 100mA

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