

HIGH SPEED CMOS GATE ARRAYS

■ DESCRIPTION

The S-MOS SLA9000 series is a family of sea-of-gates high speed gate arrays manufactured on S-MOS' state-of-the-art I/O micron double-metal SiCMOS process. The series consists of 11 arrays ranging from 2,917 to 25,058 usable gates and from 86 to 226 I/O. The SLA9000 series has been tailored for high performance designs with typical gate delays of .65 nanoseconds. Additionally, high-speed silicon efficient RAM functions are offered as customized cells. The series has a selectable output drive capability of 2, 6, 12 or 24 milliamps (two output buffers can be used in parallel to obtain 48 milliamps). The arrays are offered in a wide variety of packages including 44–256 pin quad flat packs. The SLA9000 series is supported by S-MOS' own design system with NavNet schematic editor, as well as most major CAD systems including Mentor, Valid, Viewlogic, FutureNet, Synopsys/Verilog and OrCAD.

■ FEATURES

- 1.0 micron drawn channel length (N-channel)
- Very high speed: tpd (2-input power NAND)(typ, FO=2 & 2mm AL) = .65 ns/gate
- High Drive
 - 24mA for a single output
 - 48 mA for parallel outputs
- Low gate-to-pads ratio for high pin count applications
- Megacells compatible
- Fully migratable to S-MOS standard cell families

■ PRODUCT CONFIGURATION

Array	Raw Gates	Usable Range		Total # of Pads
		Min	Max	
SLA904S	4395	2917	3713	86
SLA906S	5990	4048	5152	102
SLA908S	7580	5179	6591	112
SLA909S	9358	6545	8330	126
SLA912S	11978	7885	10035	140
SLA915S	14823	9516	12261	156
SLA919S	18802	11794	15196	172
SLA922S	21956	13172	17124	186
SLA926S	25669	15000	19500	198
SLA929S	29162	17175	22328	212
SLA933S	32645	19275	25058	226

NOTE: All arrays have 4 power / GND pads included within total pad count.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V _{DD}	V _{SS} -0.3 to 7.0	V
Input Voltage	V _{IN}	V _{SS} -0.3 to V _{DD} +0.3	V
Output Voltage	V _{OUT}	V _{SS} -0.3 to V _{DD} +0.3	V
Storage Temperature	T _{STG}	-65 to +150	°C

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	4.50	5.0	5.50	V
Input Voltage	V _{IN}	V _{SS}		V _{DD}	V
Operating Temperature	T _{OPR}	-20		85	°C

■ PERFORMANCE CHARACTERISTICS (Under Recommended Operating Conditions)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IL}	Low level input voltage				1.0	V
	CMOS Level				0.8	V
V _{IH}	High level input voltage		3.5			V
	CMOS Level		2.0			V
V _{T+}	Positive going threshold voltage				4.0	V
	CMOS Schmitt Trigger	V _{DD} = 5.0			3.0	V
V _{T-}	Negative going threshold voltage					V
	CMOS Schmitt Trigger	V _{DD} = 5.0	0.8			V
V _H	Hystereisis voltage					V
	CMOS Schmitt Trigger	V _{DD} = 5.0	0.3			V
I _{IL}	Low level input current	V _{IN} = V _{SS} No pull-up			1.0	μA
	High level input current	V _{IN} = V _{DD} No pull-up			1.0	μA
V _{OL}	Low level output voltage					
	LOT + IN2	I _{OL} = 100μA			V _{SS} +0.4V	V
	Type 1	I _{OL} = 2mA			V _{SS} +0.4V	V
	Type 2	I _{OL} = 6mA			V _{SS} +0.4V	V
	Type 3	I _{OL} = 12mA			V _{SS} +0.4V	V
	Type 4	I _{OL} = 24mA			V _{SS} +0.4V	V
V _{OH}	High level output voltage					
	LOT + IN2	I _{OH} = 100μA	V _{DD} -0.4V			V
	Type 1	I _{OH} = 1mA	V _{DD} -0.4V			V
	Type 2	I _{OH} = 3mA	V _{DD} -0.4V			V
	Type 3	I _{OH} = 6mA	V _{DD} -0.4V			V
	Type 4	I _{OH} = 12mA	V _{DD} -0.4V			V
R _{PU}	Pull up resistor	V _{DD} = 5.0				KΩ
	Type 1		50		500	
	Type 2					
R _{PD}	Pull down resistor	V _{DD} = 5.0				KΩ
	Type 1		50		500	
	Type 2					
I _{oz}	Tri-state leakage current				1.0	μA
C _{IN}	Input Capacitance			4		pF
C _{OUT}	Output Capacitance			6		pF
C _{BID}	Bi-directional pad capacitance			10		pF

■ MACRO LIBRARY

Function	Cell Name	Gates
SIMPLE GATES		
2-INPUT NAND GATE	NA2	1
3-INPUT NAND GATE	NA3	2
4-INPUT NAND GATE	NA4	2
2-INPUT NOR GATE	NO2	1
3-INPUT NOR GATE	NO3	2
4-INPUT NOR GATE	NO4	2
3-INPUT AND GATE	A3	2
6-INPUT AND GATE	A6	4
8-INPUT AND GATE	A8	5
3-INPUT OR GATE	O3	2
6-INPUT OR GATE	O6	4
8-INPUT OR GATE	O8	5
EXCLUSIVE OR GATE	EXO	3
EXCLUSIVE NOR GATE	EXN	3
COMPLEX GATES		
2-AND 2-WIDE 3-INPUT NOR GATE	AN23	2
3-AND 2-WIDE 4-INPUT NOR GATE	AN14	2
2-AND 2-WIDE 4-INPUT NOR GATE	AN24	2
2-AND 3-WIDE 4-INPUT NOR GATE	AN34	2
2-AND 3-WIDE 6-INPUT NOR GATE	AN36	5
2-AND 2-WIDE 3-INPUT OR GATE	AO23	2
3-AND 2-WIDE 6-INPUT OR GATE	AO26	4
4-AND 2-WIDE 8-INPUT OR GATE	AO28	5
2-AND 2-WIDE 3-INPUT NAND GATE	ON23	2
3-AND 2-WIDE 4-INPUT NAND GATE	ON14	2
2-AND 2-WIDE 4-INPUT NAND GATE	ON24	2
2-AND 3-WIDE 4-INPUT NAND GATE	ON34	2
2-AND 2-OR 2-WIDE 4-INPUT NAND GATE	ON44	2
2-OR 3-WIDE 6-INPUT NAND GATE	ON36	5
2-OR 2-WIDE 3-INPUT AND GATE	OA23	2
INVERTERS/BUFFERS		
NORMAL INVERTER	IN1	1
POWER INVERTER	IN2	1
POWER INVERTER	IN4	2
NORMAL BUFFER	BUF1	1
FLIP-FLOPS		
LATCH	LF	4
LATCH WITH RESET	LFR	5
LATCH WITH SET	LFS	5
D-FF	DF	6
D-FF WITH RESET	DFR	7
D-FF WITH SET	DFS	7
D-FF WITH SET AND RESET	DFSR	8
JK-FF WITH RESET	JKR	10
JK-FF WITH SET AND RESET	JKSR	11
ADDERS		
1-BIT FULL ADDER	T183	9
COMPARATORS		
4-BIT MAGNITUDE COMPARATOR WITH ENABLE	T085	39
8-BIT MAGNITUDE COMPARATOR	T688	26
COUNTERS		
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A161	57
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET AND LOAD	T161E	51
SYNCHRONOUS 2-BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A161H	29

■ MACRO LIBRARY (cont.)

Function	Cell Name	Gates
COUNTERS (cont.)		
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET AND ENABLE	A161L	46
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET	A161LE	40
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH LOAD AND ENABLE	A161R	52
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH LOAD	T161RE	46
FULLY SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A163	54
FULLY SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET AND LOAD	A163E	48
RESETABLE R-BIT BINARY UP COUNTER/LATCH WITH RESET AND LOAD	T177	39
PRESETABLE 2-BIT BINARY UP COUNTER/LATCH WITH RESET AND LOAD	T177H	21
PRESETABLE 4-BIT BINARY UP COUNTER/LATCH WITH LOAD	T177R	38
PRESETABLE 4-BIT BINARY UP COUNTER/LATCH WITH SET AND LOAD	T177V	39
PRESETABLE 2-BIT BINARY UP COUNTER/LATCH WITH SET AND LOAD	T177HV	20
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH LOAD AND ENABLE	A191	70
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH RESET	A191CE	47
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH LOAD	A191E	63
SYNCHRONOUS 2-BIT UP/DOWN COUNTER WITH LOAD AND ENABLE	A191H	35
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH RESET	A191LE	51
SYNCHRONOUS 4-BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET AND LOAD	A193	69
SYNCHRONOUS 4-BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET	A193L	53
SYNCHRONOUS 2-BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET AND LOAD	A193L	36
SYNCHRONOUS 2-BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET	A193HL	27
DECADE COUNTER WITH RESET	A390	32
4-BIT BINARY UP COUNTER WITH RESET	T93V	25
4-BIT BINARY DOWN COUNTER WITH RESET	T393V	25
DECODER/DEMULPLEXERS		
BCD-TO-DECIMAL DECODER	T042	29
3-LINE TO 8-LINE DECODE/MULTIPLEXER WITH ENABLE G	A138G2	18
2-LINE TO 4-LINE DECODER/MULTIPLEXER WITH ENABLE G	A139	9
2-LINE TO 4-LINE DECODER/MULTIPLEXER	A139G	6
DFFS/LATCHES		
4-BIT LATCH WITH RESET	T116	17
QUADRUPLE DFF WITH RESET	T175	27
QUADRUPLE DFF WITH Q, XQ WITHOUT RESET	T175R	22
QUADRUPLE DFF WITH Q ONLY	T175RX	22
OCTAL DFF WITH RESET	T175W	54
OCTAL OFF	T175WR	44
OCTAL D-TYPE TRANSPARENT LATCH WITH ENABLE	T373T	26
SELECTORS/MULTIPLEXERS		
4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T153	12
4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER	T153G	10
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T157WG	13
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER	T157G	11
OCTAL 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T157W	25
OCTAL 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER	T157WG	21
SHIFT REGISTERS		
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER WITH RESET	T164	55
8-BIT SHIFT REGISTER WITH RESET, LOAD AND ENABLE	T166	65
4-BIT SHIFT REGISTER WITH RESET, LOAD AND ENABLE	T166H	34

■ INTERNAL TRISTATES

S-MOS supports the use of internal tristate busses with the following macro library:

Name	Function	Gates	Name	Function	Gates
TSV	Tristate Inverting Buffer	5	T244H	Quad Tristate Buffer	13
TSB	Tristate Buffer	4	T373	Octal Latch With Tristates	50
T240	Octal Inverting Tristate Buffer	30	T373H	Quad Latch With Tristates	25
T240H	Quad Inverting Tristate Buffer	15	T374	Octal DFF With Tristates	72
T244	Octal Tristate Buffer	26	T374H	Quad DFF With Tristates	36

NOTE: In order to ensure design quality, S-MOS Systems requires the use of certain design practices when using internal tristate cells. Please consult S-MOS Systems for more information.

■ PACKAGE MATRIX

Package Type	No. of Pins		Device code		904S	906S	908S	909S	912S	915S	919S	922S	926S	929S	933S
	No. of Pins		No. of Pads		86	102	112	126	140	156	172	186	198	212	226
	No. of Pins		Gross Gates		4395	5990	7580	9353	11978	14823	18802	21956	25669	29162	32645
	No. of Pins		D E												
Plastic DIP	28		S28		A	A									
Plastic Shrink DIP	64		S64				A								
Plastic QFP	44		QFP-4		Q										
	44		QFP-6		A	A	A		A	A	A				
	48		QFP-12		A										
	60		QFP-5		A	Q	Q	Q	Q		Q				
	60		QFP-6		A	A	A	A	A	A					
	64		QFP-5		A*	Q	Q	Q	Q						
	64		QFP-6		A*	A	A	A	A	L					
	64		QFP-13		A	A	A	A	A						
	80		QFP-5		A	A*	A*	A*	A*	A*	A*	A*	A*	LQ	
	80		QFP-14			A	A	A	A	A	A	A			
	100		QFP-5		A*	A*	A*	A*	A*	A*	A*	A*	A*	LQ	
	100		QFP-15			A	A	A	A	A	A	A	A		
	120		QFP-8		L	A	A*	A*	A*	A*	A*	A*	A*	L	A
	128		QFP-5		L	A	A	A	A	A	A	A	LQ		
	128		QFP-8			L	A	A	A*	A*	A*	A*	A*	A*	A*
	144		QFP-8				L	A	A*	A*	A*	A*	A*	A*	A*
	144		QFP-17					L	A		A		Q		LQ
	160		QFP-8						A	A	A*	A*	A*	A*	A*
	184		QFP-16									Q	Q	Q	Q
	196		QFP-9												
	208		QFP-8								A	A	A	A	A
	256		QFP-9												
Plastic SOP	28		SOP2		A	A	A								
PLCC	44		J44		Q				Q	Q	Q				
	68		J68		A	A*	A		A	A					
	84		J84		L	A*	A*	A*	A*	A*	A*	A*	A*	Q	Q

A: Available

*: Pin-Pad table exist

L: Need Lead frame development (2.5 months for new lead frame development)

Q: Need Qualification (reliability test) (2.5 months for reliability test)

LQ: Need Lead frame and Qualification (reliability test)(2.5 months for new lead frame development and/or 2.5 months for reliability test)

■ PROCESS TECHNOLOGY

The SLA9000 Series is fabricated on our highly automated 6" fabrication line located in Fujimi, Japan. The process is similar to that used for high-volume 1 Meg SRAM which has been in production since 1988.

N-Channel is 1.0 micron drawn (0.8 micron effective) and P-Channel length is 1.2 micron drawn (1.0 micron effective).

■ PROPAGATION DELAY TIMES

The propagation delay values printed in our cell libraries and used in simulation are derived from actual measurements of silicon, not spice simulations. The measured coefficient parameters are:

● Delay Multiplier

	5%	10%
Min	0.60	0.50
Max	1.75	1.95

5% Factor

Voltage: 4.75 to 5.25 volts

Temperature = 0 to 70°C

10% Factor

Voltage: 4.50 to 5.50 Volts

Temperature = -20 to 85°C

Name	Function	From	To	Best Case		Worst Case		Loads
				tph (ns)	tphl (ns)	tph (ns)	tphl (ns)	
NA2	2-INPUT NAND	IN	OUT	.1	.1	0.4	0.4	0
				.17	.19	.63	.68	1
				.24	.28	.86	.96	2
NO2	2-INPUT NOR	IN	OUT	.2	.1	.7	0.4	0
				.32	.16	1.07	.6	1
				.44	.22	1.44	.8	2
IN1	1 x INVERTER	IN	OUT	.1	.1	0.4	.4	0
				.17	.16	.63	.6	1
				.24	.22	.86	.8	2
IN4	4 x INVERTER	IN	OUT	0.1	0.1	.2	.2	0
				.12	.12	.29	.27	1
				.14	.14	.38	.34	2
DF	D FLIP-FLOP	CLK	Q	1.1	1.1	3.5	3.7	0
				1.17	1.26	3.73	3.9	1
				1.24	1.32	3.96	4.1	2
IBT	TTL LEVEL INPUT BUFFER	IN	OUT	.5	.9	1.6	2.8	0
				.52	.92	1.69	2.87	1
				.54	.94	1.78	2.94	2
UO1	2mA OUTPUT DRIVER	IN	PAD	1.33	2.78	4.18	8.38	10pF
				2.65	6.3	8.1	18.7	50pF
				4.3	10.7	13.0	31.6	100pF
UO2	6mA OUTPUT DRIVER	IN	PAD	.68	.91	2.15	2.93	10pF
				1.4	2.15	4.35	6.65	50pF
				2.3	3.7	7.1	11.3	100pF

BEST CASE	WORST CASE
Temperature = 0°C Ambient	Temperature = 70°C Ambient
Supply Voltage = 5.25V	Supply Voltage = 4.75V
Process = Best case	Process = Worst Case

● **Workstation Support**

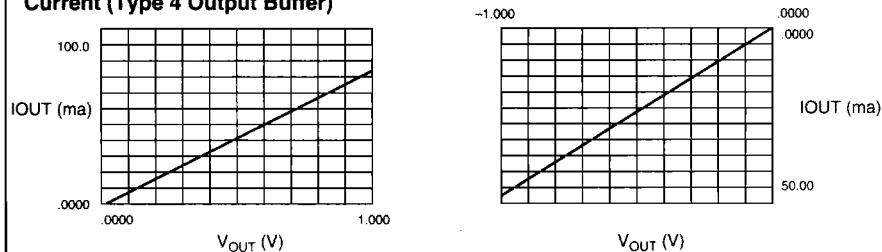
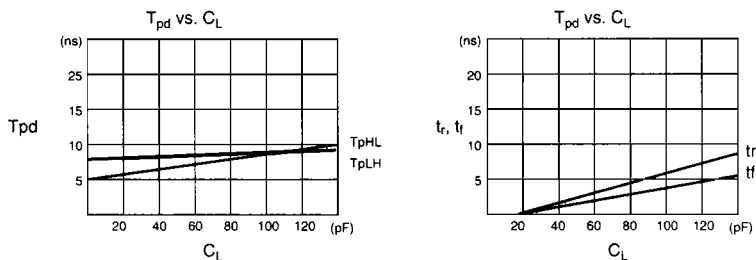
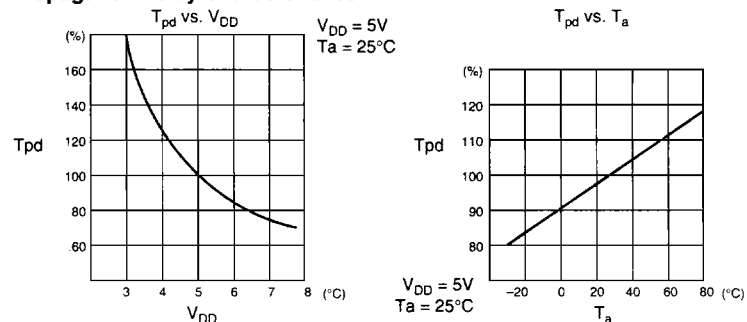
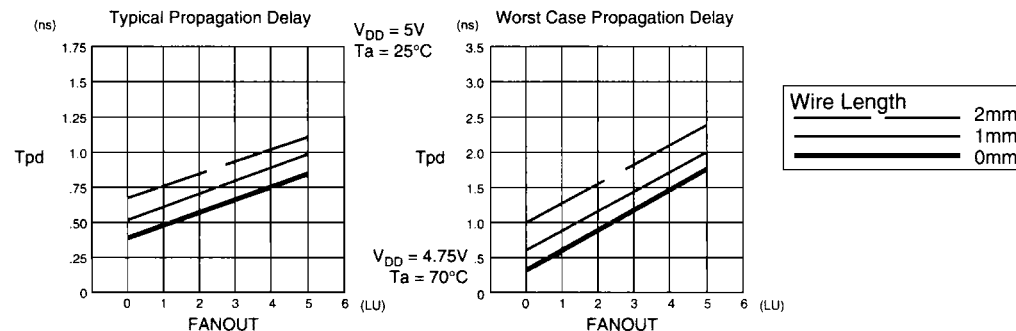
Schematic capture, electrical rule checking, design rule checking, simulation and timing verification are supported on Daisy, Mentor, Valid, NavNet and Intergraph workstations. In addition, our proprietary LADS software, used with NavNet and Intergraph workstations. In addition, our proprietary LADS software, used with NavNet, ViewLogic, OrCad or FutureNet, is available for IBM PC's and compatibles. LADS is also available on Sun and Apollo platforms.

LADS includes ERC, DRC, logic simulation and timing verification up to 6,000 gates using PCs with 640K of memory or up to 20,000 gates in PCs equipped with 4 megabytes of extended memory.

● **Megacells**

Due to the design of the SLA9000 Series, fully routed and characterized megacells be implemented effectively alongside of random logic. Available:

B8259	B82288
B8237	B146818
B82284	B8250
B8255	B8251
B16C550	B8254
	B-80

Current (Type 4 Output Buffer)**Type 2 Output Buffer Delay Characteristics****Propagation Delay Characteristics****Propagation Delay Including Interconnect**

■ S-MOS Systems ASIC Design Flow

