Product Information

High Voltage SLA6860M and SMA6860M Series Driver ICs for 3-Phase DC Motor Applications

Introduction

The SLA6860M and SMA6860M Series consists of inverter power module (IPM) devices that integrate within a single, compact package: power MOSFETs, pre-driver ICs, and fast recovery diodes. These products are especially suitable for driving the inverters of low-capacity motors, such as those used in 100 to 200 V fans or pumps for air conditioners.

Features and benefits include the following:

- Three built-in bootstrap fast recovery diodes (FRD), each with current-limiting resistor, and capable of withstanding high voltages: 600 V at 1 A
- Overcurrent limiting (OCL) function, with fault signal output and shutdown input terminal; when the user-determined maximum current level is exceeded, PWM on-off cycling is initiated to effectively limit current
- Built-in overcurrent protection (OCP) function; when an overcurrent condition, such as an output short circuit, is detected, the internal high-side and low-side logic ICs shut down the output driver gates and issue a fault signal
- Optional automatic shutdown of high-side and low-side gates if an abnormal condition occurs (overtemperature, overcurrent, undervoltage on control power supply, and so forth); enabled by connecting together the SD1 and SD2 terminals
- Built-in overtemperature protection for both high-side and low-side circuits; thermal shutdown (TSD) occurs when the temperature of the logic chips exceed a user-determined value, the internal high-side and low-side logic ICs shut down the output driver gates and issue a fault signal

Figure 1. SMA6860M Series packages are SIPs, offering compact configurations both with heatsink pad (leadforms 2171 and 2175) and without (leadforms 2451 and 2452). Both horizontal mount and vertical mount are available.

- Built-in undervoltage lockout (UVLO) protection for each control power supply, VCC1, VCC2, and VBx; when voltage falls below a set value, the gates are shut down and VCC1 and VCC2 output an alarm signal
- Alarm signal (shutdown) output when protection circuits enable; high-side faults (UVLO and TSD) are signaled on the SD1 terminal, low-side faults (TSD, OCP, and UVLO) are signaled on the SD2 terminal

Product Lineup*

Type	MOSFET Rating	Application	Input Voltage (VAC)	Heat-sink
SMA6861M	250 V / 2 A	FAN Motor, Pump	230	–
SMA6862M	500 V / 1.5 A	FAN Motor, Pump	230	–
SMA6863M	500 V / 2.5 A	FAN Motor, Pump	230	–
SLA6866M	250 V / 2 A	FAN Motor, Pump	230	Yes
SLA6867M	500 V / 1.5 A	FAN Motor, Pump	230	Yes
SLA6868M	500 V / 2.5 A	FAN Motor, Pump	230	Yes

*SMA6861M : SLA6866M, SMA6862M : SLA6867M, and also SMA6863M : SLA6868M are electrically identical respectively.

Contents

- Power MOSFETs incorporating fast recovery diodes (FRD) provide low losses in comparison with IGBT technology
- Use of SIP 24-pin power package, proven in other high-volume Sanken product lines, with L-bend and zigzag leadforms available; L-bends formed with precautions to ensure device integrity; zigzags for stable mounting; heatsink tab option

Functional Description

The functional block diagram for one of the three device phases is shown in figure 2. High voltage power and 15 VDC are input between VBB and LS1/LS2, between VCC1 and COM1, and between VCC2 and COM2. The on/off signals of the power MOSFETs are operated by six signals: HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3. These input signals are positive logic (the MOSFET turns on at V_{xINx} = high). The boot capacitors are connected between VB1 and U, VB2 and V, and VB3 and W1, as the high voltage power source.

The protection functions, including overcurrent protection (enable at detected short circuit, and so forth), overtemperature protection (at abnormal ambient temperature, overload, and so forth), and undervoltage of low control power supply voltage (at instantaneous fall, and so forth) are built-in and when any of these functions is operated, it can be monitored at the corresponding output terminal.

The current limiter (OCL) signal is provided as a control signal, and when the current flowing across the shunt resistor exceeds the typical limit value, the OCL terminal turns on. Current limiting can be enabled by connecting this signal to the SD1 terminal (for high-side limiting) or to the SD2 terminal (for low-side limiting).

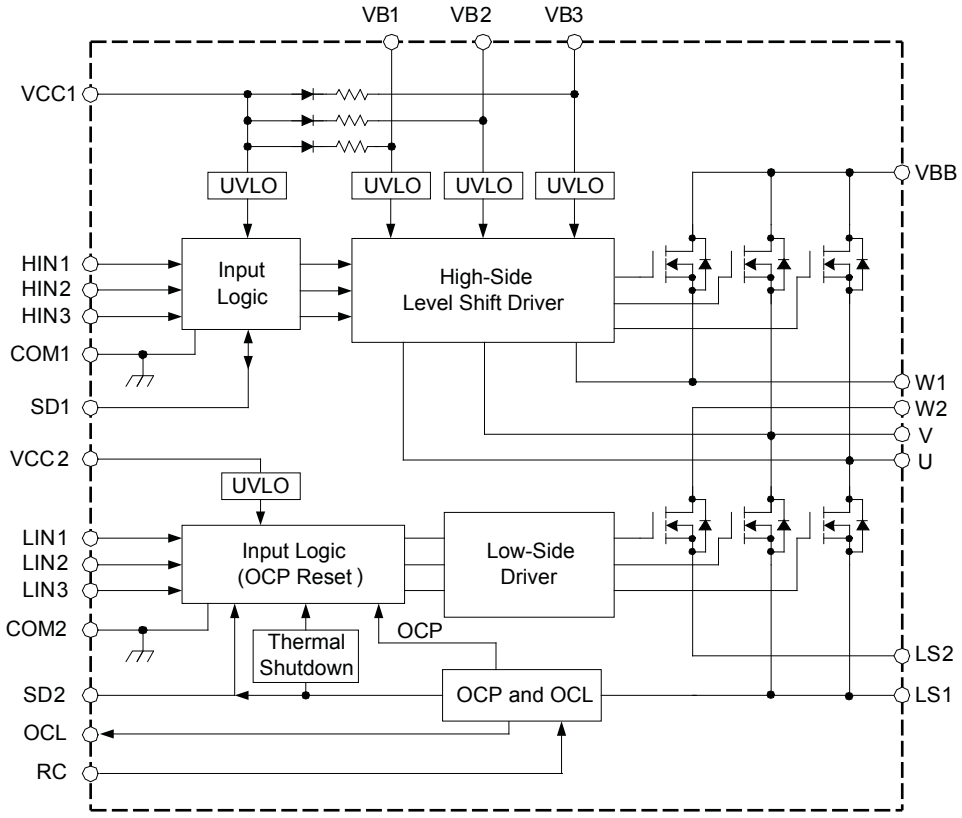


Figure 2. SLA6860M/SMA6860M Series Phase Block Diagram. These devices support high-side and low-side three-phase MOSFET output drivers.

Terminal Descriptions

A summary description of the function of the various terminals is given in the Terminal List table. Pin 1 for each package appears in figure 3. This section provides detailed functional descriptions of the individual pins.

VBB This is the terminal for the main power supply. For supplying the SMA6861M, V_{BB} should be 200 VDC or lower and in other products, 400 VDC or lower. To suppress surge voltage, a snubber capacitor (0. 01 to 0.1 µF) and an electrolytic capacitor should be connected to the device by traces having the shortest length practicable. If the trace lengths are long, surge voltages will be increased. It should be verified that surge voltage does not exceed the breakdown voltage of the MOSFETs internal to the device itself.

U, V, W1, and W2 These are the output terminals connected to the motor. W1 and W2 should be connected together externally, and are used in short circuit events.

LS1 and LS2 These are the source terminals for the low-side power MOSFETs. LS1 and LS2 should be connected together externally. When a shunt resistor is connected to this terminal, the lengths of the traces should be as short as practicable. If the trace lengths are long, malfunctions due to noise are likely to occur.

VCC1 and VCC2 These are the power supply terminals of the built-in pre-driver ICs. VCC1 and VCC2 should be should be connected together externally. In order to prevent malfunctions due to noise on the power supply lines, a ceramic bypass capacitor (0.01 to 0.1 µF) should be mounted near the terminals.

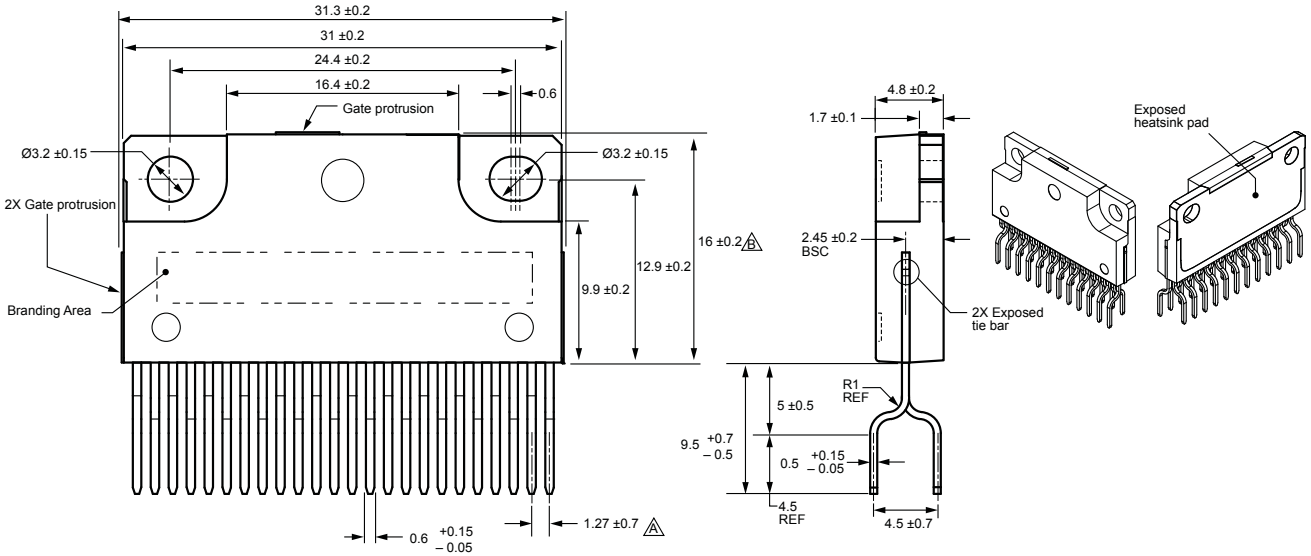
Note: If V_{CCx} exceeds 20 V, permanent damage may occur. It is recommended to add a Zener diode (V_Z = 18 to 20 V) to protect against such surge voltages.

The control power supply undervoltage protection circuit is integrated with VCC1 and VCC2. The supplied voltage should not be allowed to drop below the rated threshold voltage of VCC1 and VCC2.

Terminal List Table

Number	Name	Function
1	VB1	High side bootstrap terminal (U phase)
2	VB2	High side bootstrap terminal (V phase)
3	VB3	High side bootstrap terminal (W phase)
4	VCC1	High side logic supply voltage
5	SD1	High side shutdown input and UVLO fault signal output
6	COM1	High side logic GND terminal
7	HIN3	High side input terminal (W phase)
8	HIN2	High side input terminal (V phase)
9	HIN1	High side input terminal (U phase)
10	VBB	Main supply voltage
11	W1	Output of W phase (connect to W2 externally)
12	V	Output of V phase
13	W2	Output of W phase (connect to W1 externally)
14	LS2	Low side emitter terminal (connect to LS1 externally)
15	RC	Overcurrent protection hold time adjustment input terminal
16	LS1	Low side emitter terminal (connect to LS2 externally)
17	OCL	Output for overcurrent limiting
18	LIN3	Low side input terminal (W phase)
19	LIN2	Low side input terminal (V phase)
20	LIN1	Low side input terminal (U phase)
21	COM2	Low side GND terminal
22	SD2	Low side shutdown input and overtemperature, overcurrent, and UVLO fault signals output
23	VCC2	Low side logic supply voltage
24	U	Output of U phase

(A)



(B)

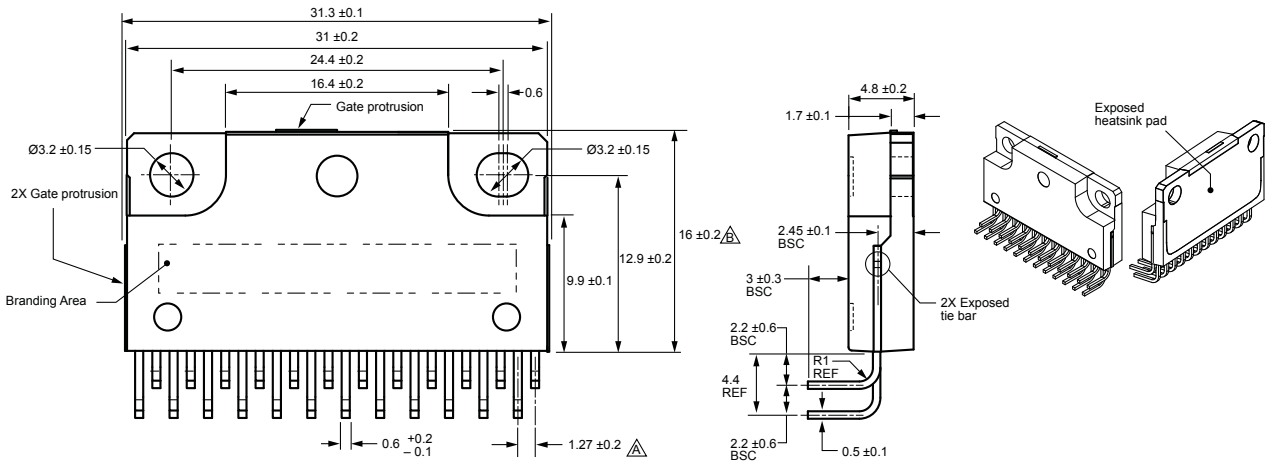
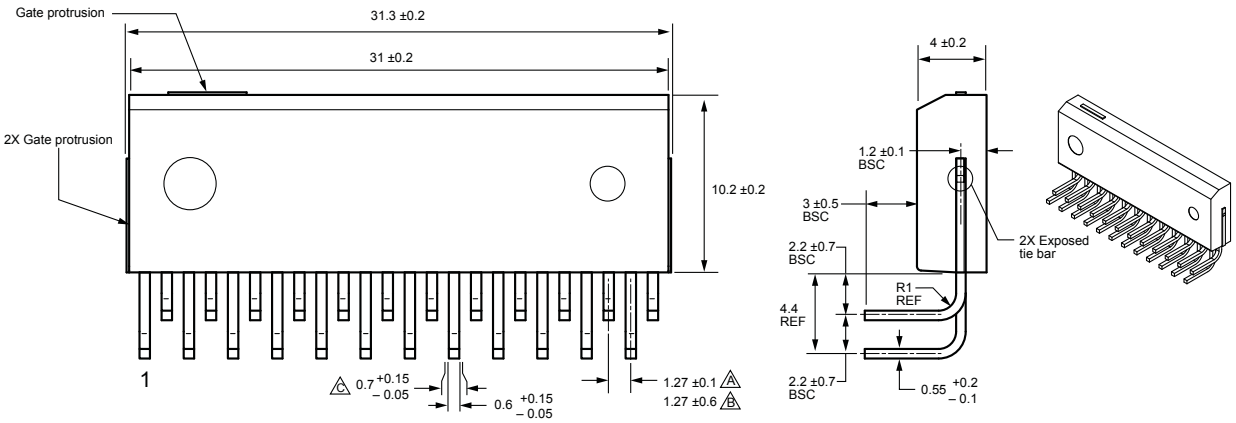


Figure 3(A) and (B). Package Outline Drawings. (A) LF2171 vertical mount, (B) LF2175 horizontal mount, with heatsink pads.

(C)



(D)

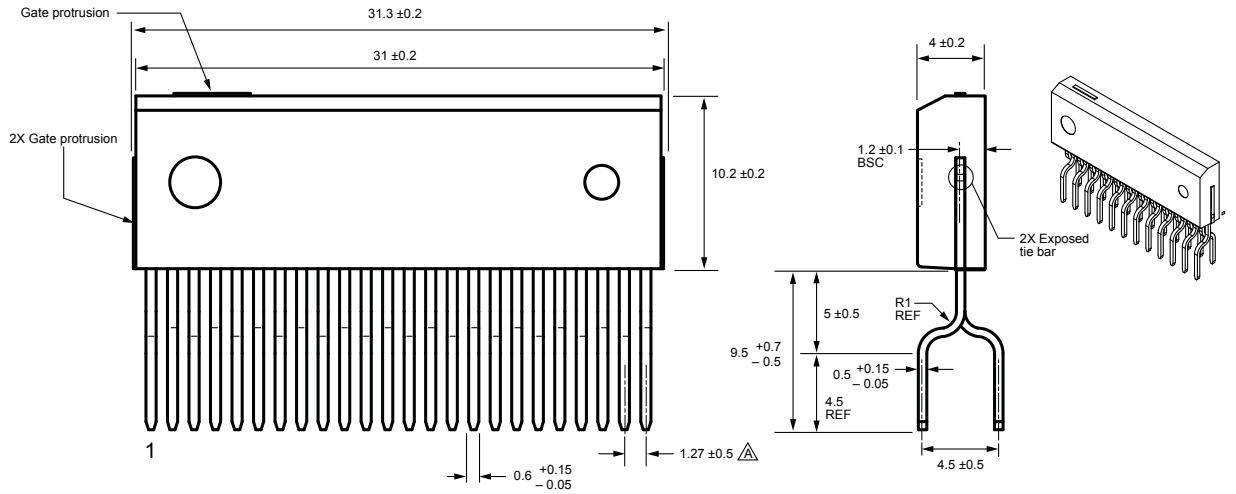


Figure 3 (C) and (D). Package Outline Drawings. (C) LF2451, L-bend horizontal mount and (D) LF2452, vertical mount; no heatsink pads.

COM1 and COM2 These are the ground terminals of the built-in logic control ICs. COM1 and COM2 should be connected together externally.

Because malfunctions are likely to be caused by variations in the potential at these terminals, attention should be paid to the external connections for these terminals. Connections should be made such that there are no appreciable variations in potential, such as due to fluctuations in power current levels, short wiring length, or other causes.

VB1, VB2, and VB3 These are the power supply terminals for driving the high-side MOSFETs. As shown in figure 4, three bootstrap capacitors, CBOOTx, should be connected, with one each between VB1 and U, VB2 and V, and VB3 and Wx. Because these bootstrap circuits perform independent operations, a capacitor is required for each phase. At start-up, the CBOOTx capacitors should be charged. CBOOTx should be sufficiently charged by turning on the low-side MOSFET at the beginning.

One 210 Ω series resistor and one 600 V/ 1 A bootstrap diode are built in inside the device. To determine the constants for the bootstrap circuit, the following factors should be taken into account:

- What constitutes the optimal capacitance value of the bootstrap capacitor is dependent on: the driving method (modulation method and output frequency), the switching frequency (carrier frequency), the modulation rate (duty cycle), and the gate input capacitance of the MOSFETs.
- Consider the time interval, t_{OFF}, when the low-side MOSFETs are not on (except when the FRD conducts); the longer t_{OFF} becomes, the further the capacitor voltage falls; therefore, the larger the capacity required.
- In the case of 2-phase modulation or a 120° conduction system, the time interval when the MOSFETs are on becomes longer.
- The relationship between t_{OFF} and the recommended capacitance of a CBOOT capacitor is shown by the following formula (given $\Delta V \leq 0.5$ V):

$$C_{BOOTx}\ (\mu F) \geq t_{OFF}\ (ms) \quad .$$

  The validity of the result yielded by this formula should be verified using the actual product.
- The control power supply undervoltage protection circuit is integrated with VB1, VB2, and VB3. The supplied voltage should not be allowed to drop below the rated threshold voltage of these terminals.

HINx and LINx These are the command signal inputs for directing power to the MOSFETs. A pull-down resistor (20 kΩ) is built-in for these active high inputs, and the command signals are received at the Schmidt trigger circuit for the input logic (see figure 5).

The input voltage is 7 V maximum; if a higher voltage is input, the circuit may be permanently damaged. Adding a series resistor

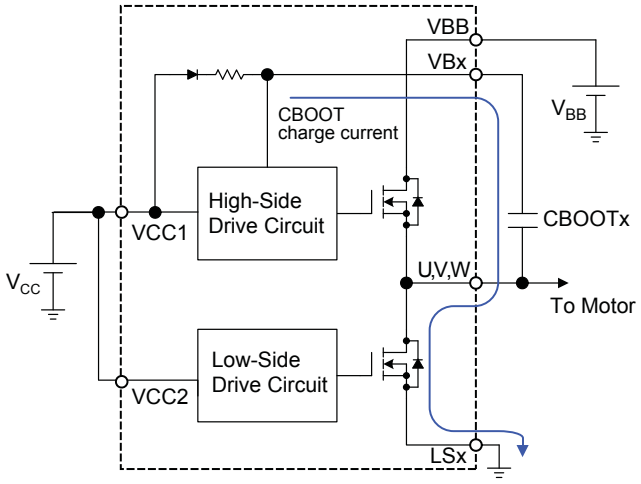


Figure 4. Connection of Bootstrap Capacitor. There is a separate CBOOT capacitor for each of the three phases.

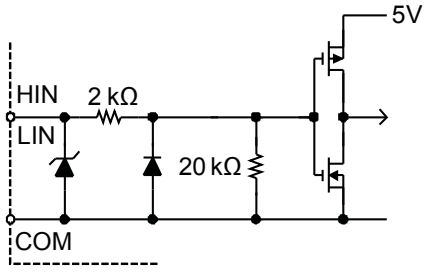


Figure 5. HINx and LINx Terminals Internal Equivalent Circuit

(100 Ω to 1 kΩ) between the external system microprocessor and this device should be considered. Also, a ceramic capacitor (100 to 1000 pF) and a Zener diode (V_Z = 5. 6 to 6. 2 V) between the xINx terminals and the corresponding COMx terminal should be considered.

RC When the current that is flowing across the shunt resistor is excessive and the voltage of the LS terminal exceeds 1 V typical, for 2 µs or longer, the device evaluates this as an overcurrent condition and initiates the overcurrent protection (OCP) function. OCP operates as follows:

1. Short-circuit the SD2 terminal (open collector).

2. Turn off the low-side power MOSFETs completely.

3. Short-circuit the RC terminal.

When the power MOSFETs are turned off, although the voltage falls below 1 V, the gate-off operation and the short-circuiting of the SD2 terminal continue for a fixed period. This period is set by an external pull-up resistor RR and capacitor CC, connected to this terminal as shown in figure 6. The relationship between the constants of RR, CC and the duration of OCP operation, t_{OCP}, is given in the following formula (given a pull-up voltage of 5 V):

$$t_{OCP}\,(\mu s) = 1.2 \times R_R\,(k\Omega) \times C_C\,(nF)\ .$$

The application should be designed for values of R_R between 33 and 390 kΩ, and C_C between 1 and 4.7 nF. In case where R_R = 360 kΩ and C_C = 4.7 nF, t_{OCP} would be approximately 2 ms.

If the pull-up resistor RR becomes disconnected (open) from the RC terminal, the OCP function will not be released.

When RR is short-circuited, the OPC function does not operate. In case of disconnection of the capacitor CC, the duration of OCP becomes short, to release protection operation immediately.

SD2 This is the terminal for fault signal output at abnormal operation, and also a shutdown command input terminal. During OCP, low-side drive circuit IC overtemperature protection, or control power supply undervoltage protection between VCC2 and COM2, the transistor of the open collector circuit is turned on (see figure 7).

Because the SD2 terminal also plays the role of shutdown command input terminal, when it is externally short-circuited between SD2 and COM2, the low-side MOSFETs are turned off completely.

A filter (3.3 µs typical) is integrated into the device, for the prevention of malfunction due to noise. A pull-up resistor, R2, with a value of 3.3 to 10 kΩ, should be externally connected, even if the SD2 terminal is not used. In addition, a capacitor, C2, of 0.01 µF or less should be connected for eliminating noise.

SD1 This is the terminal for fault signal output for high-side drive circuit IC overtemperature protection, and also a shutdown command input terminal. The transistor of the open collector circuit is turned on at the operation of overtemperature protection (see figure 8).

Because the SD1 terminal also plays the role of shutdown command input terminal, when it is externally short-circuited between SD1 and COM1, the high-side MOSFETs are turned off completely. Furthermore, after a short-circuit between SD1 and

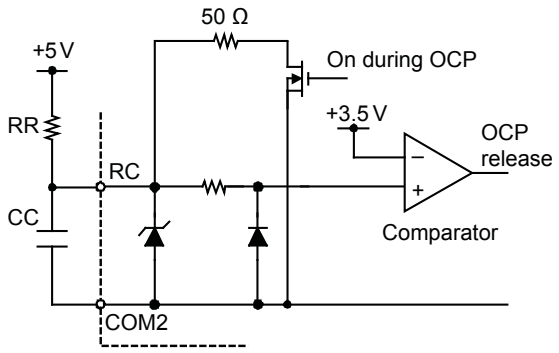


Figure 6. RC Terminal Internal Equivalent Circuit

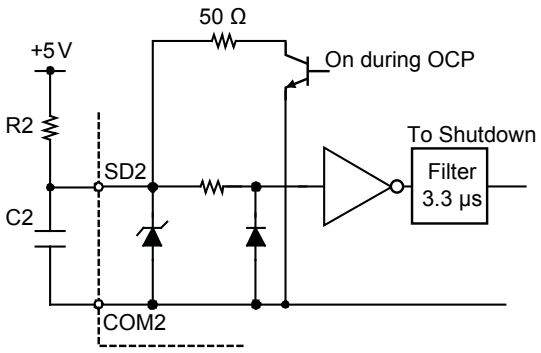


Figure 7. SD2 Terminal Internal Equivalent Circuit

COM1 is removed, the MOSFETs begin again to turn on at the rising edge of the HIN terminal signal.

A filter (3.3 µs typical) is integrated into the device, for the prevention of malfunction due to noise. A pull-up resistor, R1, with a value of 3.3 to 10 kΩ, should be externally connected, even if the SD1 terminal is not used. In addition, a capacitor, C1, of 0.01 µF or less should be connected for eliminating noise.

OCL This is the output terminal of current limiter signal. The internal circuit composition is shown in figure 9.

When the LS1 terminal voltage continuously exceeds 0.53 V typical for 2 µs or longer, the transistor of the open collector circuit connected to the OCL terminal is turned on.

In the case where the OCL signal is connected to the SD1 terminal and the SD2 terminal, each one of those connections should have RL and Cf connected as shown in figure 10. RL and Cf should be placed near the SDx terminal, which is an input terminal.

The recommended constant ranges of RL and Cf are:

$$R_L = 1 \text{ to } 10 \text{ k}\Omega$$

$$C_f = 0.001 \text{ to } 0.01 \text{ µF}$$

When the current limiter function is not used, the OCL terminal should be left floating.

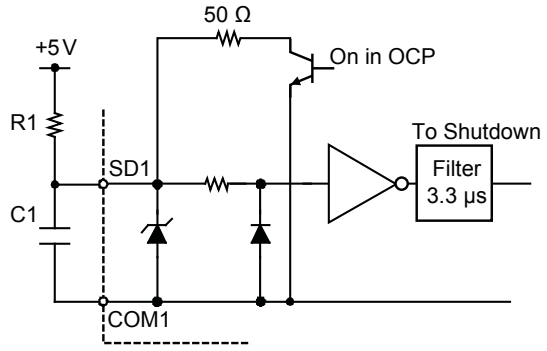


Figure 8. SD1 Terminal Internal Equivalent Circuit

Protection Functions

This section describes in detail the various device protection features provided with the SLA6860M and SMA6860M.

Undervoltage Lockout (UVLO) on Control Power Supply

When the gate-driving voltages on the output MOSFETs become too low, the losses of the power MOSFETs increase, and in the worst case the circuits may be damaged. In order to prevent this, undervoltage protection circuits are built into the control power supply.

The high-side driver IC monitors the voltage between VCC1 and COM1, the voltage between VB1 and U, VB2 and V, and VB3 and W1. As shown in the timing chart (figure 11), when the VBx voltage exceeds the UVHH voltage (10.5 V typical), that enables the HO output (gate of MOSFET) pulses on each subsequent HINx rising edge (edge operation). When the VBx voltage is below the UVHL value (10 V typical), the high-side MOSFETs are shut down.

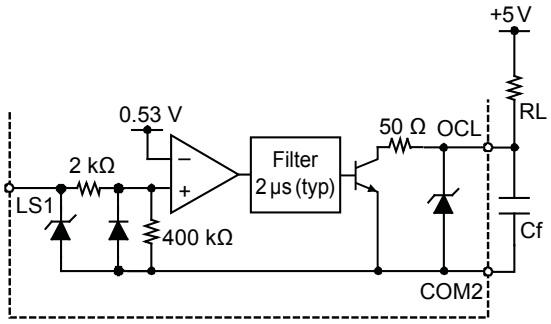


Figure 9. OCL Terminal Internal Circuit

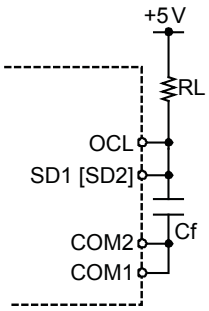


Figure 10. OCL Function Terminal Connections

When the output of the power MOSFETs is shut down by UVLO operation due to falling boot voltage, the transistor on the open collector SD1 terminal does not turn on. At UVLO operation due to VCC voltage fall, however, the SD1 terminal does turn on.

The high-side UVLO detection circuit and the internal equivalent circuit are shown in figure 12. As shown there, a filter is inserted to prevent line noise from affecting the control power supply voltage.

When the voltage between VCC1 and COM1 falls below the UVLL voltage of 11 V typical, the high-side MOSFETs are shut down. When the power supply voltage rises above the UVLH voltage level of 11.5 V typical, that enables the HO output (gate of MOSFET) pulses on each subsequent HINx rising edge (referred to as edge operation).

The low-side driver IC monitors the voltage between VCC2 and COM2. As shown in the low-side timing diagram (figure 13), when the voltage between VCC2 and COM2 falls below the UVLL voltage of 11 V typical, the low-side MOSFETs are shut down and the transistor of the open collector circuit connected to the SD2 terminal is turned on.

When the VCC2 voltage rises above the UVLH voltage of 11.5 V typical, the shutdown of the low-side MOSFETs is released and the transistor of the SD2 terminal is turned off, allowing the device to operate in accordance with the command signal input on the LINx pins (steady state operation).

As shown in figure 14, a filter is inserted to prevent line noise from affecting the control power supply voltage, as in the high-side UVLO circuits, described above. The filter protects against the sharp fall of V_{Bx}, V_{CC1}, and V_{CC2}. However, in case of: over-voltage, filter time constants being exceeded, or only V_{CC1} falling while V_{Bx} voltage is sustained, malfunction or damage to the device might be caused. To protect against these faults, a ceramic capacitor (0.01 to 0.1 µF) and a Zener diode (V_Z = 18 to 22 V) should be provided near the power supply terminal.

Table 1. Overtemperature Protection Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Units
TSD Enable	T_{DH}	120	135	150	°C
TSD Release	T_{DL}	100	115	130	°C
TSD Hysteresis	Hys	–	20	–	°C

Overtemperature Protection (TSD) A thermal shut-down (TSD) protection circuit is built in for the SLA6860M-SMA6860M Series. In the event of overheating, such as due to increased power consumption or an increase in the ambient temperature at the device, the power MOSFETs are shut down. The determination of a overtemperature condition is made by the driver circuit ICs on the high side and low side, in accordance with table 1. When the operating temperature rises above 135° typical, thermal shutdown enables. When the temperature subsequently falls below 115°, thermal shutdown is released, and the device can continue operation again in accordance with the xINx signals.

Temperature monitoring occurs both on the high side and the low side. When TSD operates on the high side, those MOSFETs are turned off, and transistor of the open collector circuit to the SD1 terminal is turned on.

Note: Because the temperatures of the power MOSFETs themselves are not monitored for overtemperature condition, the internal protection function on its own may not be sufficient to prevent damage to the device due to overheating. It also should be noted that in a case where the temperature of the MOSFETs rise very rapidly, the overtemperature detection may lag.

Overcurrent Protection (OCP) The SLA6860M-SMA6860M Series has a built-in overcurrent protection circuit. If the voltage between LS1 and COM2 (1.0 V or higher) continues for longer than the blanking time, t_{BLANK} (2 µs typical), then overcurrent protection starts operation (see figure 15).

At the start of OCP operation, the transistor connected to the SD2 terminal (through a 50 Ω resistor) turns on, and simultaneously the MOSFET connected to the RC terminal (through a 50 Ω resistor) turns on (see figure 16).

The voltages of the SD2 terminal and the RC terminal fall in accordance with the time constants determined by external capacitors C2 and CC. When the SD2 terminal voltage falls below V_{th} (2. 1 V), a shutdown operation is performed on the MOSFET gate. With the gate shut down, current decreases. As the voltage falls below the V_{TRIP} level, the MOSFET connected to the RC terminal turns off, in 5 µs, and the RC terminal voltage rises with the time constant determined by RR and CC.

When the RC terminal voltage rises to 3.5 V, the OCP reset operation starts, releasing the gate shutdown of the MOSFETs and turning off the transistor on the SD2 terminal, allowing the device to operate in accordance with the command signal input on the LINx pins (steady state operation).

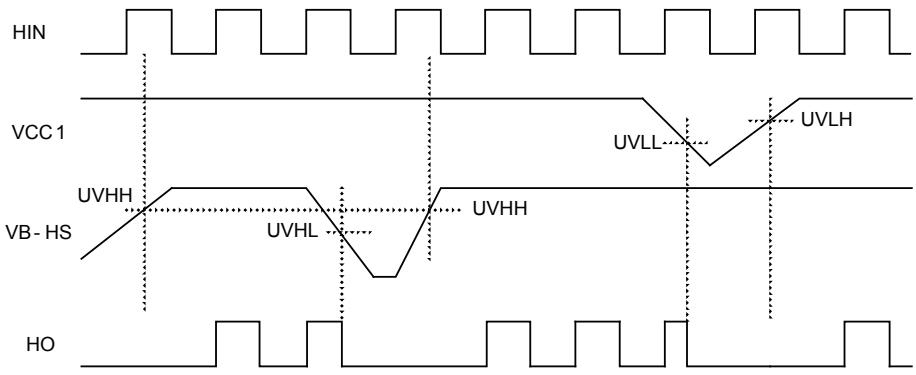


Figure 11. High-Side MOSFET Output Timing

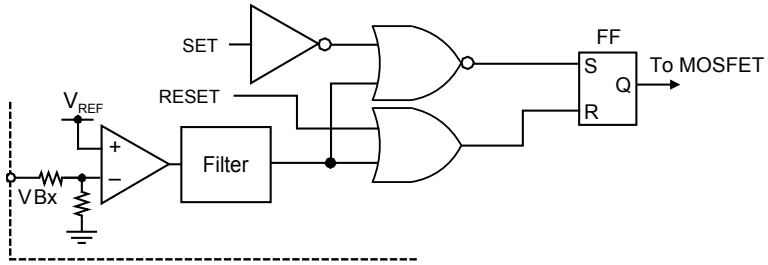


Figure 12. High-Side VCC1 UVLO Internal Equivalent Circuit

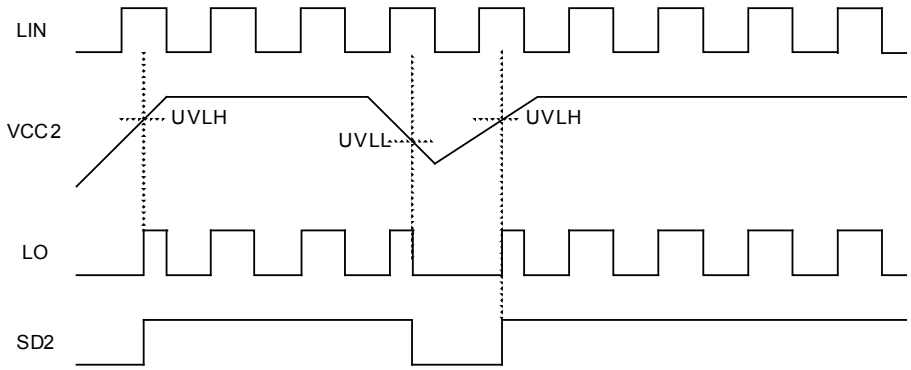


Figure 13. Low-Side MOSFET Output Timing

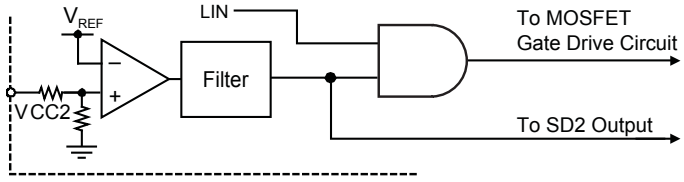
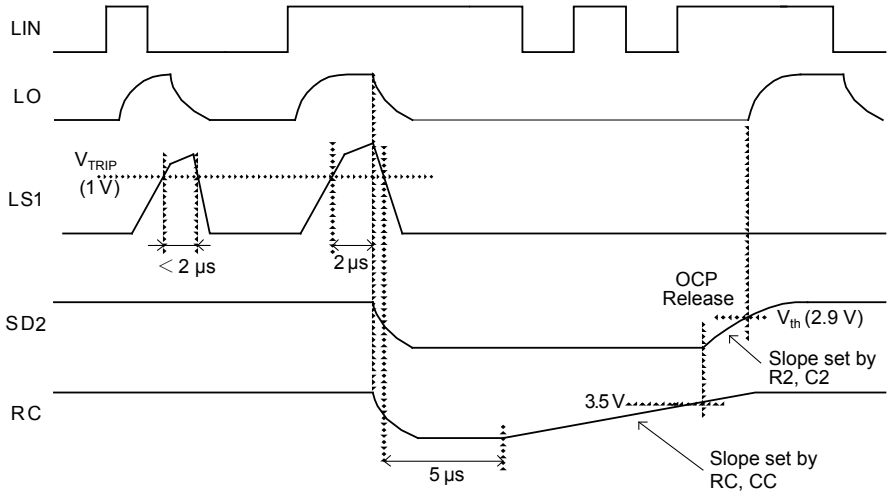


Figure 14. Low-Side VCC2 UVLO Internal Equivalent Circuit



A. The LOx signal is described, including delay imposed in accordance with the RC time constant by the input capacitance of the gate resistor and MOSFET.
B. Waveforms when both the SD2 and the RC signals are off, and include delay due to the time constants of the internal resistor (50 Ω) and the external capacitors C2, CC, and RC.

Figure 15. Overcurrent Protection Circuit Timing

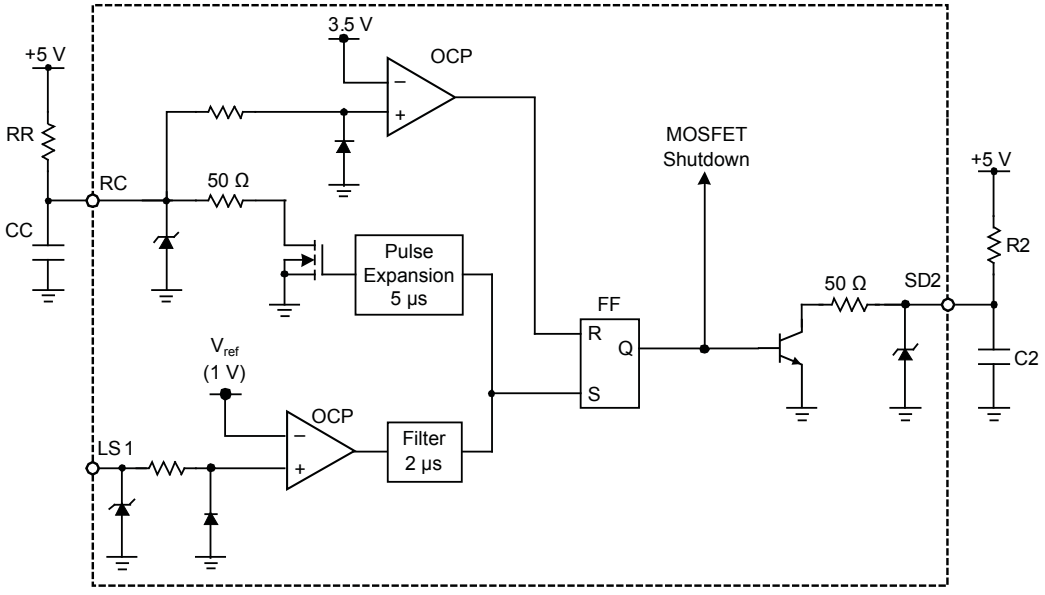


Figure 16. Overcurrent Protection Circuit

Typical Applications

This section examines typical application circuit designs using these devices, with and without output current limiting, and the timing effects that result.

Current Limiting by PWM Control This application implements current limiting by connecting the OCL and SD1 pins (figure 17). Current limiting occurs by turning off and on the power supplied to the high side of the MOSFET bridge. The timing is illustrated in figure 18.

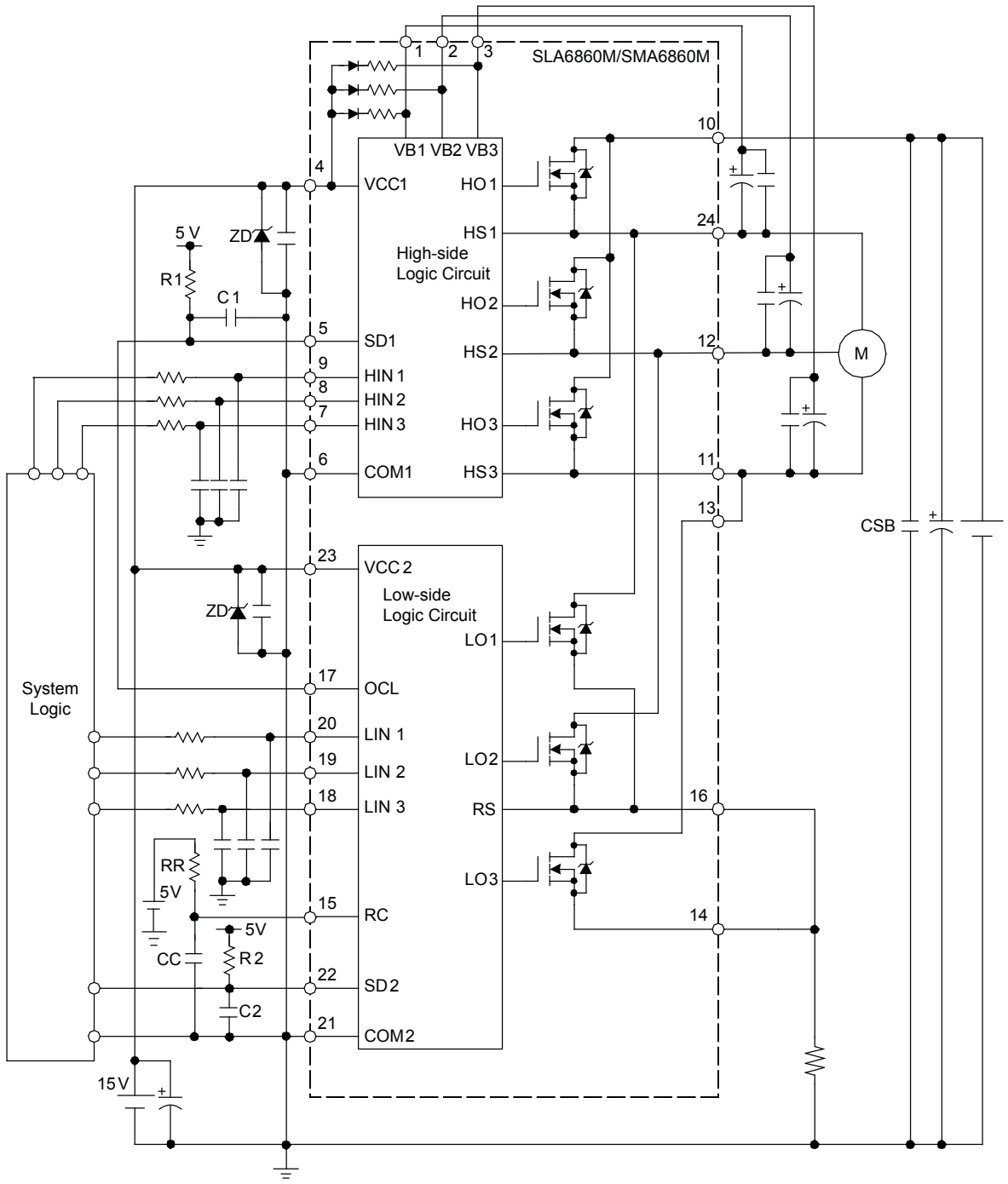


Figure 17. Typical Application. Current limiting by controlling power to high-side MOSFETs.

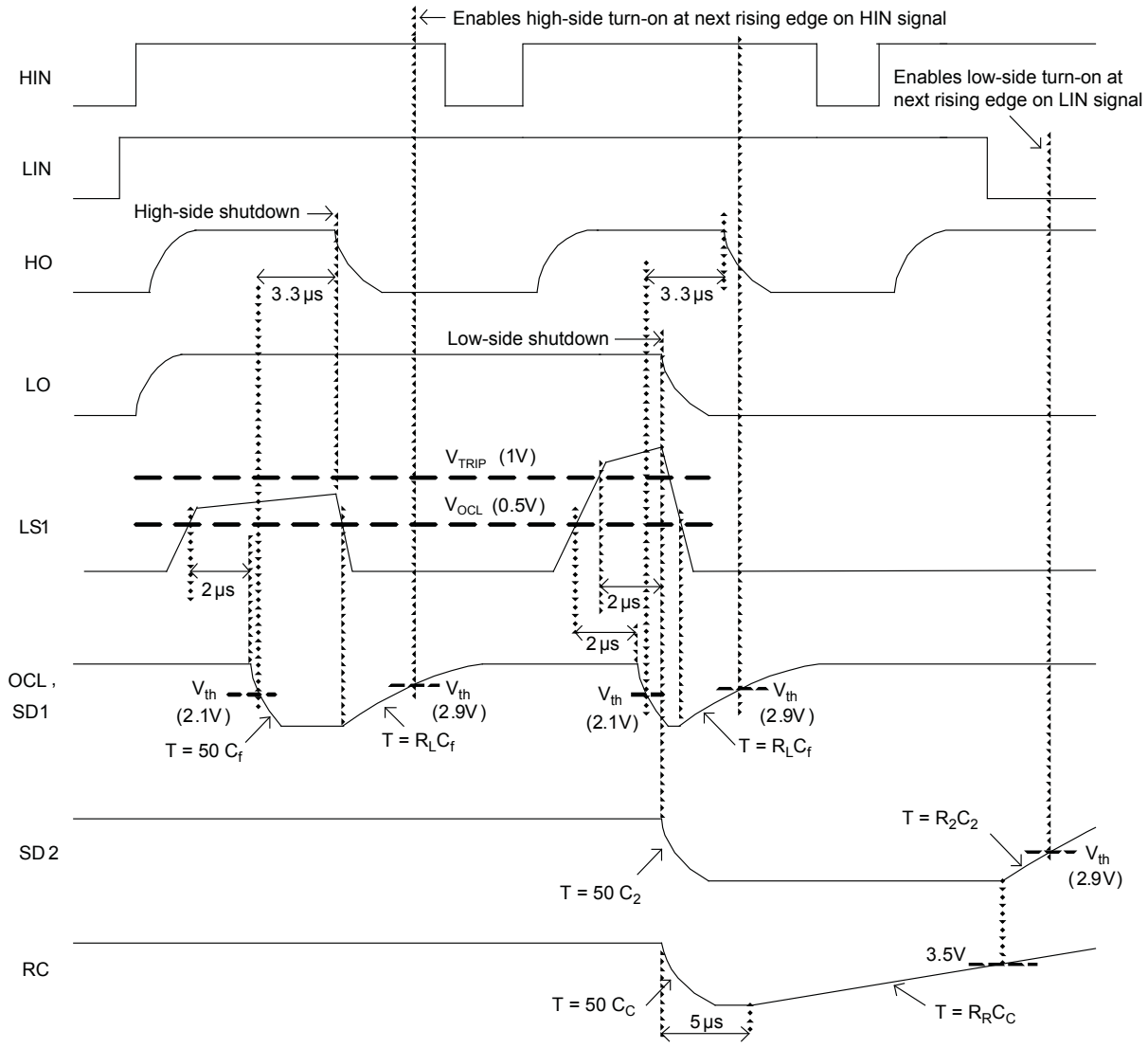


Figure 18. Output Timing Effects. Using typical application shown in figure 17.
HIN and LIN must not be in phase.

Current Limiting Using External Diode This application implements current limiting by connecting the OCL and SD1 pins as in the first application example, and also inserting a diode between OCL and SD2 (figure 19). Current limiting occurs by turning off and on the power supplied to the high side of the MOSFET bridge, according to a fault signal on the OCL-SD2 output. The effect on timing is shown in figure 20.

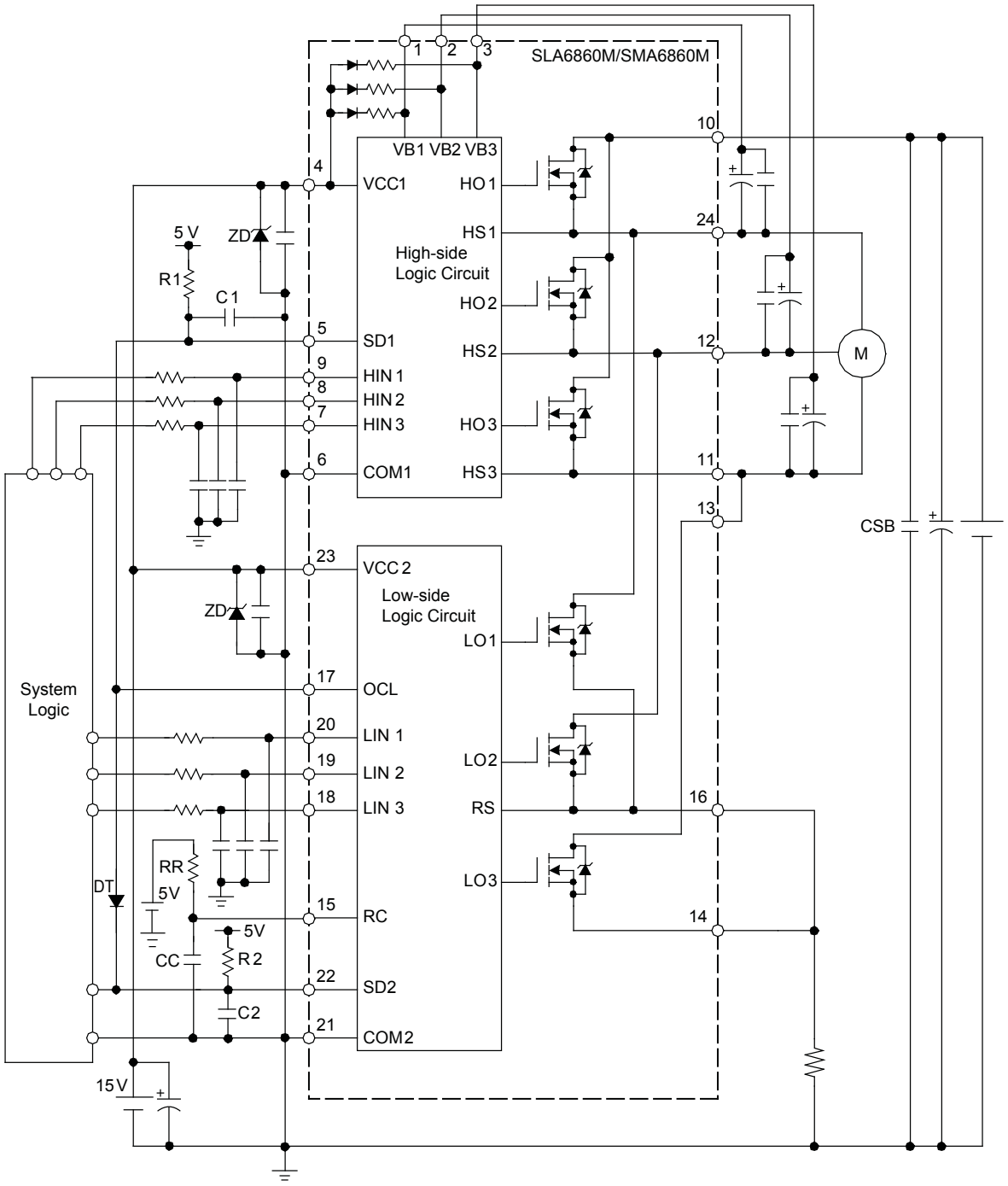


Figure 19. Typical Application. Current limiting by controlling power to high-side MOSFETs, with an external diode, DT, affecting the timing.

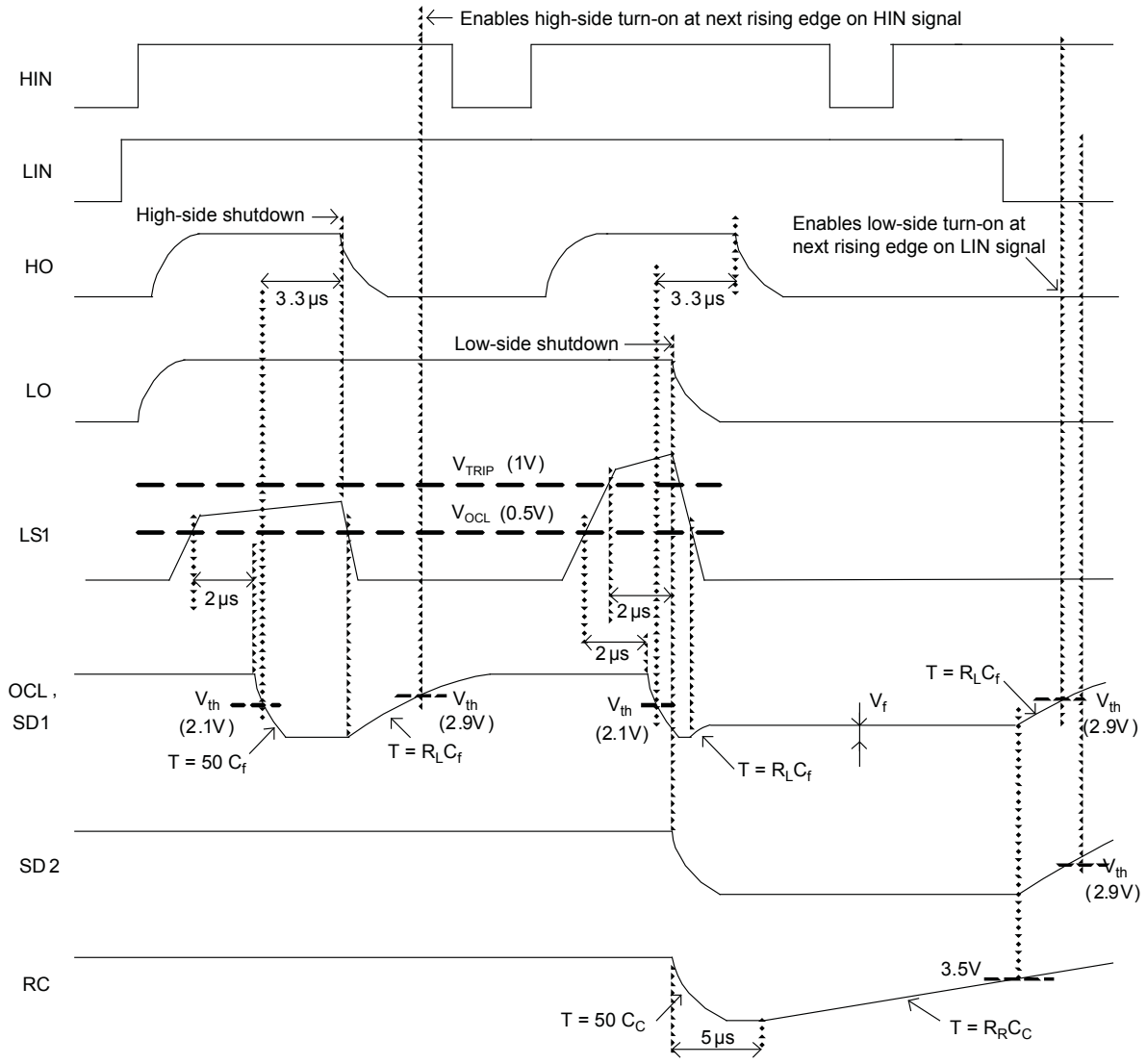


Figure 20. Output Timing Effects. Using typical application shown in figure 19.

HIN and LIN must not be in phase.

For the DT diode, use a diode for which V_f is less than 1.2 V at 5 mA (T_A = –20°C to 125°C).
Observe the following conditions:
R_L = 1.0 kΩ to 10 kΩ,
R_2 = 3.3 kΩ to 10 kΩ, and
C_f and C_2 = 0.001 µF to 0.01 µF

No Current Limiting This application does not use the device itself to limit output current. This is implemented by connecting the SD1 and SD2 pins (figure 21). The capacitors on the SD signals and the pull-up resistor on SD2 are not required. The effect on timing is shown in figure 22.

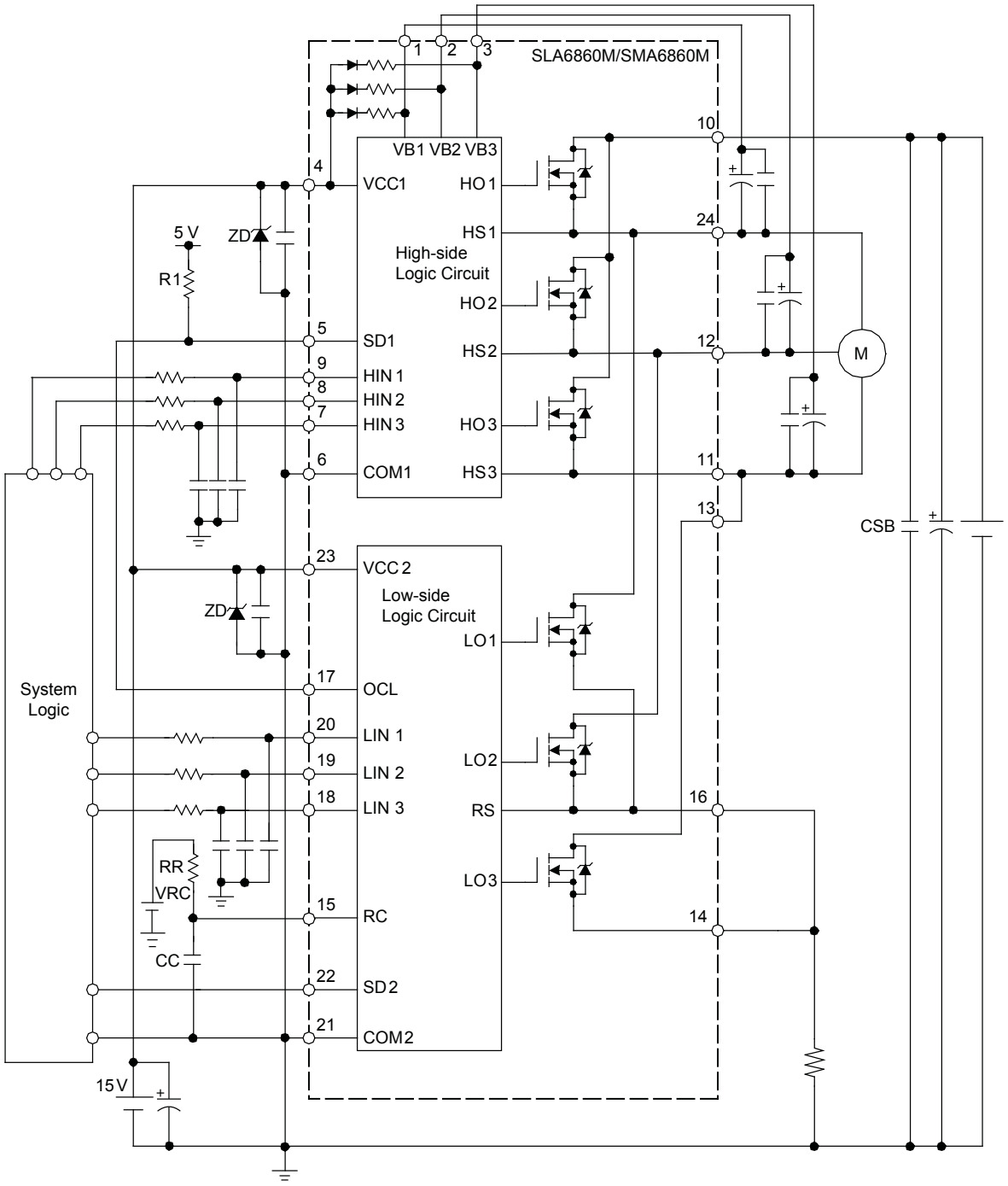


Figure 21. Typical Application. No output current limiting.

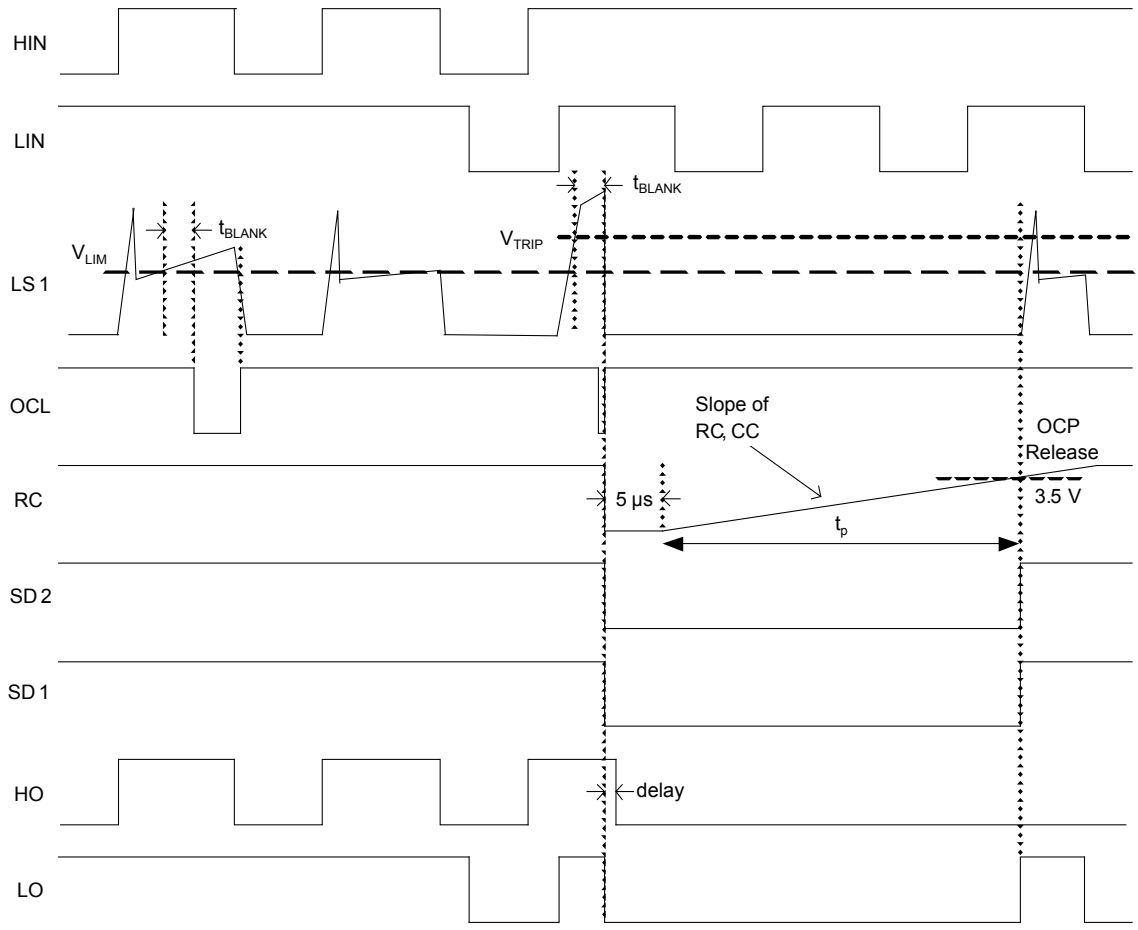


Figure 22. Output Timing Effects. Using typical application shown in figure 21 (no current limiting).
HIN and LIN must not be in phase.

Protection Function Timing

This section provides information about the timing of fault events handled by these devices.

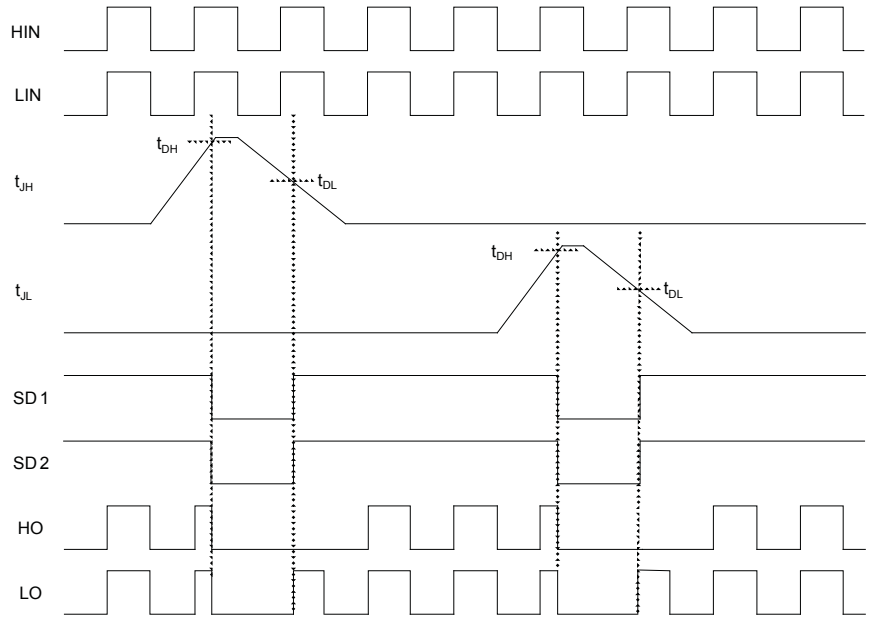


Figure 23. Overtemperature Protection Thermal Shutdown (TSD) Timing.
HIN and LIN must not be in phase.

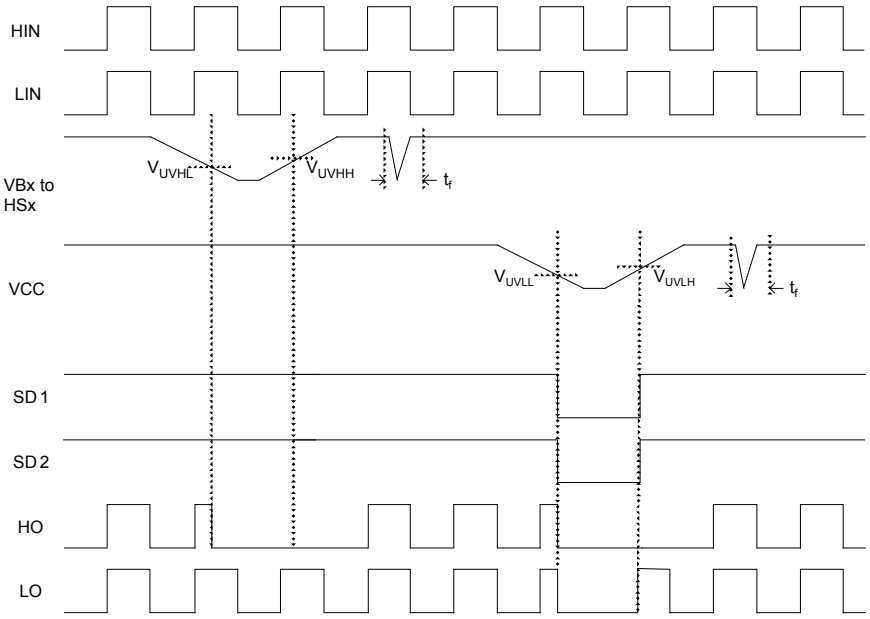


Figure 24. Undervoltage Lockout (UVLO) Protection.
HIN and LIN must not be in phase.

Application Circuit Recommendations

When designing application circuits using these devices, the following should be taken into consideration:

Supply Sequence The load power supply does not have to be provided in any particular sequence. However, commands should not be transmitted on the sequencing signal input terminals, HIN and LIN, until after the logic control power supply, VCC, has reached steady state.

Short Circuit Protection There is no built-in protection circuit against short circuits through the outputs to ground. The application circuit logic should be designed to monitor outputs to detect a short circuit condition.

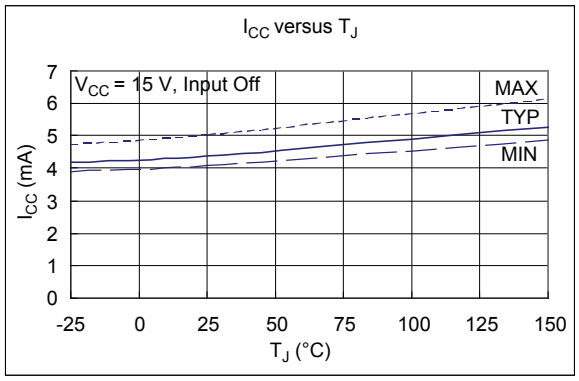
Pin to Pin Distance The device packages in the SLA6860M-SMA6860M Series have 24 pins, and a 1.27 mm pin pitch. At operating voltage levels, there may be insufficient creepage and clearance distance, and conformal coating or encapsulation of the application printed board assembly is recommended.

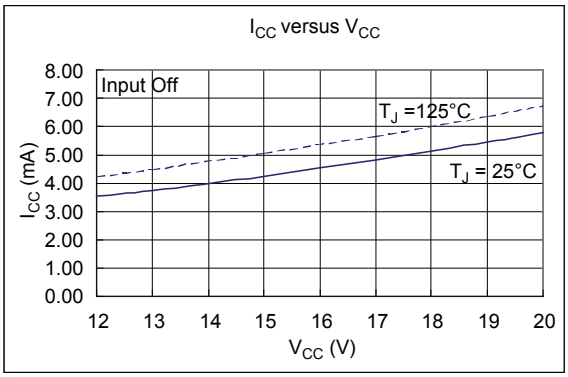
Surge Protection Each terminal should be protected against power surges by isolation using an external component such as a ceramic capacitor or Zener diode. Power surges that impinge on the device may cause critical damage to the IC as well as faulty operation.

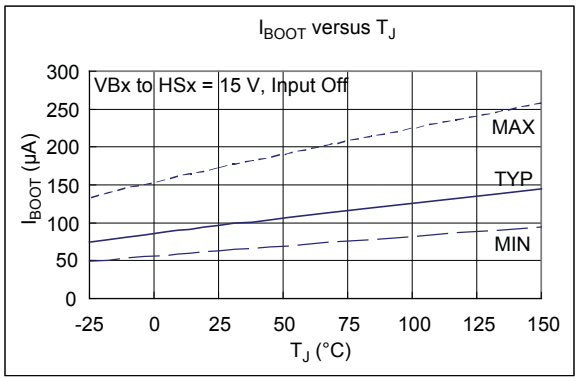
Input Blanking Time In order to avoid a high-side to low-side short-circuit, the HIN and LIN signals must never be in phase. The blanking time, t_{BLANK}, or dead-time, is the delay between rising edges on the HIN and LIN signals. It must be controlled externally by the application system logic, as it is not set internally. A t_{BLANK} of more than 1.5 µs is recommended.

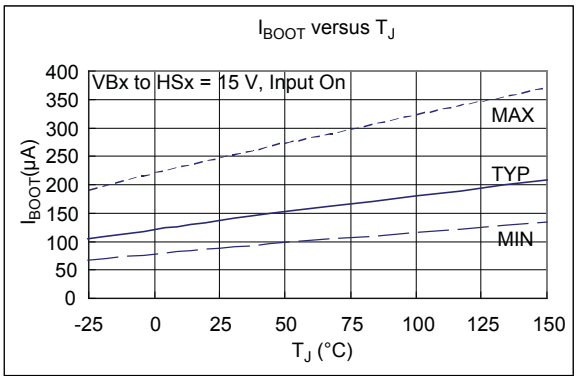
Electrical Characteristics Data

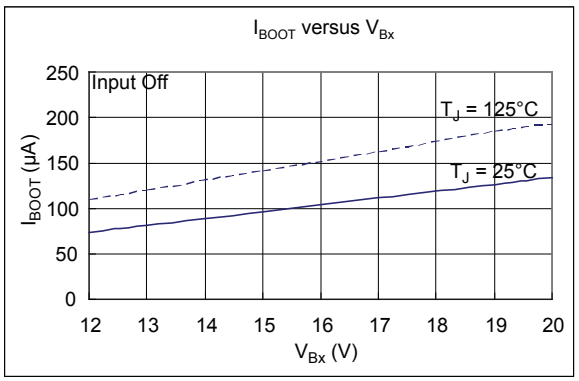
The following pages contain characteristic performance data. The information shown applies to all models of the SLA6860M-SMA6860M Series, unless otherwise specified.

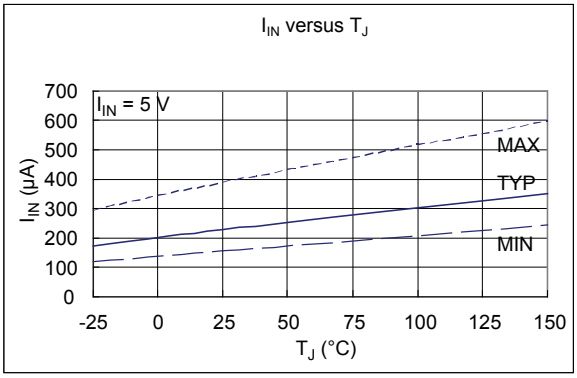

I_{CC} versus T_J
V_{CC} = 15 V, Input Off
MAX
TYP
MIN
I_{CC} (mA)
T_J (°C)

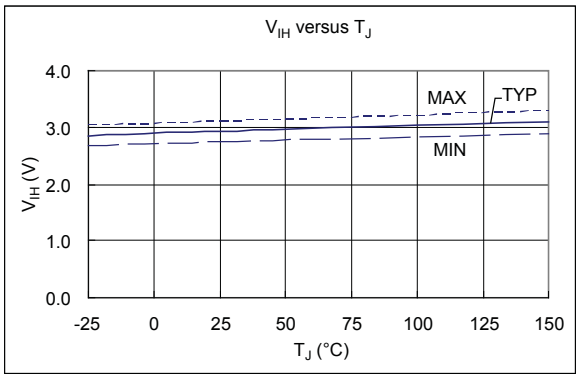

I_{CC} versus V_{CC}
Input Off
T_J =125°C
T_J = 25°C
I_{CC} (mA)
V_{CC} (V)

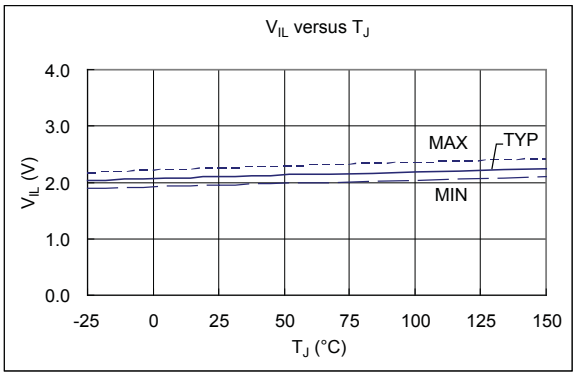

I_{BOOT} versus T_J
VBx to HSx = 15 V, Input Off
MAX
TYP
MIN
I_{BOOT} (µA)
T_J (°C)

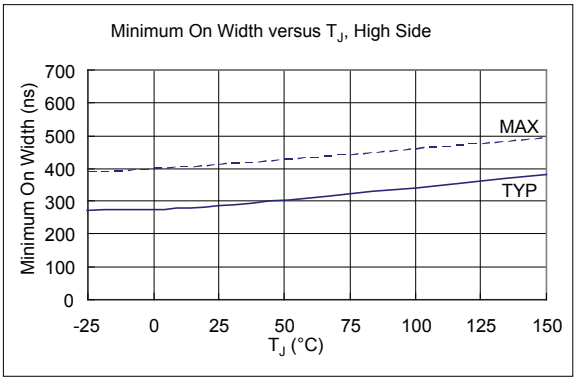

I_{BOOT} versus T_J
VBx to HSx = 15 V, Input On
MAX
TYP
MIN
I_{BOOT}(µA)
T_J (°C)

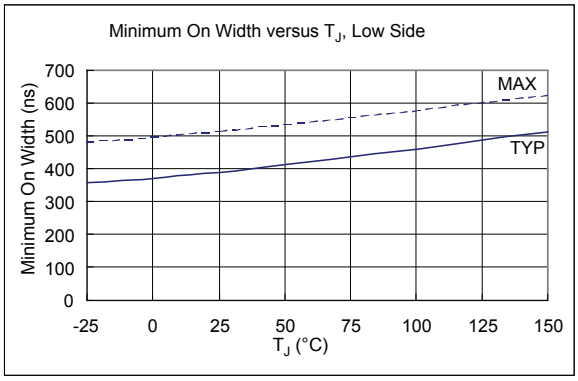

I_{BOOT} versus V_{Bx}
Input Off
T_J = 125°C
T_J = 25°C
I_{BOOT} (µA)
V_{Bx} (V)

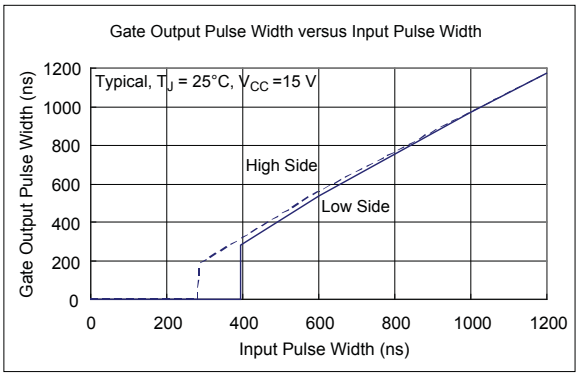

I_{IN} versus T_J
I_{IN} = 5 V
MAX
TYP
MIN
I_{IN} (µA)
T_J (°C)

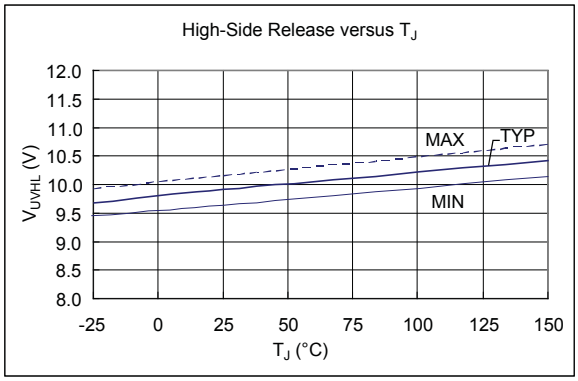

V_{IH} versus T_J
4.0
3.0
2.0
1.0
0.0
V_{IH} (V)
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

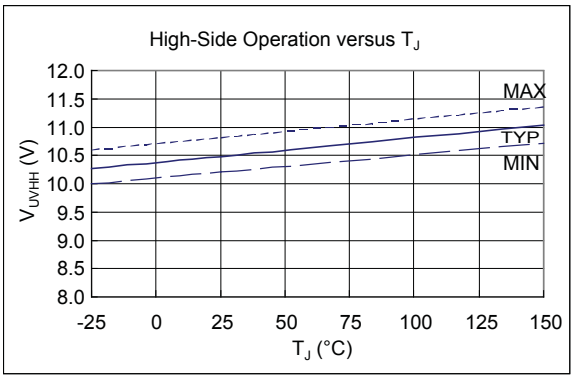

V_{IL} versus T_J
4.0
3.0
2.0
1.0
0.0
V_{IL} (V)
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

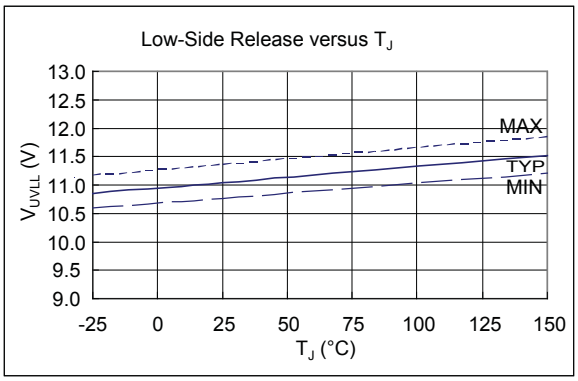

Minimum On Width versus T_J, High Side
700
600
500
400
300
200
100
0
Minimum On Width (ns)
MAX
TYP
-25
0
25
50
75
100
125
150
T_J (°C)

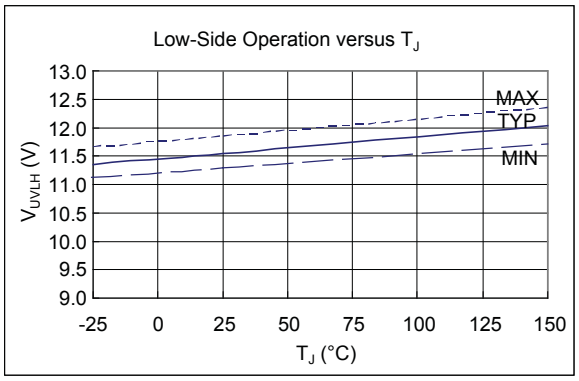

Minimum On Width versus T_J, Low Side
700
600
500
400
300
200
100
0
Minimum On Width (ns)
MAX
TYP
-25
0
25
50
75
100
125
150
T_J (°C)

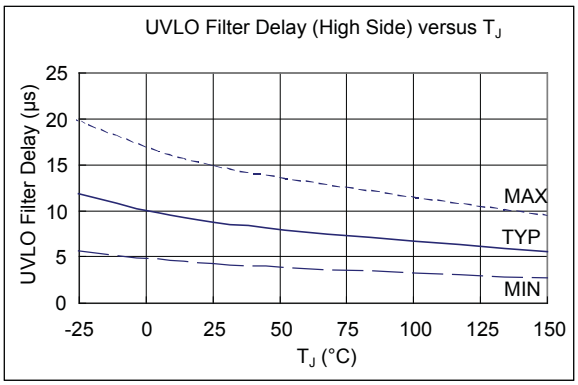

Gate Output Pulse Width versus Input Pulse Width
1200
1000
800
600
400
200
0
Gate Output Pulse Width (ns)
Typical, T_J = 25°C, V_{CC} =15 V
High Side
Low Side
0
200
400
600
800
1000
1200
Input Pulse Width (ns)

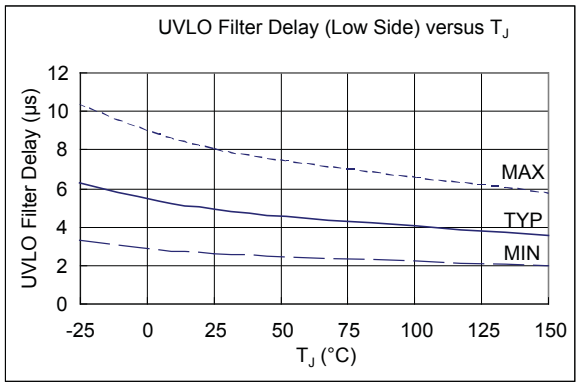

High-Side Release versus T_J
12.0
11.5
11.0
10.5
10.0
9.5
9.0
8.5
8.0
V_{UVHL} (V)
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

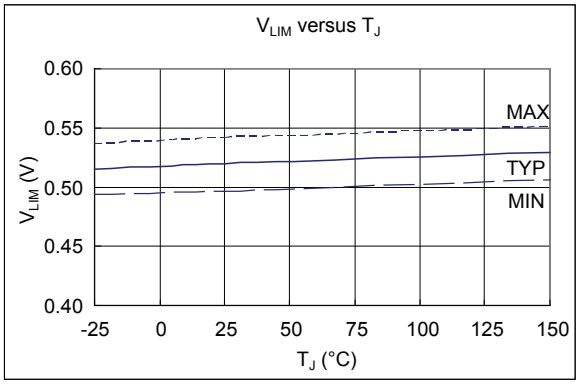

High-Side Operation versus T_J
V_{UVHH} (V)
12.0
11.5
11.0
10.5
10.0
9.5
9.0
8.5
8.0
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

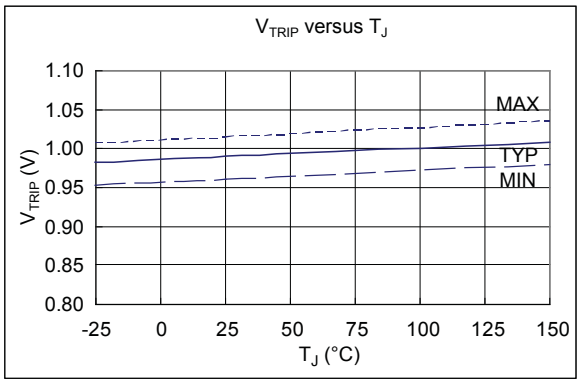

Low-Side Release versus T_J
V_{UVLL} (V)
13.0
12.5
12.0
11.5
11.0
10.5
10.0
9.5
9.0
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

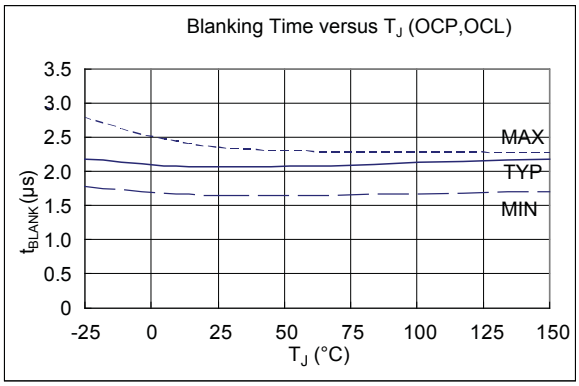

Low-Side Operation versus T_J
V_{UVLH} (V)
13.0
12.5
12.0
11.5
11.0
10.5
10.0
9.5
9.0
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

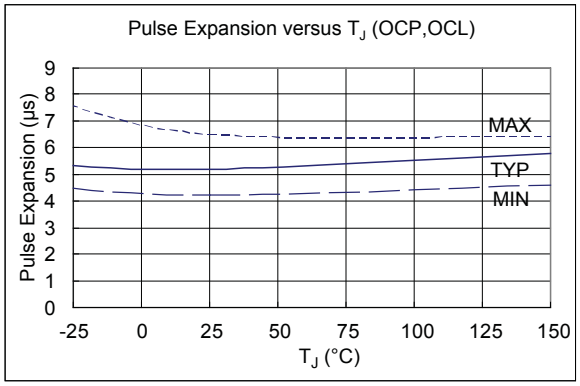

UVLO Filter Delay (High Side) versus T_J
UVLO Filter Delay (µs)
25
20
15
10
5
0
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

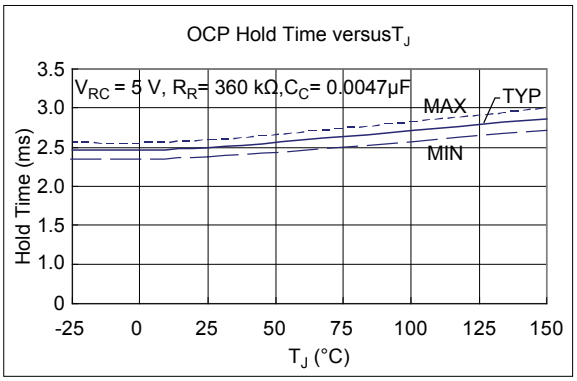

UVLO Filter Delay (Low Side) versus T_J
UVLO Filter Delay (µs)
12
10
8
6
4
2
0
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

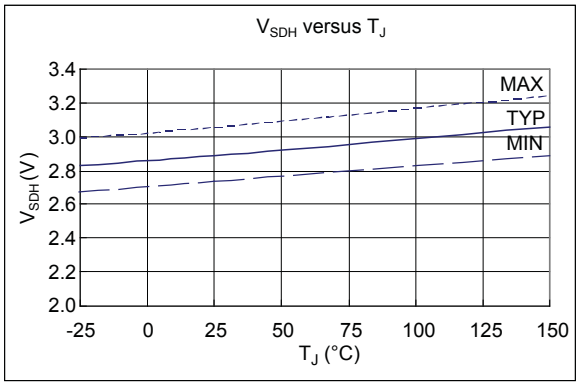

V_{LIM} versus T_J
V_{LIM} (V)
0.60
0.55
0.50
0.45
0.40
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

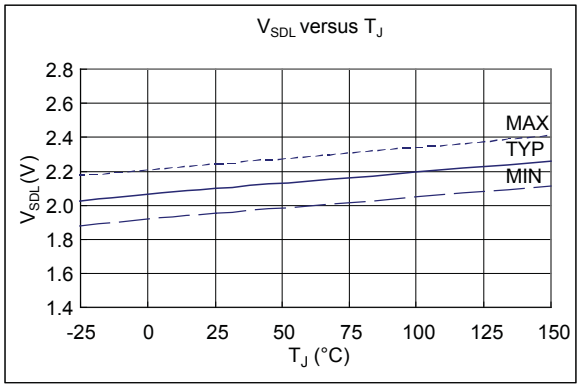

V_{TRIP} versus T_J
1.10
1.05
1.00
0.95
0.90
0.85
0.80
V_{TRIP} (V)
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

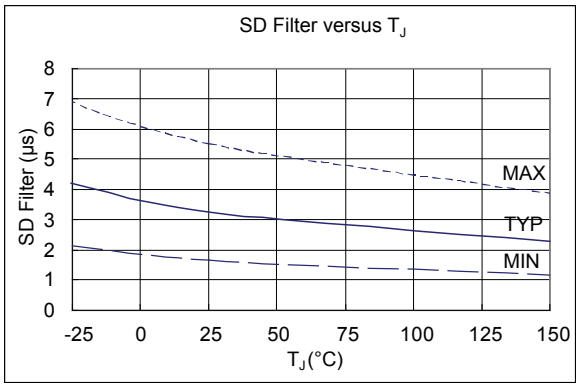

Blanking Time versus T_J (OCP,OCL)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
t_{BLANK} (µs)
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

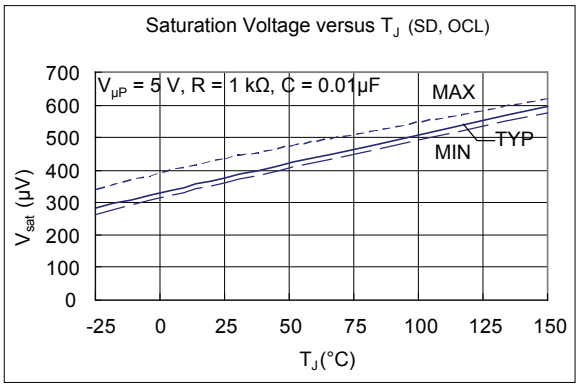

Pulse Expansion versus T_J (OCP,OCL)
9
8
7
6
5
4
3
2
1
0
Pulse Expansion (µs)
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

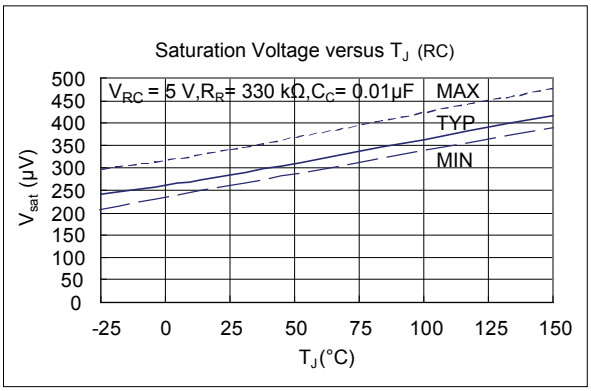

OCP Hold Time versusT_J
V_{RC} = 5 V, R_R= 360 kΩ,C_C= 0.0047µF
3.5
3.0
2.5
2.0
1.5
1.0
0
Hold Time (ms)
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)


V_{SDH} versus T_J
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
V_{SDH} (V)
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

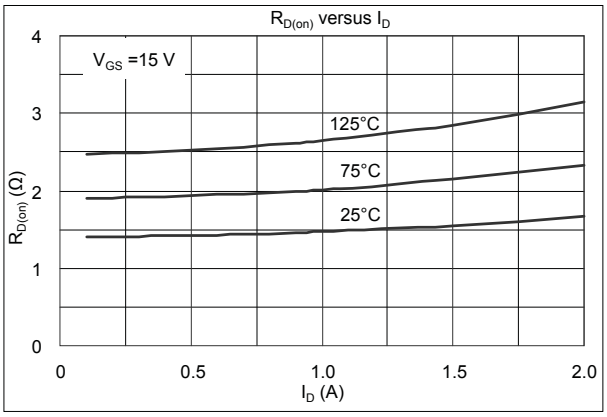

V_{SDL} versus T_J
2.8
2.6
2.4
2.2
2.0
1.8
1.6
1.4
V_{SDL} (V)
MAX
TYP
MIN
-25
0
25
50
75
100
125
150
T_J (°C)

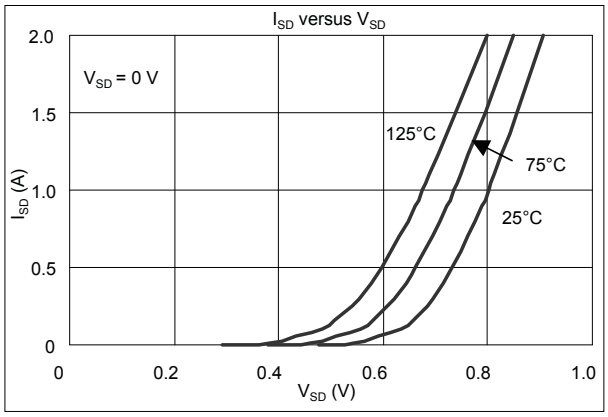

SD Filter versus T_J
SD Filter (µs)
8
7
6
5
4
3
2
1
0
-25
0
25
50
75
100
125
150
T_J(°C)
MAX
TYP
MIN


Saturation Voltage versus T_J (SD, OCL)
$V_{µP}$ = 5 V, R = 1 kΩ, C = 0.01µF
V_{sat} (µV)
700
600
500
400
300
200
100
0
-25
0
25
50
75
100
125
150
T_J(°C)
MAX
TYP
MIN

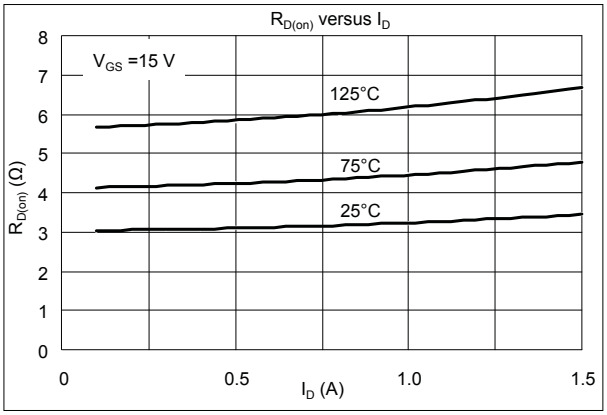

Saturation Voltage versus T_J (RC)
V_{RC} = 5 V,R_R= 330 kΩ,C_C= 0.01µF
V_{sat} (µV)
500
450
400
350
300
250
200
150
100
50
0
-25
0
25
50
75
100
125
150
T_J(°C)
MAX
TYP
MIN

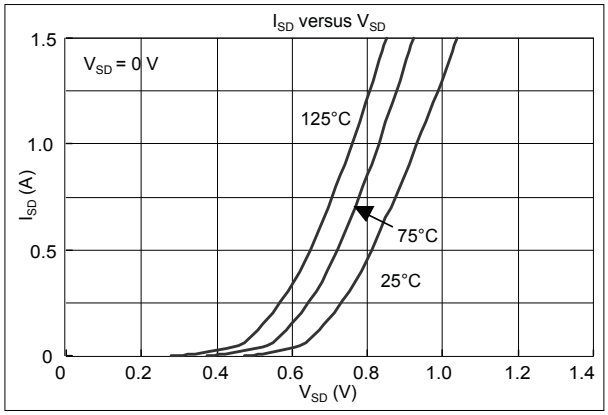
SMA6861M MOSFET Characteristics



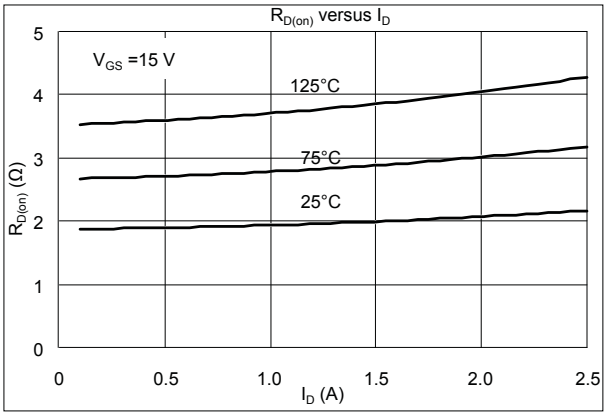


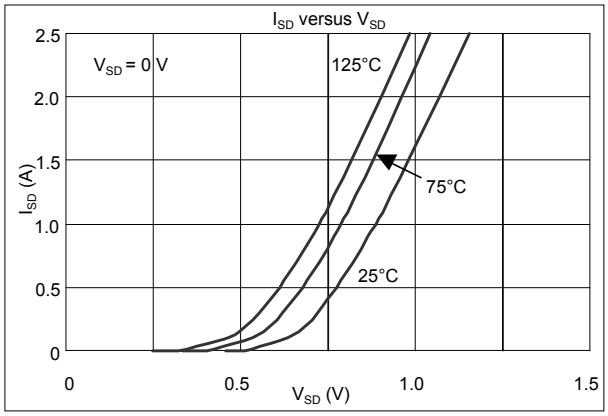
SMA6862M MOSFET Characteristics





SMA6863M MOSFET Characteristics





All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature of 25°C, unless otherwise stated.

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