

1/2 inch CCD Image Sensor for EIA B/W Camera

Description

The ICX038BLB is an interline transfer CCD solid-state image sensor suitable for EIA 1/2 inch B/W video cameras. High resolution, high sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time. Also, this outline is miniaturized by using original package.

Features

- High resolution high sensitivity (+6dB compare with ICX038ALA) and low dark current
- Consecutive variable speed shutter
1/60s. (Typ.), 1/100s. to 1/10000s
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Horizontal register final stage 5V drive
- Reset gate 5V drive

Device Structure

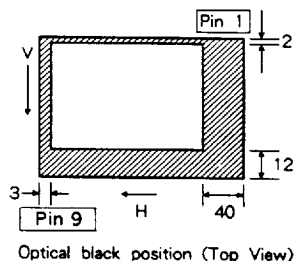
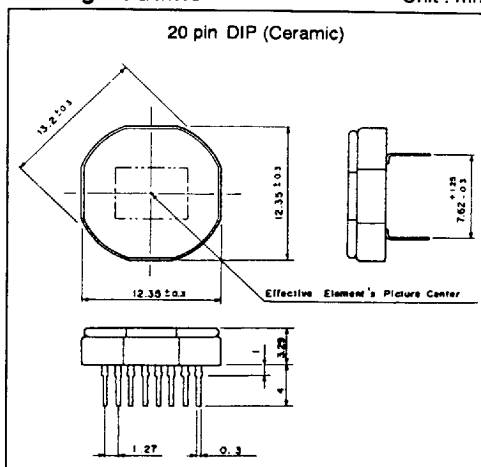
- Optical size 1/2 inch format
- Number of effective pixels 768 (H) × 494 (V) Approx. 380k pixels
- Number of total pixels 811(H) × 508 (V) Approx. 410k pixels
- Interline transfer CCD image sensor
- Chip size 7.95mm (H) × 6.45mm (V)
- Unit cell size 8.4 μm (H) × 9.8 μm (V)
- Optical black

Horizontal (H) direction	Front 3 pixels Rear 40 pixels
Vertical (V) direction	Front 12 pixels Rear 2 pixels
- Number of dummy bits

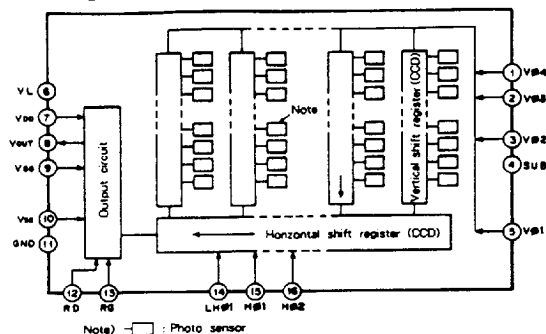
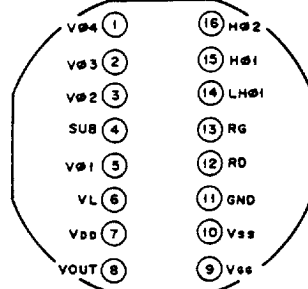
Horizontal	22
Vertical	1 (even field only)
- Substrate material silicon

Package Outline

Unit : mm



Block Diagram

Pin Configuration
(Top View)

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	$V_{\phi 4}$	Vertical register transfer clock	9	V_{GG}	Output amplifier gate bias
2	$V_{\phi 3}$	Vertical register transfer clock	10	V_{SS}	Output amplifier source
3	$V_{\phi 2}$	Vertical register transfer clock	11	GND	GND
4	SUB	Substrate (Overflow drain)	12	RD	Reset drain bias
5	$V_{\phi 1}$	Vertical register transfer clock	13	RG	Reset gate clock
6	V_L	Protective transistor bias	14	$LH\phi_1$	Horizontal register final stage transfer clock
7	V_{DD}	Output amplifier drain supply	15	$H\phi_1$	Horizontal register transfer clock
8	V_{OUT}	Signal output	16	$H\phi_2$	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		-0.3 to +55	V	
Supply voltage	$V_{DD}, V_{RD}, V_{OUT}, V_{SS} - GND$	-0.3 to +18	V	
	$V_{DD}, V_{RD}, V_{OUT}, V_{SS} - SUB$	-55 to +10	V	
Clock input voltage	$V_{\phi 1}, V_{\phi 2}, V_{\phi 3}, V_{\phi 4} - GND$	-15 to +20	V	
	$V_{\phi 1}, V_{\phi 2}, V_{\phi 3}, V_{\phi 4} - SUB$	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*(Max.)
Voltage difference between horizontal clock input pins		to +17	V	
$H\phi_1, H\phi_2 - V_{\phi 4}$		-17 to +17	V	
$LH\phi_1, RG, V_{GG} - GND$		-10 to +15	V	
$LH\phi_1, RG, V_{GG} - SUB$		-55 to +10	V	
$V_L - SUB$		-65 to +0.3	V	
Beside GND, SUB- V_L		-0.3 to +30	V	
Storage temperature		-30 to +80	°C	
Operating temperature		-10 to +60	°C	

* +27V (Max.) when clock width < 10 μ s, duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD}=V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 390 Ω resistor				$\pm 5\%$
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*2
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	-3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*2 *6
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	-3		+3	%	
Protective transistor bias	V_L	*3				

DC Characteristics

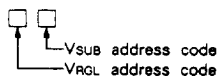
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

*2 Substrate voltage (V_{SUB}) + reset gate clock voltage (V_{RGL}) setting value display.

Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is $\pm 3\%$.

V_{SUB} code address—1 digit display

V_{RGL} code address—1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" $\rightarrow V_{RGL}=3.0V$

$V_{SUB}=12.0V$

*3 V_L setting is the V_L voltage of the vertical transfer clock waveform.

- *4 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, V_{SS} and SUB pins, while pins that are not tested are grounded.
 2. Current to each pins when 20V is applied sequentially to V ϕ 1, V ϕ 2, V ϕ 3, V ϕ 4, H ϕ 1 and H ϕ 2, while pins that are not tested are grounded. However, 20V is applied to SUB.
 3. Current to each pins when 15V is applied sequentially to pins RG, LH ϕ 1 and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
 4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.
- *5 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

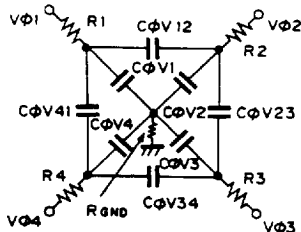
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V _{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V _{VH1} , V _{VH2}	-0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V _{VH3} , V _{VH4}	-0.2	0	0.05	V	2	
	V _{VL1} , V _{VL2} , V _{VL3} , V _{VL4}	-9.6	-9.0	-8.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	V ϕ v	8.3	9.0	9.65	V	2	$V_{\phi v} = V_{VHN} - V_{VLN}$ (n=1 to 4)
	V _{VH1} - V _{VH2}			0.1	V	2	
	V _{VH3} - V _{VH}	-0.25		0.1	V	2	
	V _{VH4} - V _{VH}	-0.25		0.1	V	2	
	V _{VHH}			0.5	V	2	High level coupling
	V _{VHL}			0.5	V	2	High level coupling
	V _{VLH}			0.5	V	2	Low level coupling
	V _{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	V ϕ H	4.75	5.0	5.25	V	3	
	V _{HL}	-0.05	0	0.05	V	3	
Horizontal final stage transfer clock voltage	V ϕ LH	4.75	5.0	5.25	V	4	
	V _{LHL}	-0.05	0	0.05	V	4	
Reset gate clock voltage	V ϕ RG	4.5	5.0	5.5	V	5	*6
	V _{RGLH} - V _{RGLL}			0.8	V	5	Low level coupling
Substrate clock voltage	V ϕ SUB	23.0	24.0	25.0	V	6	

- *6 No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

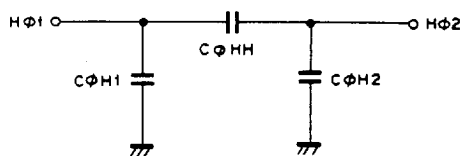
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	VRGL	-0.2	0	0.2	V	5	
	VφRG	8.5	9.0	9.5	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	CφV1, CφV3		1800		pF	
	CφV2, CφV4		2200		pF	
Capacitance between vertical transfer clocks	CφV12, CφV34		450		pF	
	CφV23, CφV41		270		pF	
Capacitance between horizontal transfer clock and GND	CφH1, CφH2		62		pF	
Capacitance between horizontal transfer clocks	CφHH		47		pF	
Capacitance between horizontal final stage transfer clock and GND	CφLH		8		pF	
Capacitance between reset gate clock and GND	CφRG		8		pF	
Capacitance between substrate clock and GND	CφSUB		400		pF	
Vertical transfer clock serial resistor	R1, R2, R3, R4		68		Ω	
Vertical transfer clock ground resistor	RGND		15		Ω	



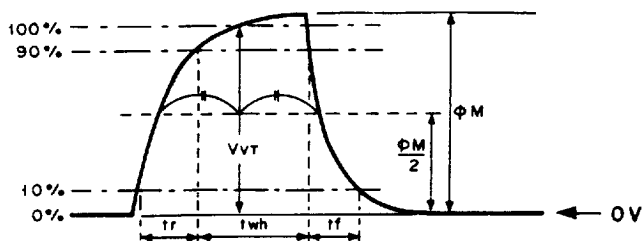
Vertical transfer clock equivalent circuit



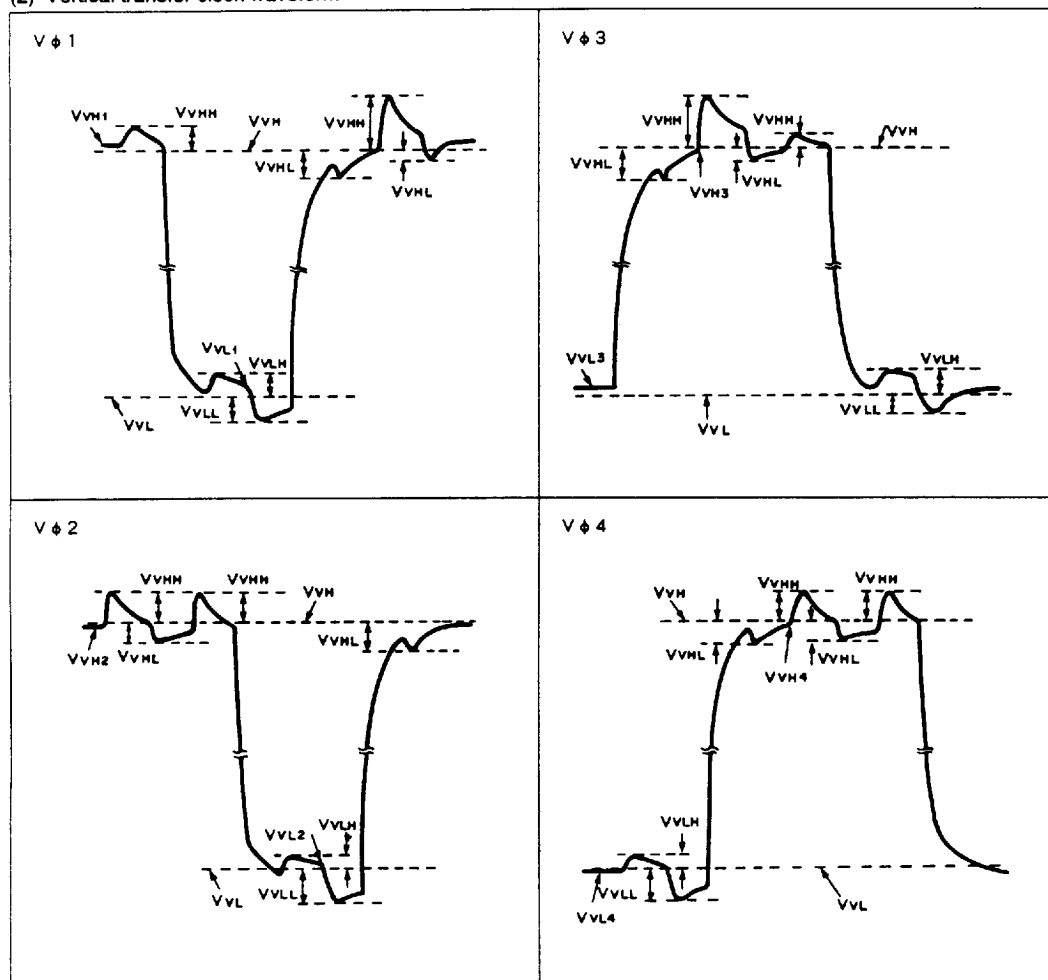
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

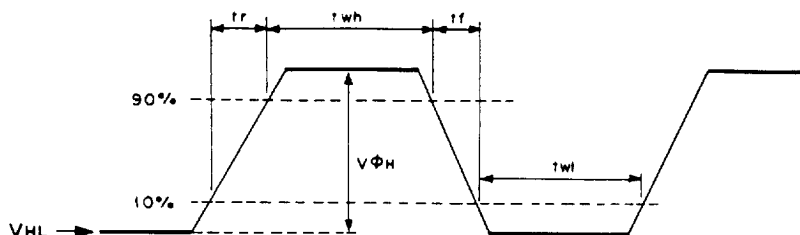
(1) Read out clock waveform



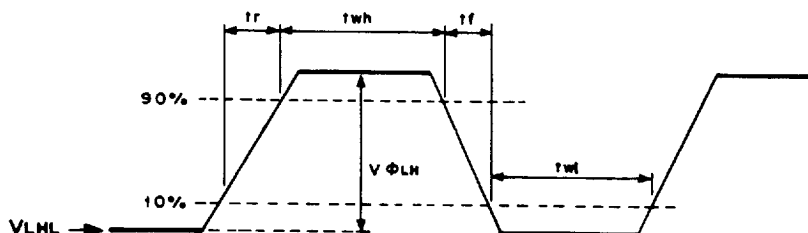
(2) Vertical transfer clock waveform



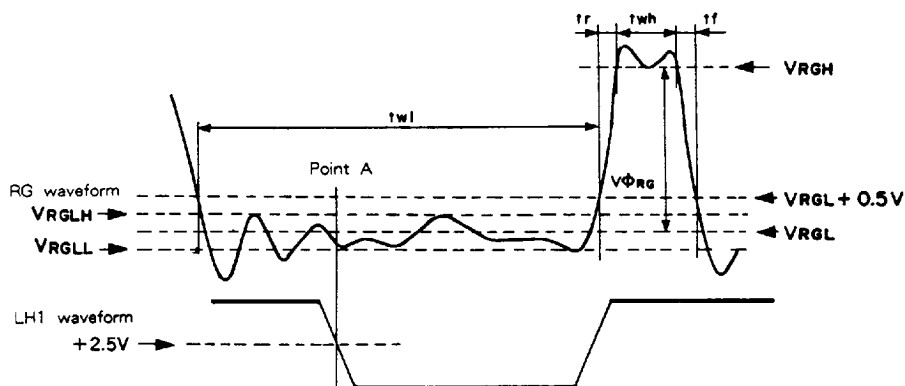
(3) Horizontal transfer clock waveform diagram



(4) Horizontal final stage transfer clock waveform diagram



(5) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

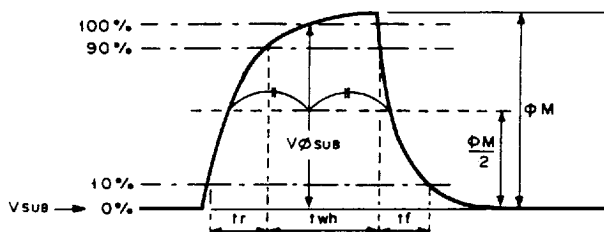
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL} .

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

V_{RGH} is the minimum value for t_{wh} period.

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

(6) Substrate clock waveform



Clock switching characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_r	2.3	2.5						0.5			0.5		μs	During read out
Vertical transfer clock	$V_{\phi 1}, V_{\phi 2}, V_{\phi 3}, V_{\phi 4}$										0.015		0.25	μs	* 7
Horizontal transfer clock	H_{ϕ}		20			20		15	19	* 8	15	19		ns	During imaging
Horizontal final stage clock	LH_{ϕ}		20			20		15	19	* 8	15	19		ns	During imaging
Horizontal transfer/horizontal final stage clock	$H_{\phi 1}, LH_{\phi}$		5.38					0.01			0.01			μs	During parallel serial conversion.
Horizontal transfer clock	$H_{\phi 2}$					5.38		0.01			0.01			μs	
Reset gate clock	ϕ_{RG}	11	13			51		3			3			ns	
Substrate clock	ϕ_{sus}	1.5	1.8						0.5			0.5		μs	During charge drain.

* 7 When vertical transfer clock driver CXD1250 is in use.

* 8 $t_f \geq t_r - 2 \text{ ns}$

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H_{ϕ}	16	20		ns	* 9
Horizontal transfer/horizontal final stage clock	$H_{\phi 2}, LH_{\phi}$	16	20		ns	* 10

* 9 "two" is the overlap period of horizontal transfer clocks $H_{\phi 1}$ and $H_{\phi 2}$'s twh and twl.* 10 "two" is the overlap period of horizontal transfer clock $H_{\phi 2}$'s twl and horizontal final stage transfer clock LH_{ϕ} 's twh.

Operating Characteristics

(Ta=25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	300	380		mV	1	
Saturation signal	Vsat	600			mV	2	Ta=60 °C
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta=60 °C
Dark signal shading	Δ Vdt			1	mV	6	Ta=60 °C
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone chart of Video signal shading

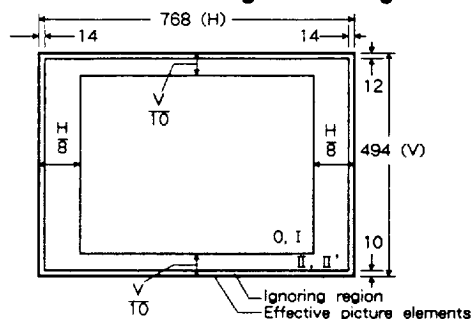


Image Sensor Characteristics Test Method

◎ Test conditions

- ① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.
- ② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference, the values obtained at ① point in the figure of the Drive Circuit are utilized.

⑥ Definition of standard imaging conditions

- ① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m², color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F8. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity. Signal output average value in this condition is called V_A.
- ② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity

Set to standard image condition I. After selecting the electronic shutter mode at a 1/250s. shutter speed, measure the signal (V_s) at the center of the screen and substitute in the following formula.

$$S = V_s \times \frac{250}{60}$$

2. Saturation signal

Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value V_A=200mV, then test signal output minimum value.

3. Smear

Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value (V_A=200mV). Stop read out clock. When the charge drain executed by the electric shutter at the respective H blankings takes place, test the maximum value V_{sm} of signal output.

$$S_m = \frac{V_{sm}}{200} \times \frac{1}{500} \times \frac{1}{10} \times 100 (\%) (1/10V)$$

4. Video signal shading

Set to standard imaging condition II. Adjust light intensity to signal output average value V_A=200mV with lens diaphragm at F5.6 to F8. Then test maximum (V_{max}) and minimum (V_{min}) values of signal output.

$$SH = (V_{max} - V_{min}) / 200 \times 100 (\%)$$

5. Dark signal

Test signal output average value V_{dt} when the device ambient temperature is at 60 °C and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading

Following 5, test maximum (V_{dmax}) and minimum (V_{dmin}) values of dark signal output.

$$\Delta V_{dt} = V_{dmax} - V_{dmin}$$

7. Flicker

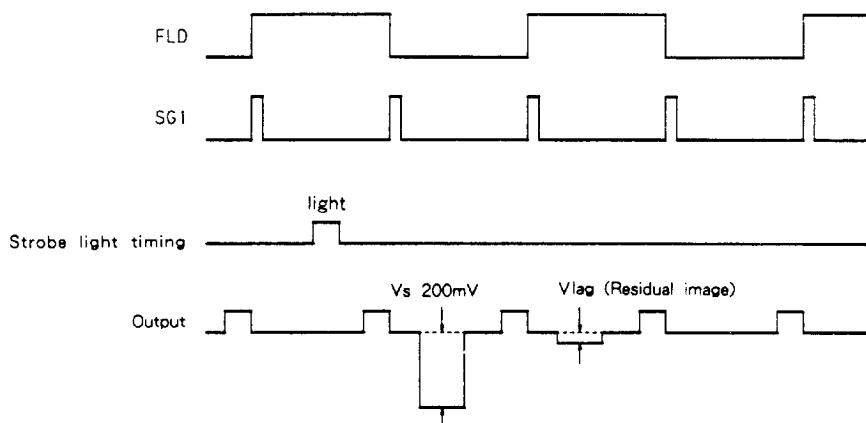
Set to standard imaging condition II. Adjust light intensity to signal output average value $V_A = 200\text{mV}$. Then test the signal output difference (ΔV_f) between even field and odd field.

$$F = (\Delta V_f / 200) \times 100 (\%)$$

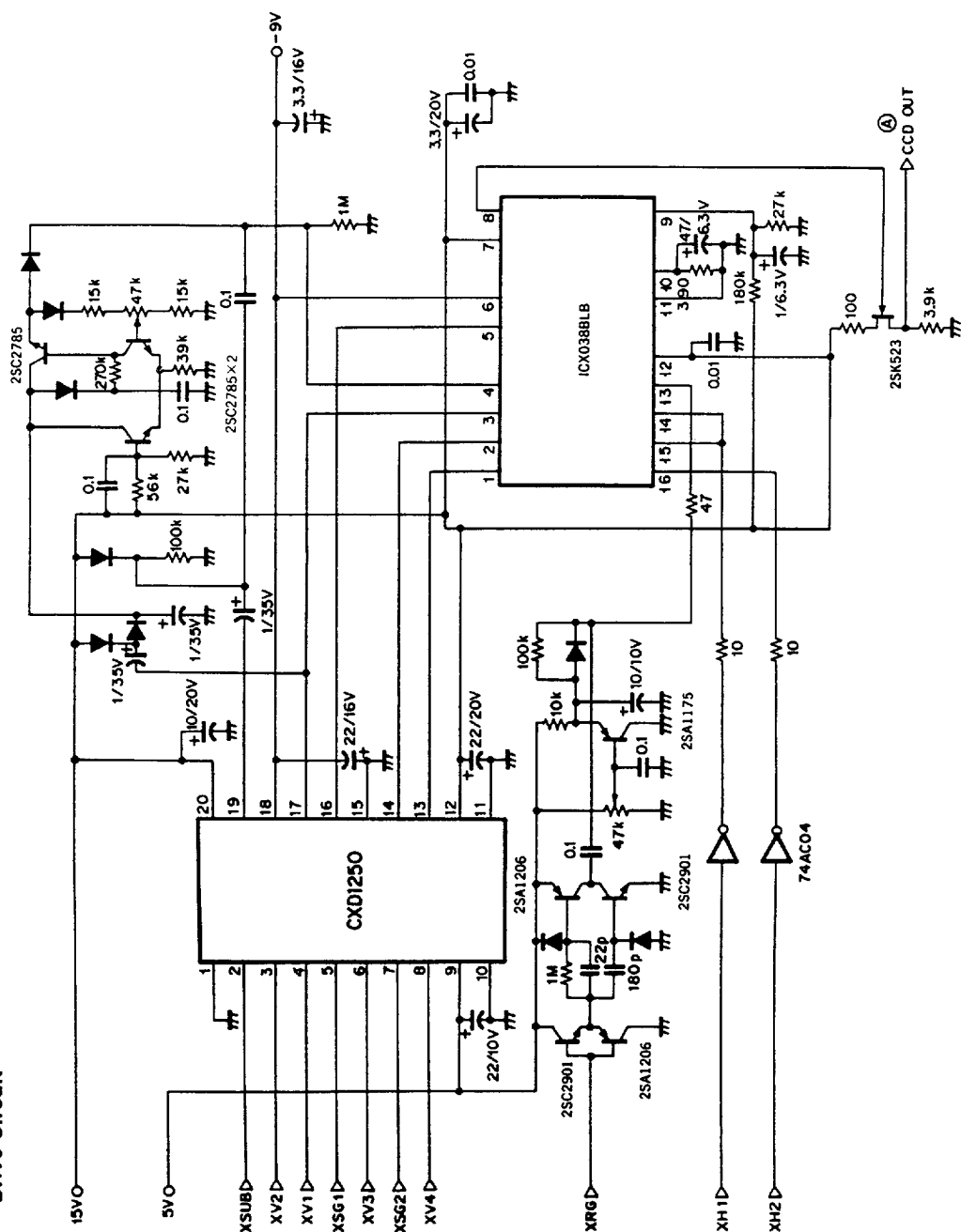
8. Residual image

Adjust signal output value (V_s) by strobe light to 200mV . Then light a stroboscopic tube with the following timing and test the residual image (V_{lag}).

$$Lag = (V_{lag} / V_s) \times 100 (\%)$$

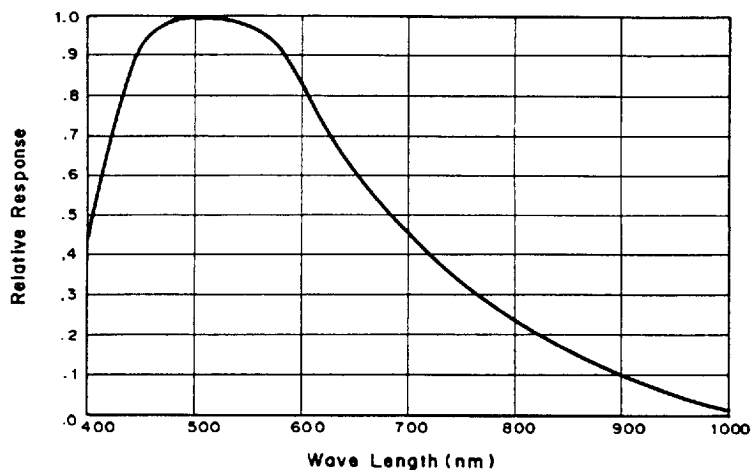
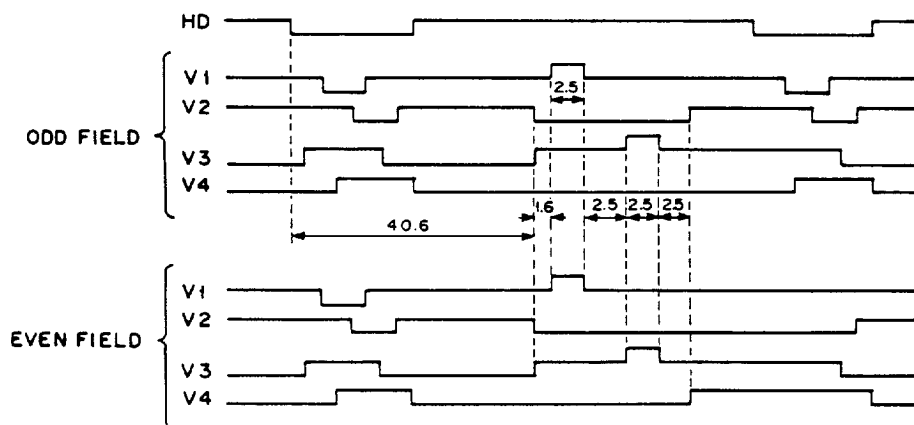


Drive Circuit

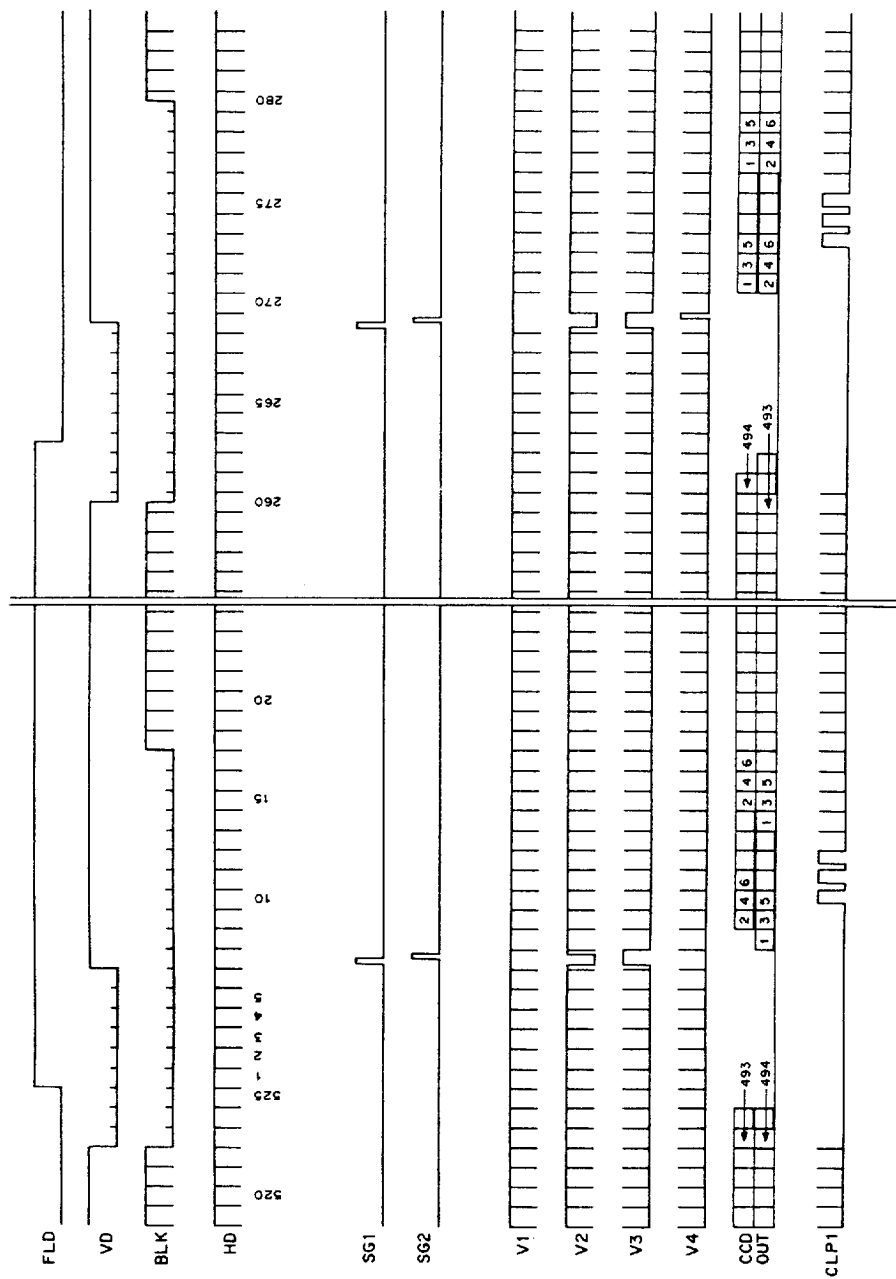


Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

**Using read out clock timing chart**Unit : μ s

Drive Timing Chart (Vertical sync)



The timing diagram illustrates the relationship between various signals and time. The horizontal axis represents time in nanoseconds (ns), with major ticks at 760, 765, 770, 775, 780, 785, 790, 795, 800, 805, 810, 815, 820, 825, 830, 835, 840, 845, 850, 855, 860, 865, 870, 875, 880, 885, 890, 895, 900, 905, 910, 915, 920, 925, 930, 935, 940, 945, 950, 955, 960, 965, 970, 975, 980, 985, 990, 995, and 1000. The signals are as follows:

- HD**: High Data bus signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- BLK**: Block signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- H1 / LH1**: High 1 / Low 1 signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- H2**: High 2 signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- RG**: Register Gate signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- SHP**: Shift Pulse signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- SHD**: Shift Data signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- V1**: Voltage 1 signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- V2**: Voltage 2 signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- V3**: Voltage 3 signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- V4**: Voltage 4 signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- CLP1**: Clock Pulse 1 signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.
- SUB**: Substrate signal, active low. It transitions from high to low at approximately 765 ns and back to high at approximately 775 ns.

Handling Instructions

- 1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
 - a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
 - b) When handling directly use an earth band.
 - c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
 - d) Ionized air is recommended for discharge when handling CCD image sensor.
 - e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.
- 2) Soldering
 - a) Make sure the package temperature does not exceed 80 °C .
 - b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
 - c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.
- 3) Dust and dirt protection
 - a) Operate in clean environments (around class 1000 will be appropriate).
 - b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
 - c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
 - d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
 - e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.
- 4) Do not expose to strong light (sun rays) for long periods.
- 5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- 6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.