ADVANCE INFORMATION

CY7C1610KV18, CY7C1625KV18 CY7C1612KV18, CY7C1614KV18

144-Mbit QDR™-II SRAM 2-Word Burst Architecture

Features

- Separate independent read and write data ports
  - Supports concurrent transactions
- 333 MHz clock for high bandwidth
- 2-word burst on all accesses
- Double Data Rate (DDR) interfaces on both read and write ports (data transferred at 666 MHz) at 333 MHz
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Two input clocks for output data (C and $\overline{C}$) to minimize clock skew and flight time mismatches
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high speed systems
- Single multiplexed address input bus latches address inputs for read and write ports
- Separate port selects for depth expansion
- Synchronous internally self timed writes
- QDR™-II operates with 1.5 cycle read latency when DOFF is asserted HIGH
- Operates similar to QDR I device with 1 cycle read latency when DOFF is asserted LOW
- Available in ×8, x9, x18, and x36 configurations
- Full data coherency providing most current data
- Core VDD = 1.8V(±0.1V); IO VDDQ = 1.4V to VDD
- Available in 165-ball FBGA package (15 x 17 x 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- Variable drive HSTL output buffers
- JTAG 1149.1 compatible test access port
- Phase Locked Loop (PLL) for accurate data placement

Configurations

CY7C1610KV18 – 16M x 8
CY7C1625KV18 – 16M x 9
CY7C1612KV18 – 8M x 18
CY7C1614KV18 – 4M x 36

Functional Description

The CY7C1610KV18, CY7C1625KV18, CY7C1612KV18, and CY7C1614KV18 are 1.8V Synchronous Pipelined SRAMs, equipped with QDR-II architecture. QDR-II architecture consists of two separate ports to access the memory array. The read port has dedicated data outputs to support read operations and the write port has dedicated data inputs to support write operations. QDR-II architecture has separate data inputs and data outputs to completely eliminate the need to turn around the data bus that exists with common IO devices. Each port is accessed through a common address bus. The read address is latched on the rising edge of the K clock and the write address is latched on the rising edge of the $\overline{K}$ clock. Accesses to the QDR-II read and write ports are completely independent of one another. To maximize data throughput, both read and write ports are equipped with DDR interfaces. Each address location is associated with two 8-bit words (CY7C1610KV18), 9-bit words (CY7C1625KV18), 18-bit words (CY7C1612KV18), or 36-bit words (CY7C1614KV18) that burst sequentially into or out of the device. Because data is transferred into and out of the device on every rising edge of input clocks (K and $\overline{K}$ and C and $\overline{C}$), memory bandwidth is maximized while simplifying system design by eliminating bus turn arounds.

Port selects for each port enable depth expansion. Port selects allow each port to operate independently.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the C or $\overline{C}$ (or K or $\overline{K}$ in a single clock domain) input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

Selection Guide

Parameter		333 MHz	300 MHz	250 MHz	200 MHz	Unit
Maximum Operating Frequency		333	300	250	200	MHz
Maximum Operating Current	x8/x9	850	780	680	580	mA
	x18	870	810	700	590	
	x36	1060	980	850	710	

Overview

Figure 1. Logic Block Diagram (CY7C1610KV18)

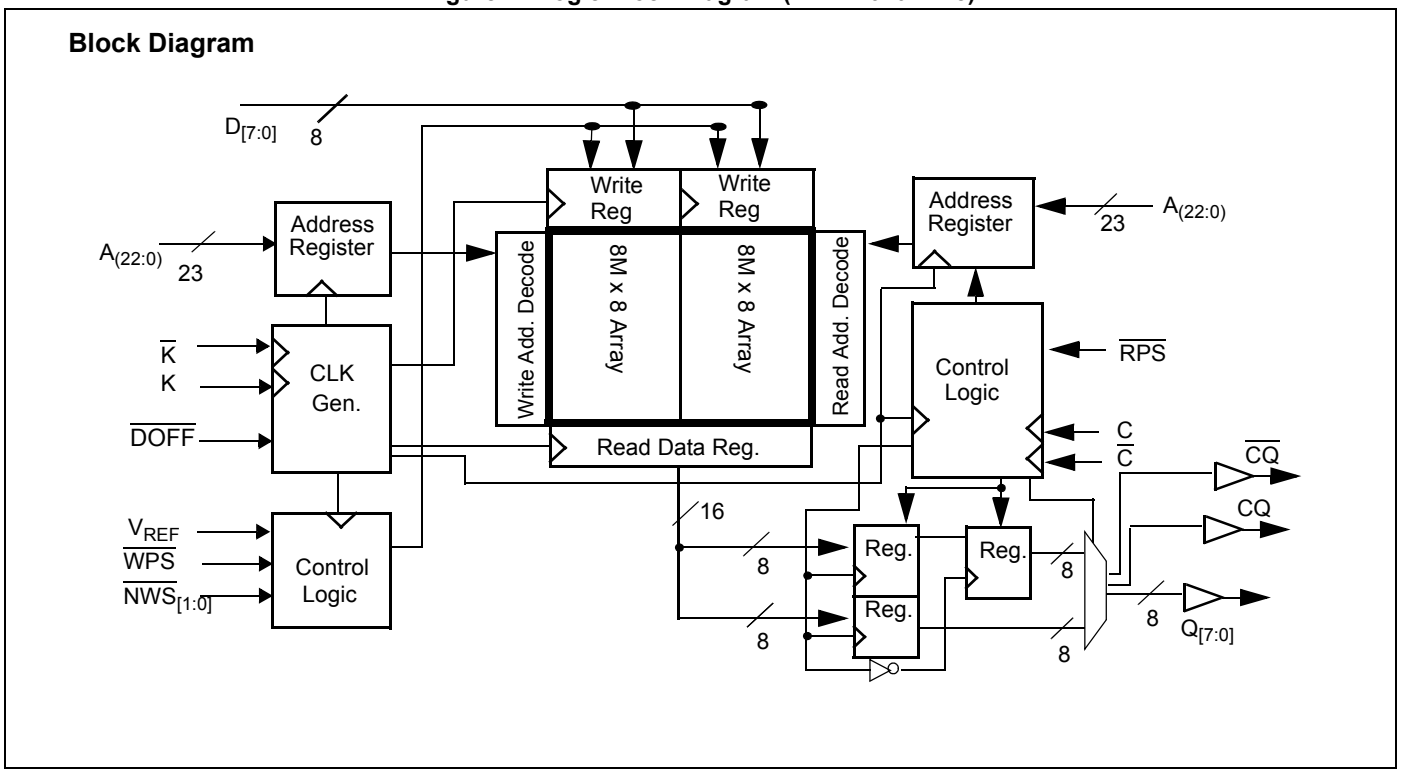


Figure 2. Logic Block Diagram (CY7C1625KV18)

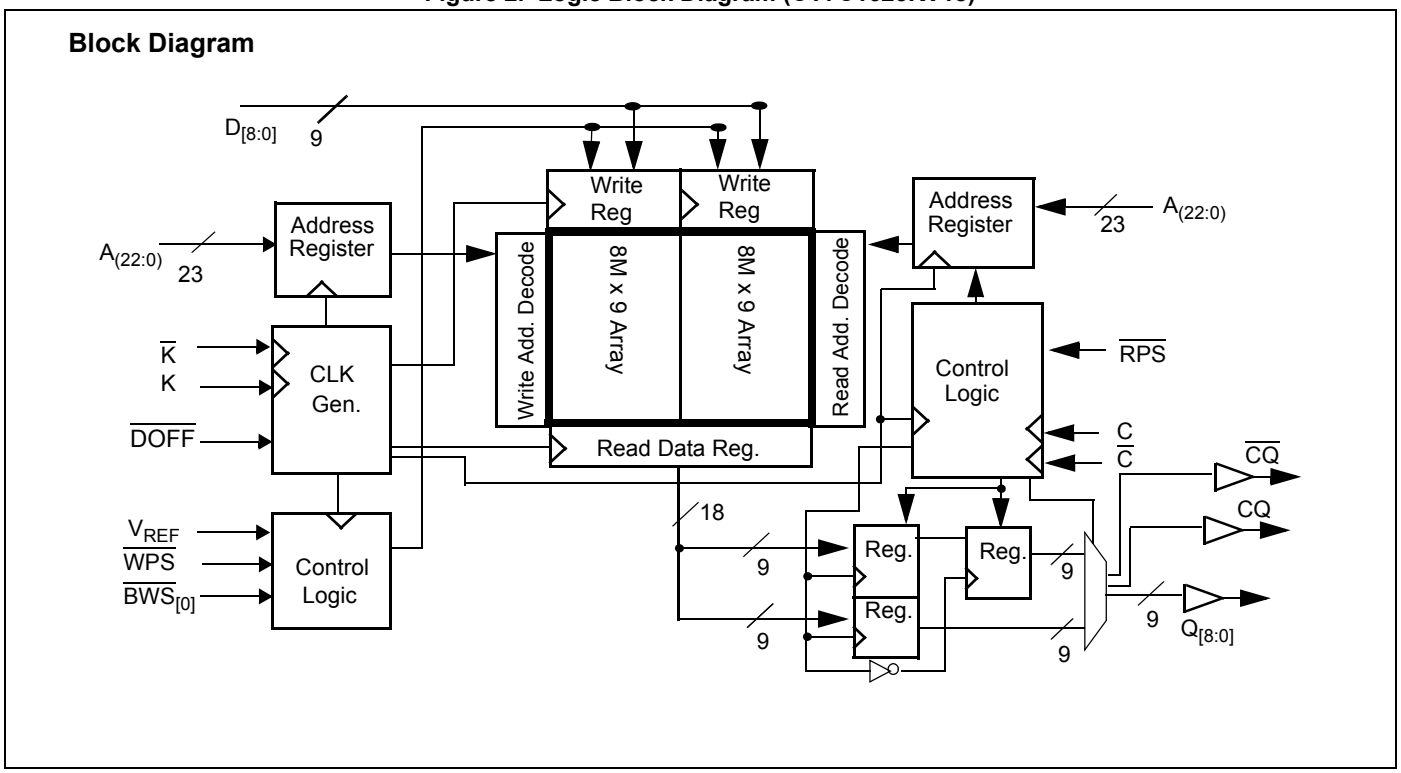


Figure 3. Logic Block Diagram (CY7C1612KV18)

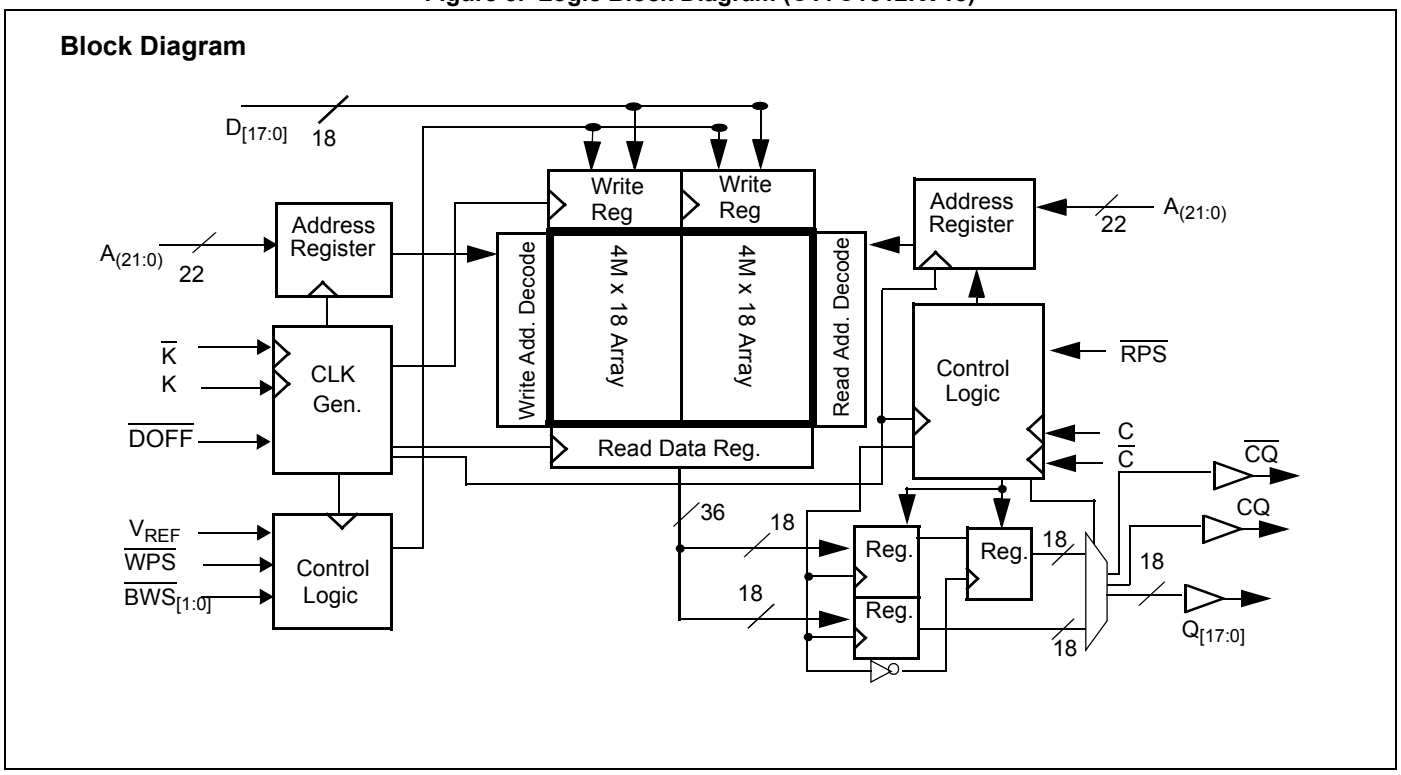
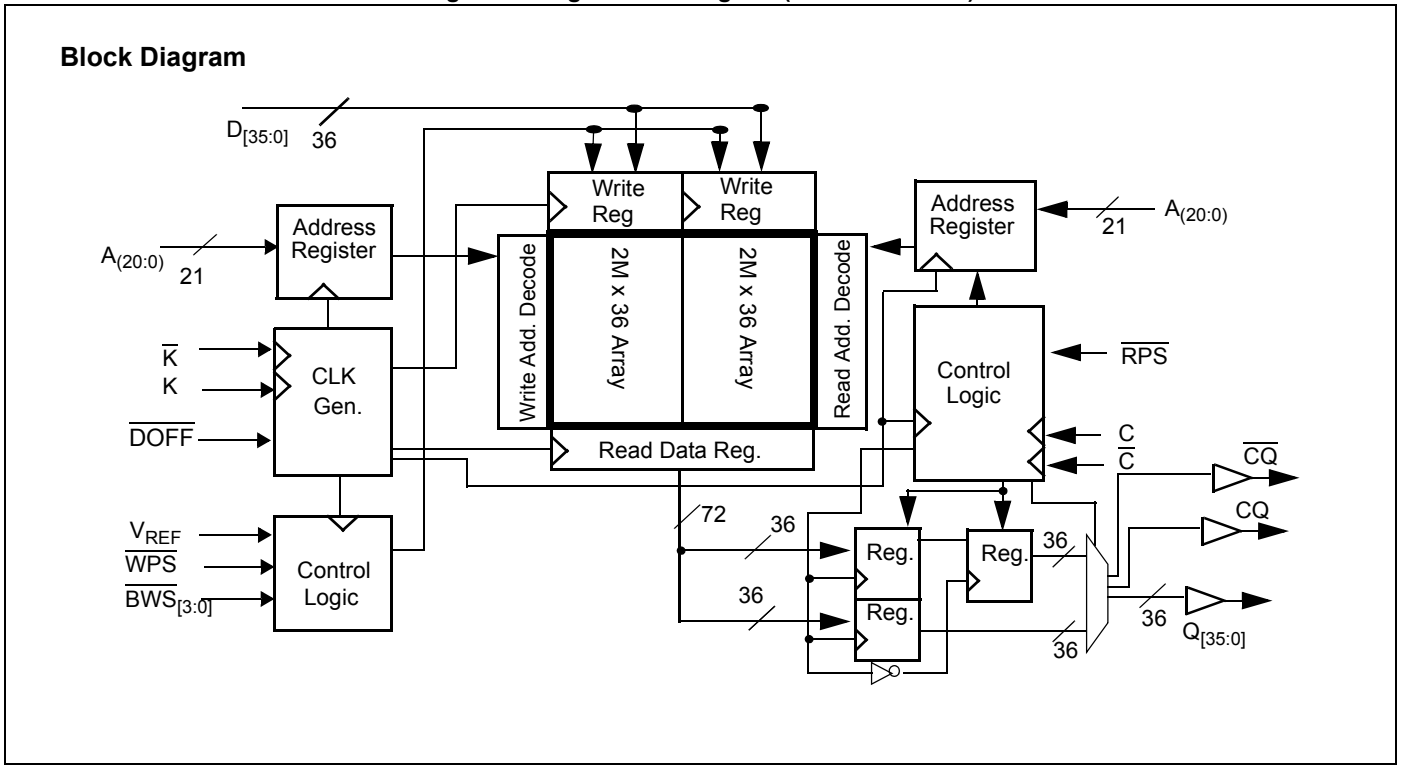


Figure 4. Logic Block Diagram (CY7C1614KV18)



Pin Configurations

165-Ball FBGA (15 x 17 x 1.4 mm) Pinout

Table 1. CY7C1610KV18 (16M x 8)[1]

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	A	A	$\overline{WPS}$	$\overline{NWS_1}$	$\overline{K}$	A	$\overline{RPS}$	A	A	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{NWS_0}$	A	NC	NC	Q3
C	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	D3
D	NC	D4	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D2	Q2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	D5	Q5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q1	D1
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	Q6	D6	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D0
N	NC	D7	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	Q7	A	A	C	A	A	NC	NC	NC
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Table 2. CY7C1625KV18 (16M x 9)[1]

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	A	A	$\overline{WPS}$	NC	$\overline{K}$	A	$\overline{RPS}$	A	A	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	Q4
C	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	D4
D	NC	D5	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D3	Q3
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	D6	Q6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q2	D2
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	Q7	D7	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D1
N	NC	D8	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	Q8	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Note
1. NC/288M is not connected to the die and can be tied to any voltage level.

165-Ball FBGA (15 x 17 x 1.4 mm) Pinout

Table 3. CY7C1612KV18 (8M x 18)[1]

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	A	A	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC/288M	$\overline{RPS}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	A	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Table 4. CY7C1614KV18 (4M x 36)[1]

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/288M	A	$\overline{WPS}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{RPS}$	A	A	CQ
B	Q27	Q18	D18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	A	A	A	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	VDDQ	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	A	A	A	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	A	A	C	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Ordering Information

Not all of the speed, package and temperature ranges are available. Contact your local sales representative or visit www.cypress.com for actual products offered.

Table 5. Ordering Information

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
333	CY7C1610KV18-333BZC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1625KV18-333BZC			
	CY7C1612KV18-333BZC			
	CY7C1614KV18-333BZC			
	CY7C1610KV18-333BZXC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1625KV18-333BZXC			
	CY7C1612KV18-333BZXC			
	CY7C1614KV18-333BZXC			
	CY7C1610KV18-333BZI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1625KV18-333BZI			
	CY7C1612KV18-333BZI			
	CY7C1614KV18-333BZI			
	CY7C1610KV18-333BZXI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1625KV18-333BZXI			
	CY7C1612KV18-300BZXI			
	CY7C1614KV18-333BZXI			
300	CY7C1610KV18-300BZC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1625KV18-300BZC			
	CY7C1612KV18-300BZC			
	CY7C1614KV18-300BZC			
	CY7C1610KV18-300BZXC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1625KV18-300BZXC			
	CY7C1612KV18-300BZXC			
	CY7C1614KV18-300BZXC			
	CY7C1610KV18-300BZI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1625KV18-300BZI			
	CY7C1612KV18-300BZI			
	CY7C1614KV18-300BZI			
	CY7C1610KV18-300BZXI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1625KV18-300BZXI			
	CY7C1612KV18-300BZXI			
	CY7C1614KV18-300BZXI			

Table 5. Ordering Information (continued)

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
250	CY7C1610KV18-250BZC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1625KV18-250BZC			
	CY7C1612KV18-250BZC			
	CY7C1614KV18-250BZC			
	CY7C1610KV18-250BZXC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1625KV18-250BZXC			
	CY7C1612KV18-250BZXC			
	CY7C1614KV18-250BZXC			
	CY7C1610KV18-250BZI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1625KV18-250BZI			
	CY7C1612KV18-250BZI			
	CY7C1614KV18-250BZI			
	CY7C1610KV18-250BZXI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1625KV18-250BZXI			
	CY7C1612KV18-250BZXI			
	CY7C1614KV18-250BZXI			
200	CY7C1610KV18-200BZC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1625KV18-200BZC			
	CY7C1612KV18-200BZC			
	CY7C1614KV18-200BZC			
	CY7C1610KV18-200BZXC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1625KV18-200BZXC			
	CY7C1612KV18-200BZXC			
	CY7C1614KV18-200BZXC			
	CY7C1610KV18-200BZI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1625KV18-200BZI			
	CY7C1612KV18-200BZI			
	CY7C1614KV18-200BZI			
	CY7C1610KV18-200BZXI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1625KV18-200BZXI			
	CY7C1612KV18-200BZXI			
	CY7C1614KV18-200BZXI			

Document History Page

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REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1184523	See ECN	VKN	New Data Sheet