NEC
ELECTRON DEVICE

DATA SHEET

MOS INTEGRATED CIRCUIT
μPD3725

5000-BIT × 3 CCD COLOR LINEAR IMAGE SENSOR

The μPD3725 is a high sensitivity 5000-bit × 3 color linear image sensor consisting of charge coupled devices (CCDs).

The μPD3725 is suitable for high resolution color image scanner and digital color copier.

FEATURES

- Valid photocell: 5000 bits × 3 (Red, Green, Blue)
- Distance of each line: 112 μm (8 lines)
- Color filter: Red, Green, Blue primary color
- Data rate: 16 MHz MAX.
- Input clock level: CMOS output when 5 V operation
- Power supply: +12 V

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD3725D-01	24-pin ceramic DIP (CERDIP)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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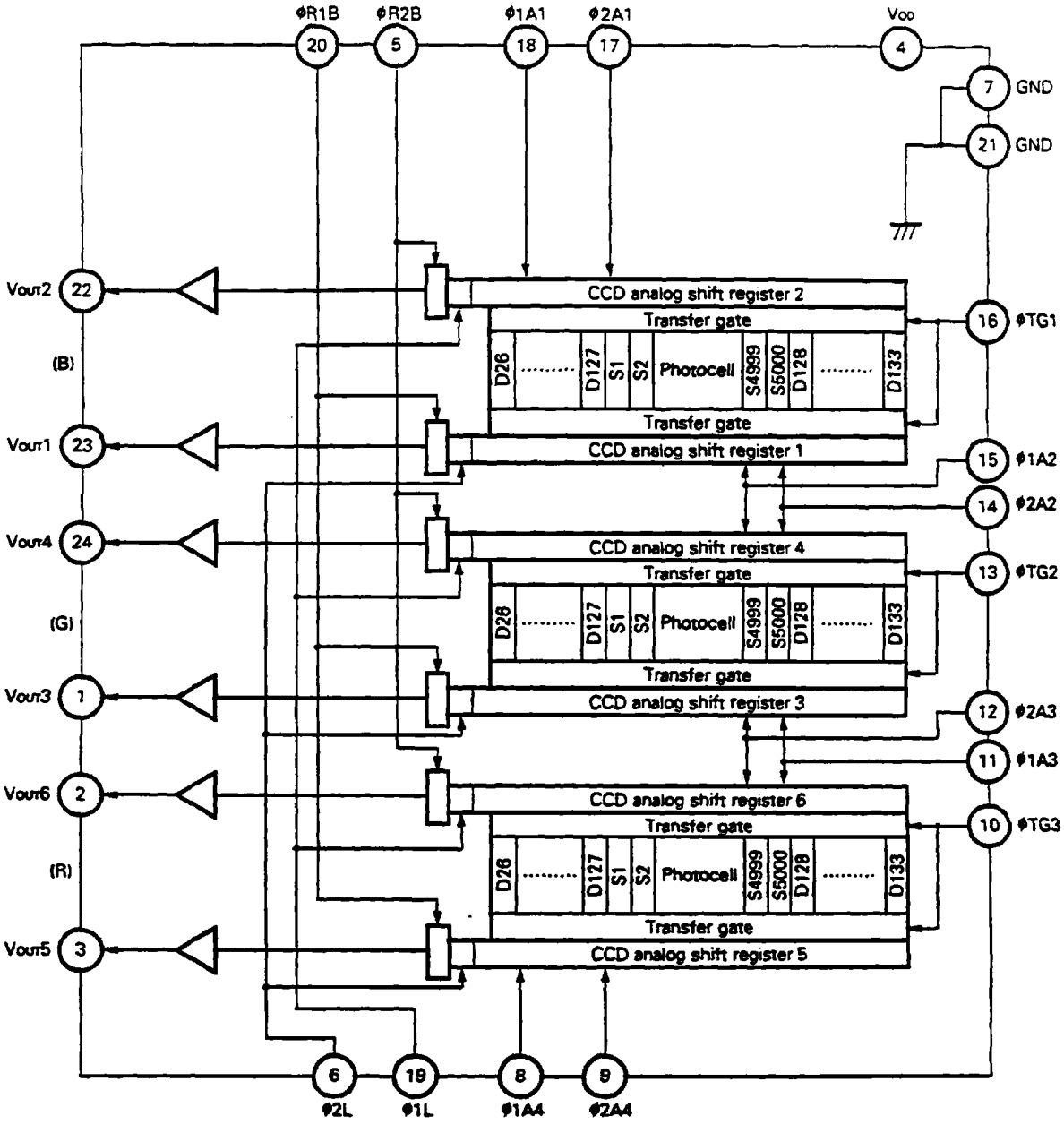
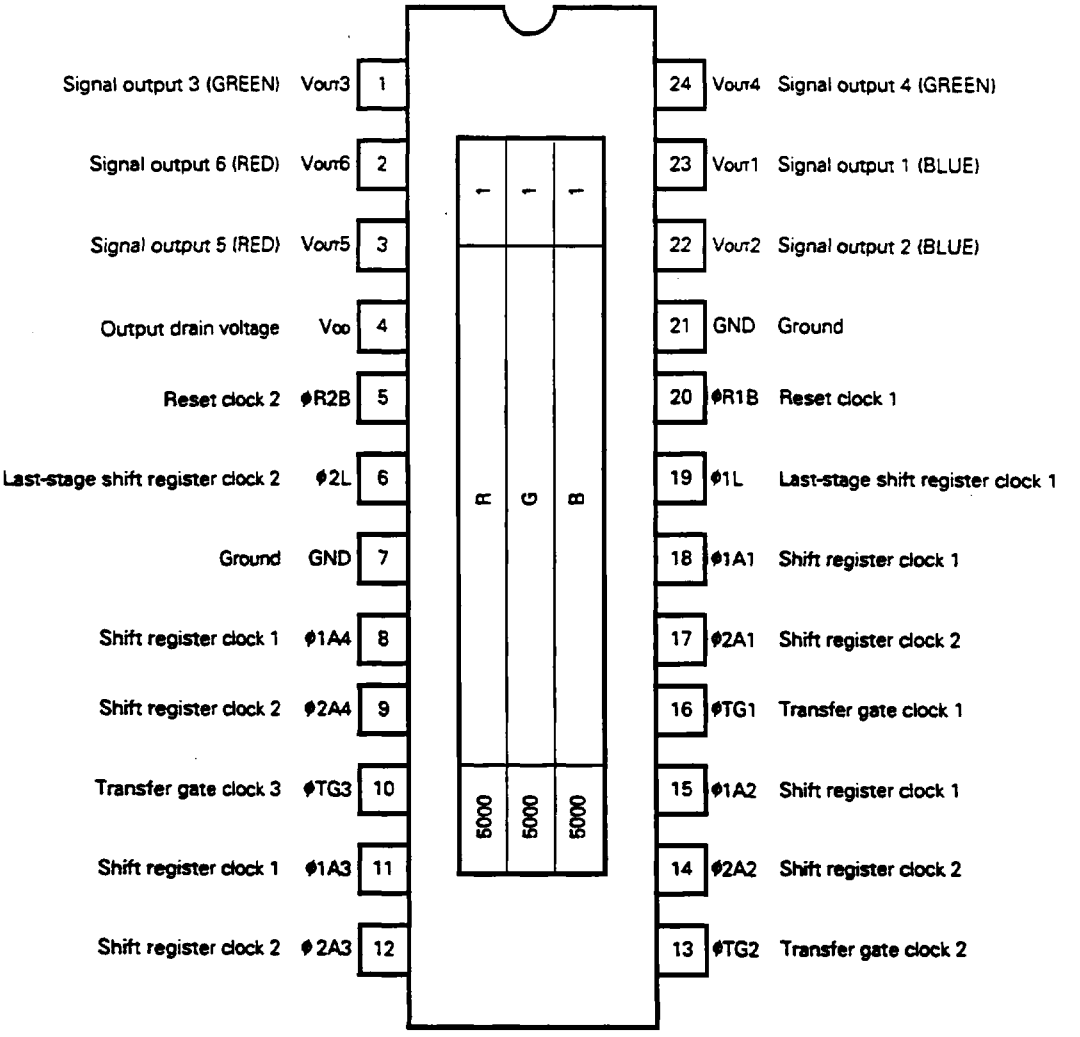
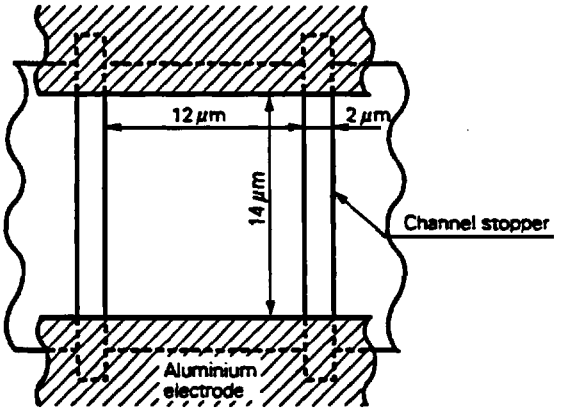
BLOCK DIAGRAM



PIN CONFIGURATIONS (Top View)



PHOTOCELL STRUCTURE DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	−0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	−0.3 to +15	V
Reset signal voltage	$V_{\phi RB}$	−0.3 to +15	V
Transfer gate signal voltage	$V_{\phi TG}$	−0.3 to +15	V
Operating ambient temperature	T_{opt}	−25 to +60	°C
Storage temperature	T_{stg}	−40 to +100	°C

RECOMMENDED OPERATING CONDITIONS (T_a = +25 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power supply	V_{OD}	11.4	12.0	12.6	V
Shift register clock signal high level	$V_{\phi 1H}$, $V_{\phi 2H}$	4.5	5	5.5	V
Shift register clock signal low level	$V_{\phi 1L}$, $V_{\phi 2L}$	−0.3	0	0.5	V
Reset signal high level	$V_{\phi RBH}$	4.5	5	5.5	V
Reset signal low level	$V_{\phi RBL}$	−0.3	0	0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	4.5	5	5.5	V
Transfer gate signal low level	$V_{\phi TGL}$	−0.3	0	0.5	V
Data rate	$2 \times f_{\phi R1}$	–	2	16	MHz

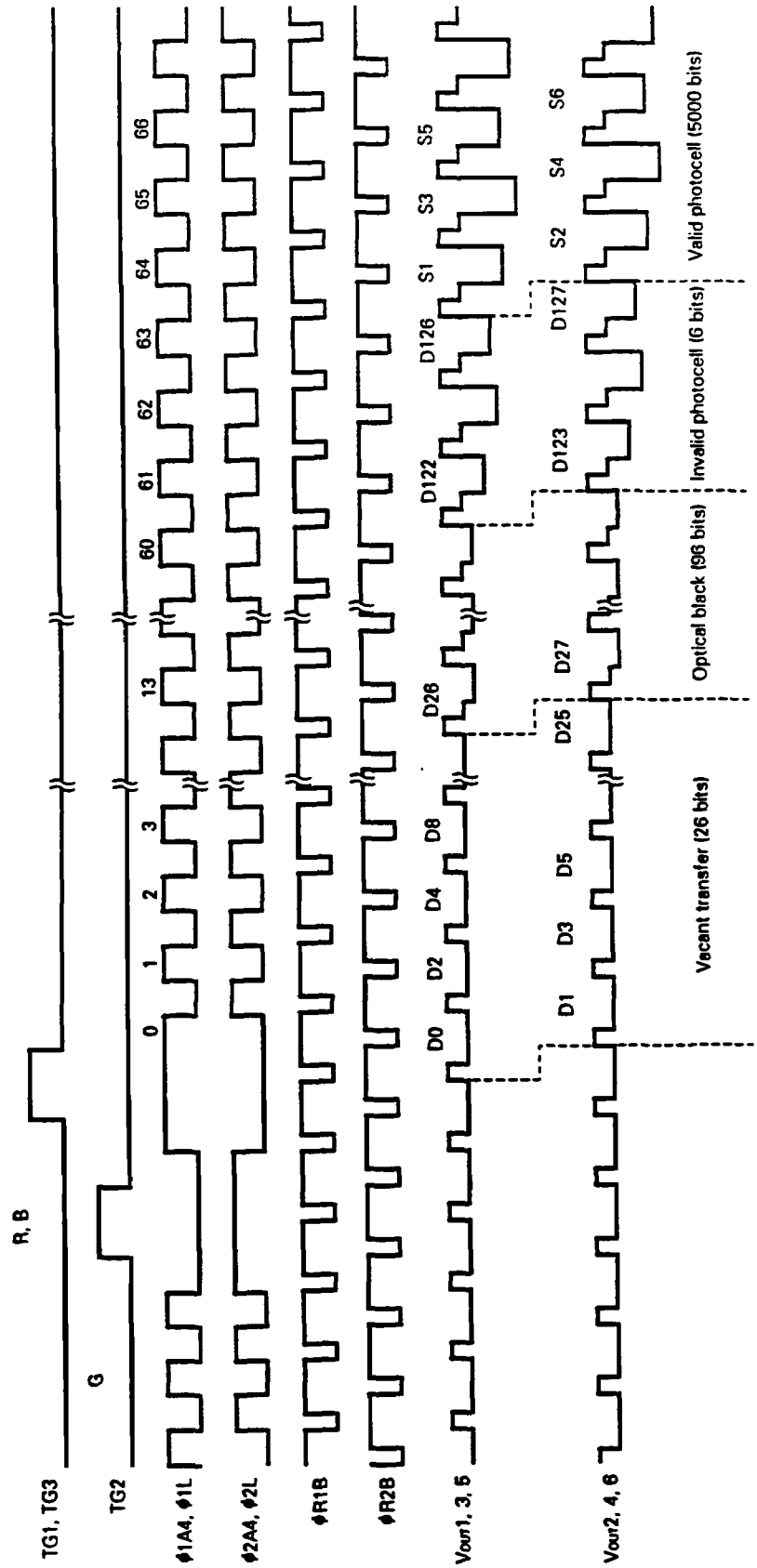
Remark $\phi 1$: $\phi 1A1$ to $\phi 1A4$, $\phi 1L$
$\phi 2$: $\phi 2A1$ to $\phi 2A4$, $\phi 2L$
ϕRB: $\phi R1B$ and $\phi R2B$

ELECTRICAL CHARACTERISTICS

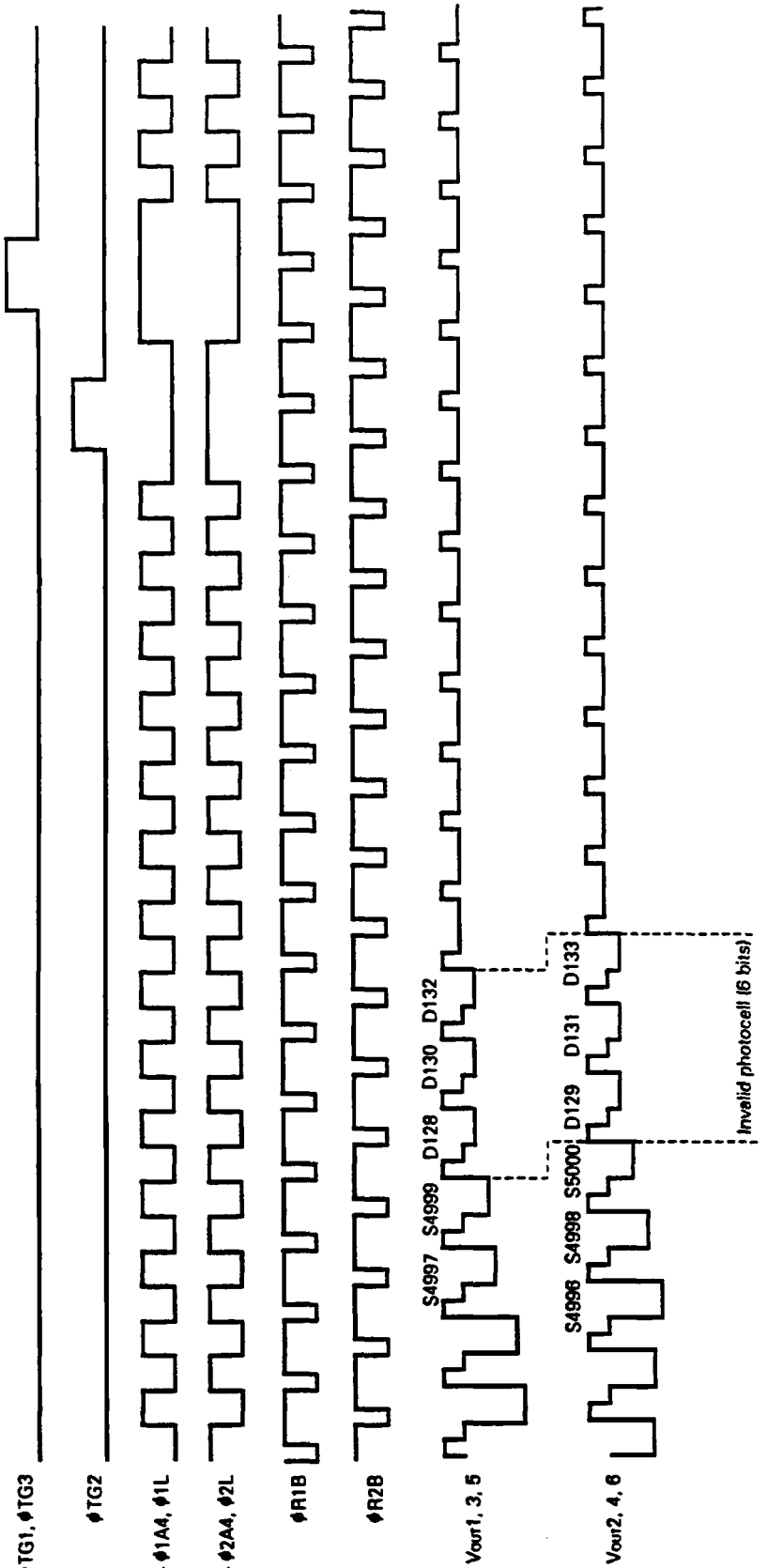
T_a = +25 °C, V_{OD} = 12 V, $f_{\phi R1}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms
light source; 3200 K halogen lamp +C500 (infrared cut filter), input signal clock = 5 V_{p-p}

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{SAT}		1.0	1.5	–	V
Saturation exposure	SE					
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV		±6	±15	%
Average dark signal	ADS			0.1	5	mV
Dark signal non-uniformity	DSNU			0.5	5	mV
Power consumption	Pw			300		mV
Output impedance	Zo			0.5	1	kΩ
Response	R_R			3.9		V/lx•s
	R_G			4.0		V/lx•s
	R_B			2.1		V/lx•s
Image lag	IL	V_{OUT} = 500 mV		2	5	%
Offset level	V_{OS}		5	7	9	V
Output fall delay time	t_d			40		ns
Transfer efficiency	TTE		92	98		%

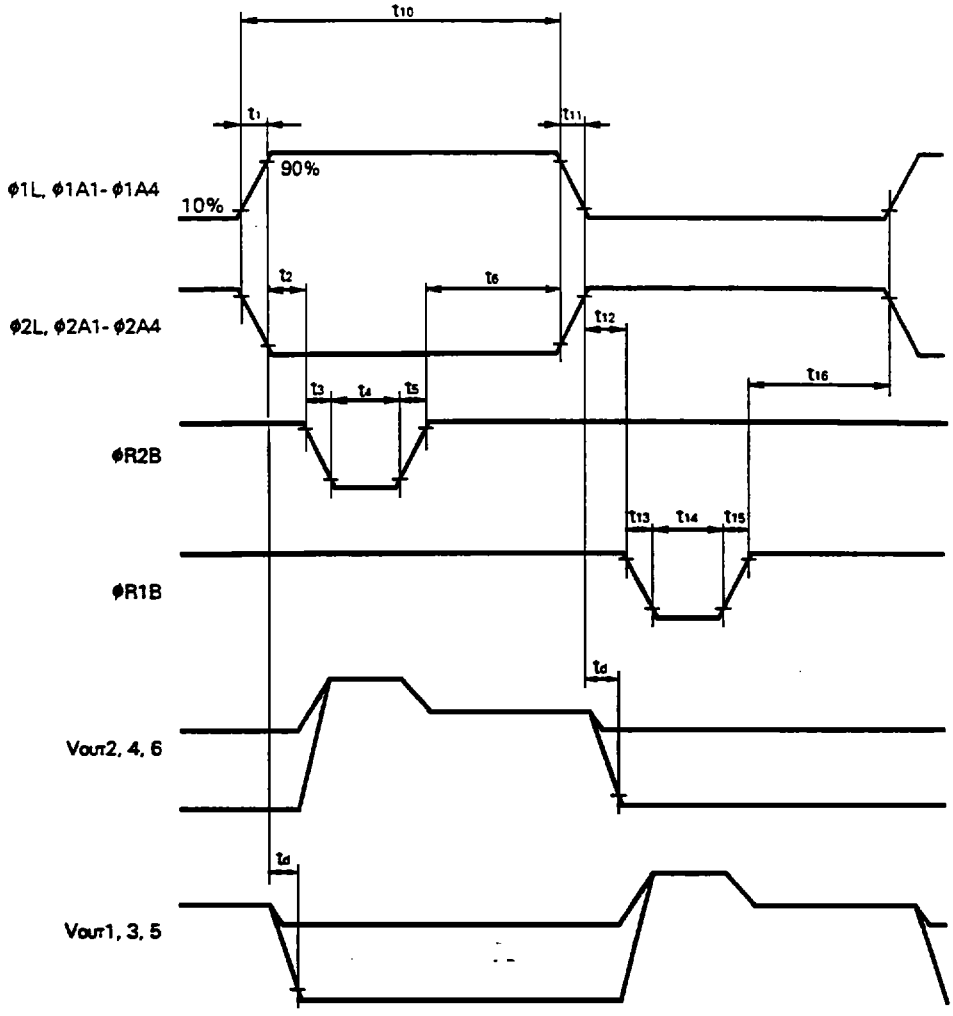
TIMING CHART 1



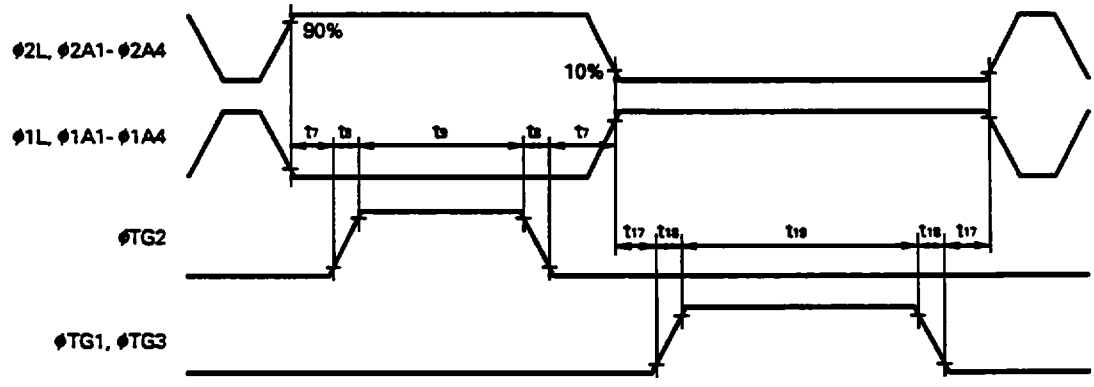
TIMING CHART 2



TIMING CHART 3



TIMING CHART 4

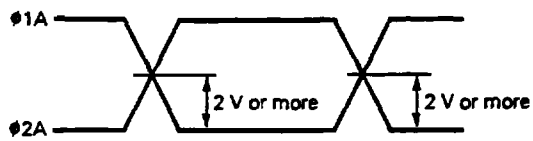


Recommended Timing

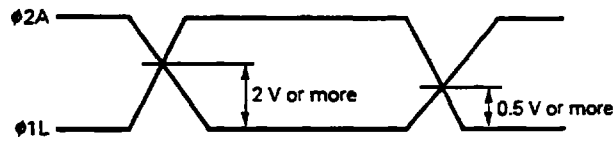
[Unit: ns]

Symbol	MIN.	TYP.	MAX.
t_1, t_{11}	0	10	–
t_2, t_{12}	0	50	–
t_3, t_5, t_{13}, t_{15}	0	5	–
t_4, t_{14}	20	50	–
t_6, t_{16}	20	50	–
t_7, t_{17}	20	50	–
t_8, t_{18}	0	50	–
t_9, t_{19}	1000	2000	–

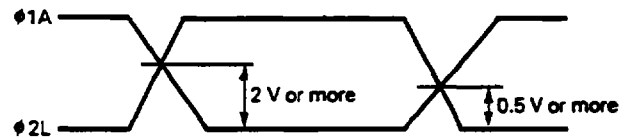
φ1A, φ2A cross points



φ1L, φ2A cross points



φ1A, φ2L cross points



Remark 1. Adjust input registance of each pin for cross points (φ1A, φ2A), (φ1L, φ2A) and (φ1A, φ2L)

2. φ1A: φ1A1, φ1A2, φ1A3
   φ2A: φ2A1, φ2A2, φ2A3

DEFINITIONS OF CHARACTERISTIC ITEMS

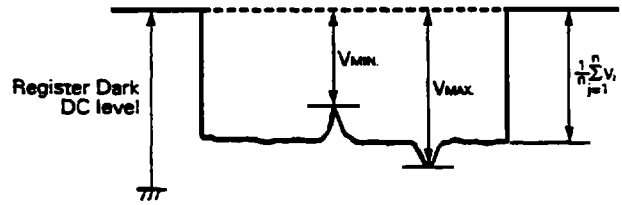
1. Saturation voltage: V_{SAT}
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE
   Product of intensity of illumination (lx) and storage time(s) when saturation of output voltage occurs.

3. Photo response non-uniformity: PRNU
   The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU(\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

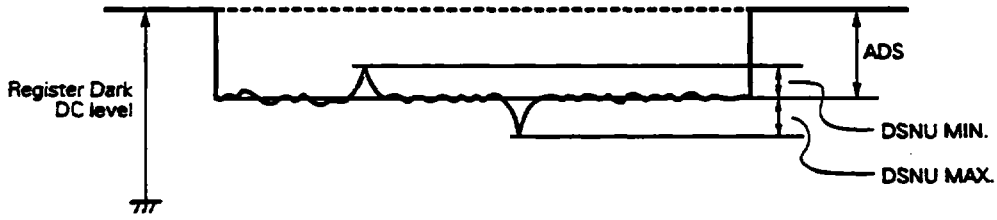
n: Number of valid bits
V_j: Output voltage of each bit



4. Average dark signal: ADS
   Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

5. Dark signal non-uniformity: DSNU
   The difference between peak or bottom output voltage in light shielding and ADS.

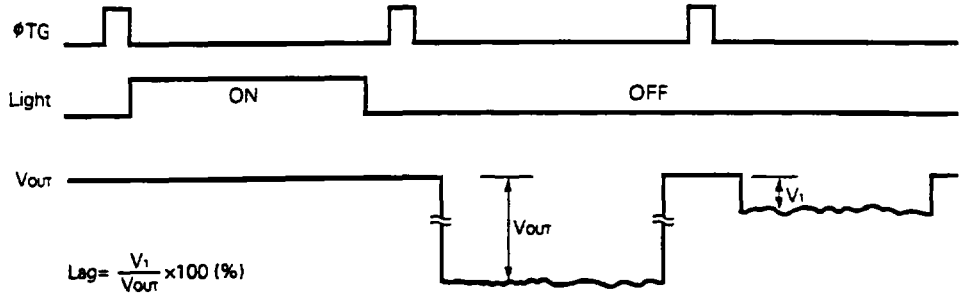


6. Output impedance: Zo
   Output pin impedance viewed from outside.

7. Response: R
   Output voltage divided by exposure (lx•s).
   Note that the response varies with the light source.

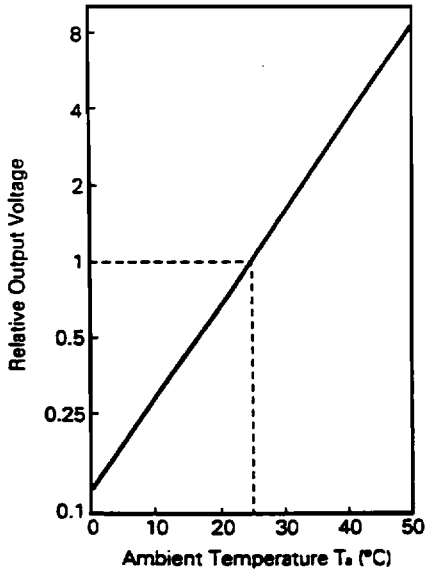
8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.

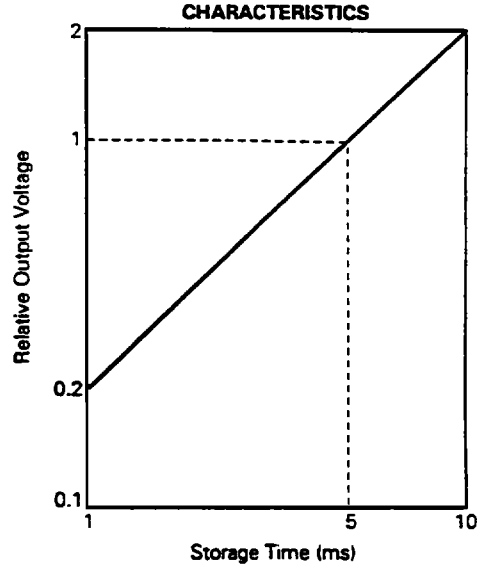


STANDARD CHARACTERISTIC CURVES (T_a = +25 °C)

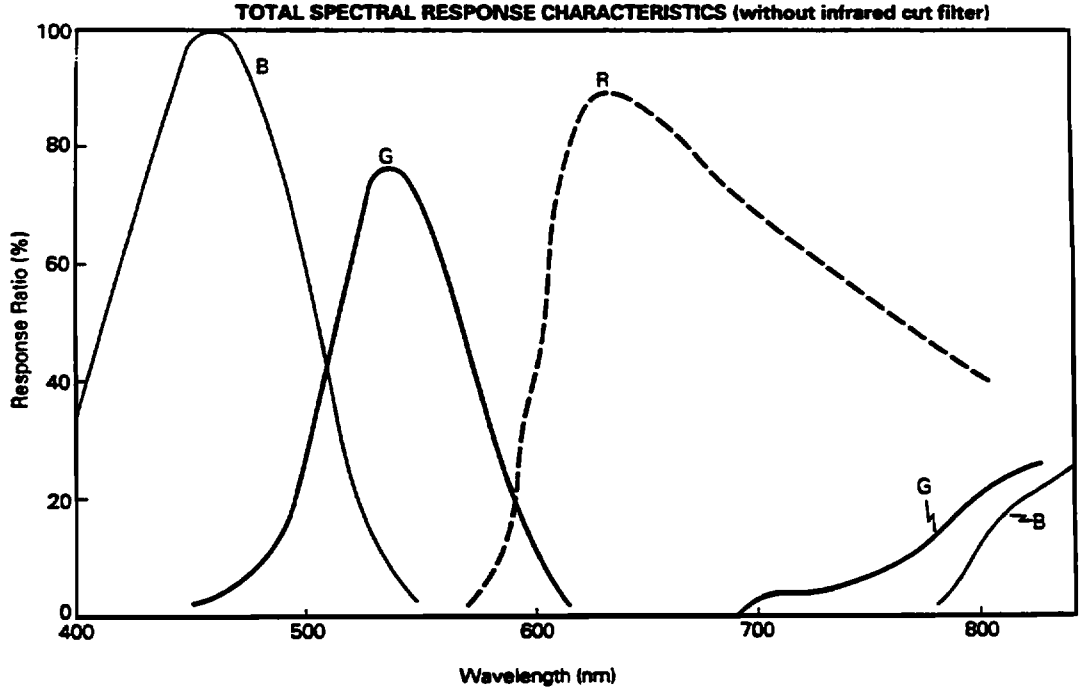
DARK OUTPUT TEMPERATURE CHARACTERISTICS



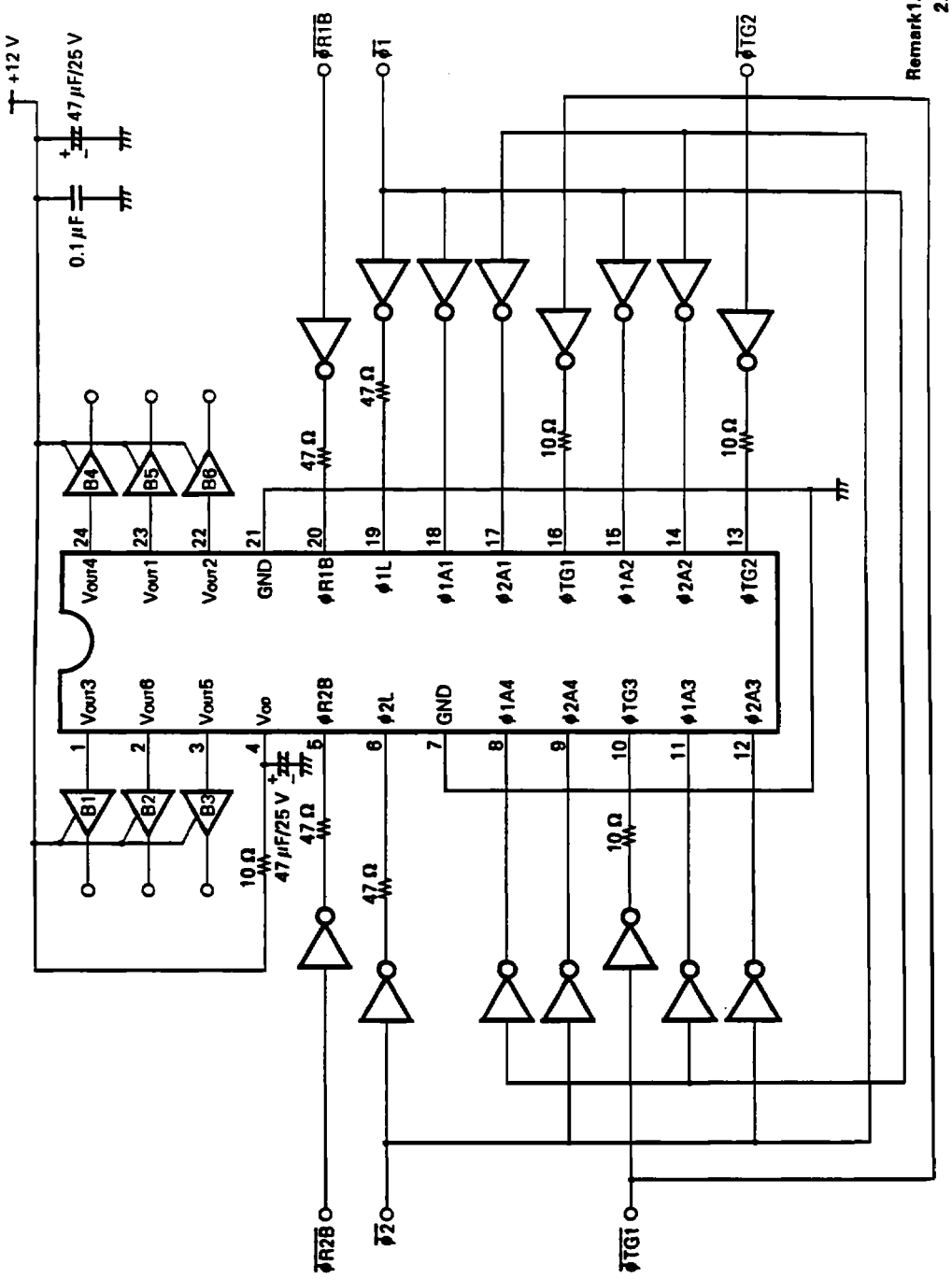
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTICS



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter)



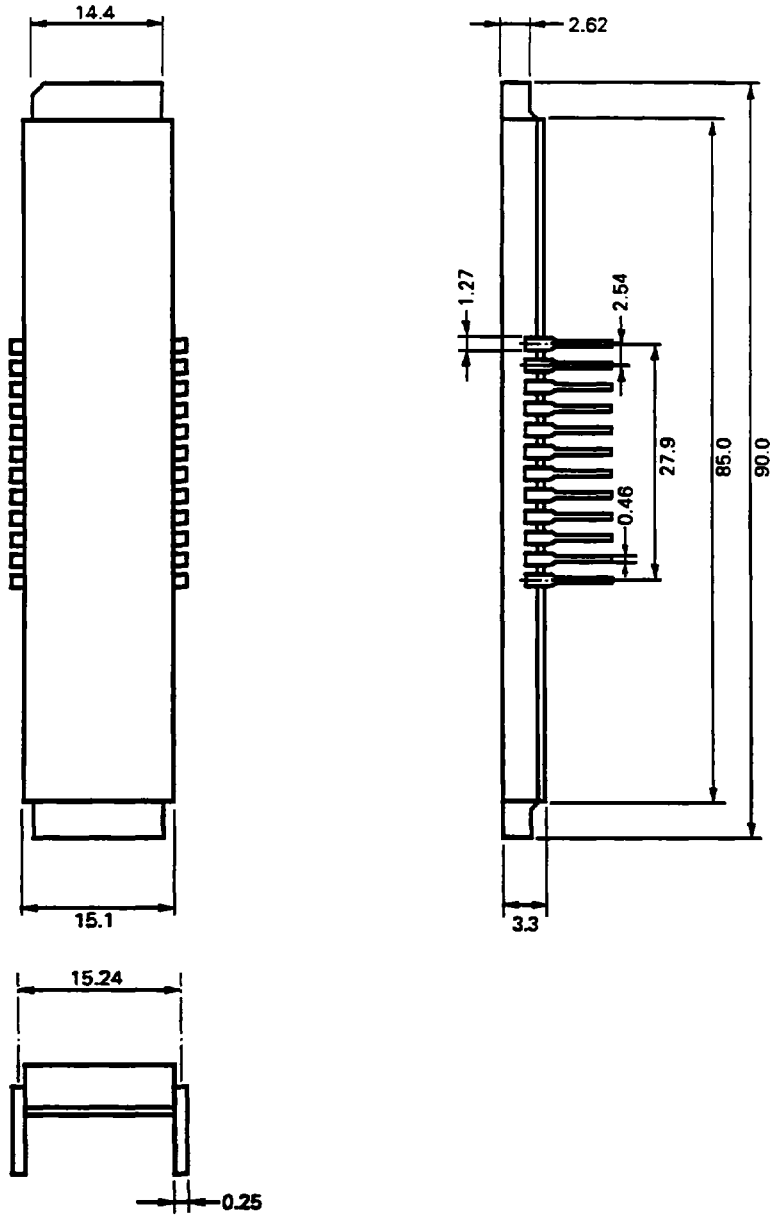
APPLICATION CIRCUIT



Remark 1. Inverter : μPD74HC4
2. B1 to B6 : Analog buffers

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

OUTLINE DIMENSIONS (Unit: mm) [Preliminary]



Remark Form of glass window is not defined yet.