NCP705

500 mA, Ultra-Low Quiescent Current, I_Q 13 μA, Ultra-Low Noise, LDO Voltage Regulator

Noise sensitive RF applications such as Power Amplifiers in satellite radios, infotainment equipment, and precision instrumentation require very clean power supplies. The NCP705 is 500 mA LDO that provides the engineer with a very stable, accurate voltage with ultra low noise and very high Power Supply Rejection Ratio (PSRR) suitable for RF applications. The device doesn't require any additional noise bypass capacitor to achieve ultra−low noise performance. In order to optimize performance for battery operated portable applications, the NCP705 employs dynamic Iq management for ultra−low quiescent current consumption at light−load conditions and great dynamic performance.

Features

- Operating Input Voltage Range: 2.5 V to 5.5 V
- Available in Fixed Voltage Options: 0.8 to 3.5 V Contact Factory for Other Voltage Options
- Ultra−Low Quiescent Current of Typ. 13 μA
- Ultra−Low Noise: 12 μV_{RMS} from 100 Hz to 100 kHz
- Very Low Dropout: 230 mV Typical at 500 mA
- ±2% Accuracy Over Load/Line/Temperature
- High PSRR: 71 dB at 1 kHz
- Internal Soft−Start to Limit the Turn−On Inrush Current
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μF Ceramic Output Capacitor
- Active Output Discharge for Fast Turn−Off
- These are Pb−Free Devices

Typical Applicaitons

- PDAs, Mobile Phones, GPS, Smartphones
- Wireless Handsets, Wireless LAN, Bluetooth, Zigbee
- Portable Medical Equipment
- Other Battery Powered Applications

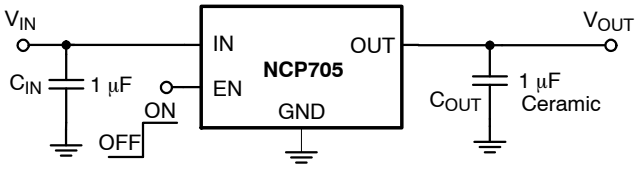


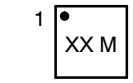
Figure 1. Typical Application Schematic

ON Semiconductor®

http://onsemi.com

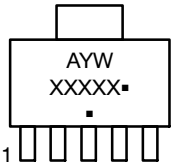
MARKING DIAGRAMS

WDFN6
CASE 511BR



XX = Specific Device Code
M = Date Code

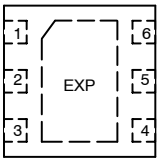
SOT223−6
CASE 419AY



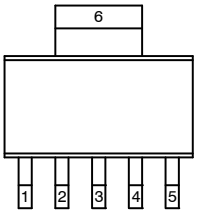
A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

PIN CONNECTIONS



WDFN6 2x2 mm
(Top View)



SOT223−6
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

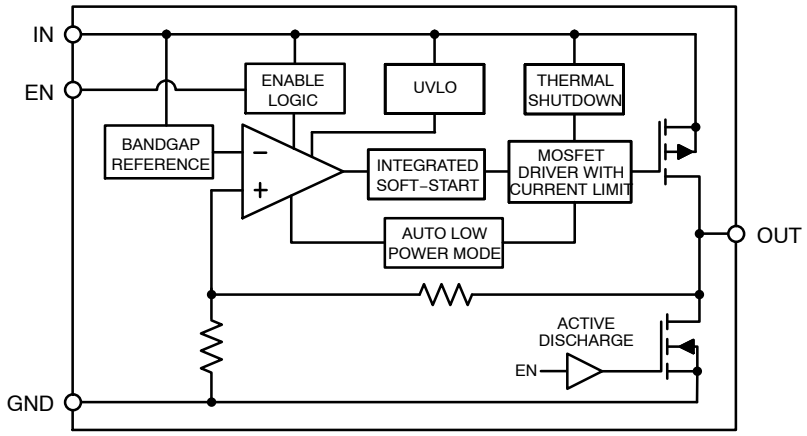


Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. WDFN6	Pin No. SOT223−6	Pin Name	Description
1	4	OUT	Regulated output voltage pin. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.
2	5	N/C	Not connected. This pin can be tied to ground to improve thermal dissipation.
3	3, 6	GND	Power supply ground. Expose pad must be tied with GND pin. Soldered to the copper plane allows for effective heat dissipation.
4	1	EN	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
5	−	N/C	Not connected. This pin can be tied to ground to improve thermal dissipation.
6	2	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6 V	V
Output Voltage	V_{OUT}	−0.3 V to V_{IN} + 0.3 V	V
Enable Input	V_{EN}	−0.3 V to V_{IN} + 0.3 V	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFN6 2x2 mm Thermal Resistance, Junction−to−Air Thermal Resistance Parameter, Junction−to−Board	 θ_{JA} Ψ_{JB}	 116.5 40	°C/W
Thermal Characteristics, SOT223−6 Thermal Resistance, Junction−to−Air Thermal Resistance Parameter, Junction−to−Board	 θ_{JA} Ψ_{JB}	 72 29	°C/W

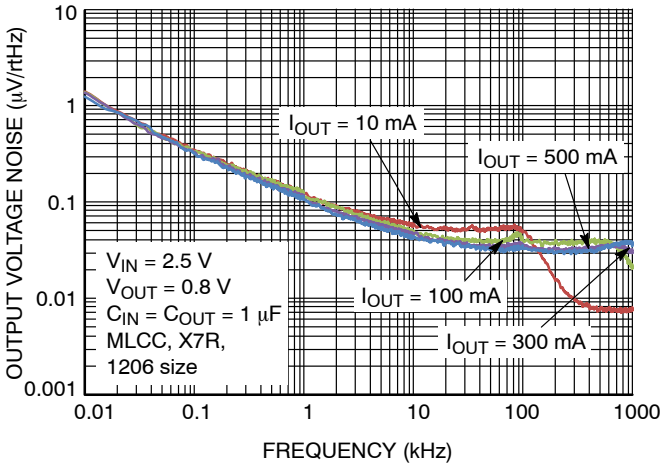
3. Single component mounted on 1 oz, FR 4 PCB with 645 mm^2 Cu area.

Table 4. ELECTRICAL CHARACTERISTICS
$-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 0.5$ V or 2.5 V, whichever is greater; V_{EN} = 0.9 V, I_{OUT} = 10 mA, $C_{IN} = C_{OUT}$ = 1 μF unless otherwise noted. Typical values are at T_J = +25°C. (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	2.5		5.5	V
Undervoltage Lock−out	V_{IN} rising		UVLO	1.2	1.6	1.9	V
Output Voltage Accuracy	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 0 − 500 mA		V_{OUT}	−2		+2	%
Line Regulation	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 4.5 V, I_{OUT} = 10 mA V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		Reg_{LINE}		550 750		μV/V
Load Regulation	I_{OUT} = 0 mA to 500 mA		Reg_{LOAD}		12		μV/mA
Load Transient	I_{OUT} = 1 mA to 500 mA or 500 mA to 1 mA in 1 μs, C_{OUT} = 1 μF		$Tran_{LOAD}$		±120		mV
Dropout Voltage (Note 5)	I_{OUT} = 500 mA, $V_{OUT(nom)}$ = 2.8 V		V_{DO}		230	350	mV
Output Current Limit	V_{OUT} = 90% $V_{OUT(nom)}$		I_{CL}	510	750	950	mA
Quiescent Current	I_{OUT} = 0 mA		I_Q		13	25	μA
Ground Current	I_{OUT} = 500 mA		I_{GND}		260		μA
Shutdown Current	V_{EN} ≤ 0.4 V, T_J = +25°C		I_{DIS}		0.12		μA
	V_{EN} ≤ 0 V, V_{IN} = 2.0 to 4.5 V, T_J = −40 to +85°C		I_{DIS}		0.55	2	μA
EN Pin Threshold Voltage High Threshold Low Threshold	 V_{EN} Voltage increasing V_{EN} Voltage decreasing		 V_{EN_HI} V_{EN_LO}	 0.9		 0.4	V
EN Pin Input Current	V_{EN} = 5.5 V		I_{EN}		100	500	nA
Turn−On Time	C_{OUT} = 1.0 μF, from assertion EN pin to 98% $V_{OUT(nom)}$		t_{ON}		150		μs
Power Supply Rejection Ratio	V_{IN} = 3.8 V, V_{OUT} = 2.8 V I_{OUT} = 500 mA	f = 100 Hz f = 1 kHz f = 10 kHz	PSRR		73 71 56		dB
Output Noise Voltage	V_{OUT} = 2.5 V, V_{IN} = 3.5 V, I_{OUT} = 500 mA f = 100 Hz to 100 kHz		V_N		12		μV_{rms}
Thermal Shutdown Temperature	Temperature increasing from T_J = +25°C		T_{SD}		160		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}	−	20	−	°C

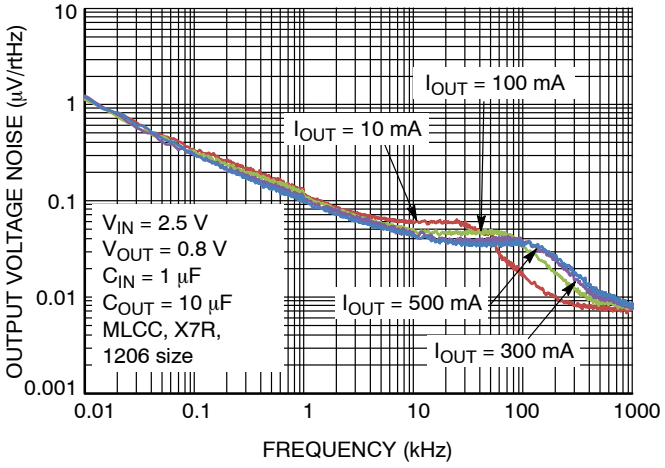
4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when V_{OUT} falls 100 mV below the regulated voltage at $V_{IN} = V_{OUT(NOM)} + 0.5$ V.

TYPICAL CHARACTERISTICS



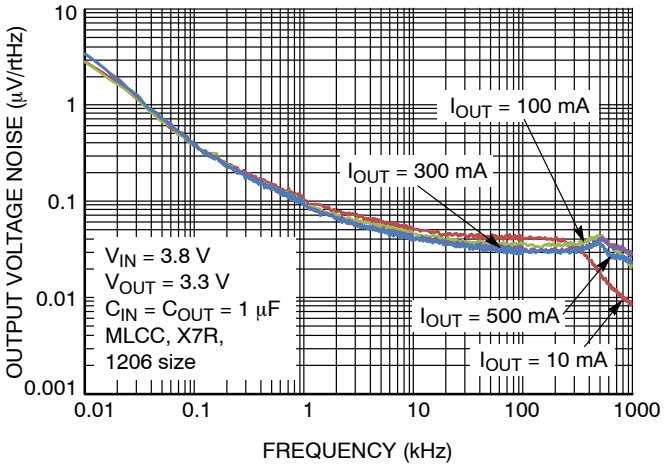
I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
10 mA	19.06	18.21
100 mA	15.99	15.04
300 mA	14.42	13.39
500 mA	13.70	12.60

Figure 3. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 1 μF



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
10 mA	16.17	15.28
100 mA	16.41	15.65
300 mA	14.94	14.10
500 mA	14.08	13.11

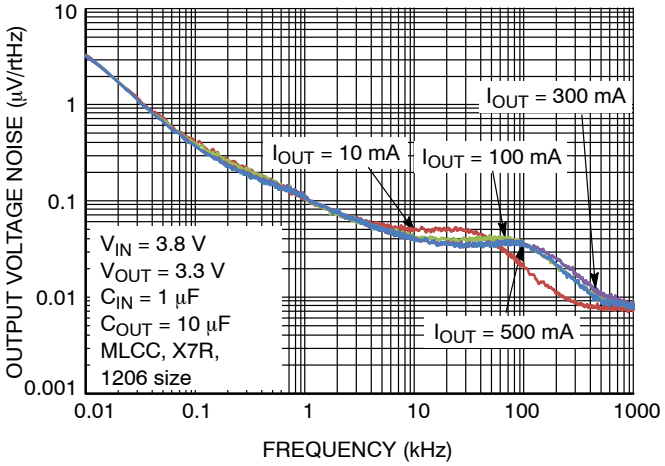
Figure 4. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 10 μF



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
10 mA	18.12	15.39
100 mA	16.42	13.50
300 mA	16.35	12.47
500 mA	16.00	12.10

Figure 5. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 1 μF

TYPICAL CHARACTERISTICS



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	17.35	14.07
100 mA	17.43	14.29
300 mA	16.55	13.33
500 mA	16.48	13.20

Figure 6. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 10 μF

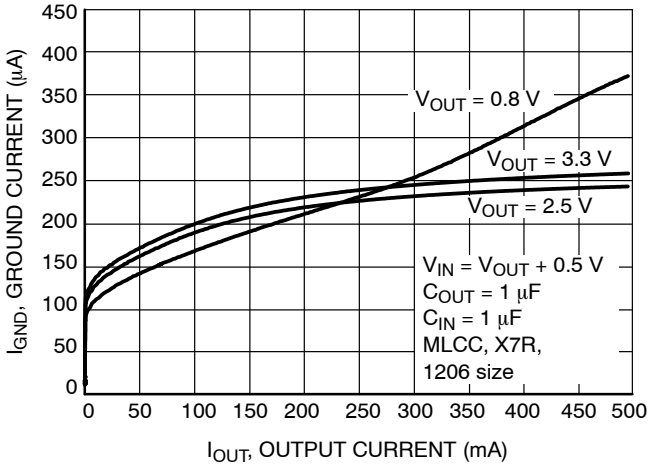


Figure 7. Ground Current vs. Output Current

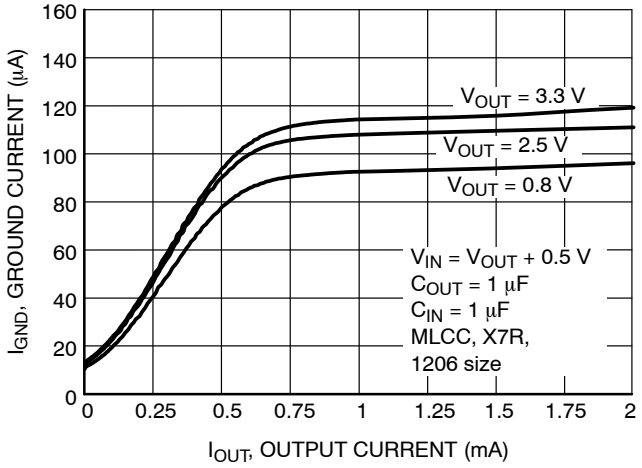


Figure 8. Ground Current vs. Output Current from 0 mA to 2 mA

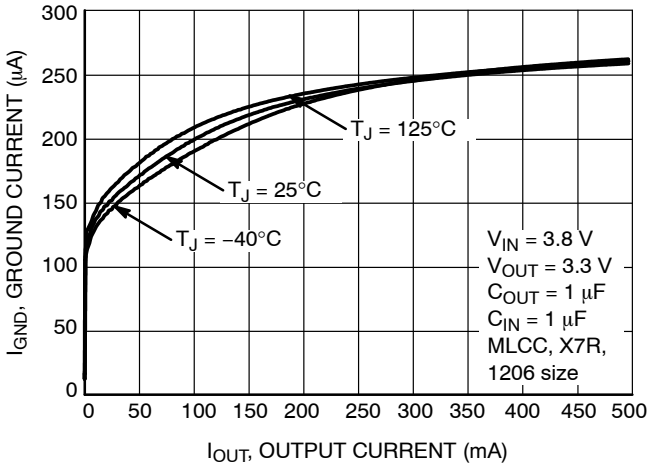


Figure 9. Ground Current vs. Output Current at Temperatures

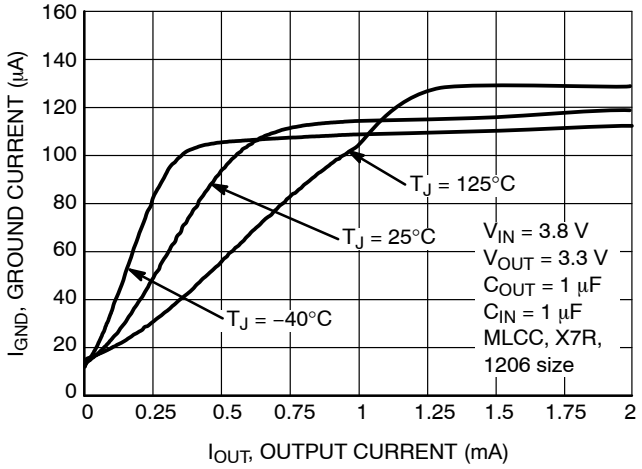


Figure 10. Ground Current vs. Output Current 0 mA to 2 mA at Temperature

TYPICAL CHARACTERISTICS

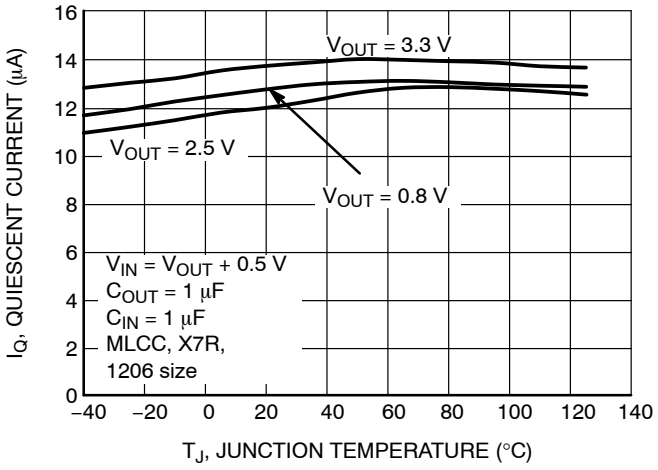


Figure 11. Quiescent Current vs. Temperature

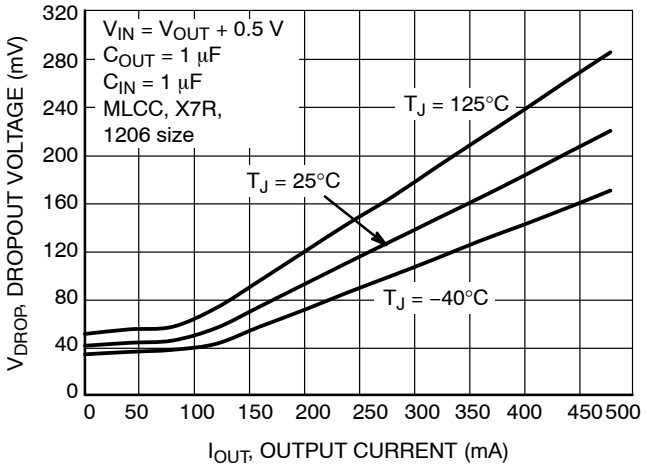


Figure 12. Dropout Voltage vs. Output Current at Temperature (2.5 V)

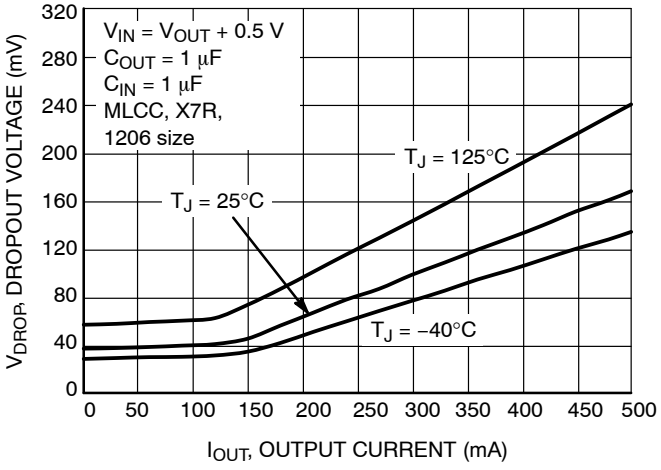


Figure 13. Dropout Voltage vs. Output Current at Temperatures (3.3 V)

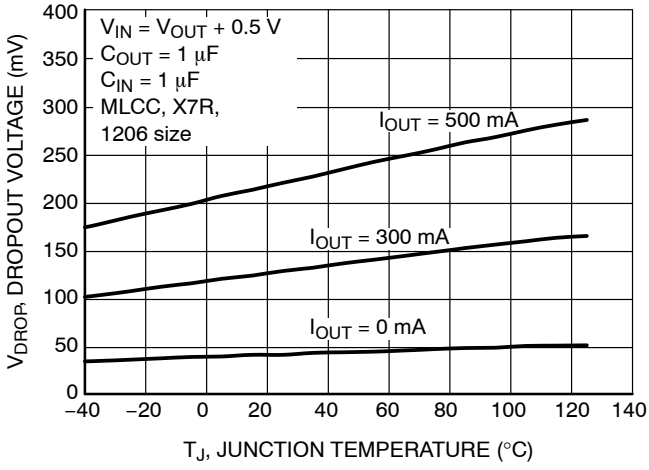


Figure 14. Dropout Voltage vs. Temperature (2.5 V)

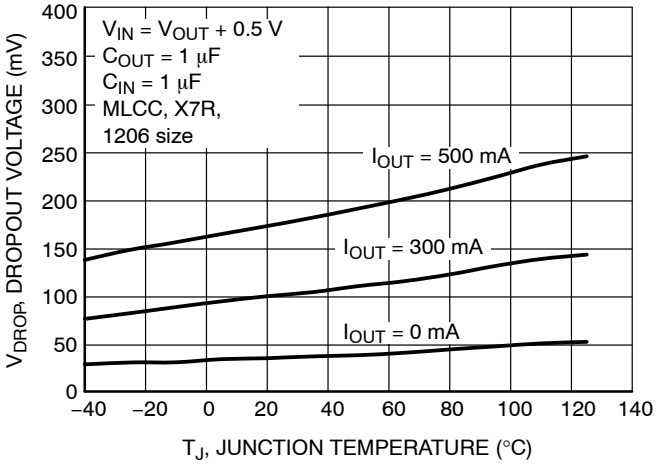


Figure 15. Dropout Voltage vs. Temperature, (3.3 V)

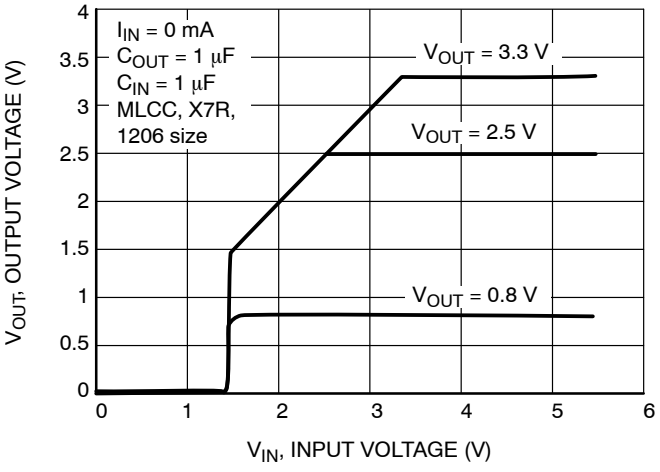


Figure 16. Input Voltage vs. Output Voltage

TYPICAL CHARACTERISTICS

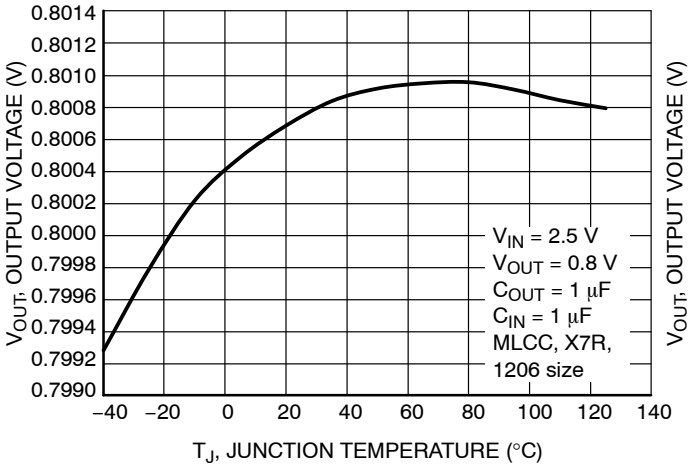


Figure 17. Output Voltage vs. Temperature, (0.8 V)

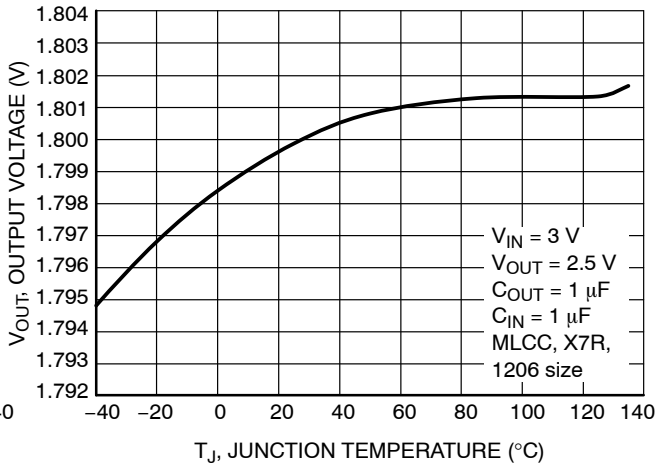


Figure 18. Output Voltage vs. Temperature, (2.5 V)

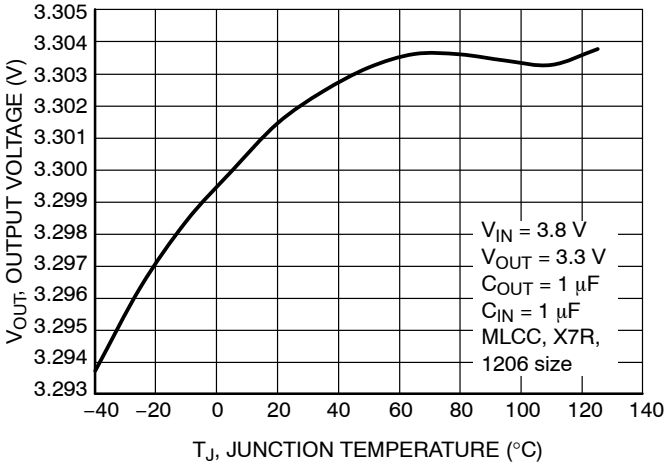


Figure 19. Output Voltage vs. Temperature, (3.3 V)

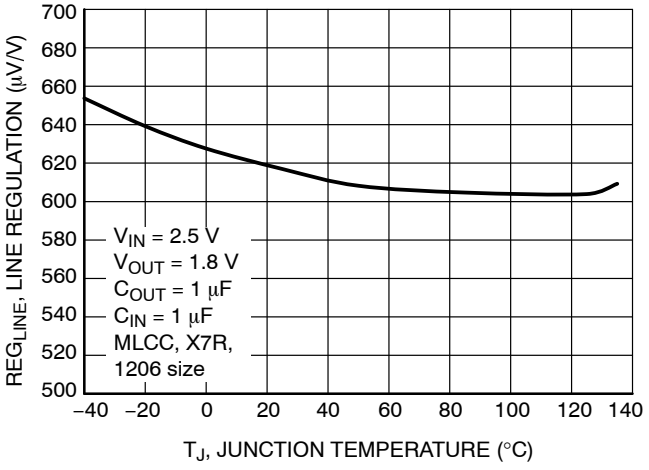


Figure 20. Line Regulation vs. Temperature, (1.8 V)

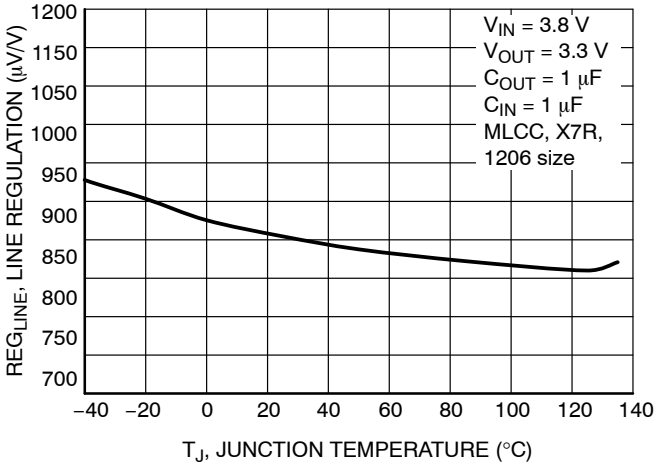


Figure 21. Line Regulation vs. Temperature, (3.3 V)

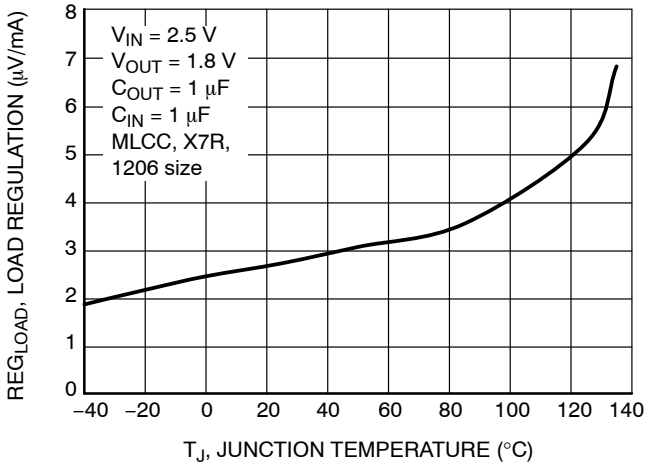


Figure 22. Load Regulation vs. Temperature, (1.8 V)

TYPICAL CHARACTERISTICS

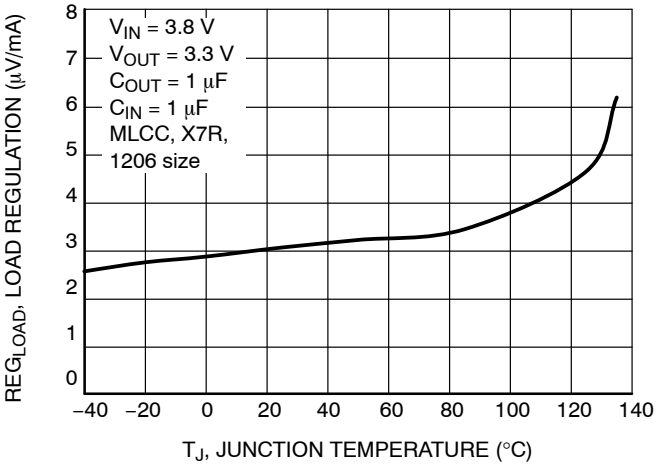


Figure 23. Load Regulation vs. Temperature, (3.3 V)

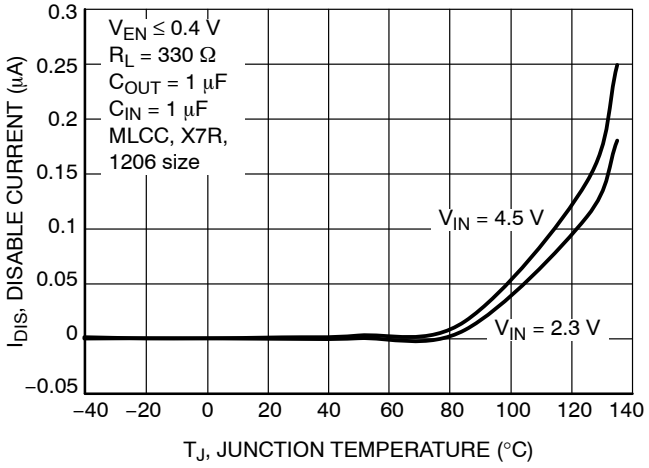


Figure 24. Disable Current vs. Temperature

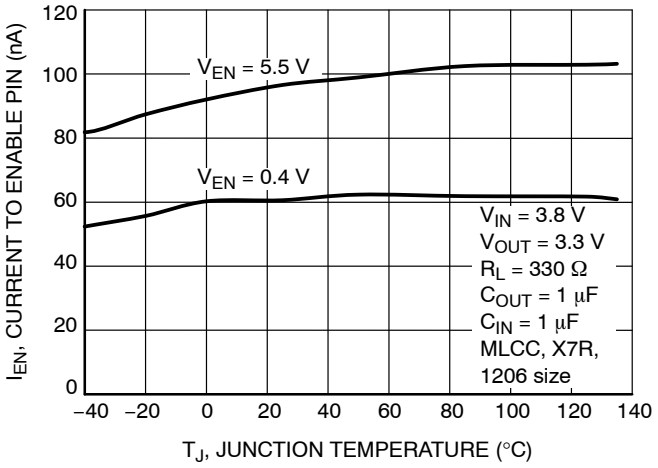


Figure 25. Enable Current vs. Temperature

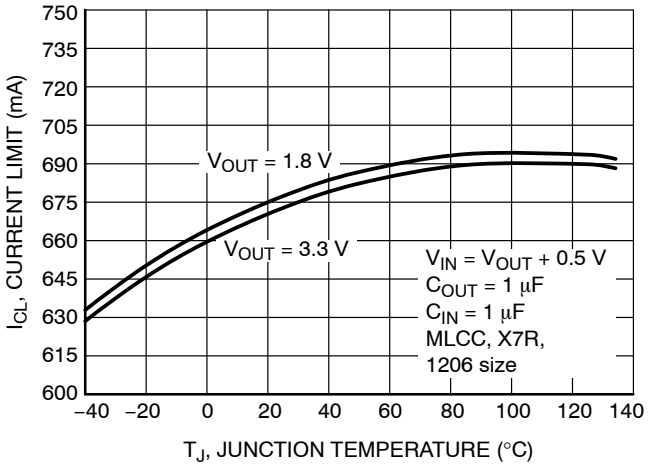


Figure 26. Current Limit vs. Temperature

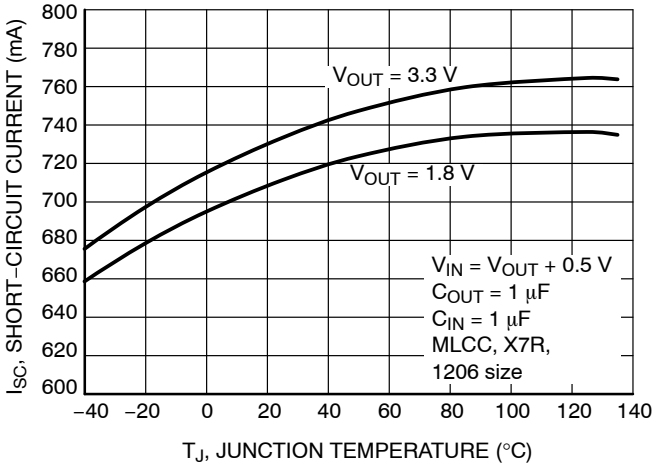


Figure 27. Short−Circuit vs. Temperature

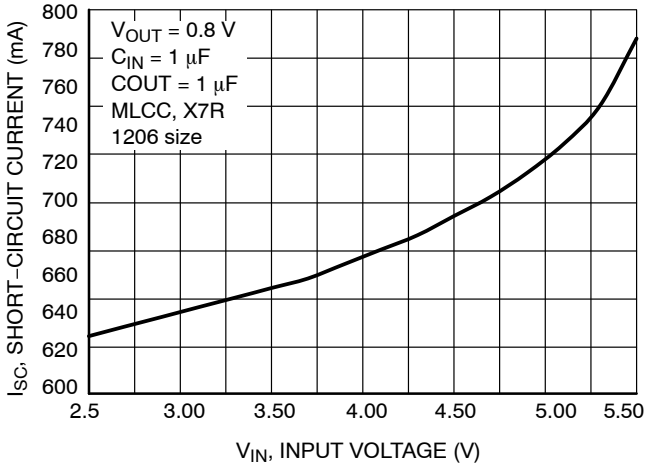


Figure 28. Short−Circuit Current vs. Temperature

TYPICAL CHARACTERISTICS

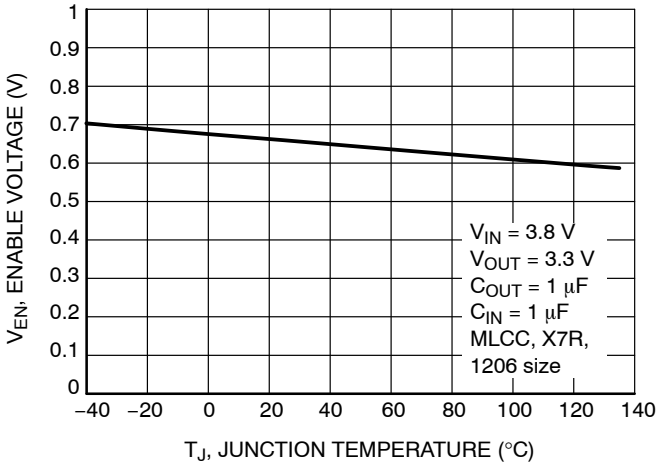


Figure 29. Enable Threshold (High)

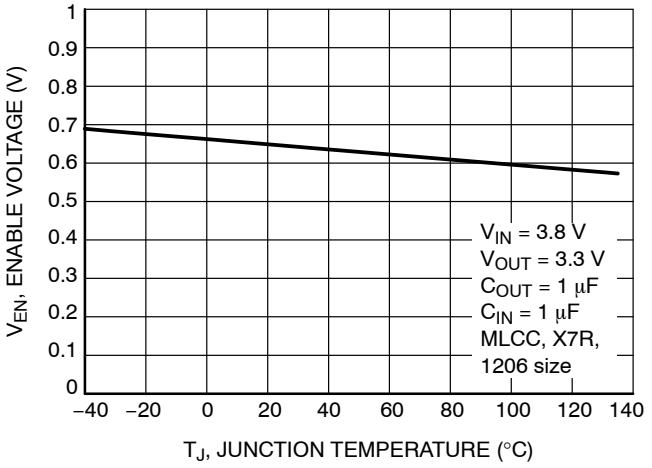


Figure 30. Enable Threshold (Low)

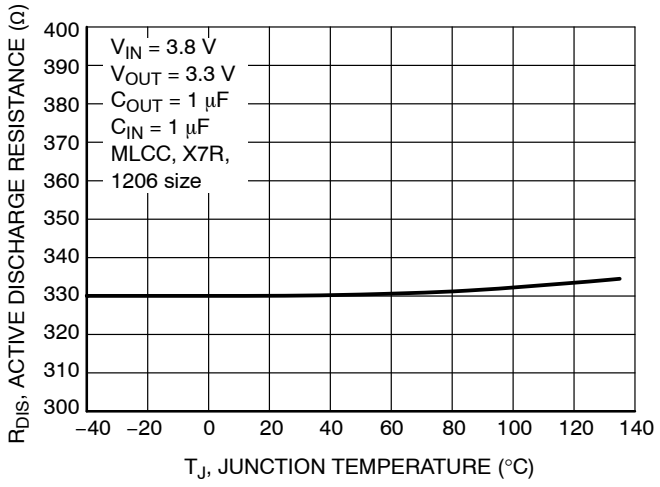


Figure 31. Discharge Resistance vs. Temperature

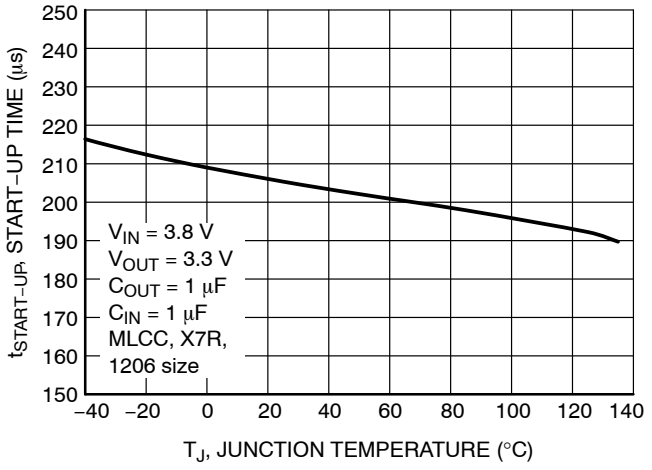


Figure 32. Start−up Time vs. Temperature

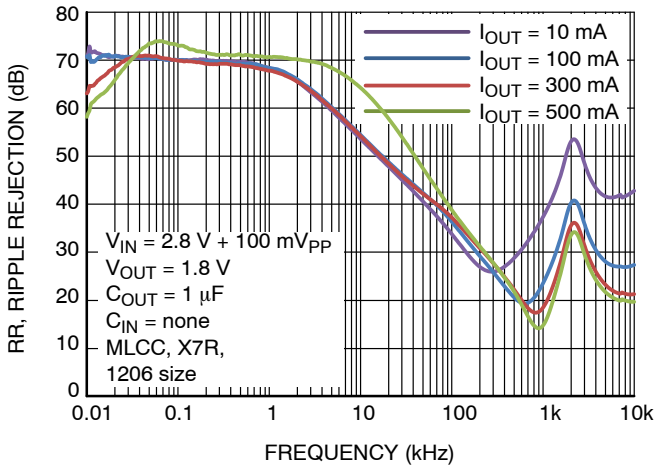


Figure 33. Power Supply Rejection Ratio, V_{OUT} = 1.8 V

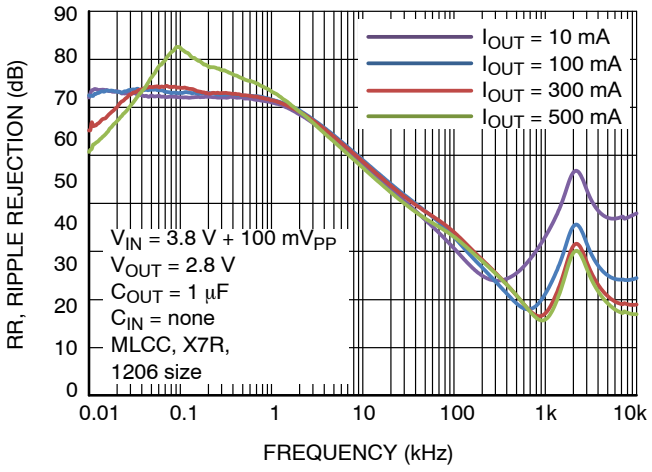


Figure 34. Power Supply Rejection Ratio, V_{OUT} = 2.8 V

TYPICAL CHARACTERISTICS

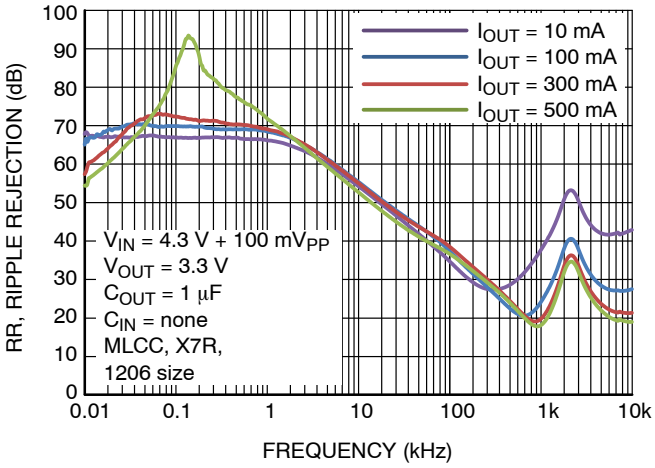


Figure 35. Power Supply Rejection Ratio, V_{OUT} = 3.3 V

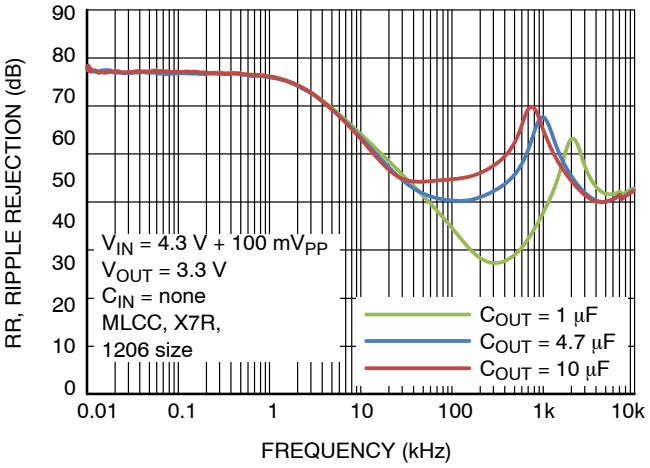


Figure 36. Power Supply Rejection Ratio, V_{OUT} = 3.3 V, I_{OUT} = 10 mA – Different C_{OUT}

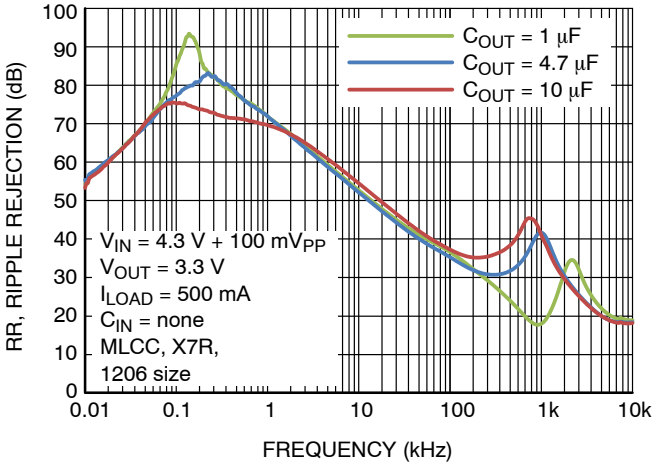


Figure 37. Power Supply Rejection Ratio, V_{OUT} = 3.3 V, I_{OUT} = 500 mA – Different C_{OUT}

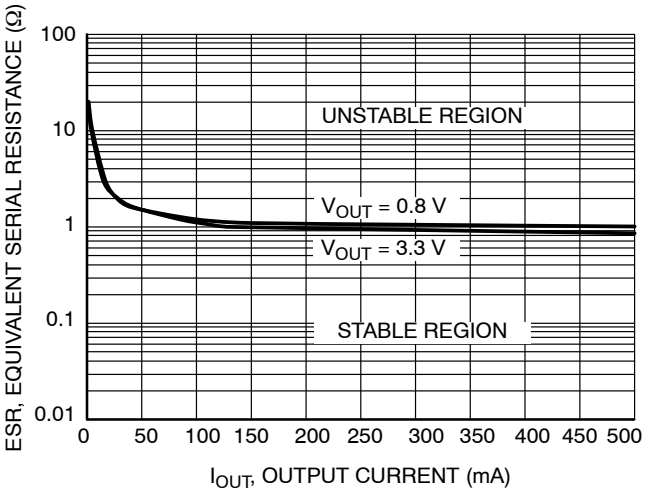


Figure 38. Output Capacitor ESR vs. Output Current

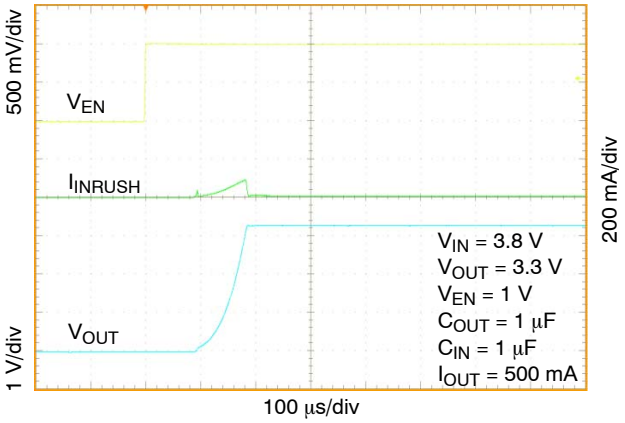


Figure 39. Enable Turn−on Response, C_{OUT} = 1 μF, I_{OUT} = 10 mA

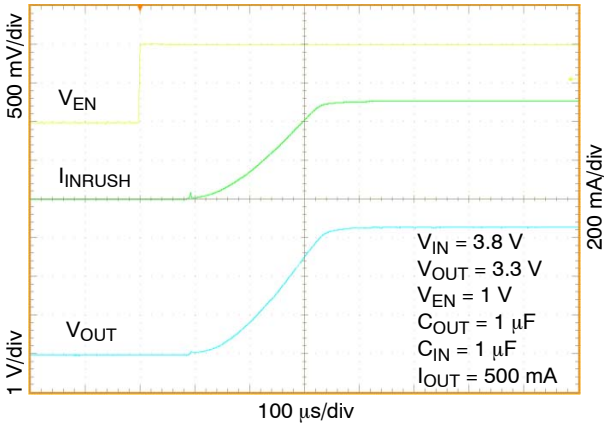


Figure 40. Enable Turn−on Response, C_{OUT} = 1 μF, I_{OUT} = 500 mA

TYPICAL CHARACTERISTICS

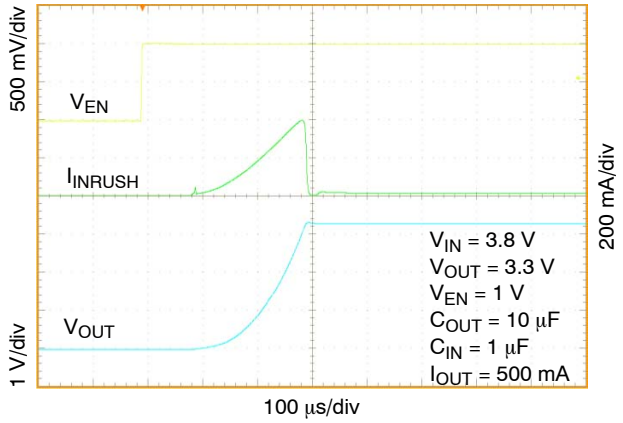


Figure 41. Enable Turn−on Response, C_{OUT} = 10 μF, I_{OUT} = 10 mA

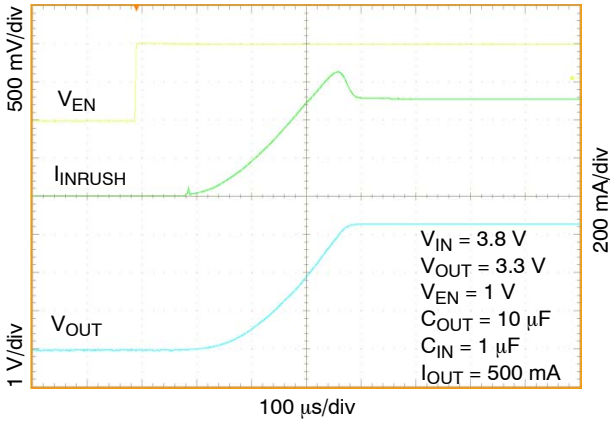


Figure 42. Enable Turn−on Response, C_{OUT} = 10 μF, I_{OUT} = 500 mA

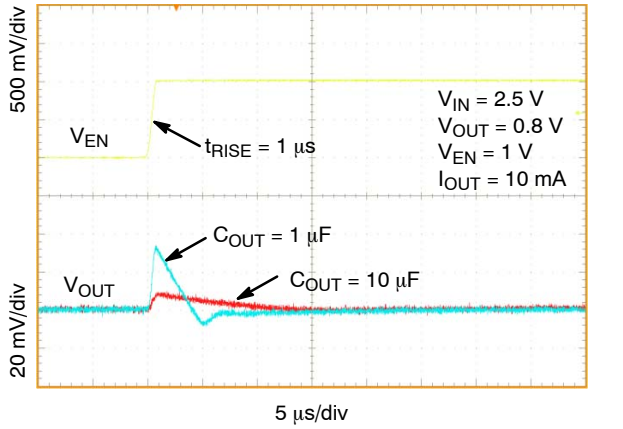


Figure 43. Line Transient Response − Rising Edge, V_{OUT} = 0.8 V, I_{OUT} = 10 mA

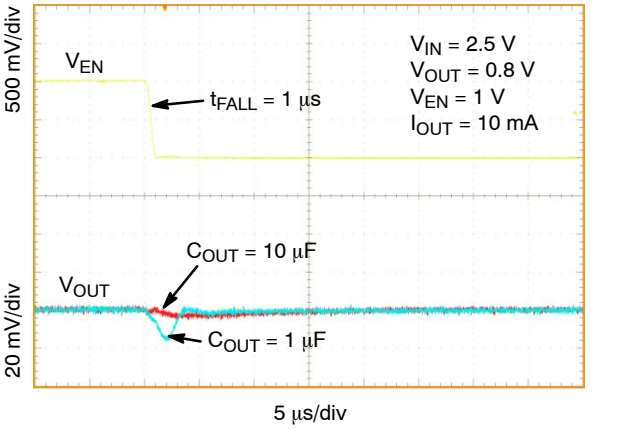


Figure 44. Line Transient Response − Falling Edge, V_{OUT} = 0.8 V, I_{OUT} = 10 mA

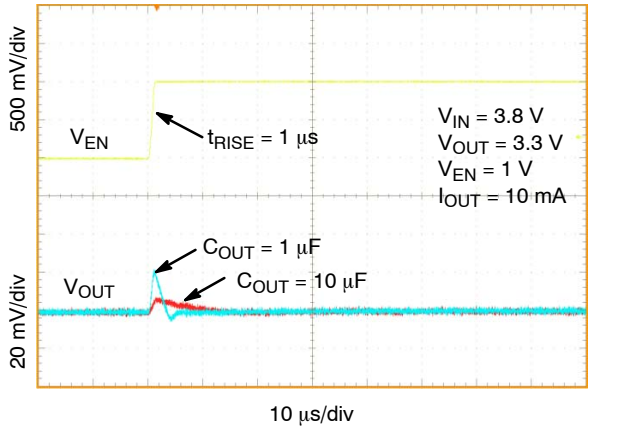


Figure 45. Line Transient Response − Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 10 mA

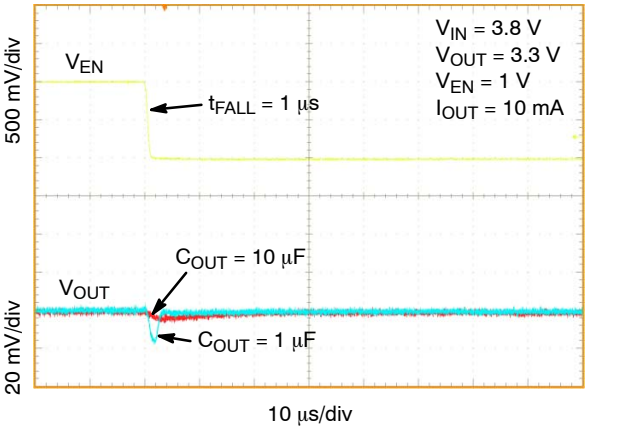


Figure 46. Line Transient Response − Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 10 mA

TYPICAL CHARACTERISTICS

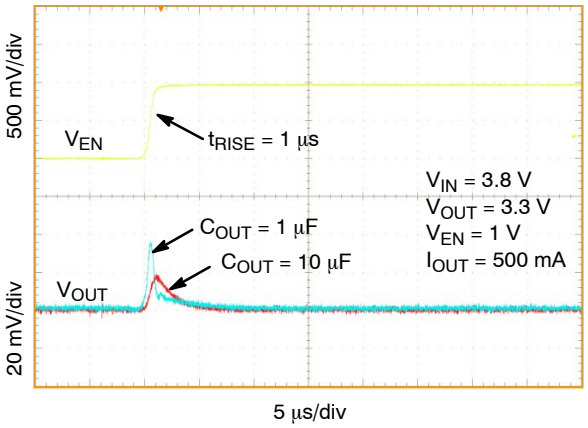


Figure 47. Line Transient Response – Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

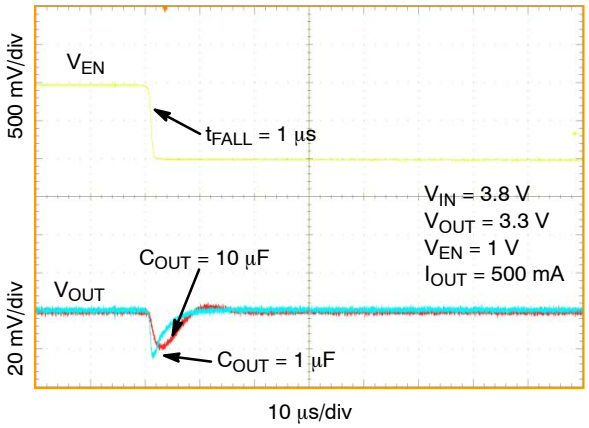


Figure 48. Line Transient Response – Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

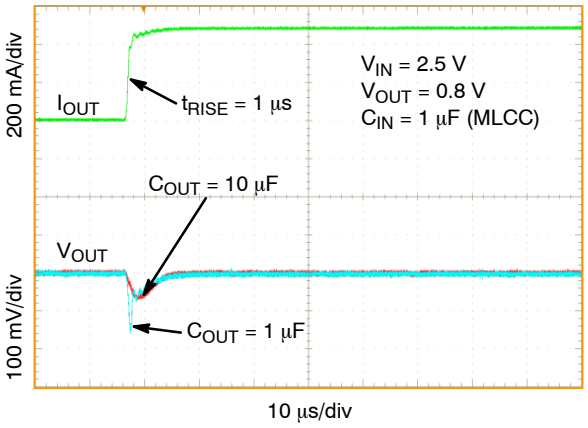


Figure 49. Load Transient Response – Rising Edge, V_{OUT} = 0.8 V, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 1 μF, 10 μF

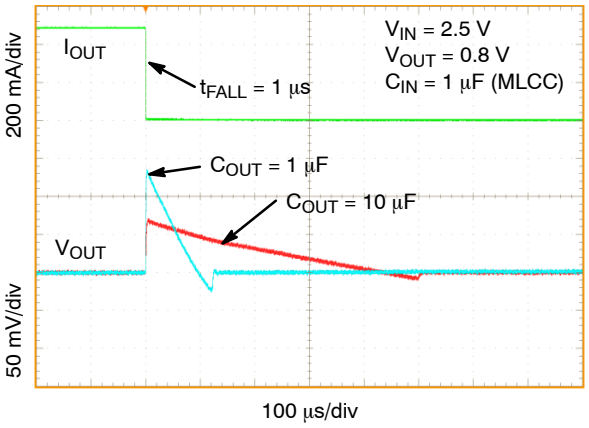


Figure 50. Load Transient Response – Falling Edge, V_{OUT} = 0.8 V, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 1 μF, 10 μF

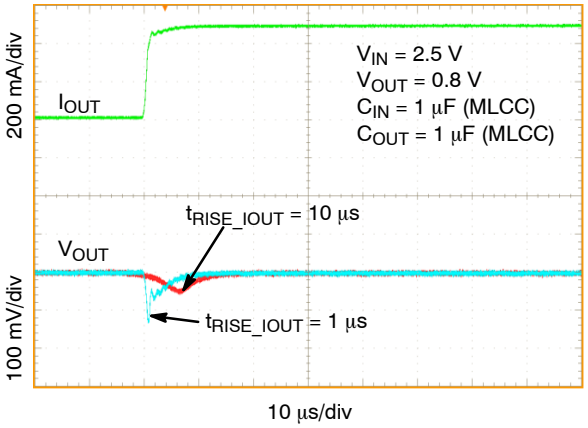


Figure 51. Load Transient Response – Rising Edge, V_{OUT} = 0.8 V, I_{OUT} = 1 mA to 500 mA, t_{RISE_IOUT} = 1 μs, 10 μs

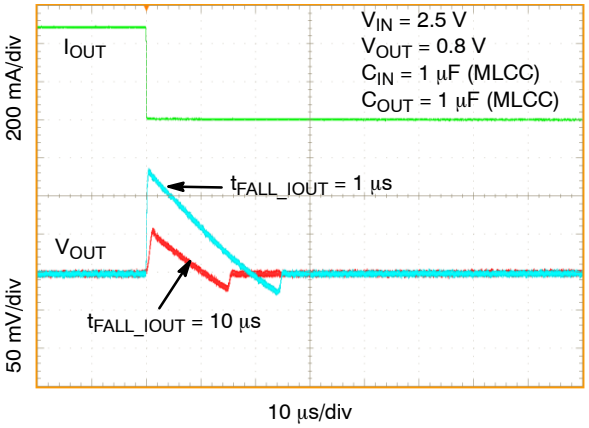


Figure 52. Load Transient Response – Falling Edge, V_{OUT} = 0.8 V, I_{OUT} = 1 mA to 500 mA, t_{FALL_IOUT} = 1 μs, 10 μs

TYPICAL CHARACTERISTICS

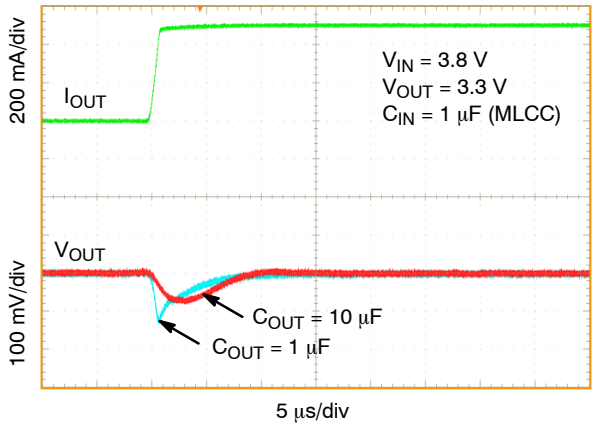


Figure 53. Load Transient Response – Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 1 μF, 10 μF

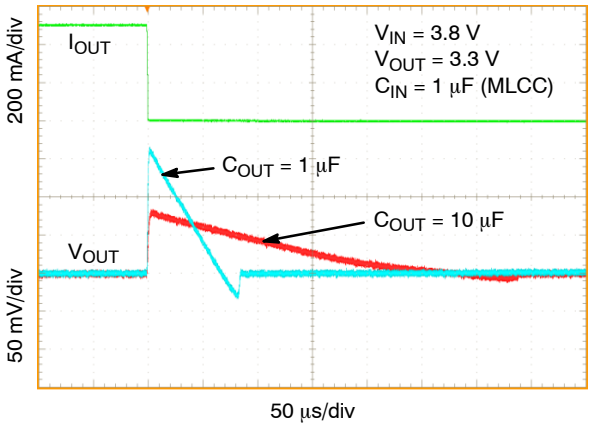


Figure 54. Load Transient Response – Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 1 μF, 10 μF

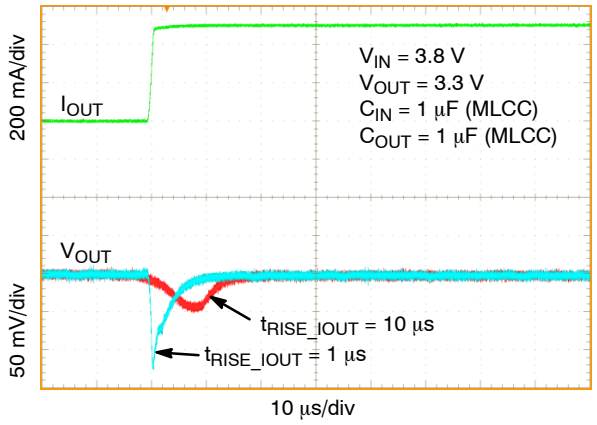


Figure 55. Load Transient Response – Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 1 mA to 500 mA, t_{RISE_IOUT} = 1 μs, 10 μs

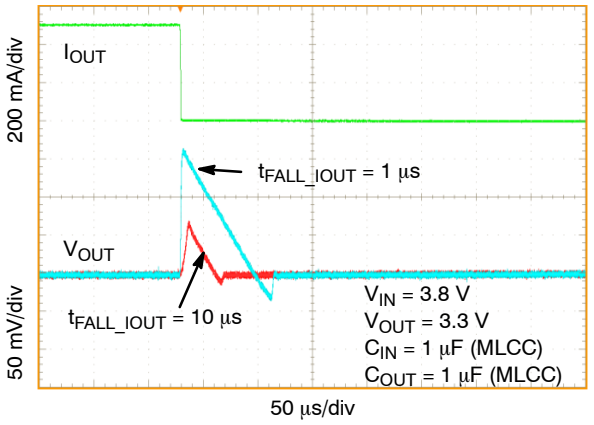


Figure 56. Load Transient Response – Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 1 mA to 500 mA, t_{FALL_IOUT} = 1 μs, 10 μs

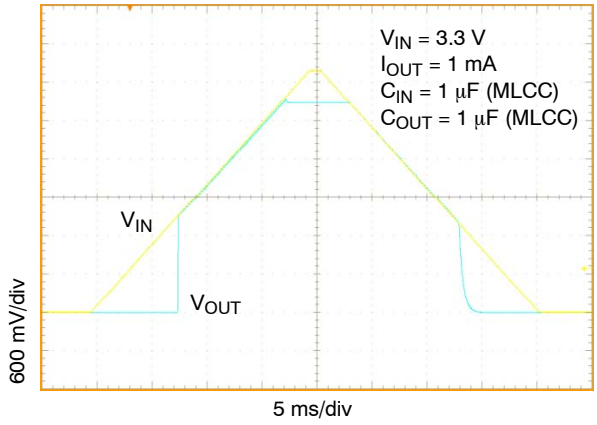


Figure 57. Turn−on/off, Slow Rising V_{IN}

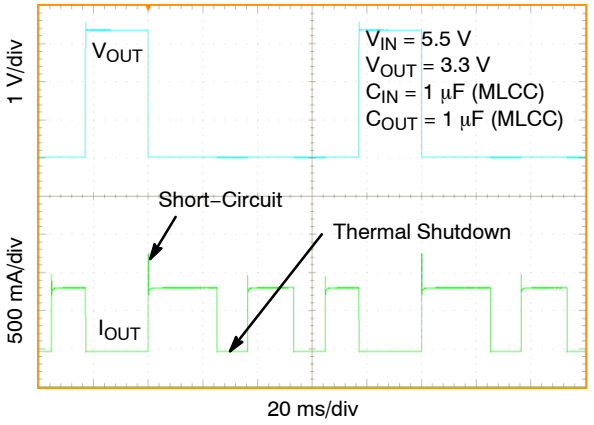


Figure 58. Short−Circuit and Thermal Shutdown

TYPICAL CHARACTERISTICS

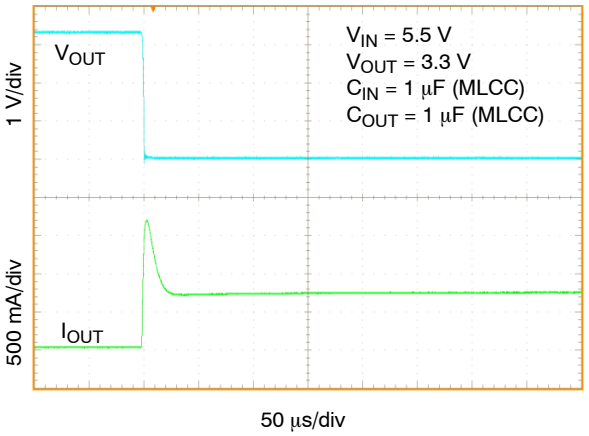


Figure 59. Short−Circuit Current Peak

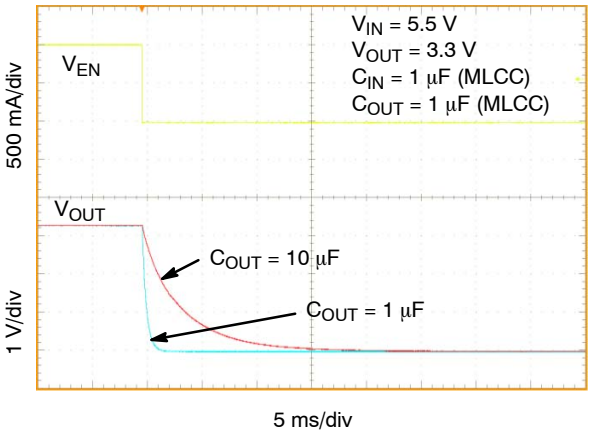


Figure 60. Enable Turn−off

APPLICATIONS INFORMATION

General

The NCP705 is a high performance 500 mA Low Dropout Linear Regulator. This device delivers excellent noise and dynamic performance. Thanks to its adaptive ground current feature the device consumes only 13 μA of quiescent current at no − load condition. The regulator features ultra − low noise of 12 μVRMS, PSRR of 71 dB at 1 kHz and very good load/line transient performance. Such excellent dynamic parameters and small package size make the device an ideal choice for powering the precision analog and noise sensitive circuitry in portable applications. The LDO achieves this ultra low noise level output without the need for a noise bypass capacitor. A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 10 nA from the IN pin. The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (CIN)

It is recommended to connect a minimum of 1 μF Ceramic X5R or X7R capacitor close to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. /max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

Output Decoupling (COUT)

The NCP705 requires an output capacitor connected as close as possible to the output pin of the regulator. The minimal capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCP705 is designed to remain stable with minimum effective capacitance of 1 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0402 the effective capacitance drops rapidly with the applied DC bias. Refer to the Figure 61, for the capacitance vs. package size and DC bias voltage dependence.

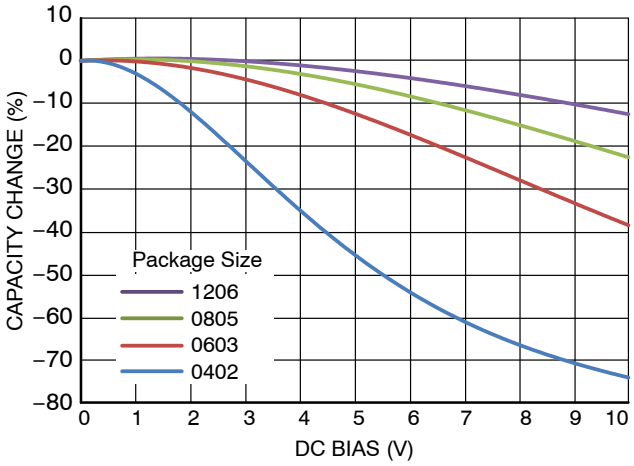


Figure 61. Capacitance Change vs. DC Bias

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 900 mΩ. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR as shown in typical characteristics. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature. The tantalum capacitors are generally more costly than ceramic capacitors.

No−load Operation

The regulator remains stable and regulates the output voltage properly within the ±2% tolerance limits even with no external load applied to the output.

Enable Operation

The NCP705 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCP705 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 110 nA which assures that the device is turned−off when the EN pin is not connected. Build in 2 mV

hysteresis into the EN prevents from periodic on/off oscillations that can occur due to noise.

In the case where the EN function isn't required the EN should be tied directly to IN.

Undervoltage Lockout

The internal UVLO circuitry assures that the device becomes disabled when the V_{IN} falls below typ. 1.5V. When the V_{IN} voltage ramps−up the NCP705 becomes enabled, if V_{IN} rises above typ. 1.6V. The 100mV hysteresis prevents from on/off oscillations that can occur due to noise on V_{IN} line.

Output Current Limit

Output Current is internally limited within the IC to a typical 750 mA. The NCP705 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 800 mA (typ). The current limit and short circuit protection will work properly up to V_{IN} = 5.5 V at T_A = 125°C. There is no limitation for the short circuit duration.

Internal Soft−Start circuit

NCP705 contains an internal soft−start circuitry to protect against large inrush currents which could otherwise flow during the start−up of the regulator. Soft−start feature protects against power bus disturbances and assures a controlled and monotonic rise of the output voltage.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking. For reliable operation junction temperature should be limited to +125°C maximum.

Power Dissipation

As power dissipated in the NCP705 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCP705 can handle is given by:

$$P_{D(MAX)} = \frac{\left[+\ 125^{o}C - T_A\right]}{\theta_{JA}} \qquad \text{(eq. 1)}$$

The power dissipated by the NCP705 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}@I_{OUT}\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

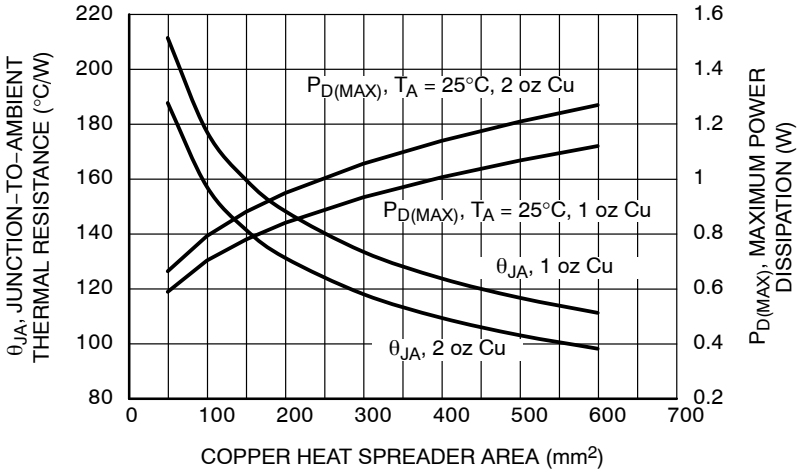


Figure 62. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (WDFN6)

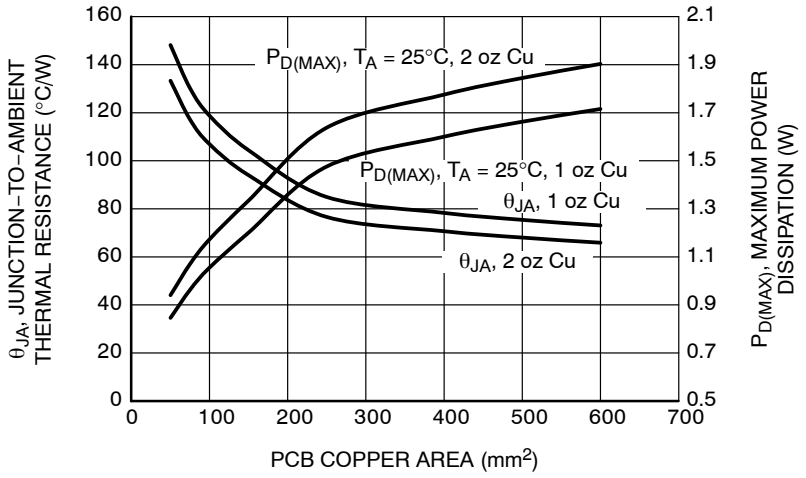


Figure 63. θ_{JA} vs. Copper Area (SOT223−6L)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Load Regulation

The NCP705 features very good load regulation of maximum 2 mV in 0 mA to 500 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 mΩ which will cause 50 mV voltage drop at full load current, deteriorating the excellent load regulation.

Line Regulation

The IC features very good line regulation of 0.75 mV/V measured from $V_{IN} = V_{OUT} + 0.5$ V to 5.5V. For battery operated applications it may be important that the line regulation from $V_{IN} = V_{OUT} + 0.5$ V up to 4.5 V is only 0.55 mV/V.

Power Supply Rejection Ratio

The NCP705 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Output Noise

The IC is designed for ultra−low noise output voltage without external noise filter capacitor (C_{nr}). Figures 3 – 6 shows NCP705 noise performance. Generally the noise performance in the indicated frequency range improves with increasing output current.

Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2).

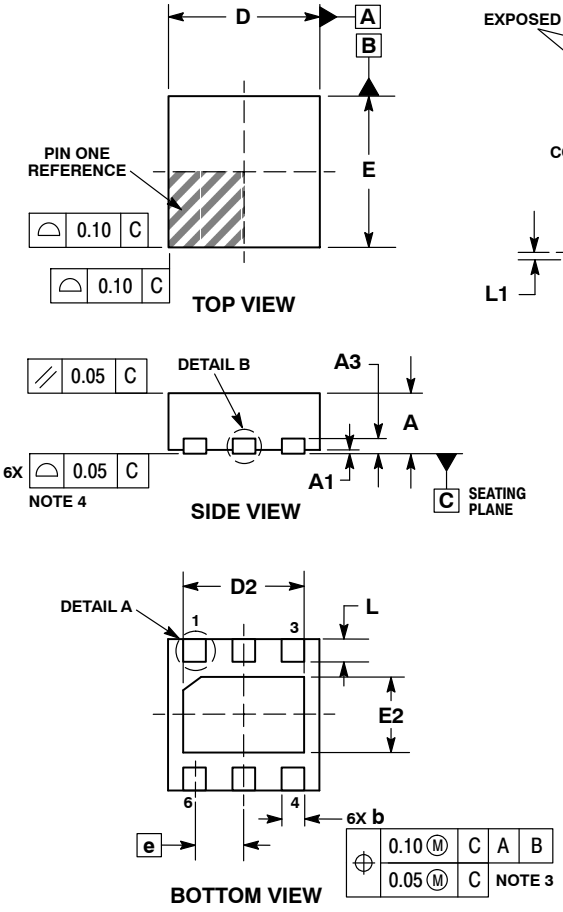
ORDERING INFORMATION

Device	Voltage Option	Marking	Package	Shipping†
NCP705MT18TCG	1.8 V	5A	WDFN6 (Pb−Free)	3000 / Tape & Reel
NCP705MT28TCG	2.8 V	5C		
NCP705MT30TCG	3.0 V	5D		
NCP705MT33TCG	3.3 V	5E		
NCP705ST18T3G	1.8 V	5AA	SOT223−6 (Pb−Free)	2500 / Tape & Reel (Available Soon)
NCP705ST28T3G	2.8 V	5AC		
NCP705ST30T3G	3.0 V	5AD		
NCP705ST33T3G	3.3 V	5AE		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

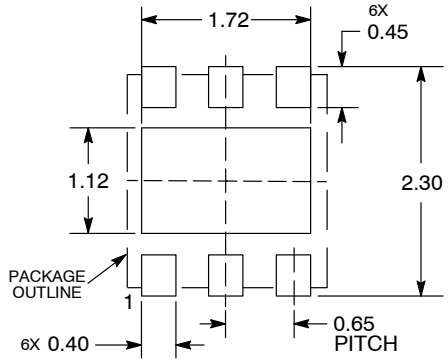
WDFN6 2x2, 0.65P
CASE 511BR
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
L	0.20	0.40
L1	---	0.15

RECOMMENDED MOUNTING FOOTPRINT*

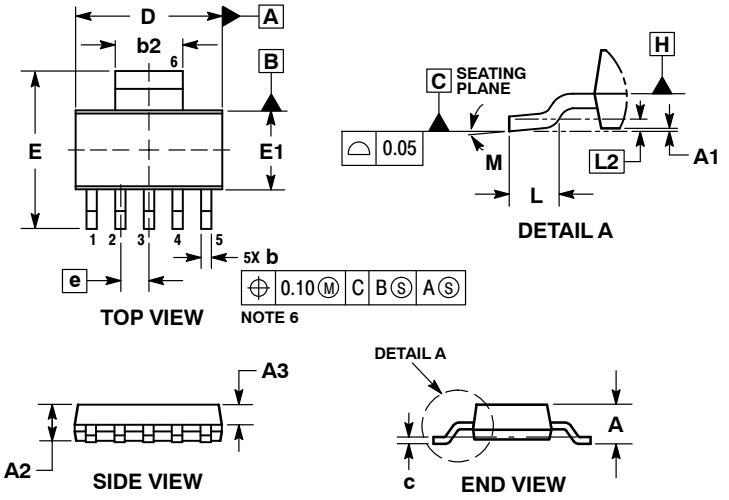


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

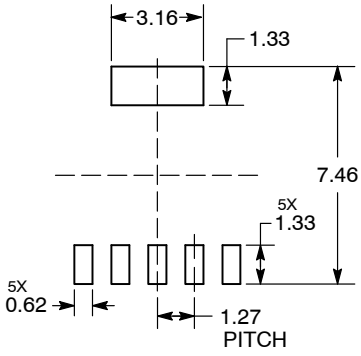
SOT−223 6−LEAD
CASE 419AY
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. POSITIONAL TOLERANCE ALSO APPLIES TO DIMENSION b2.

	MILLIMETERS	
DIM	MIN	MAX
A	1.57	1.75
A1	0.00	0.10
A2	1.55	1.65
A3	0.89 REF	
b	0.41	0.51
b2	2.95	3.05
c	0.24	0.32
D	6.45	6.55
E	6.86	7.26
E1	3.45	3.55
e	1.27 BSC	
L	0.91	1.14
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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