SMALL-OUTLINE DDR SDRAM MODULE

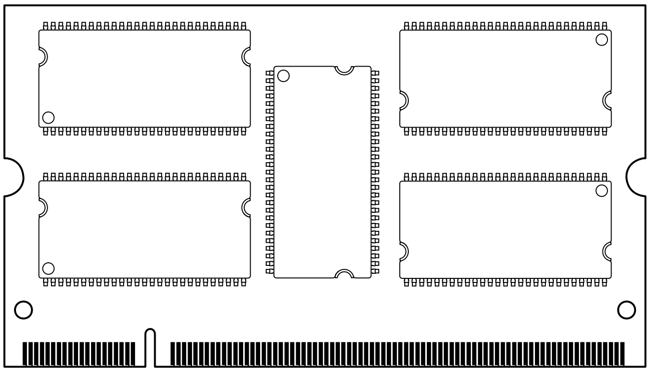
MT9VDDT1672H(I) –128MB, MT9VDDT3272H(I) –256MB,
MT18VDDS6472H(I) – 512MB (ADVANCE),
MT9VDDT6472H(I) – 512MB,
MT18VDDS12872H(I) – 1GB (ADVANCE)

For the latest data sheet, please refer to the Micron® Web site: www.micron.com/moduleds

Features

- 200-pin, small-outline, dual in-line memory module (SODIMM)
- Fast data transfer rates: PC1600, PC2100, or PC2700
- Utilizes 200 MT/s, 266 MT/s, and 333 MT/s DDR SDRAM components or TwinDie™ DDR SDRAM components
- ECC, 1-bit error detection and correction
- 128MB (16 Meg x 72), 256MB (32 Meg x 72), 512MB (64 Meg x 72), and 1GB (128 Meg x 72)
- VDD = VDDQ = +2.5V
- VDDSPD = +2.3V to +3.6V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs CK and CK#
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.625µs (MT9VDDT1672H), 7.8125µs (MT9VDDT3272H, MT18VDDS6472H, MT9VDDT6472H, and MT18VDDS12872H) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency

Figure 1: 200-Pin SODIMM (MO-224)



OPTIONS	MARKING
• Package	
200-pin SODIMM (gold)	G
• Frequency/CAS Latency	
6.0ns/167 MHz (333 MT/s) CL = 2.5[1]	-335[2]
7.5ns/133 MHz (266 MT/s) CL = 2	-26A
7.5ns/133 MHz (266 MT/s) CL = 2.5	-265
10ns/100 MHz (200 MT/s) CL = 2	-202
• Operating Temperature Range	
Commercial (0°C ≤ T_A ≤ +70°C)	None
Industrial (-40°C ≤ T_A ≤ +85°C)	IT[3]

NOTE:
1. CL = Device CAS (READ) Latency.
2. -335 speed grade available in single-rank module only.
3. Consult Micron for availability; industrial temperature option available in -265 speed only.

Table 1: Address Table

	MT9VDDT1672H	MT9VDDT3272H	MT18VDDS6472H	MT9VDDT6472H	MT18VDDS12872H
Refresh Count	4K	8K	8K	8K	8K
Row Addressing	4K (A0–A11)	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	16 Meg x 8	32 Meg x 8	64 Meg x 8	32 Meg x 8	64 Meg x 8
Column Addressing	1K (A0–A9)	1K (A0–A9)	2K (A0–A9, A11)	1K (A0–A9)	2K (A0–A9, A11)
Module Rank Addressing	1 (S0#)	1 (S0#)	1 (S0#)	2 (S0#, S1#)	2 (S0#, S1#)

Table 2: Part Numbers and Timing Parameters

PART NUMBER	MODULE DENSITY	CONFIGURATION	MODULE BANDWIDTH	MEMORY CLOCK/ DATA BIT RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT9VDDT1672H(I)G-335__	128MB	16 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT1672H(I)G-26A__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT1672H(I)G-265__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT1672H(I)G-202__	128MB	16 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT9VDDT3272H(I)G-335__	256MB	32 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT3272H(I)G-26A__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT3272H(I)G-265__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT3272H(I)G-202__	256MB	32 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT18VDDS6472H(I)G-335__	512MB	64 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT18VDDS6472H(I)G-26A__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT18VDDS6472H(I)G-265__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT18VDDS6472H(I)G-202__	512MB	64 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT9VDDT6472H(I)G-26A__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT6472H(I)G-265__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT6472H(I)G-202__	512MB	64 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT18VDDS12872H(I)G-26A__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT18VDDS12872H(I)G-265__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT18VDDS12872H(I)G-202__	1GB	128 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2

NOTE:

All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9VDDT3272HG-265A1.

Table 3: Pin Assignment (200-Pin SODIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	51	VSS	101	A9	151	DQ42
3	VSS	53	DQ19	103	VSS	153	DQ43
5	DQ0	55	DQ24	105	A7	155	Vdd
7	DQ1	57	VDD	107	A5	157	Vdd
9	VDD	59	DQ25	109	A3	159	VSS
11	DQS0	61	DQS3	111	A1	161	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48
15	VSS	65	DQ26	115	A10	165	DQ49
17	DQ3	67	DQ27	117	BA0	167	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6
21	VDD	71	CB0	121	S0#	171	DQ50
23	DQ9	73	CB1	123	NC	173	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51
27	VSS	77	DQS8	127	DQ32	177	DQ56
29	DQ10	79	CB2	129	DQ33	179	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57
33	VDD	83	CB3	133	DQS4	183	DQS7
35	CK0	85	NC	135	DQ34	185	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58
39	VSS	89	CK2	139	DQ35	189	DQ59
41	DQ16	91	CK2#	141	DQ40	191	VDD
43	DQ17	93	VDD	143	VDD	193	SDA
45	VDD	95	CKE1	145	DQ41	195	SCL
47	DQS2	97	NC	147	DQS5	197	VDDSPD
49	DQ18	99	NC/A12	149	VSS	199	NC

Table 4: Pin Assignment (200-pin SODIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
2	VREF	52	VSS	102	A8	152	DQ46
4	VSS	54	DQ23	104	VSS	154	DQ47
6	DQ4	56	DQ28	106	A6	156	VDD
8	DQ5	58	VDD	108	A4	158	CK1#
10	VDD	60	DQ29	110	A2	160	CK1
12	DM0	62	DM3	112	A0	162	VSS
14	DQ6	64	VSS	114	VDD	164	DQ52
16	VSS	66	DQ30	116	BA1	166	DQ53
18	DQ7	68	DQ31	118	RAS#	168	VDD
20	DQ12	70	VDD	120	CAS#	170	DM6
22	VDD	72	CB4	122	S1#	172	DQ54
24	DQ13	74	CB5	124	NC	174	VSS
26	DM1	76	VSS	126	VSS	176	DQ55
28	VSS	78	DM8	128	DQ36	178	DQ60
30	DQ14	80	CB6	130	DQ37	180	VDD
32	DQ15	82	VDD	132	VDD	182	DQ61
34	VDD	84	CB7	134	DM4	184	DM7
36	VDD	86	NC	136	DQ38	186	VSS
38	VSS	88	VSS	138	VSS	188	DQ62
40	VSS	90	VSS	140	DQ39	190	DQ63
42	DQ20	92	VDD	142	DQ44	192	VDD
44	DQ21	94	VDD	144	VDD	194	SA0
46	VDD	96	CKE0	146	DQ45	196	SA1
48	DM2	98	NC	148	DM5	198	SA2
50	DQ22	100	A11	150	VSS	200	NC

NOTE:

Pin 99 is a No Connect for MT9VDDT1672H modules, or A12 for all other modules.

Figure 2: Module Layout

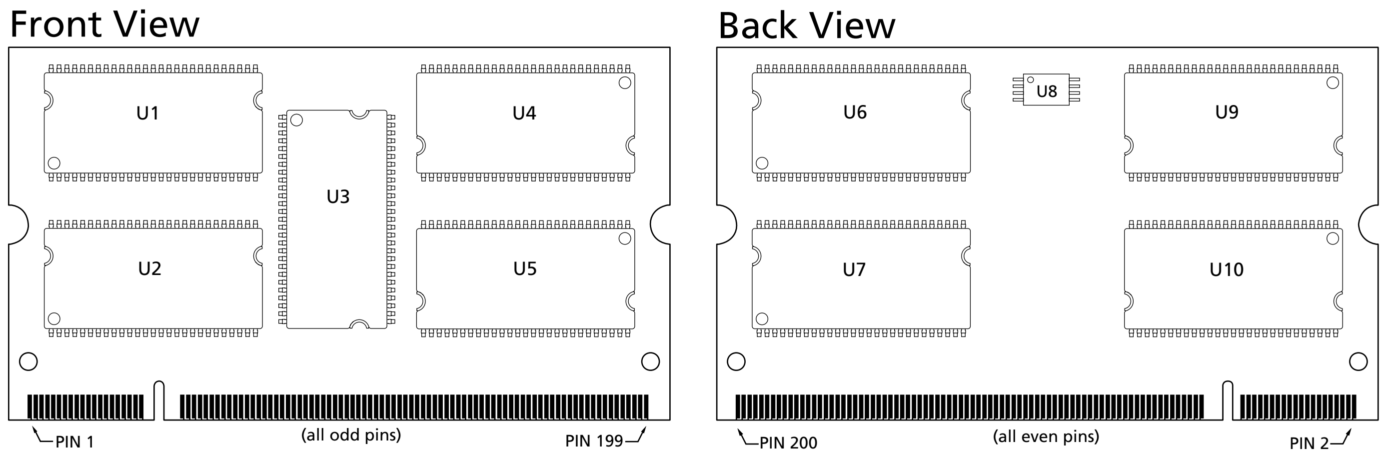


Table 5: Pin Descriptions

Refer to Pin Assignment Tables on page 3 for pin number and symbol information

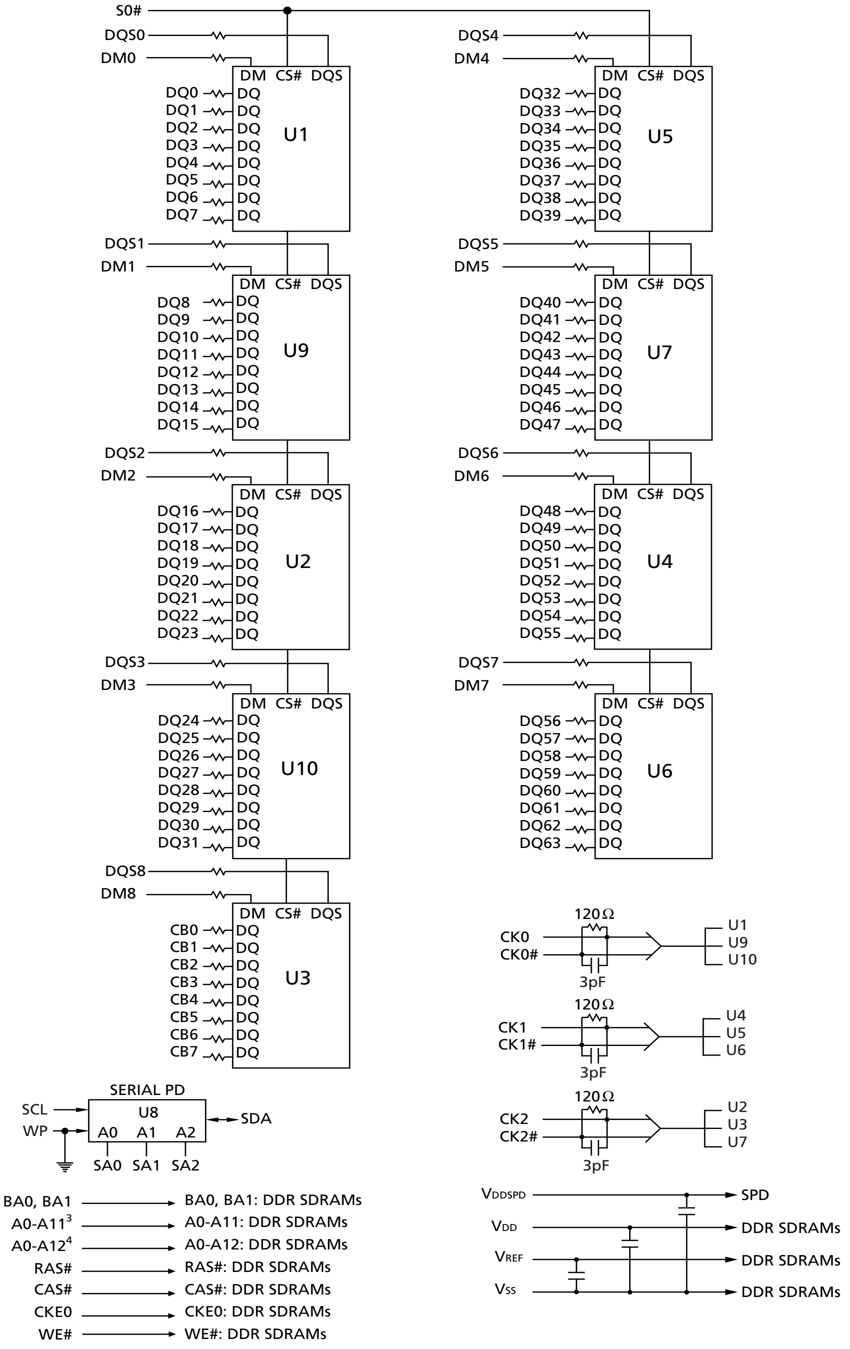
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 2	VREF	Input	SSTL_2 reference voltage.
118, 119, 120	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
35, 37, 89, 91, 158, 160	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clock: CK, CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK,and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
95, 96	CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank).CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after VDD is applied.
121, 122	S0#, S1#	Input	Chip Selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
116, 117	BA0, BA1	Input	Bank Address: BA0, BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
99 (A12), 100, 101, 102, 105, 106, 107, 108, 109, 110, 111, 112, 115	A0-A11 MT9VDDT1672H A0-A12 (99) MT9VDDT3272H, MT18VDDS6472H, MT9VDDT6472H, MT18VDDS12872H	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/ WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
11, 25, 47, 61, 77, 133, 147, 169, 183	DQS0-DQS8	Input/ Output	Data Strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
12, 26, 48, 62, 78, 134, 148, 170, 184	DM0-DM8	Input	Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
71,72, 73, 74, 79, 80, 83, 84	CB0-CB7	Input/ Output	Check Bits: ECC, 1-bit error detection and correction.

Table 5: Pin Descriptions (Continued)

Refer to Pin Assignment Tables on page 3 for pin number and symbol information

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5-8, 13-20, 23-24, 29-32, 41-44, 49-50, 53-56, 59-60, 65-68, 127-130, 135-136, 139-142, 145-146, 151-154, 163-166, 171-172, 175-178, 181-182, 187-190	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
195	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
194, 196, 198	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
193	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
9-10, 21-22, 33-34, 36, 45-46, 57-58, 69-70, 81-82, 92-94, 113-114, 131-132, 143-144, 155-157, 167-168, 17-180, 191-192	VDD	Supply	Power Supply: +2.5V ±0.2V. Please see note 49 on page 26.
3-4 15-16, 27-28, 38-40, 51-52, 63-64, 75-76, 87-88, 90, 103-104, 125-126, 137-138, 149-150, 159, 161-162, 173-174, 185-186	VSS	Supply	Ground.
197	VDDSPD	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
85, 97, 99 (only for MT9VDDT1672H), 123, 199, 98, 124, 200	NC	—	No Connect: These pins should be left unconnected.

Figure 3: Functional Block Diagram, (MT9VDDT1672H(I), MT9VDDT3272H(I), MT9VDDT6472H(I))

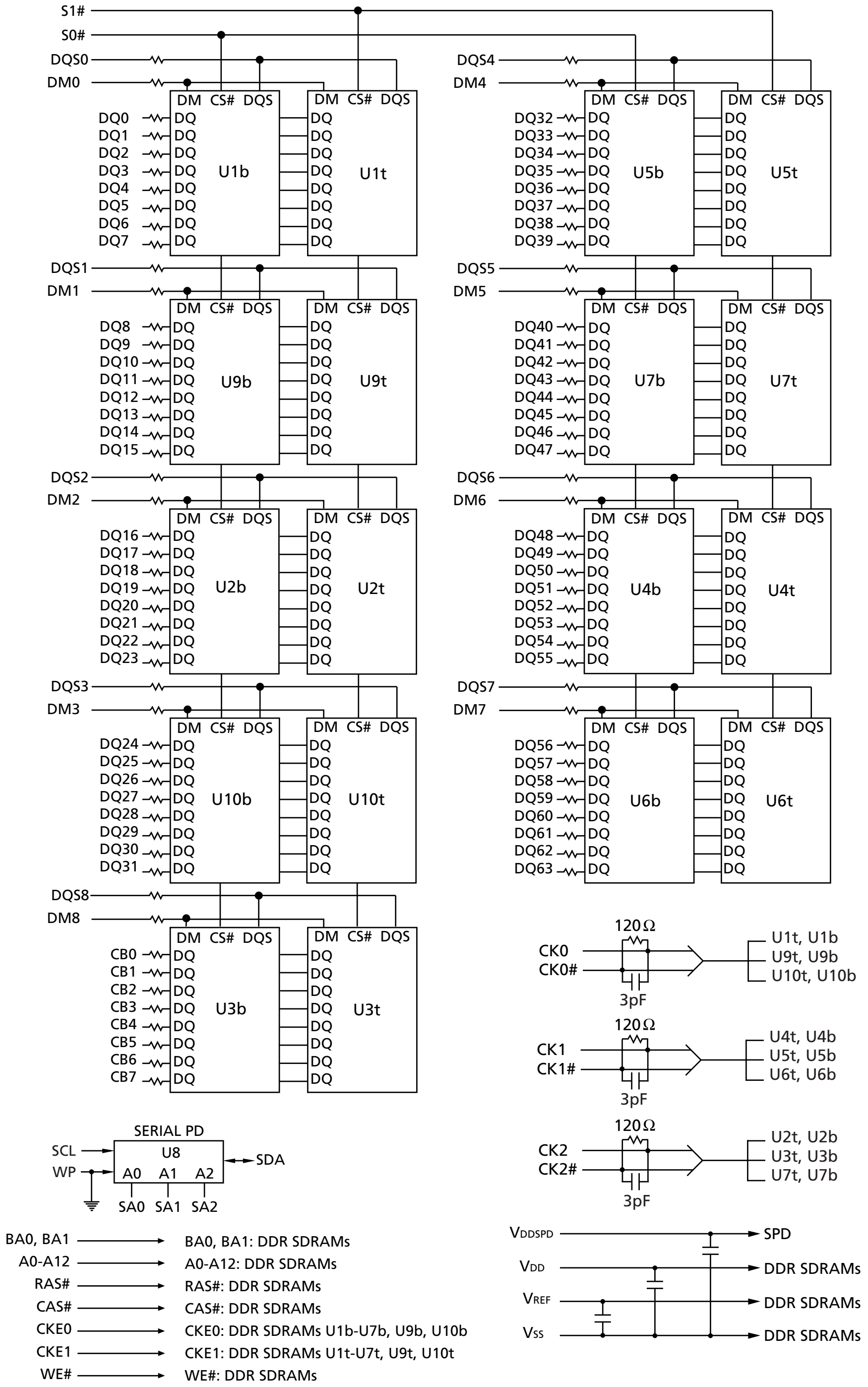


NOTE:

1. All resistor values are 22Ω unless otherwise specified.
2. Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part numbering guide at www.micron.com/numberguide.
3. MT9VDDT1672H
4. MT9VDDT3272H and MT9VDDT6472H

DDR SDRAMs = MT46V16M8TG for MT9VDDT1672HG (commercial temp.)
DDR SDRAMs = MT46V32M8TG for MT9VDDT3272HG (commercial temp.)
DDR SDRAMs = MT46V64M8TG for MT18VDDS6472HG (commercial temp.)
DDR SDRAMs = MT46V16M8TG-ITfor MT9VDDT1672HG (indust. temp.)
DDR SDRAMs = MT46V32M8TG-IT for MT9VDDT3272HG (indust. temp.)
DDR SDRAMs = MT46V64M8TG-IT for MT18VDDS6472HG (indust. temp.)
Contact Micron for availability of -IT modules.

Figure 4: Functional Block Diagram, (MT18VDDS6472H(I), MT18VDDS12872H(I))



NOTE:

1. All resistor values are 22Ω unless otherwise specified.
2. 'b' = bottom portion of TwinDie SDRAM, 't' = top portion of TwinDie SDRAM.
3. Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part numbering guide at www.micron.com/numberguide.

DDR SDRAMs = MT46V64M8S2 for MT9VDDT6472HG
DDR SDRAMs = MT46V64M8S2 for MT18VDDS12872HG
-IT option is not available for TwinDie components.

General Description

The MT9VDDT1672H(I), MT9VDDT3272H(I), MT18VDDS6472H(I), MT9VDDT6472H(I), and MT18VDDS12872H(I) are high-speed CMOS, dynamic random-access, 128MB, 256MB, 512MB, and 1GB memory modules organized in x72 (ECC) configuration. These modules use internally configured quad-bank DDR SDRAMs.

These DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

These DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed [BA0, BA1 select device bank; A0–A11 select device row for the module MT9VDDT1672H(I); A0–A12 select device row for modules MT9VDDT3272H(I), MT18VDDS6472H(I), MT9VDDT6472H(I), and MT18VDDS12872H(I)]. The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

These DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 128Mb, 256Mb, and 512Mb DDR SDRAM and 512Mb and 1Gb DDR TwinDie component data sheets.

Serial Presence-Detect Operation

These DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Mode Register Definition

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 5, Mode Register Definition Diagram, on page 9. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 [for

MT9VDDT1672H(I)] or A7–A12 [for MT9VDDT3272H(I), MT18VDDS6472H(I), MT9VDDT6472H(I), and MT18VDDS12872H(I)] specify the operating mode.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Mode Register Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A*i* when the burst length is set to two, by A2–A*i* when the burst length is set to four and by A3–A*i* when the burst length is set to eight (where A*i* is the most significant column address bit for a given configuration; see Note 5 of Table 6, Burst Definition Table, on page 10). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 6, Burst Definition Table, on page 10.

Read Latency

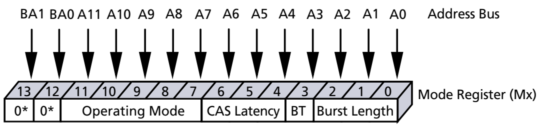
The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks, as shown in Figure 6, CAS Latency Diagram, on page 10.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table 7, CAS Latency (CL) Table, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

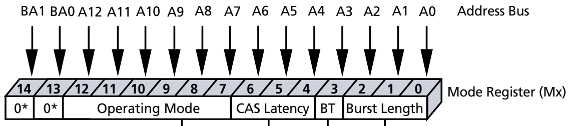
Figure 5: Mode Register Definition Diagram

MT9VDDT1672H Module Address Bus



* M13 and M12 (BA1and BA0) must be "0, 0" to select the base mode register (vs. the extended mode register).

MT9VDDT3272H; MT18VDDT6472H; MT9VDDS6472H, MT18VDDS12872H Module Address Bus



* M14 and M13 (BA1 and BA0) must be "0, 0" to select the base mode register (vs. the extended mode register).

M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	2.5
1 1 1	Reserved

M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Table 6: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS			ORDER OF ACCESSES WITHIN A BURST	
				TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2			**A0**		
			0	0-1	0-1
			1	1-0	1-0
4		**A1**	**A0**		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	**A2**	**A1**	**A0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:

1. For a burst length of two, A1–A*i* select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2–A*i* select the four-data-element block; A0–A1 select the first access within the block.
3. For a burst length of eight, A3–A*i* select the eight-data-element block; A0–A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
5. *i* = 9 for MT9VDDT1672H, MT9VDDT3272H, and MT18VDDS6472H;
   i = 11 for MT9VDDT6472H and MT18VDDS12872H.

Table 7: CAS Latency (CL) Table

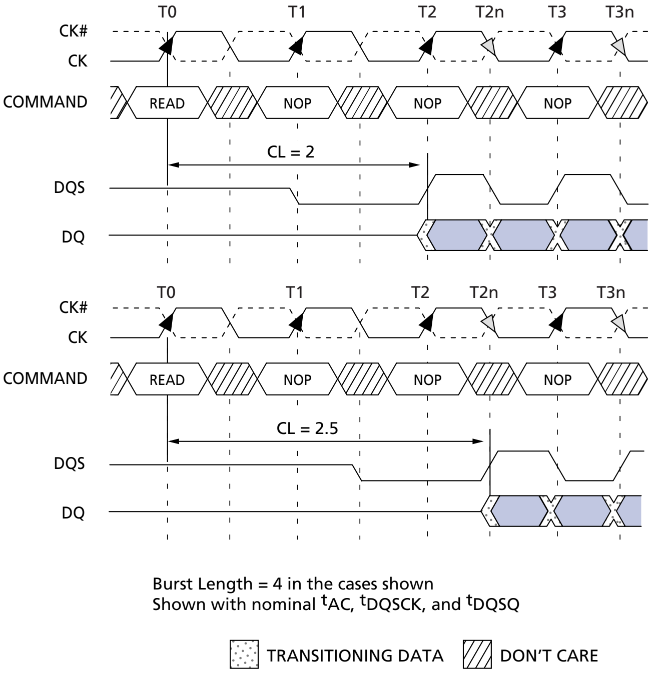
SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHZ)	
	CL = 2	CL = 2.5
-335	NA	75 ≤ f ≤ 167
-26A	75 ≤ f ≤ 133	75 ≤ f ≤ 133
-265	75 ≤ f ≤ 100	75 ≤ f ≤ 133
-202	75 ≤ f ≤ 100	NA

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7–A11 [for MT9VDDT1672H(I)], or A7–A12 (for MT9VDDT3272H(I), MT18VDDS6472H(I), MT9VDDT6472H(I), and MT18VDDS12872H(I)] each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9–A11 [for MT9VDDT1672H(I)], or A7 and A9–A12 [for MT9VDDT3272H(I), MT18VDDS6472H(I), MT9VDDT6472H(I), and MT18VDDS12872H(I)] each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7–A11, or A7–A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Figure 6: CAS Latency Diagram



Burst Length = 4 in the cases shown
Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, and QFC#. These functions are controlled via the bits shown in Figure 7, Extended Mode Register Definition Diagram. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

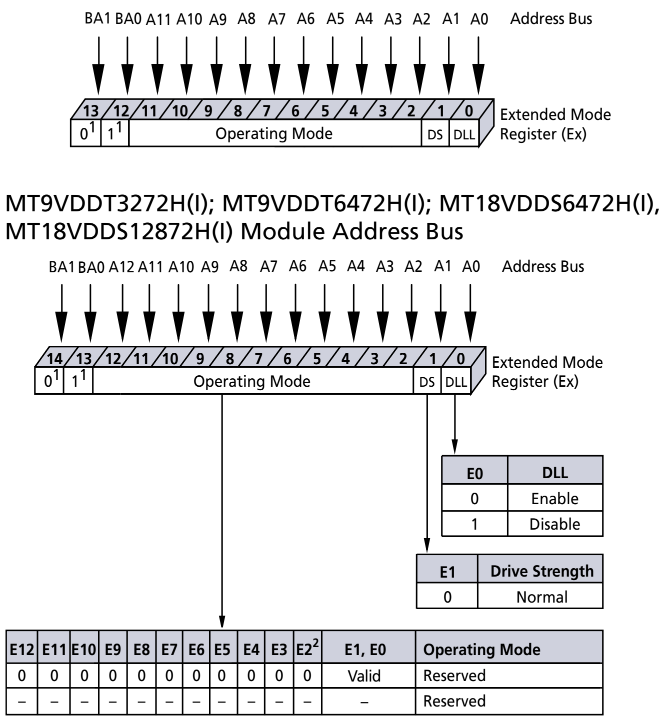
DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Figure 7: Extended Mode Register Definition Diagram

MT9VDDT1672H(I) Module Address Bus

MT9VDDT3272H(I); MT9VDDT6472H(I); MT18VDDS6472H(I), MT18VDDS12872H(I) Module Address Bus



E0	DLL
0	Enable
1	Disable

E1	Drive Strength
0	Normal

E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2[2]	E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	–	Reserved

NOTE:

1. E13 and E12 (MT9VDDT1672H(I)), or E14 and E13 [MT9VDDT3272H(I), MT18VDDS6472H(I), MT9VDDT6472H(I), and MT18VDDS12872H(I)] (BA1 and BA0) must be "0, 1" to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.

Commands

The Truth Tables below provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 128Mb, 256Mb, or 512Mb DDR SDRAM and 512Mb and 1Gb DDR TwinDie component data sheets.

Table 8: Commands Truth Table

Note: 1

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDRESS	NOTES
DESELECT (NOP)	H	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	2
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	5
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	6
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	7, 8
LOAD MODE REGISTER	L	L	L	L	Op-Code	9

NOTE:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. DESELECT and NOP are functionally interchangeable.
3. BA0–BA1 provide device bank address and A0–A11 [MT9VDDT1672H(I)] or A0–A12 [MT9VDDT3272H(I), MT18VDDS6472H(I), MT9VDDT6472H(I), and MT18VDDS12872H(I)] provide row address.
4. BA0–BA1 provide device bank address; A0–A9 [MT9VDDT1672H(I), MT9VDDT3272H(I), and MT9VDDT6472H(I)] or A0–A9,11 [MT18VDDS6472H(I), MT18VDDS12872H(I)], provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
6. A10 LOW: BA0–BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0-BA1 are “Don’t Care.”
7. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
8. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
9. BA0–BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A11 [MT9VDDT1672H(I)] or A0–A12 [MT9VDDT3272H(I), MT18VDDS6472H(I), MT9VDDT6472H(I), MT18VDDS12872H(I)] provide the op-code to be written to the selected mode register.

Table 9: DM Operation Truth Table

Used to mask write data; provided coincident with the corresponding data.

NAME (FUNCTION)	DM	DQS
WRITE Enable	L	Valid
WRITE Inhibit	H	X

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on VDD Supply
  Relative to VSS. . . . . -1V to +3.6V
Voltage on VDDQ Supply
  Relative to VSS. -1V to +3.6V
Voltage on VREF and Inputs
  Relative to VSS. -1V to +3.6V
Voltage on I/O Pins
  Relative to VSS. . . . . -0.5V to VDDQ +0.5V

Operating Temperature,
  T_A (commercial). . . . . 0°C to +70°C
  T_A (industrial). . . . . -40°C to +85°C
Storage Temperature (plastic) . . . . . . -55°C to +150°C
Power Dissipation
  Single rank modules 9W
  Dual rank modules 18W
Short Circuit Output Current. 50mA

Table 10: DC Electrical Characteristics and Operating Conditions (MT9VDDT1672H(I), MT9VDDT3272H(I), MT9VDDT6472H(I))

Notes: 1–5, 14, 49; notes appear on pages 23–26; 0°C ≤ T_A ≤ +70°C

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		VDD	2.3	2.7	V	32, 36
I/O Supply Voltage		VDDQ	2.3	2.7	V	32, 36, 39
I/O Reference Voltage		VREF	0.49 x VDDQ	0.51 x VDDQ	V	6, 39
I/O Termination Voltage (system)		VTT	VREF - 0.04	VREF + 0.04	V	7, 39
Input High (Logic 1) Voltage		VIH(DC)	VREF + 0.15	VDD + 0.3	V	25
Input Low (Logic 0) Voltage		VIL(DC)	-0.3	VREF - 0.15	V	25
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD, VREF pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	Command/ Address, RAS#, CAS#, WE#, CKE, S#	II	-18	18	µA	48
	CK, CK#		-6	6		
	DQS, DM		-2	2		
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	DQ	IOZ	-5	5	µA	48
OUTPUT LEVELS High Current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT)		IOH	-16.8	–	mA	33, 34
Low Current (VOUT = 0.373V, maximum VREF, maximum VTT)		IOL	16.8	–	mA	

Table 11: DC Electrical Characteristics and Operating Conditions (MT18VDDS6472H(I), MT18VDDS12872H(I))

Notes: 1–5, 14, 49; notes appear on pages 23–26; 0°C ≤ T_A ≤ +70°C

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		VDD	2.3	2.7	V	32, 36
I/O Supply Voltage		VDDQ	2.3	2.7	V	32, 36, 39
I/O Reference Voltage		VREF	0.49 x VDDQ	0.51 x VDDQ	V	6, 39
I/O Termination Voltage (system)		VTT	VREF - 0.04	VREF + 0.04	V	7, 39
Input High (Logic 1) Voltage		VIH(DC)	VREF + 0.15	VDD + 0.3	V	25
Input Low (Logic 0) Voltage		VIL(DC)	-0.3	VREF - 0.15	V	25
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD, VREF pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	Command/ Address, RAS#, CAS#, WE#,	II	-36	36	µA	48
	CKE0, CKE1, S0#, S1#		18	18		
	CK, CK#		-12	12		
	DQS, DM		-4	4		
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	DQ	IOZ	-10	10	µA	48
OUTPUT LEVELS High Current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT)		IOH	-16.8	–	mA	33, 34
Low Current (VOUT = 0.373V, maximum VREF, maximum VTT)		IOL	16.8	–	mA	

Table 12: AC Input Operating Conditions

Notes: 1–5,14, 16, 49; notes appear on pages 23–26; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	VIH(AC)	VREF + 0.310	–	V	12, 25, 35
Input Low (Logic 0) Voltage	VIL(AC)	–	VREF - 0.310	V	12, 25, 35
I/O Reference Voltage	VREF(AC)	0.49 x VDDQ	0.51 x VDDQ	V	6

Table 13: IDD Specifications and Conditions (MT9VDDT1672H(I))

DDR SDRAM components only
Notes: 1–5, 8, 10, 12, 49; notes appear on pages 23–26; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-335**	**-26A/-265**	**-202**	**UNITS**	**NOTES**
OPERATING CURRENT: One device bank; Active-Precharge; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles	IDD0	TBD	945	900	mA	20, 43
OPERATING CURRENT: One device bank; Active -Read Precharge; Burst = 2; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle	IDD1	TBD	1,080	990	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = (LOW)	IDD2P	TBD	27	27	mA	21, 28,45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^{t}CK = ^{t}CK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	TBD	405	315	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = LOW	IDD3P	TBD	180	180	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^{t}RC = ^{t}RAS (MAX); ^{t}CK = ^{t}CK (MIN); DQ, DM andDQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	TBD	405	315	mA	42
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); IOUT = 0mA	IDD4R	TBD	1,125	945	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	TBD	1,035	945	mA	20
AUTO REFRESH CURRENT ^{t}RC = ^{t}RC (MIN)	IDD5	TBD	1,890	1,845	mA	20, 45
^{t}RC = 15.625µs	IDD5A	TBD	45	45	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V	IDD6	TBD	18	18	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); Address and control inputs change only during Active READ, or WRITE commands	IDD7	TBD	2,925	2,475	mA	20, 44

Table 14: I_{DD} Specifications and Conditions (MT9VDDT3272H(I))

DDR SDRAM components only

Notes: 1–5, 8, 10, 12, 49; notes appear on pages 23–26; $0°C \le T_A \le +70°C$; $V_{DD} = V_{DDQ} = +2.5V \pm 0.2V$

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-335**	**-26A/-265**	**-202**	**UNITS**	**NOTES**
OPERATING CURRENT: One device bank; Active-Precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles	I_{DD0}	TBD	1,080	1,035	mA	20, 43
OPERATING CURRENT: One device bank; Active -Read Precharge; Burst = 2; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle	I_{DD1}	TBD	1,260	1,125	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = (LOW)	I_{DD2P}	TBD	36	36	mA	21,28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM	I_{DD2F}	TBD	360	360	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW	I_{DD3P}	TBD	270	225	mA	21, 28 , 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM andDQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{DD3N}	TBD	405	360	mA	42
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA	I_{DD4R}	TBD	1,620	1,350	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I_{DD4W}	TBD	1,710	1,440	mA	20
AUTO REFRESH CURRENT $^{t}RC = {}^{t}RC(MIN)$	I_{DD5}	TBD	2,205	1,935	mA	20,45
$^{t}RC = 7.8125\mu s$	I_{DD5A}	TBD	54	54	mA	24, 45
SELF REFRESH CURRENT: CKE $\le$ 0.2V	I_{DD6}	TBD	36	45	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during Active READ, or WRITE commands	I_{DD7}	TBD	3,285	3,150	mA	20, 44

Table 15: IDD Specifications and Conditions (MT9VDDT6472H(I))

DDR SDRAM components only
Notes: 1–5, 8, 10, 12, 49; notes appear on pages 23–26; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-335**	**-26A/-265**	**-202**	**UNITS**	**NOTES**
OPERATING CURRENT: One device bank; Active-Precharge; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles	IDD0	TBD	1,305	1,170	mA	20, 43
OPERATING CURRENT: One device bank; Active -Read Precharge; Burst = 2; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle	IDD1	TBD	1,440	1,305	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = (LOW)	IDD2P	TBD	54	54	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^{t}CK = ^{t}CK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	TBD	315	315	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = LOW	IDD3P	TBD	225	225	mA	21,28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^{t}RC = ^{t}RAS (MAX); ^{t}CK = ^{t}CK (MIN); DQ, DM andDQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	TBD	405	315	mA	42
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); IOUT = 0mA	IDD4R	TBD	1,800	1,485	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	TBD	1,845	1,575	mA	20
AUTO REFRESH CURRENT ^{t}RC = ^{t}RC(MIN)	IDD5	TBD	3,015	2,835	mA	20, 45
^{t}RC = 7.8125µs	IDD5A	TBD	90	90	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V	IDD6	TBD	63	63	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); Address and control inputs change only during Active READ, or WRITE commands	IDD7	TBD	4,050	3,825	mA	20, 44

Table 16: IDD Specifications and Conditions (MT18VDDS6472H(I))

DDR SDRAM components only
Notes: 1–5, 8, 10, 12, 49; notes appear on pages 23–26; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

		MAX			
PARAMETER/CONDITION	**SYMBOL**	**-26A/-265**	**-202**	**UNITS**	**NOTES**
OPERATING CURRENT: (IDD0 Condition) One device bank; Active-Precharge; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles	IDD0[a]	TBD	TBD	mA	20, 43
OPERATING CURRENT: (IDD1 Condtion) One device bank; Active-Read-Precharge; Burst = 2; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN)); IOUT = 0mA; Address and control inputs changing once per clock cycle	IDD1[a]	TBD	TBD	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: (IDD2P Condition) All device banks idle; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = (LOW)	IDD2P[b]	TBD	TBD	mA	21, 28, 45
IDLE STANDBY CURRENT: (IDD2F Condition) CS# = HIGH; All device banks are idle; ^{t}CK = ^{t}CK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F[b]	TBD	TBD	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: (IDD3P Condition) One device bank active; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = LOW	IDD3P[b]	TBD	TBD	mA	21, 28, 45
ACTIVE STANDBY CURRENT: (IDD3N Condtion) CS# = HIGH; CKE = HIGH; One device bank active; ^{t}RC = ^{t}RAS (MAX); ^{t}CK = ^{t}CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N[c]	TBD	TBD	mA	42
OPERATING CURRENT: (IDD4R condition) Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); IOUT = 0mA	IDD4R[a]	TBD	TBD	mA	20,43
OPERATING CURRENT: (IDD4W Condtion) Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W[a]	TBD	TBD	mA	20
AUTO REFRESH BURST CURRENT: An AUTO REFRESH command is given to one module rank, and on the next clock cycle the second module rank recieves an AUTO REFRESH command. CKE = HIGH ^{t}RC = ^{t}RC(MIN)	IDD5[b]	TBD	TBD	mA	20, 45
AUTO REFRESH DISTRUBUTED CURRENT: An AUTO REFRESH command is given to one module rank, and on the next clock cycle the second module rank recieves an AUTO REFRESH command; CKE = LOW for ^{t}RFC time ^{t}RC = 7.8125µs	IDD5A[b]	TBD	TBD	mA	24, 45
SELF REFRESH CURRENT: Both module rank are in IDD6 condition, CKE ≤ 0.2V	IDD6[b]	TBD	TBD	mA	9
OPERATING CURRENT: One module rank in IDD7 condtion, one module rank in IDD3N condition. (IDD7 Condtion) Four device bank interleaving READs (BL=4) with auto precharge, ^{t}RC = ^{t}RC (MIN); ^{t}CK = t^{t}CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7[a]	TBD	TBD	mA	20,44

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
b - Value calculated reflects all module ranks in this operating condition.
c - Value calculated as one module rank in this operating condition, and all other module ranks in IDD3N.

Table 17: IDD Specifications and Conditions (MT18VDDS12872H(I))

DDR SDRAM components only

Notes: 1–5, 8, 10,12, 49; notes appear on pages 23–26; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

			MAX			
PARAMETER/CONDITION		**SYMBOL**	**-26A/-265**	**-202**	**UNITS**	**NOTES**
OPERATING CURRENT: (IDD0 Condition) One device bank; Active-Precharge; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		IDD0[a]	TBD	TBD	mA	20, 43
OPERATING CURRENT: (IDD1 Condtion) One device bank; Active-Read-Precharge; Burst = 2; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN)); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1[a]	TBD	TBD	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: (IDD2P Condition) All device banks idle; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = (LOW)		IDD2P[b]	TBD	TBD	mA	21, 28, 45
IDLE STANDBY CURRENT: (IDD2F Condition) CS# = HIGH; All device banks are idle; ^{t}CK = ^{t}CK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F[b]	TBD	TBD	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: (IDD3P Condition) One device bank active; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = LOW		IDD3P[b]	TBD	TBD	mA	21, 28, 45
ACTIVE STANDBY CURRENT: (IDD3N Condtion) CS# = HIGH; CKE = HIGH; One device bank active; ^{t}RC = ^{t}RAS (MAX); ^{t}CK = ^{t}CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N[c]	TBD	TBD	mA	42
OPERATING CURRENT: (IDD4R condition) Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); IOUT = 0mA		IDD4R[a]	TBD	TBD	mA	20, 43
OPERATING CURRENT: (IDD4W Condtion) Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W[a]	TBD	TBD	mA	20
AUTO REFRESH BURST CURRENT: An AUTO REFRESH command is given to one module rank, and on the next clock cycle the second module rank recieves an AUTO REFRESH command. CKE = HIGH	^{t}RC = ^{t}RC(MIN)	IDD5[b]	TBD	TBD	mA	20, 45
AUTO REFRESH DISTRUBUTED CURRENT: An AUTO REFRESH command is given to one module rank, and on the next clock cycle the second module rank recieves an AUTO REFRESH command; CKE = LOW for ^{t}RFC time	^{t}RC = 7.8125µs	IDD5A[b]	TBD	TBD	mA	24, 45
SELF REFRESH CURRENT: Both module rank are in IDD6 condition, CKE ≤ 0.2V		IDD6[b]	TBD	TBD	mA	9
OPERATING CURRENT: One module rank in IDD7 condtion, one module rank in IDD3N condition. (IDD7 Condtion) Four device bank interleaving READs (BL=4) with auto precharge, ^{t}RC = ^{t}RC (MIN); ^{t}CK = t^{t}CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.		IDD7[a]	TBD	TBD	mA	20,44

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

b - Value calculated reflects all module ranks in this operating condition.

c - Value calculated as one module rank in this operating condition, and all other module ranks in IDD3N.

Table 18: Capacitance (MT9VDDT1672H(I), MT9VDDT3272H(I), MT9VDDT6472H(I))

Note: 11; notes appear on pages 23–26

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	4	5	pF
Input Capacitance: Command and Address	C_{I1}	18	27	pF
Input Capacitance: S#	C_{I2}	18	27	pF
Input Capacitance:CK, CK#	C_{I3}	9	12	pF
Input Capacitance: CKE	C_{I4}	18	27	pF

Table 19: Capacitance (MT18VDDS6472H(I), MT18VDDS12872H(I))

Note: 11; notes appear on pages 23–26

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	8	10	pF
Input Capacitance: Command and Address	C_{I1}	36	54	pF
Input Capacitance: S#	C_{I2}	18	27	pF
Input Capacitance:CK, CK#	C_{I3}	15	21	pF
Input Capacitance: CKE	C_{I4}	18	27	pF

Table 20: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–5, 12-15, 29, 49; notes appear on pages 23–26; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

AC CHARACTERISTICS			-335		-26A/-265		-202			
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access window of DQs from CK/ CK#		^{t}AC	-0.7	+0.7	-0.75	0.75	-0.8	0.8	ns	
CK high-level width		^{t}CH	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CK	26
CK low-level width		^{t}CL	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CK	26
Clock cycle time	CL=2.5	^{t}CK (2.5)	6	13	7.5	13	8	13	ns	40, 47
	CL=2	^{t}CK (2)	7.5	13	7.5/10	13	10	13	ns	40, 47
DQ and DM input hold time relative to DQS		^{t}DH	0.45		0.5		0.6		ns	23, 27
DQ and DM input setup time relative to DQS		^{t}DS	0.45		0.5		0.6		ns	23, 27
DQ and DM input pulse width (for each input)		^{t}DIPW	1.75		1.75		2		ns	27
Access window of DQS from CK/CK#		^{t}DQSCK	-0.60	+0.60	-0.75	+0.75	-0.8	+0.8	ns	
DQS input high pulse width		^{t}DQSH	0.35		0.35		0.35		^{t}CK	
DQS input low pulse width		^{t}DQSL	0.35		0.35		0.35		^{t}CK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		^{t}DQSQ		0.45		0.5		0.6	ns	22, 23
Write command to first DQS latching transition		^{t}DQSS	0.75	1.25	0.75	1.25	0.75	1.25	^{t}CK	
DQS falling edge to CK rising - setup time		^{t}DSS	0.2		0.2		0.2		^{t}CK	
DQS falling edge from CK rising - hold time		^{t}DSH	0.2		0.2		0.2		^{t}CK	
Half clock period		^{t}HP	^{t}CH, ^{t}CL		^{t}CH, ^{t}CL		^{t}CH, ^{t}CL		ns	30
Data-out high-impedance window from CK/CK#		^{t}HZ		+0.70		+0.75		+0.8	ns	16, 37
Data-out low-impedance window from CK/CK#		^{t}LZ	-0.70		-0.75		-0.8		ns	16, 38
Address and control input hold time (fast slew rate)		^{t}IH$_F$	.75		.90		1.1		ns	12
Address and control input setup time (fast slew rate)		^{t}IS$_F$	.75		.90		1.1		ns	12
Address and control input hold time (slow slew rate)		^{t}IH$_S$	.80		1		1.1		ns	12
Address and control input setup time (slow slew rate)		^{t}IS$_S$	.80		1		1.1		ns	12
LOAD MODE REGISTER command cycle time		^{t}MRD	12		15		16		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^{t}QH	^{t}HP - ^{t}QHS		^{t}HP - ^{t}QHS		^{t}HP - ^{t}QHS		ns	22, 23
Data hold skew factor		^{t}QHS		0.60		0.75		1	ns	
ACTIVE to PRECHARGE command		^{t}RAS	42	70,000	40	120,000	40	120,000	ns	31
ACTIVE to READ with Auto precharge command	MT9VDDT1672H	^{t}RAP	18		^{t}RAS(MIN) - (burst length * ^{t}CK/2)				ns	41
ACTIVE to READ with Auto precharge command	All others	^{t}RAP	18		20		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^{t}RC	60		65		70		ns	
AUTO REFRESH command period		^{t}RFC	72		75		80		ns	45
ACTIVE to READ or WRITE delay		^{t}RCD	18		20		20		ns	
PRECHARGE command period		^{t}RP	18		20		20		ns	
DQS read preamble		^{t}RPRE	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CK	37
DQS read postamble		^{t}RPST	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	
ACTIVE bank a to ACTIVE bank b command		^{t}RRD	12		15		15		ns	
DQS write preamble		^{t}WPRE	0.25		0.25		0.25		^{t}CK	
DQS write preamble setup time		^{t}WPRES	0		0		0		ns	18, 19

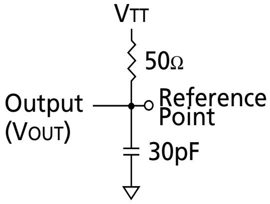
Table 20: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions (Continued)

Notes: 1–5, 12-15, 29, 49; notes appear on pages 23–26; 0°C $\leq T_A \leq$ +70°C; VDD = VDDQ = +2.5V ±0.2V

AC CHARACTERISTICS			-335		-26A/-265		-202			
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
DQS write postamble		^{t}WPST	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	17
Write recovery time		^{t}WR	15		15		15		ns	
Internal WRITE to READ command delay		^{t}WTR	1		1		1		^{t}CK	
Data valid output window		na	^{t}QH - ^{t}DQSQ		^{t}QH - ^{t}DQSQ		^{t}QH - ^{t}DQSQ		ns	22
REFRESH to REFRESH command interval	MT9VDDT1672H	^{t}REFC		140.6		140.6		140.6	µs	21
REFRESH to REFRESH command interval	All others	^{t}REFC		70.3		70.3		70.3	µs	21
Average periodic refresh interval	MT9VDDT1672H	^{t}REFI		15.6		15.6		15.6	µs	21
Average periodic refresh interval	All others	^{t}REFI		7.8		7.8		7.8	µs	21
Terminating voltage delay to VDD		^{t}VTD	0		0		0		ns	
Exit SELF REFRESH to non-READ command		^{t}XSNR	75		75		80		ns	
Exit SELF REFRESH to READ command		^{t}XSRD	200		200		200		^{t}CK	

Notes

1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:

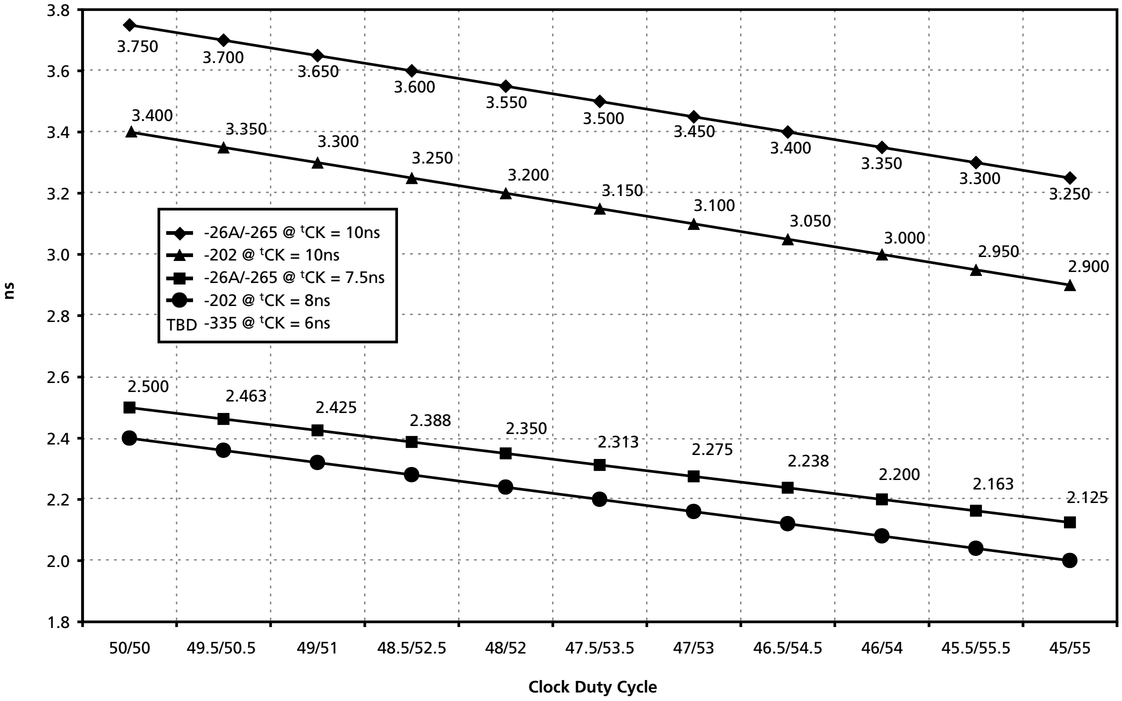


4. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between VIL(AC) and VIH(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on VREF may not exceed ±2 percent of the DC value. Thus, from VDDQ/2, VREF is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest VREF by-pass capacitor.
7. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
8. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for -26A and -202, CL = 2.5 for -265 and -335 with the outputs open.
9. Enables on-chip refresh and address counters.
10. IDD specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. VDD = +2.5V ±0.2V, VDDQ = +2.5V ±0.2V, VREF = VSS, f = 100 MHz, T_A = 25°C, VOUT (DC) = VDDQ/2, VOUT (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. Command/Address input slew rate = 0.5V/ns. For -335 and -265with slew rates 1V/ns and faster, ^{t}IS and ^{t}IH are reduced to 900ps. If the slew rate is less than 0.5V/ ns, timing must be derated: ^{t}IS has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. ^{t}IH has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is VREF.
14. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE ≤ 0.3 x VDDQ is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is VTT.
16. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
20. MIN (^{t}RC or ^{t}RFC) for IDD measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for IDD measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.

21. The refresh period 64ms. This equates to an average refresh rate of 15.625µs (MT9VDDT1672H) or 7.8125µs (MT9VDDT3272H, MT18VDDS6472H, MT9VDDT6472H, and MT18VDDS12872H). However, an AUTO REFRESH command must be asserted at least once every 140.6µs (MT9VDDT1672H) or 70.3µs (MT9VDDT3272H, MT18VDDS6472H, MT9VDDT6472H, and MT18VDDS12872H); burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The valid data window is derived by achieving other specifications - ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55. The Derating Data Valid Window figure is shown below.
23. Each byte lane has a dedicated DQS, with components, DQ0–DQ7.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, VIL(AC) or VIH(AC).
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).
26. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.
28. VDD must not vary more than 4 percent if CKE is not active while any bank is active.

Figure 8: Derating Data Valid Window

(^{t}QH – ^{t}DQSQ)



29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
30. ^{t}HP min is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK/ inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS(MIN) can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch in the nominal voltage must be less than 1/3 of the clock and not more than +400mV or 2.9V maximum, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V minimum, whichever is more positive.
33. Normal Output Drive Curves:
    a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 9, Pull-Down Characteristics.
    b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 9, Pull-Down Characteristics.
    c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 10, Pull-Up Characteristics.
    d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 10, Pull-Up Characteristics.
    e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between .71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
    f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.
34. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. VIH overshoot: VIH (MAX) = VDDQ + 1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL (MIN) = -1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
36. VDD and VDDQ must track each other.
37. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for ^{t}HZ (MAX) and the last DVW. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition. ^{t}LZ (MIN) will prevail over ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
38. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
39. During initialization, VDDQ, VTT, and VREF must be equal to or less than VDD + 0.3V. Alternatively, VTT may be 1.35V maximum during power up, even if VDD/VDDQ are 0V, provided a minimum of 42Ω of series resistance is used between the VTT supply and the input pin.

Figure 9: Pull-Down Characteristics

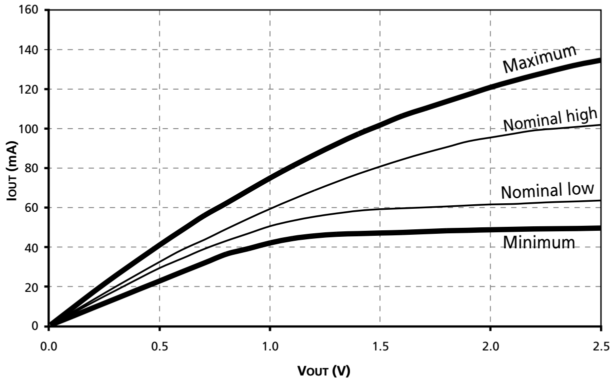
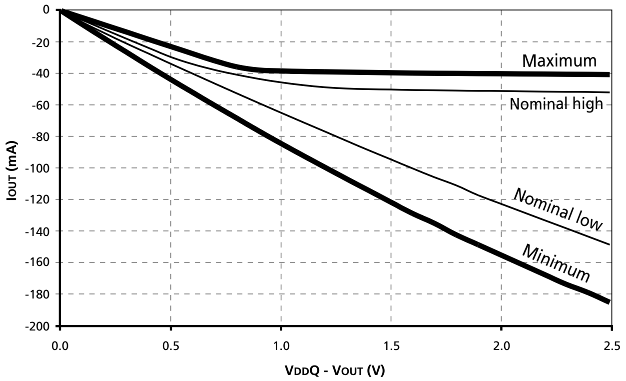


Figure 10: Pull-Up Characteristics



40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. ^{t}RAP ≥ ^{t}RCD.
42. For the -335, -265, and -26A, IDD3N is specified to be 35mA at 100 MHz.
43. Random addressing changing and 50 percent of data changing at every transfer.
44. Random addressing changing and 100 percent of data changing at every transfer.
45. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
46. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is "worst case."
47. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).
48. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
49. The -335 module speed grade, using the -6R speed device, has VDD (MIN) = 2.4V.

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 11, Data Validity, and Figure 12, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 13, Acknowledge Response From Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 11: Data Validity

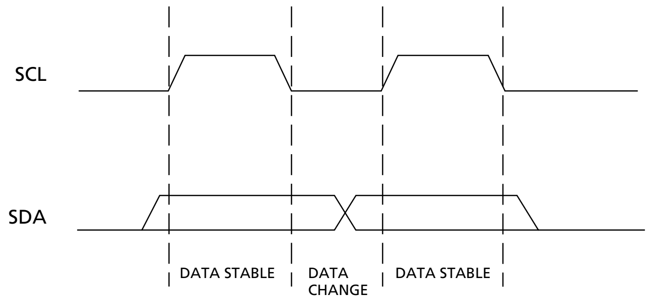


Figure 12: Definition of Start and Stop

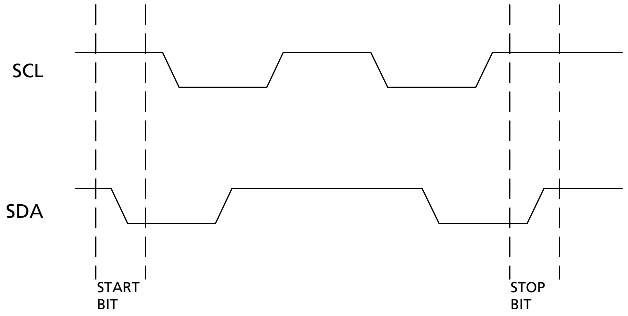


Figure 13: Acknowledge Response From Receiver

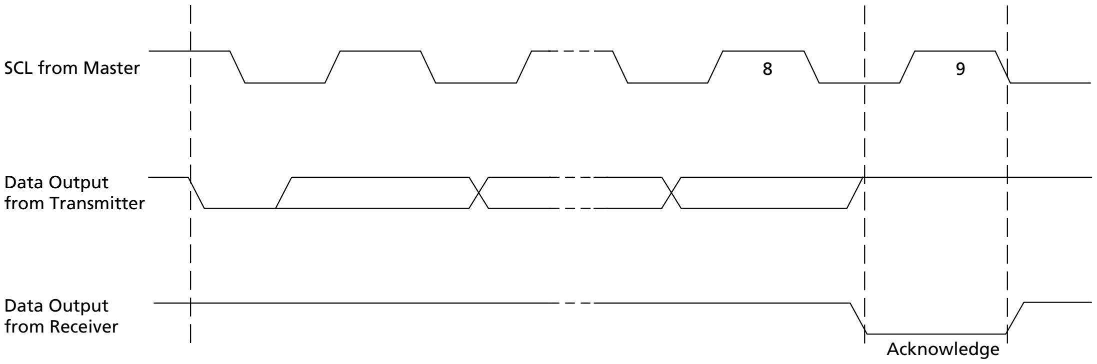


Table 21: EEPROM Device Select Code

Most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			R$\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	R$\overline{W}$
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	R$\overline{W}$

Table 22: EEPROM Operating Modes

MODE	R$\overline{W}$ BIT	$\overline{WC}$	BYTES	INITIAL SEQUENCE
Current Address Read	1	V_{IH} or V_{IL}	1	START, Device Select, R$\overline{W}$ = ‘1’
Random Address Read	0	V_{IH} or V_{IL}	1	START, Device Select, R$\overline{W}$ = ‘0’, Address
	1	V_{IH} or V_{IL}	1	reSTART, Device Select, R$\overline{W}$ = ‘1’
Sequential Read	1	V_{IH} or V_{IL}	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, R$\overline{W}$ = ‘0’
Page Write	0	V_{IL}	≤ 16	START, Device Select, R$\overline{W}$ = ‘0’

Table 23: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DDSPD}	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA

Figure 14: SPD EEPROM Timing Diagram

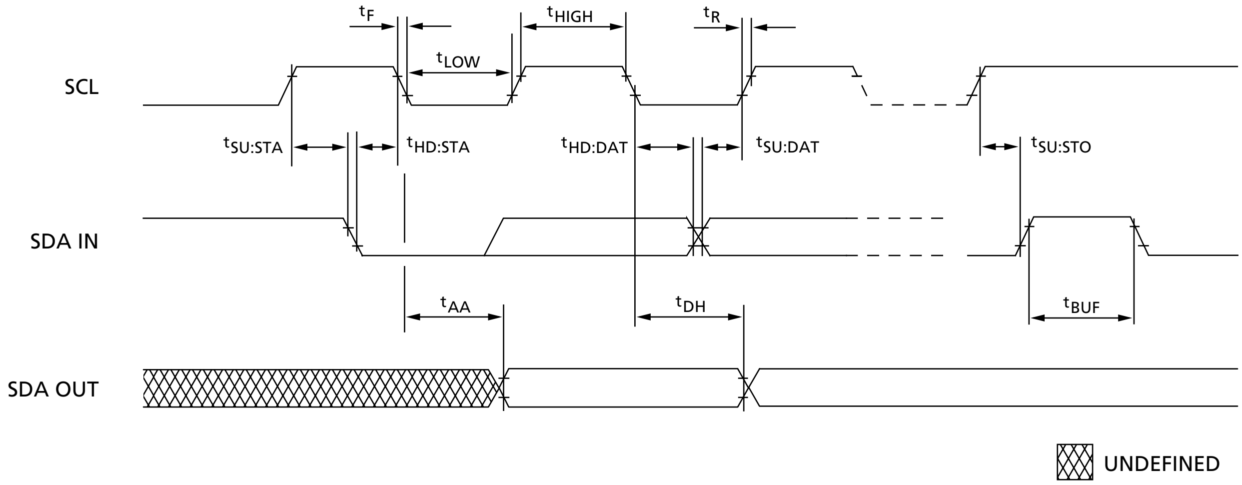


Table 24: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to Vss; VDDSPD = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	^{t}HD:DAT	0		µs	
Start condition hold time	^{t}HD:STA	4		µs	
Clock HIGH period	^{t}HIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	^{t}SU:DAT	250		ns	
Start condition setup time	^{t}SU:STA	4.7		µs	
Stop condition setup time	^{t}SU:STO	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	1

NOTE:

1. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 25: Serial Presence-Detect Matrix (MT9VDDT1672H(I), MT9VDDT3272H(I), MT9VDDT6472H(I))

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT9VDDT1672H	MT9VDDT3272H	MT9VDDT6472H
0	Number of SPD Bytes Used By Micron	128	80	80	80
1	Total Number of Bytes in SPD Device	256	08	08	08
2	Fundamental Memory Type	SDRAM DDR	07	07	07
3	Number of Row Addresses on Assembly	12 or 13	0C	0D	0D
4	Number of Column Addresses on Assembly	10 or 11	0A	0A	0B
5	Number of Physical Ranks on DIMM	1	01	01	01
6	Module Data Width	72	48	48	48
7	Module Data Width (Continued)	0	00	00	00
8	Module Voltage Interface Levels (VDDQ)	SSTL 2.5V	04	04	04
9	SDRAM Cycle Time, (^{t}CK) CAS Latency = 2.5, (See note 1)	6ns (-335) 7ns (-26A) 7.5ns (-265) 8ns (-202)	60 70 75 80	60 70 75 80	60 70 75 80
10	SDRAM Access From Clock, (^{t}AC) CAS Latency = 2.5	0.7ns (-335) 0.75ns (-26A/-265) 0.8ns (-202)	70 75 80	70 75 80	70 75 80
11	Module Configuration Type	ECC	02	02	02
12	Refresh Rate/type	15.62µs, 7.8µs/SELF	80	82	82
13	SDRAM Device Width (Primary DDR SDRAM)	8	08	08	08
14	Error-checking Ddr Sdram Data Width	8	08	08	08
15	Minimum Clock Delay, Back-to-Back Random Column Access	1 clock	01	01	01
16	Burst Lengths Supported	2, 4, 8	0E	0E	0E
17	Number of Banks on DDR SDRAM Device	4	04	04	04
18	CAS Latencies Supported	2, 2.5	0C	0C	0C
19	CS Latency	0	01	01	01
20	WE Latency	1	02	02	02
21	SDRAM Module Attributes	Unbuffered/Diff. Clock	20	20	20
22	SDRAM Device Attributes: General	Fast/Concurrent AP	C0	C0	C0
23	SDRAM Cycle Time, (^{t}CK) CAS Latency = 2 (See note 1)	7.5ns (-335/-26A) 10ns (-265/-202)	75 A0	75 A0	75 A0
24	SDRAM Access from CK, (^{t}AC) CAS Latency = 2	0.7ns (-335) 0.75ns (-26A/-265) 0.8ns (-202)	70 75 80	70 75 80	70 75 80
25	SDRAM Cycle Time, (^{t}CK) CAS Latency = 1.5	N/A	00	00	00
26	SDRAM Access from CK , (^{t}AC) CAS Latency = 1.5	N/A	00	00	00
27	Minimum Row Precharge Time, (^{t}RP)	18ns (-335) 20ns (-202/-265/-26A)	48 50	48 50	48 50
28	Minimum Row Active to Row Active, (^{t}RRD)	12ns (-335) 15ns (-202/-265/-26A)	30 3C	30 3C	30 3C

Table 25: Serial Presence-Detect Matrix (MT9VDDT1672H(I), MT9VDDT3272H(I), MT9VDDT6472H(I)) (Continued)

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT9VDDT1672H	MT9VDDT3272H	MT9VDDT6472H
29	Minimum RAS# to CAS# Delay, (^{t}RCD)	18ns (-335) 20ns (-202/-265/-26A)	48 50	48 50	48 50
30	Minimum RAS# Pulse Width, (^{t}RAS) (See note 2)	42ns 45ns (-26A/-265) 40ns (-202)	2A 2D 28	2A 2D 28	2A 2D 28
31	Module Rank Density	128MB, 256MB, 512MB	20	40	80
32	Address and Command Setup Time, (^{t}IS) Value Set to Slow Slew Rate (^{t}IS$_{S}$), (See note 3)	0.8ns (-335) 1.0ns (-26A/-265) 1.1ns (-202)	80 A0 B0	80 A0 B0	80 A0 B0
33	Address and Command Hold Time, (^{t}IH) Value Set to Slow Slew Rate (^{t}IH$_{S}$), (See note 3)	0.8ns (-335) 1.0ns (-26A/-265) 1.1ns (-202)	80 A0 B0	80 A0 B0	80 A0 B0
34	Data/Data Mask Input Setup Time, (^{t}DS)	0.45ns (-335) 0.5ns (-26A/-265) 0.6ns (-202)	45 50 60	45 50 60	45 50 60
35	Data/Data Mask Input Hold Time, (^{t}DH)	0.45ns (-335) 0.5ns (-26A/-265) 0.6ns (-202)	45 50 60	45 50 60	45 50 60
36-40	Reserved		00	00	00
41	Min Active Auto Refresh Time (^{t}RC)	60ns (-335) 65ns (-26A/-265) 70ns (-202)	3C 41 46	3C 41 46	3C 41 46
42	Minimum Auto Refresh to Active/ Auto Refresh Command Period, (^{t}RFC)	72ns (-335) 75ns (-26A/-265) 80ns (-202)	48 4B 50	48 4B 50	48 4B 50
43	SDRAM Device Max Cycle Time (^{t}CKMAX)	12ns (-335) 13ns (-202/-265/-26A)	30 34	30 34	30 34
44	SDRAM Device Max DQS-DQ Skew Time (^{t}DQSQ)	0.45ns (-335) 0.5ns (-26A/-265) 0.6ns (-202)	2D 32 3C	2D 32 3C	2D 32 3C
45	SDRAM Device Max Read Data Hold Skew Factor (^{t}QHS)	0.6ns (-335) 0.75ns (-26A/-265) 1.0ns (-202)	60 75 A0	60 75 A0	60 75 A0
46-61	Reserved		00	00	00
62	SPD Revision	Release 0.0	00	00	00
63	Checksum For Bytes 0-62	-335 -26A -265 -202	10 C5 F5 90	33 E8 18 B3	74 29 59 F4
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C	2C
65-71	Manufacturer's JEDEC ID Code	(Continued)	FF	FF	FF
72	Manufacturing Location	01–11	01–B0	01–B0	01–B0
73-90	Module Part Number (ASCII)		Variable Data	Variable Data	Variable Data
91	PCB Identification Code	1-9	01-09	01-09	01-09

Table 25: Serial Presence-Detect Matrix (MT9VDDT1672H(I), MT9VDDT3272H(I), MT9VDDT6472H(I)) (Continued)

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT9VDDT1672H	MT9VDDT3272H	MT9VDDT6472H
92	Identification Code (Continued)	0	00	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data	Variable Data
94	Week of Manufacture in BCD		Variable Data	Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data	Variable Data
99-127	Manufacturer- Specific Data (RSVD)		–	–	–

NOTE:

1. Device latencies used for SPD values.
2. The value of ^{t}RAS used for -26A/-265 modules is calculated from ^{t}RC - ^{t}RP. Actual device spec value is 40 ns.
3. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.

Table 26: Serial Presence-Detect Matrix (MT18VDDS6472H(I), MT18VDDS12872H(I))

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT18VDDS6472H	MT18VDDS12872H
0	Number of SPD Bytes Used By Micron	128	80	80
1	Total Number of Bytes in SPD Device	256	08	08
2	Fundamental Memory Type	SDRAM DDR	07	07
3	Number of Row Addresses on Assembly	13	0D	0D
4	Number of Column Addresses on Assembly	10 or 11	0A	0B
5	Number of Physical Ranks on DIMM	2	02	02
6	Module Data Width	72	48	48
7	Module Data Width (Continued)	0	00	00
8	Module Voltage Interface Levels (VDDQ)	SSTL 2.5V	04	04
9	SDRAM Cycle Time, (^{t}CK) CAS Latency = 2.5, (See note 1)	7ns (-26A) 7.5ns (-265) 8ns (-202)	70 75 80	70 75 80
10	SDRAM Access From Clock,(^{t}AC) CAS Latency = 2.5	0.75ns (-26A/-265) 0.8ns (-202)	75 80	75 80
11	Module Configuration Type	ECC	02	02
12	Refresh Rate/type	7.81µs/SELF	82	82
13	SDRAM Device Width (Primary DDR SDRAM)	8	08	08
14	Error-checking Ddr Sdram Data Width	8	08	08
15	Minimum Clock Delay, Back-to-Back Random Column Access	1 clock	01	01
16	Burst Lengths Supported	2, 4, 8	0E	0E
17	Number of Banks on DDR SDRAM Device	4	04	04
18	CAS Latencies Supported	2, 2.5	0C	0C
19	CS Latency	0	01	01
20	WE Latency	1	02	02
21	SDRAM Module Attributes	Unbuffered/Diff. Clock	20	20
22	SDRAM Device Attributes: General	Fast/Concurrent AP	C0	C0
23	SDRAM Cycle Time, (^{t}CK) CAS Latency = 2 (See note 1)	7.5ns (-26A) 10ns (-265/-202)	75 A0	75 A0
24	SDRAM Access from CK , (^{t}AC) CAS Latency = 2	7.5ns (-26A/-265) 8ns (-202)	75 80	75 80
25	SDRAM Cycle Time, (^{t}CK) CAS Latency = 1.5	N/A	00	00
26	SDRAM Access From CK , (^{t}AC) (CAS Latency = 1.5)	N/A	00	00
27	Minimum Row Precharge Time, (^{t}RP)	20 ns	50	50
28	Minimum Row Active to Row Active, (^{t}RRD)	15 ns	3C	3C
29	Minimum RAS# to CAS# Delay, (^{t}RCD)	20 ns	50	50
30	Minimum RAS# Pulse Width, (^{t}RAS) (See note 2)	45ns (-26A/-265) 40ns (-202)	2D 28	2D 28
31	Module Rank Density	256MB, 512MB	40	80
32	Address and Command Setup Time, (^{t}IS) Value Set to Slow Slew Rate (^{t}IS$_S$), (See note 3)	1.0ns (-26A/-265) 1.1ns (-202)	A0 B0	A0 B0

Table 26: Serial Presence-Detect Matrix (MT18VDDS6472H(I), MT18VDDS12872H(I)) (Continued)

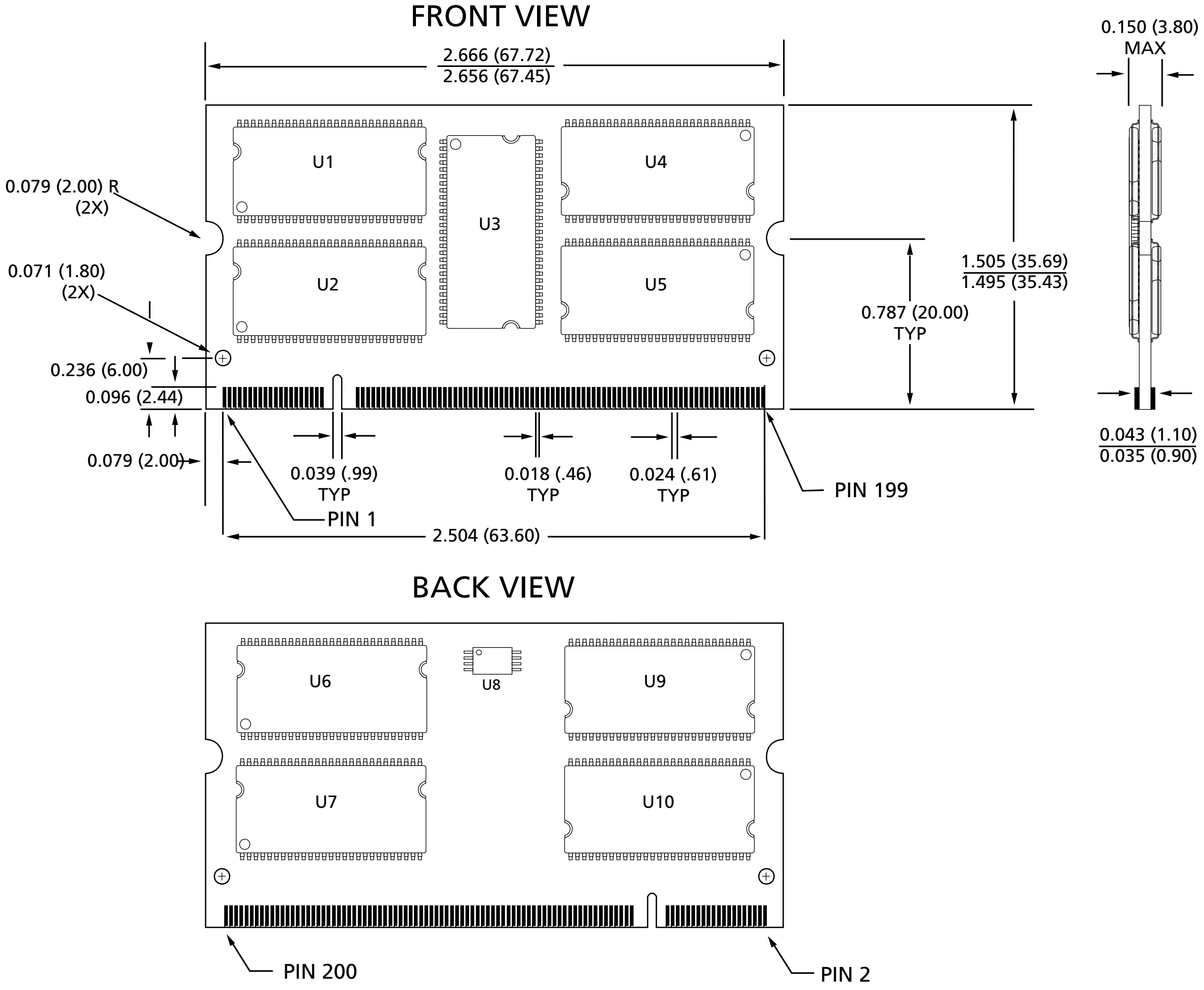
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT18VDDS6472H	MT18VDDS12872H
33	Address and Command Hold Time, (^{t}IH) Value set to Slow Slew Rate ($^{t}IH_S$), (See note 3)	1.0ns (-26A/-265) 1.1ns (-202)	A0 B0	A0 B0
34	Data/Data Mask Input Setup Time, (^{t}DS)	0.5ns (-26A/-265) 0.6ns (-202)	50 60	50 60
35	Data/Data Mask Input Hold Time, (^{t}DH)	0.5ns (-26A/-265) 0.6ns (-202)	50 60	50 60
36-40	Reserved		00	00
41	Min Active Auto Refresh Time (^{t}RC)	65ns (-26A/-265) 70ns (-202)	41 46	41 46
42	Minimum Auto Refresh to Active/ Auto Refresh Command Period, (^{t}RFC)	75ns (-26A/-265) 80ns (-202)	4B 50	4B 50
43	SDRAM Device Max Cycle Time (^{t}CKMAX)	^{t}CK (MAX) = 13.0ns	34	34
44	SDRAM Device Max DQS-DQ Skew Time (^{t}DQSQ)	0.5ns (-26A/-265) 0.6ns (-202)	32 3C	32 3C
45	SDRAM Device Max Read Data Hold Skew Factor (^{t}QHS)	0.75ns (-26A/-265) 1.0ns (-202)	75 A0	75 A0
46-61	Reserved		00	00
62	SPD Revision	Release 0.0	00	00
63	Checksum For Bytes 0-62	-26A -265 -202	E9 19 B4	2A 5A F5
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC ID Code	(Continued)	FF	FF
72	Manufacturing Location	01–11	01–B0	01–B0
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	PCB Identification Code	1-9	01-09	01-09
92	Identification Code (Continued)	0	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data
94	Week of Manufacture in BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-127	Manufacturer- Specific Data (RSVD)		–	–

NOTE:

1. Device latencies used for SPD values.
2. The value of ^{t}RAS used for -26A/-265 modules is calculated from ^{t}RC - ^{t}RP. Actual device spec value is 40 ns.
3. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.

Figure 15: 200-PIN SODIMM DDR Modules



NOTE:

All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Data Sheet Designation

Advance: This datasheet contains initial descriptions of products still under development. This designation applies to part numbers MT18VDDS6472H(I) and MT18VDDS12872H(I).

Released: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur. This designation applies to part numbers MT9VDDT1672H(I), MT9VDDT3272H(I), and MT9VDDT6472H(I).

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