SYNCHRONOUS DRAM MODULE

MT8LSD(T)264A
MT16LSD(T)464A

FEATURES

- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- PC100-compliant functionality (-10A)
- Utilizes 83 MHz, 100 MHz and 125 MHz SDRAM components
- Nonbuffered
- 16MB [MT8LSD(T)264A] and 32MB [MT16LSD(T)464A]
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Dual internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh modes
- 64ms, 4,096-cycle refresh (15.6µs/row)
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

OPTIONS — MARKING

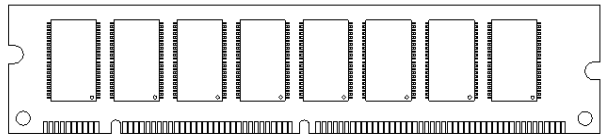
- Components
  - SOJ — D
  - TSOP — DT
- Package
  - 168-pin DIMM (gold) — G
- Frequency/CAS Latency
  - 100 MHz/CL = 3 (8ns SDRAMs) — -10A
  - 66 MHz/CL = 2 (10ns SDRAMs) — -662
  - 66 MHz/CL = 3 (12ns SDRAMs) — -663
- Component Revision Designator
  - Alpha character — Factory Defined
- Printed Circuit Board Revision Designator
  - Numeric character — Factory Defined

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIMES	HOLD TIMES
-10A	-8A	3	6ns	2ns	1ns
-662	-10	2	9ns	3ns	1ns
-663	-12	3	9ns	3ns	1ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#*
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vcc	48	DU	90	Vcc	132	RFU
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1*	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#*	156	DQ59
31	DU	73	Vcc	115	RAS#	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	RFU	81	NC	123	RFU	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	CK1	167	SA2
42	CK0	84	Vcc	126	RFU	168	Vcc

* 32MB version only

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT8LSD264AG-10A__	2 Meg x 64	100 MHz
MT8LSD264AG-662__	2 Meg x 64	66 MHz
MT8LSD264AG-663__	2 Meg x 64	66 MHz
MT8LSDT264AG-10A__	2 Meg x 64	100 MHz
MT8LSDT264AG-662__	2 Meg x 64	66 MHz
MT8LSDT264AG-663__	2 Meg x 64	66 MHz
MT16LSD464AG-10A__	4 Meg x 64	100 MHz
MT16LSD464AG-662__	4 Meg x 64	66 MHz
MT16LSD464AG-663__	4 Meg x 64	66 MHz
MT16LSDT464AG-10A__	4 Meg x 64	100 MHz
MT16LSDT464AG-662__	4 Meg x 64	66 MHz
MT16LSDT464AG-663__	4 Meg x 64	66 MHz

Note: All part numbers end with a two-place code (not shown) designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSDT264AG-10D2.

GENERAL DESCRIPTION

The MT8LSD(T)264A and MT16LSD(T)464A are high-speed CMOS, dynamic random-access 16MB and 32MB solid-state memories organized in a x64 configuration. These modules are configured as dual banks with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-3).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 selects the bank; A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or full page, with burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless high-speed random-access operation.

The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided along with a power-saving power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding the SDRAM operation, refer to the 16Meg: x4, x8 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

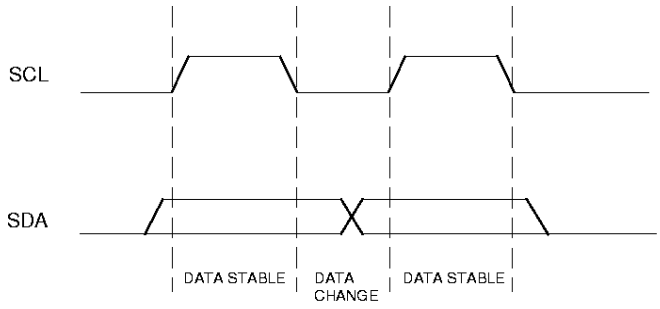


Figure 1
DATA VALIDITY

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

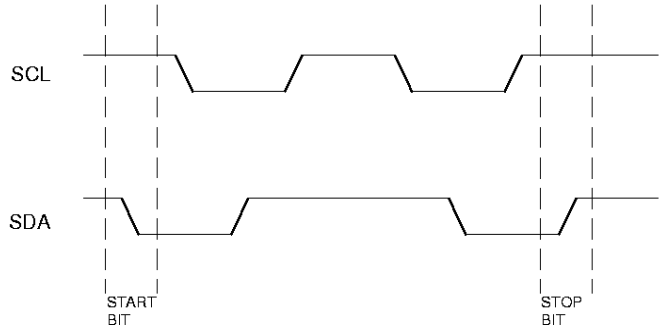


Figure 2
DEFINITION OF START AND STOP

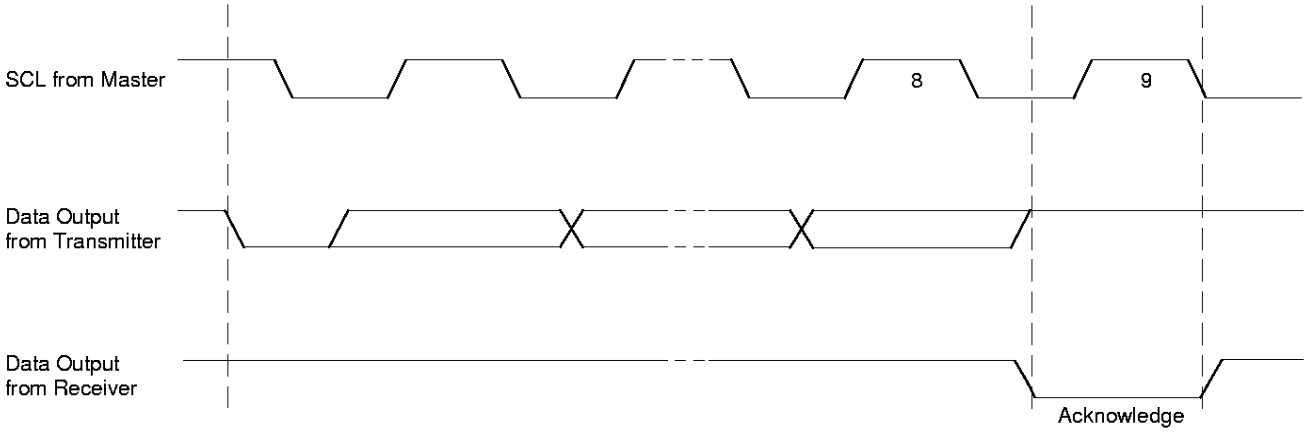
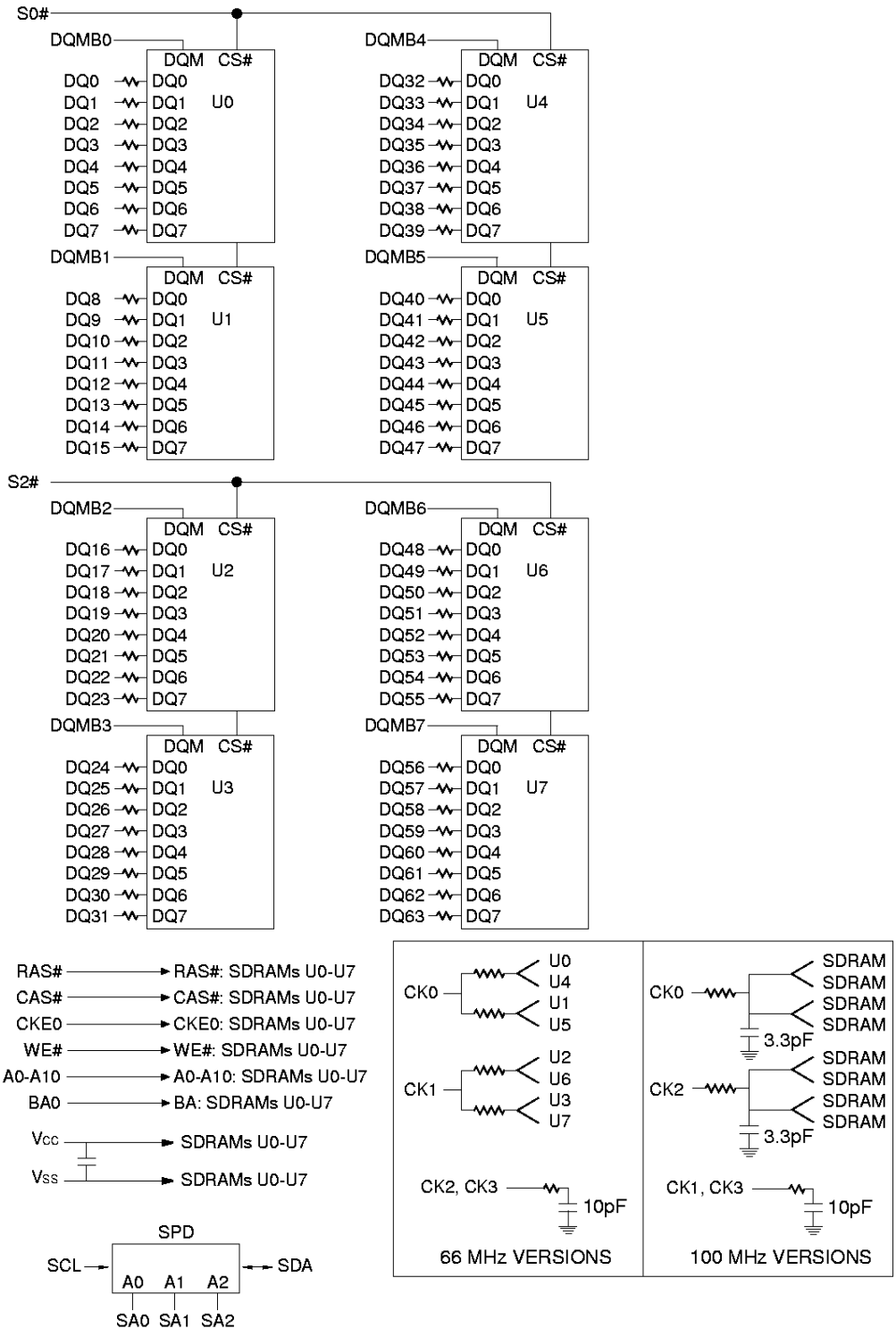


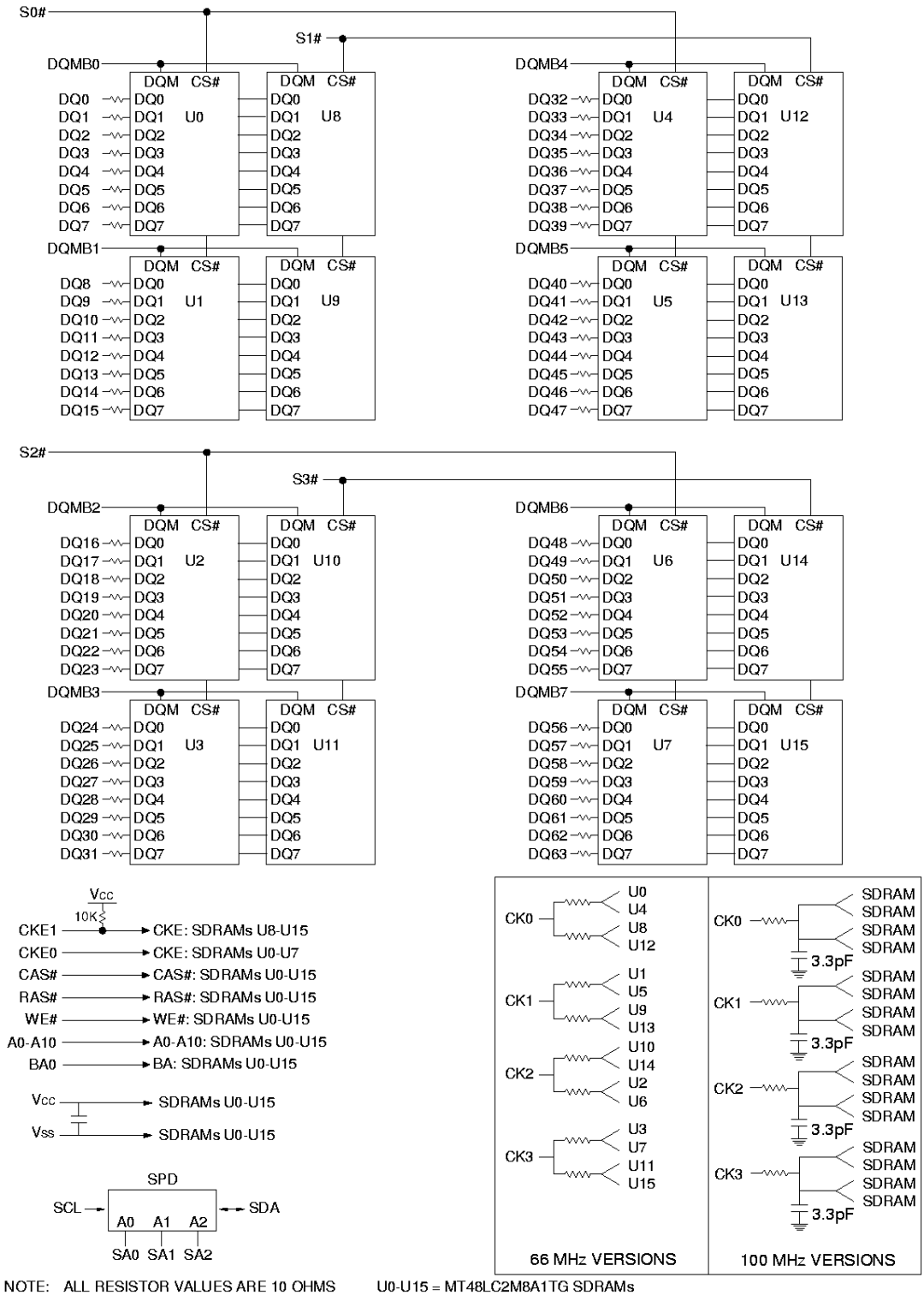
Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

FUNCTIONAL BLOCK DIAGRAM
MT8LSD(T)264A (16MB)



NOTE: ALL RESISTOR VALUES ARE 10 OHMS. U0-U7 = MT48LC2M8A1TG SDRAMs

FUNCTIONAL BLOCK DIAGRAM
MT16LSD(T)464A (32MB)



NOTE: ALL RESISTOR VALUES ARE 10 OHMS UNLESS OTHERWISE SPECIFIED.

U0-U15 = MT48LC2M8A1TG SDRAMs

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
115, 111, 27	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with S0#-S3#) define the command being entered.
42, 79, 125, 163	CK0-CK3	Input	Clock: CK0-CK3 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
63, 128	CKE0, CKE1	Input	Clock Enable: CKE0-CKE1 activate (HIGH) and deactivate (LOW) the CK0-3 signals. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle), or CLOCK SUSPEND operation (burst access in progress). CKE0-CKE1 are synchronous except after the device enters power-down and self refresh modes, where CKE0-CKE1 become asynchronous until after exiting the same mode. The input buffers, including CK0-3, are disabled during power-down and self refresh modes, providing low standby power.
30, 45, 114, 129	S0#-S3#	Input	Chip Select: S0#-S3# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0#-S3# are registered HIGH. S0#-S3# are considered part of the command code.
28-29, 46-47, 112-113, 130-131	DQMB0-DQMB7	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
122	BA0	Input	Bank Address: BA0 defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 is also used to program the twelfth bit of the mode register.
33-38, 117-121	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row address A0-A10) and READ/WRITE command (column address A0-A8 with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2-5, 7-11, 13-17, 19-20, 153-156, 158-161	DQ0-DQ63	Input/ Output	Data I/O: Data bus.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{CC}	Supply	Power Supply: +3.3V ±0.3V.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	Vss	Supply	Ground.
82	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
83	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
39, 123, 126, 132	RFU	—	Reserved for Future Use: These pins should be left unconnected.
31, 44, 48	DU	—	Don't Use: These pins are not connected on these modules but are assigned pins on the compatible DRAM version.

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128		1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256		0	0	0	0	1	0	0	0	08
2	MEMORY TYPE	SDRAM		0	0	0	0	0	1	0	0	04
3	NUMBER OF ROW ADDRESSES	11		0	0	0	0	1	0	1	1	0B
4	NUMBER OF COLUMN ADDRESSES	9		0	0	0	0	1	0	0	1	09
5	NUMBER OF BANKS	1 (16MB)		0	0	0	0	0	0	0	1	01
		2 (32MB)		0	0	0	0	0	0	1	0	02
6	MODULE DATA WIDTH	64		0	1	0	0	0	0	0	0	40
7	MODULE DATA WIDTH (continued)	0		0	0	0	0	0	0	0	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL		0	0	0	0	0	0	0	1	01
9	SDRAM CYCLE TIME	8 (-10A)	^{t}CK	1	0	0	0	0	0	0	0	80
	(CAS LATENCY = 3)	10 (-662)		1	0	1	0	0	0	0	0	A0
		12 (-663)		1	1	0	0	0	0	0	0	C0
10	SDRAM ACCESS FROM CLOCK	6 (-10A)	^{t}AC	0	1	1	0	0	0	0	0	60
	(CAS LATENCY = 3)	7.5 (-662)		0	1	1	1	0	1	0	1	75
		9 (-663)		1	0	0	1	0	0	0	0	90
11	MODULE CONFIGURATION TYPE	NONPARITY		0	0	0	0	0	0	0	0	00
12	REFRESH RATE/TYPE	15.6µs/SELF		1	0	0	0	0	0	0	0	80
13	SDRAM WIDTH (PRIMARY SDRAM)	8		0	0	0	0	1	0	0	0	08
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE		0	0	0	0	0	0	0	0	00
15	MINIMUM CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES	1	^{t}CCD	0	0	0	0	0	0	0	1	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE		1	0	0	0	1	1	1	1	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	2		0	0	0	0	0	0	1	0	02
18	CAS LATENCIES SUPPORTED	1, 2, 3		0	0	0	0	0	1	1	1	07
19	CS# LATENCY	0		0	0	0	0	0	0	0	1	01
20	WE# LATENCY	0		0	0	0	0	0	0	0	1	01
21	SDRAM MODULE ATTRIBUTES	NONBUFFERED		0	0	0	0	0	0	0	0	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E		0	0	0	0	1	1	1	0	0E
23	SDRAM CYCLE TIME	13 (-10A)	^{t}CK	1	1	0	1	0	0	0	0	D0
	(CAS LATENCY = 2)	15 (-662/-663)		1	1	1	1	0	0	0	0	F0
24	SDRAM ACCESS FROM CLK	9	^{t}AC	1	0	0	1	0	0	0	0	90
	(CAS LATENCY = 2)											
25	SDRAM CYCLE TIME	30	^{t}CK	0	1	1	1	1	0	0	0	78
	(CAS LATENCY = 1)											
26	SDRAM ACCESS FROM CLK	27	^{t}AC	0	1	1	0	1	1	0	0	6C
	(CAS LATENCY = 1)											
27	MINIMUM ROW PRECHARGE TIME	30 (-662/-10A)	^{t}RP	0	0	0	1	1	1	1	0	1E
		36 (-663)		0	0	1	0	0	1	0	0	24
28	MINIMUM ROW ACTIVE TO ROW ACTIVE	20	^{t}RRD	0	0	0	1	0	1	0	0	14
29	MINIMUM RAS# TO CAS# DELAY	30	^{t}RCD	0	0	0	1	1	1	1	0	1E
30	MINIMUM RAS# PULSE WIDTH	50 (-10A)	^{t}RAS	0	0	1	1	0	0	1	0	32
		60 (-662)		0	0	1	1	1	1	1	0	3C
		72 (-663)		0	1	0	0	1	0	0	0	48
31	MODULE BANK DENSITY	16MB		0	0	0	0	0	1	0	0	04
32-61	RESERVED			-	-	-	-	-	-	-	-	--
62	SPD REVISION	REV. 1		0	0	0	0	0	0	0	1	01

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH" / "driven to LOW."

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
63	CHECKSUM FOR BYTES 0-62	16MB -10A		1	0	1	1	0	0	0	1	B1
		16MB -662		0	0	1	0	0	0	1	0	22
		16MB -663		0	1	1	0	1	1	1	1	6F
		32MB -10A		1	0	1	1	0	0	1	0	B2
		32MB -662		0	0	1	0	0	0	1	1	23
		32MB -663		0	1	1	1	0	0	0	0	70
64	MANUFACTURER'S JEDEC ID CODE	MICRON		0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC ID CODE (CONT.)			1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION			0	0	0	0	0	0	0	1	01
				0	0	0	0	0	0	1	0	02
				0	0	0	0	0	0	1	1	03
				0	0	0	0	0	1	0	0	04
73-90	MODULE PART NUMBER (ASCII)			x	x	x	x	x	x	x	x	x
91	PCB REVSION CODE	A		0	0	0	0	0	0	0	1	01
		B		0	0	0	0	0	0	1	0	02
		C		0	0	0	0	0	0	1	1	03
		D		0	0	0	0	0	1	0	0	04
92	REVISION CODE (CONT.)	0		0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	x
94	WEEK OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	x
95-98	MODULE SERIAL NUMBER			x	x	x	x	x	x	x	x	x
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)			-	-	-	-	-	-	-	-	-
126	SYSTEM FREQUENCY FOR 66 MHz	66 MHz		0	1	1	0	0	1	1	0	66
127	CAS LATENCY FOR 66 MHz	CL2		0	0	0	0	0	1	1	0	06
		CL3		0	0	0	0	0	1	0	0	04

COMMANDS

Truth Table 1 provides a quick reference of available commands.

TRUTH TABLE 1 – Commands and DQMB Operation

(Notes: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	X	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	X	Bank/Col	VALID	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	2
Write enable/output enable	-	-	-	-	L	-	Active	8
Write inhibit/output High-Z	-	-	-	-	H	-	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0 through A10 and BA0 define the op-code written to the mode register.
3. A0 through A10 provide row address, and BA0 determines which bank is made active (BA0 LOW = Bank 0 and BA0 HIGH = Bank 1).
4. A0 through A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0 determines which bank is being read from or written to (BA0 LOW = Bank 0 and BA0 HIGH = Bank 1).
5. A10 LOW: BA0 determines bank being precharged (BA0 LOW = Bank 0 and BA0 HIGH = Bank 1). A10 HIGH: both banks precharged and BA0 is a "don't care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "don't care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

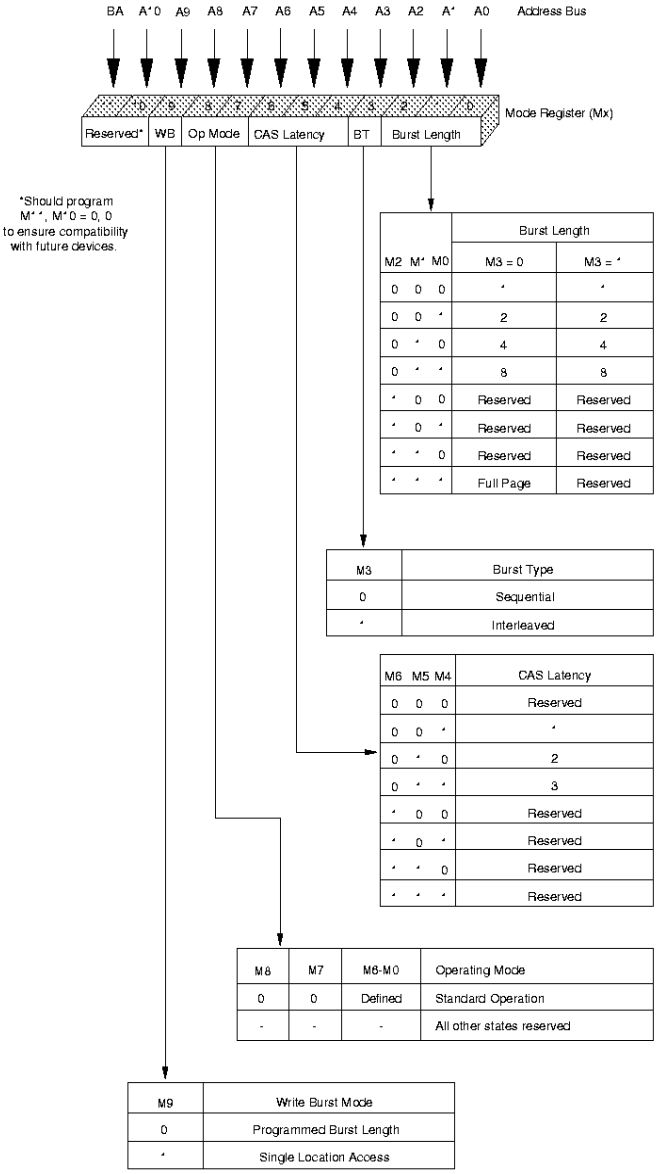


Figure 1
MODE REGISTER DEFINITION

Table 1
BURST DEFINITION

Burst Length	Starting Column Address	Order of Accesses within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (512)	n = A0-A8 (location 0-511)	Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not Supported

NOTE:
1. For a burst length of two, A1-A8 select the block-of-two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2-A8 select the block-of-four burst; A0-A1 select the starting column within the block.
3. For a burst length of eight, A3-A8 select the block-of-eight burst; A0-A2 select the starting column within the block.
4. For a full-page burst, the full row is selected, and A0-A8 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0-A8 select the unique column to be accessed, and mode register bit M3 is ignored.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to Vss ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3	3.6	V	
Input High (Logic 1) Voltage, All inputs		V_{IH}	2	V_{CC} + 0.3	V	
Input Low (Logic 0) Voltage, All inputs		V_{IL}	-0.3	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	DQMB0-DQMB7	I_{I1}	-4	4	µA	23
	CK0-3, S0#-S3#	I_{I2}	-8	8	µA	
	CKE0-1	I_{I3}	-16	16	µA	
	RAS#, CAS#, A0-A10, BA0, WE#	I_{I4}	-32	32	µA	23
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{CC})	DQ0-DQ63	I_{OZ}	-10	10	µA	23
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

Icc OPERATING CONDITIONS AND MAXIMUM LIMITS

(Note: 1, 6, 13) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -10A	MAX -662	MAX -663	UNITS	NOTES
OPERATING CURRENT: Active Mode, Burst = 2, READ or WRITE, tRC ≥ tRC (MIN), CAS latency = 3	I_{CC1}	16MB	840	720	680	mA	3, 18, 19
		32MB	1,200	1,040	1,000		
STANDBY CURRENT: Power-Down Mode, tCK = 15ns (10ns for -10A), CKE ≤ V_{IL} (MAX), All banks idle	I_{CC2}	16MB	16	16	24	mA	
		32MB	32	32	48		
STANDBY CURRENT: CS# > V_{IH} (MIN), tCK = 15ns (10ns for -10A), CKE ≥ V_{IH} (MIN), All banks idle	I_{CC3}	16MB	240	200	200	mA	12, 19
		32MB	480	400	400		
STANDBY CURRENT: CS# ≥ V_{IH} (MIN), tCK = 15ns (10ns for -10A), CKE ≥ V_{IH} (MIN), All banks active after tRCD met, No accesses in progress	I_{CC4}	16MB	360	320	320	mA	12, 19
		32MB	720	640	640		
OPERATING CURRENT: Burst Mode, Continuous burst, READ or WRITE, tCK = 15ns (10ns for -10A), All banks active, Addresses transition once per clock cycle, CAS latency = 3	I_{CC5}	16MB	760	680	640	mA	3, 18, 19
		32MB	1,120	1,000	960		
AUTO REFRESH CURRENT: tRC ≥ tRC (MIN), CAS latency = 3	I_{CC6}	16MB	760	680	640	mA	3, 18, 19
		32MB	1,120	1,000	960		
SELF REFRESH CURRENT: CKE ≤ 0.2V	I_{CC7}	16MB	16	16	16	mA	4
		32MB	32	32	32		

CAPACITANCE

		MAX			
PARAMETER	SYMBOL	16MB	32MB	UNITS	NOTES
Input Capacitance: A0-A10, BA0, RAS#, CAS#, WE#	C_{I1}	45	88	pF	2
Input Capacitance: S0#-S3#, CK0-CK3	C_{I2}	25	25	pF	2
Input Capacitance: CKE0, CKE1	C_{I3}	45	45	pF	2
Input Capacitance: DQMB0#-DQMB7#	C_{I4}	8	14	pF	2
Input Capacitance: SCL, SA0-SA2	C_{I5}	6	6	pF	2
Input/Output Capacitance: DQ0-DQ63, SDA	C_{IO}	10	15	pF	2

SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11)

AC CHARACTERISTICS			-10A		-662		-663			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (positive edge)	CL = 3	^tAC		6		7.5		9	ns	
	CL = 2	^tAC		9		9		9	ns	
	CL = 1	^tAC		27		27		27	ns	
Address hold time		^tAH	1		1		1		ns	
Address setup time		^tAS	2		3		3		ns	
CLK high-level width		^tCH	3		3.5		3.5		ns	
CLK low-level width		^tCL	3		3.5		3.5		ns	
Clock cycle time	CL = 3	^tCK	8		10		12		ns	
	CL = 2	^tCK	10		15		15		ns	
	CL = 1	^tCK	30		30		30		ns	
CKE hold time		^tCKH	1		1		1		ns	
CKE setup time		^tCKS	2		3		3		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	1		1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	2		3		3		ns	
Data-in hold time		^tDH	1		1		1		ns	
Data-in setup time		^tDS	2		3		3		ns	
Data-out high-impedance time	CL = 3	^tHZ		6		8		9	ns	10
	CL = 2	^tHZ		7		10		10	ns	10
	CL = 1	^tHZ		15		15		15	ns	10
Data-out low-impedance time		^tLZ	1		2		2		ns	
Data-out hold time		^tOH	3		3		3		ns	
ACTIVE to PRECHARGE command period		^tRAS	50	120,000	60	120,000	72	120,000	ns	
AUTO REFRESH and ACTIVE to ACTIVE command period		^tRC	80		90		105		ns	
ACTIVE to READ or WRITE delay		^tRCD	30		30		30		ns	
Refresh period (4,096 cycles)		^tREF		64		64		64	ms	
PRECHARGE command period		^tRP	30		30		36		ns	
ACTIVE bank A to ACTIVE bank B command period		^tRRD	20		20		20		ns	
Transition time		^tT	0.3	1.2	0.3	10	1	20	ns	7
WRITE recovery time		^tWR	1		1		1		^tCK	21
Exit SELF REFRESH to ACTIVE command		^tXSR	80		96		105		ns	20

*Specifications for the SDRAM components used on the module.

AC FUNCTIONAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11)

PARAMETER		SYMBOL	-10A	-662	-663	UNITS	NOTES
READ/WRITE command to READ/WRITE command		tCCD	1	1	1	tCK	17
CKE to clock disable or power-down entry mode		tCKED	1	1	1	tCK	14
CKE to clock enable or power-down exit setup mode		tPED	1	1	1	tCK	14
DQM to input data delay		tDQD	0	0	0	tCK	17
DQM to data mask during WRITEs		tDQM	0	0	0	tCK	17
DQM to data high-impedance during READs		tDQZ	2	2	2	tCK	17
WRITE command to input data delay		tDWD	0	0	0	tCK	17
Data-in to ACTIVE command		tDAL	4	3	4	tCK	15
Data-in to PRECHARGE command		tDPL	1	1	1	tCK	16
Last data-in to PRECHARGE command		tRDL	1	1	1	tCK	17
Last data-in to burst STOP command		tBDL	0	0	0	tCK	17
Last data-in to new READ/WRITE command		tCDL	1	1	1	tCK	17
LOAD MODE REGISTER command to command		tMRD	2	2	2	tCK	17
Data-out to high-impedance from PRECHARGE command	CL = 3	tROH	3	3	3	tCK	17
	CL = 2	tROH	2	2	2	tCK	17
	CL = 1	tROH	1	1	1	tCK	17

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3	3.6	V	
Input High (Logic 1) Voltage, All inputs	V_{IH}	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V	
Input Low (Logic 0) Voltage, All inputs	V_{IL}	-1	$V_{CC} \times 0.3$	V	
OUTPUT LOW VOLTAGE, I_{OUT} = 3mA	V_{OL}		0.4	V	
INPUT LEAKAGE CURRENT, V_{IN} = GND to V_{CC}	I_{LI}		10	µA	
OUTPUT LEAKAGE CURRENT, V_{OUT} = GND to V_{CC}	I_{LO}		10	µA	
STANDBY CURRENT SCL = SDA = V_{CC} - 0.3V, All other inputs = GND or 3.3V +10%	I_{SB}		30	µA	
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I_{CC}		2	mA	

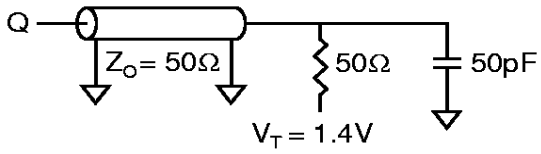
SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	4		µs	
Clock HIGH period	$^{t}HIGH$	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	$^{t}SU:DAT$	250		ns	
Start condition setup time	$^{t}SU:STA$	4.7		µs	
Stop condition setup time	$^{t}SU:STO$	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	24

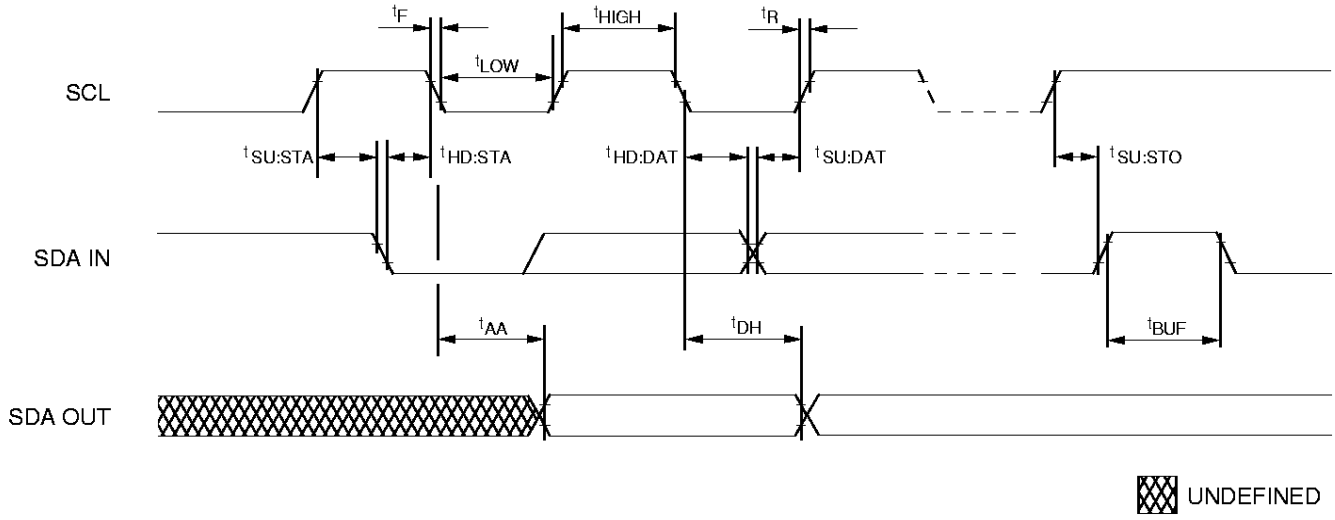
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V ±0.3V; f = 1MHz.
3. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
9. Outputs measured at 1.4V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing tests have VIL = 0V and VIH = 3V with timing referenced to 1.4V crossover point.
12. Other input signals are allowed to transition no more than once in any 30ns period (20ns on -10A) and are otherwise at valid VIH or VIL levels.
13. Icc specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR; clock(s) specified as a reference only at minimum cycle rate.
17. Clocks required are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The Icc current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every 30ns (20ns on -10A).
20. CLK must be toggled a minimum of two times during this period.
21. The SDRAM component is designed to trade off ^{t}RP for faster ^{t}WR, i.e., 30ns and one clock, respectively. However, designs should support a ^{t}WR of two clocks for future compatibility.
22. Based on ^{t}CK = 100 MHz for -8 and 66 MHz for -10.
23. 16MB module values will be half of those shown.
24. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

SPD EEPROM

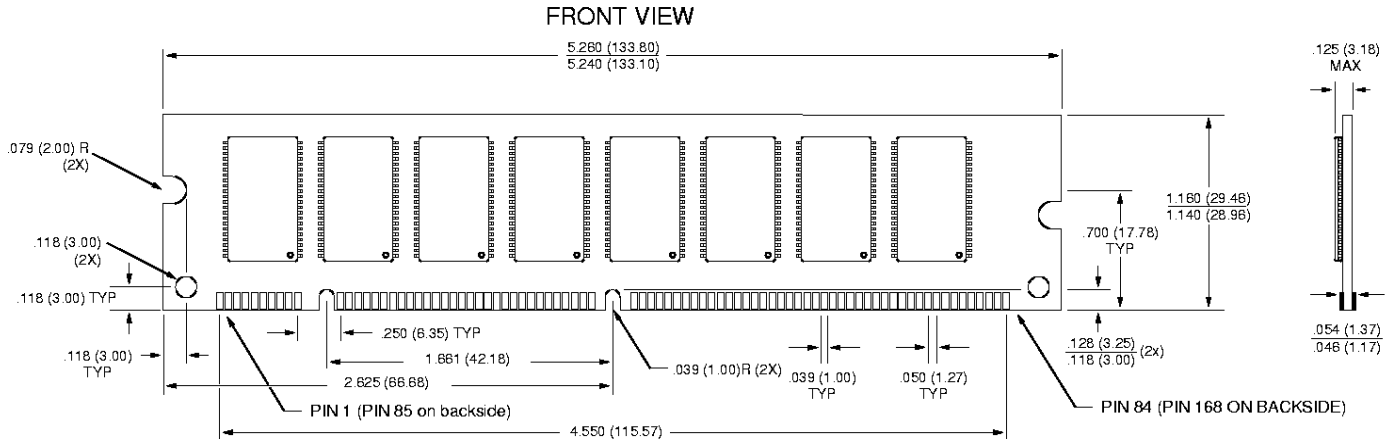


SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

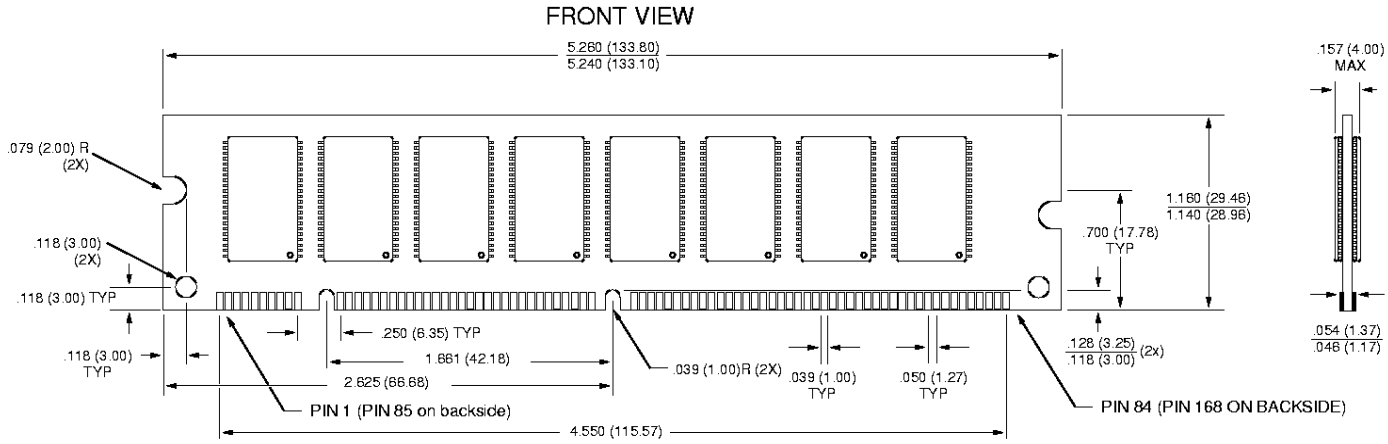
SYMBOL	MIN	MAX	UNITS
tAA	0.3	3.5	µs
tBUF	4.7		µs
tDH	300		ns
tF		300	ns
tHD:DAT	0		µs
tHD:STA	4		µs

SYMBOL	MIN	MAX	UNITS
tHIGH	4		µs
tLOW	4.7		µs
tR		1	µs
tSU:DAT	250		ns
tSU:STA	4.7		µs
tSU:STO	4.7		µs

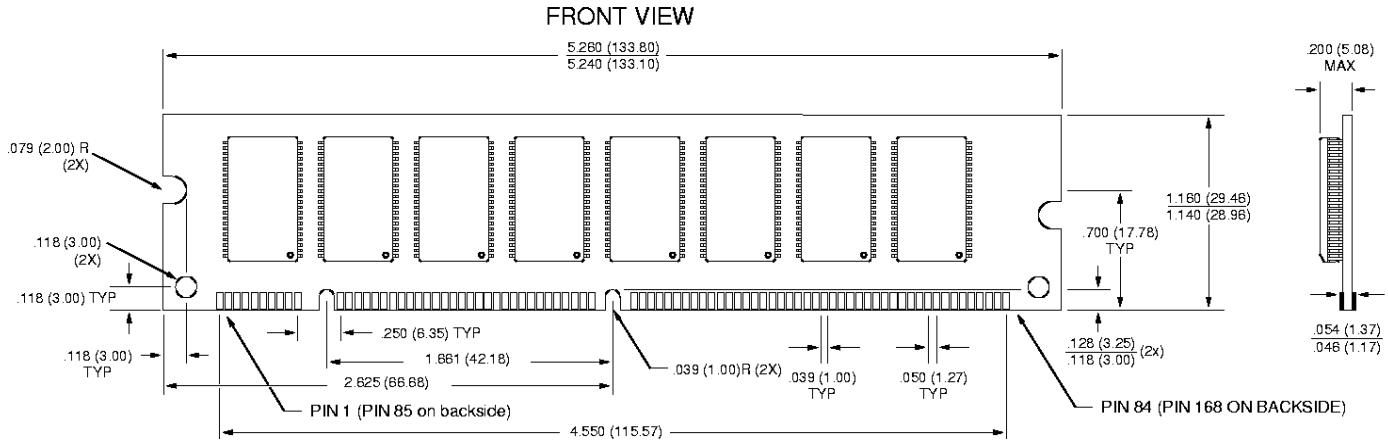
168-PIN DIMM
(MT8LSDT264AG)



168-PIN DIMM
(MT16LSDT464AG)



168-PIN DIMM
(MT8LSD264AG)



168-PIN DIMM
(MT16LSD464AG)