

## Low Voltage PLL Clock Driver

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The MPC991 is a 3.3 V compatible, PLL based ECL/PECL clock driver. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC991 makes the device ideal for Workstation, Mainframe Computer and Telecommunication applications. The MPC991 offers a differential ECL/PECL input for applications which need to lock to an existing clock signal. It also offers a secondary single-ended ECL clock for system test capabilities.

- Fully Integrated PLL
- Output Frequency up to 400 MHz
- ECL/PECL Inputs and Outputs
- Operates from a 3.3 V Supply
- Output Frequency Configurable
- TQFP Packaging
- $\pm 50$  ps Cycle-to-Cycle Jitter

The MPC991 offers three banks of outputs which can each be programmed via the the four fsel pins of the device. There are 16 different output frequency configurations available in the device. The configurations include output ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2. The programming table in this data sheet illustrates the various programming options. The SYNC output monitors the relationship between the Qa and Qc output banks. The output pulses per the timing diagrams in this data sheet signal the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The Sync\_Sel input toggles the Qd outputs between sync signals and extensions to the Qc bank of outputs.

The MPC991 provides a separate output for the feedback to the PLL. This allows for the feedback frequency to be programmed independently of the other outputs allowing for unique input vs output frequency relationships. The fselFB inputs provide 6 different feedback frequencies from the QFB differential output pair.

The MPC991 features an external differential ECL/PECL feedback to the PLL. This external feedback feature allows the MPC991 to be used as a "zero" delay buffer. The propagation delay between the input reference and the output is dependent on the input reference frequency. The selection of higher reference frequencies will provide near zero delay through the device.

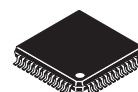
The PLL\_En, Ref\_Sel and the Test\_Clk input pins provide a means of bypassing the PLL and driving the output buffers directly. This allows the user to single step a design during system debug. Note that the Test\_Clk input is routed through the dividers so that depending on the programming several edges on the Test\_Clk input will be needed to get corresponding edge transitions on the outputs. The VCO\_Sel input provides a means of recentering the VCO to provide a broader range of VCO frequencies for stable PLL operation.

If the frequency select or the VCO\_Sel pins are changed during operation, a master reset signal must be applied to ensure output synchronization and phase-lock. If the VCO is driven beyond its maximum frequency, the VCO can outrun the internal dividers when the VCO\_Sel pin is low. This will also prevent the PLL from achieving lock. Again, a master reset signal will need to be applied to allow for phase-lock. The device employs a power-on reset circuit which will ensure output synchronization and PLL lock on initial power-up.

**MPC991**

See Upgrade Product – MPC9991

**LOW VOLTAGE  
PLL CLOCK DRIVER**



**FA SUFFIX**  
52-LEAD TQFP PACKAGE  
CASE 848D-03

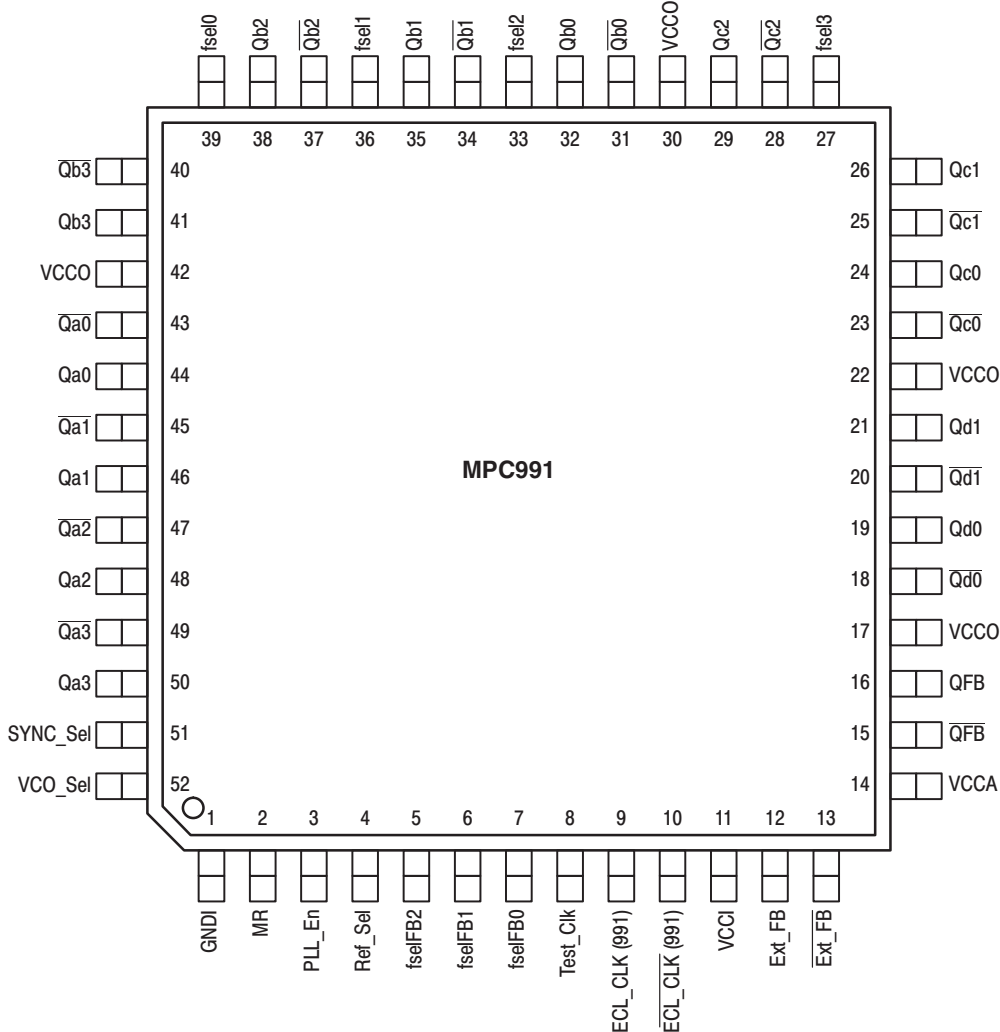


Figure 1. 52-Lead Pinout (Top View)

FUNCTION TABLE 1

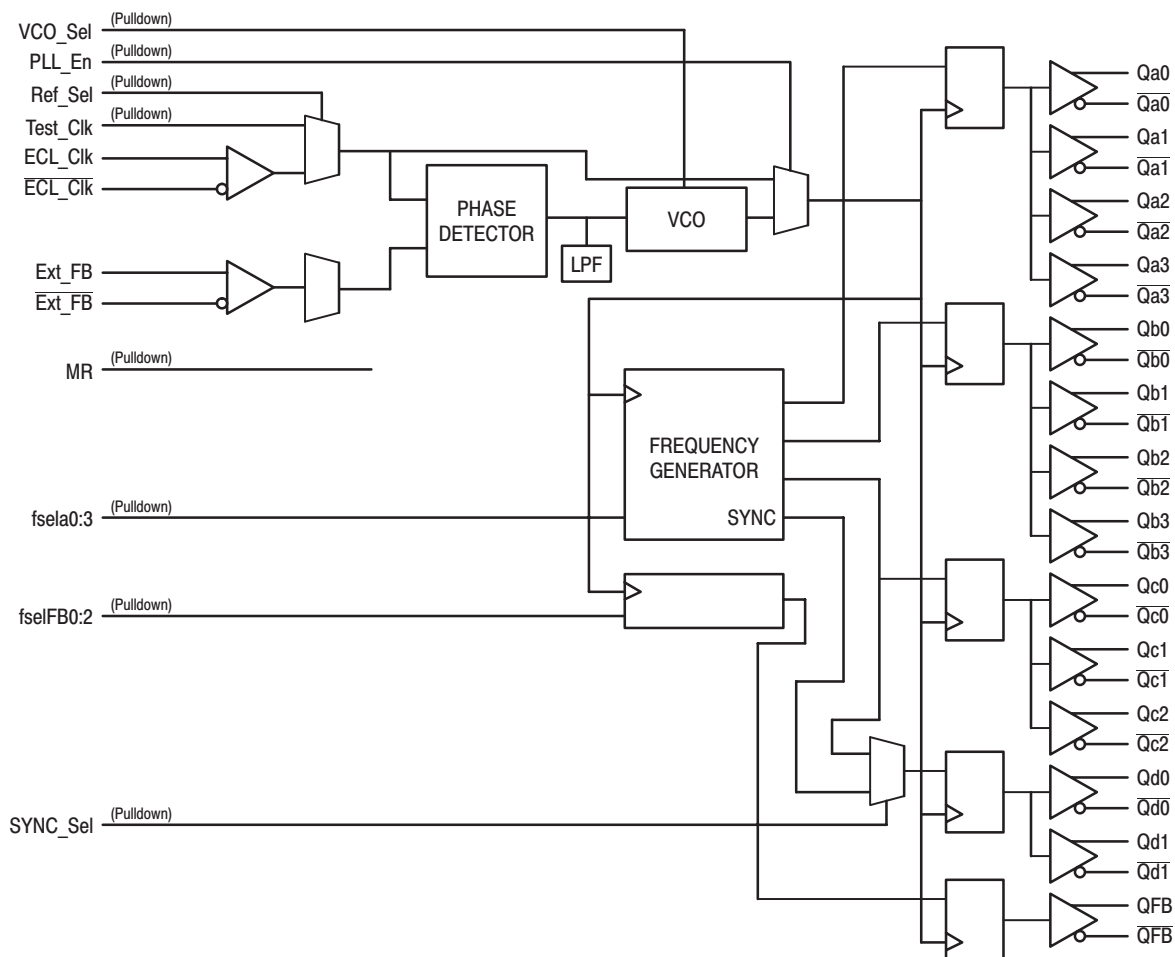
INPUTS				OUTPUTS		
fsel3	fsel2	fsel1	fsel0	Qa	Qb	Qc
0	0	0	0	+2	+2	+2
0	0	0	1	+2	+2	+4
0	0	1	0	+2	+4	+4
0	0	1	1	+2	+2	+6
0	1	0	0	+2	+6	+6
0	1	0	1	+2	+4	+6
0	1	1	0	+2	+4	+8
0	1	1	1	+2	+6	+8
1	0	0	0	+2	+2	+8
1	0	0	1	+2	+8	+8
1	0	1	0	+4	+4	+6
1	0	1	1	+4	+6	+6
1	1	0	0	+4	+6	+8
1	1	0	1	+6	+6	+8
1	1	1	0	+6	+8	+8
1	1	1	1	+8	+8	+8

FUNCTION TABLE 2

fselFB2	fselFB1	fselFB0	QFB
0	0	0	+2
0	0	1	+4
0	1	0	+6
0	1	1	+8
1	0	0	+8
1	0	1	+16
1	1	0	+24
1	1	1	+32

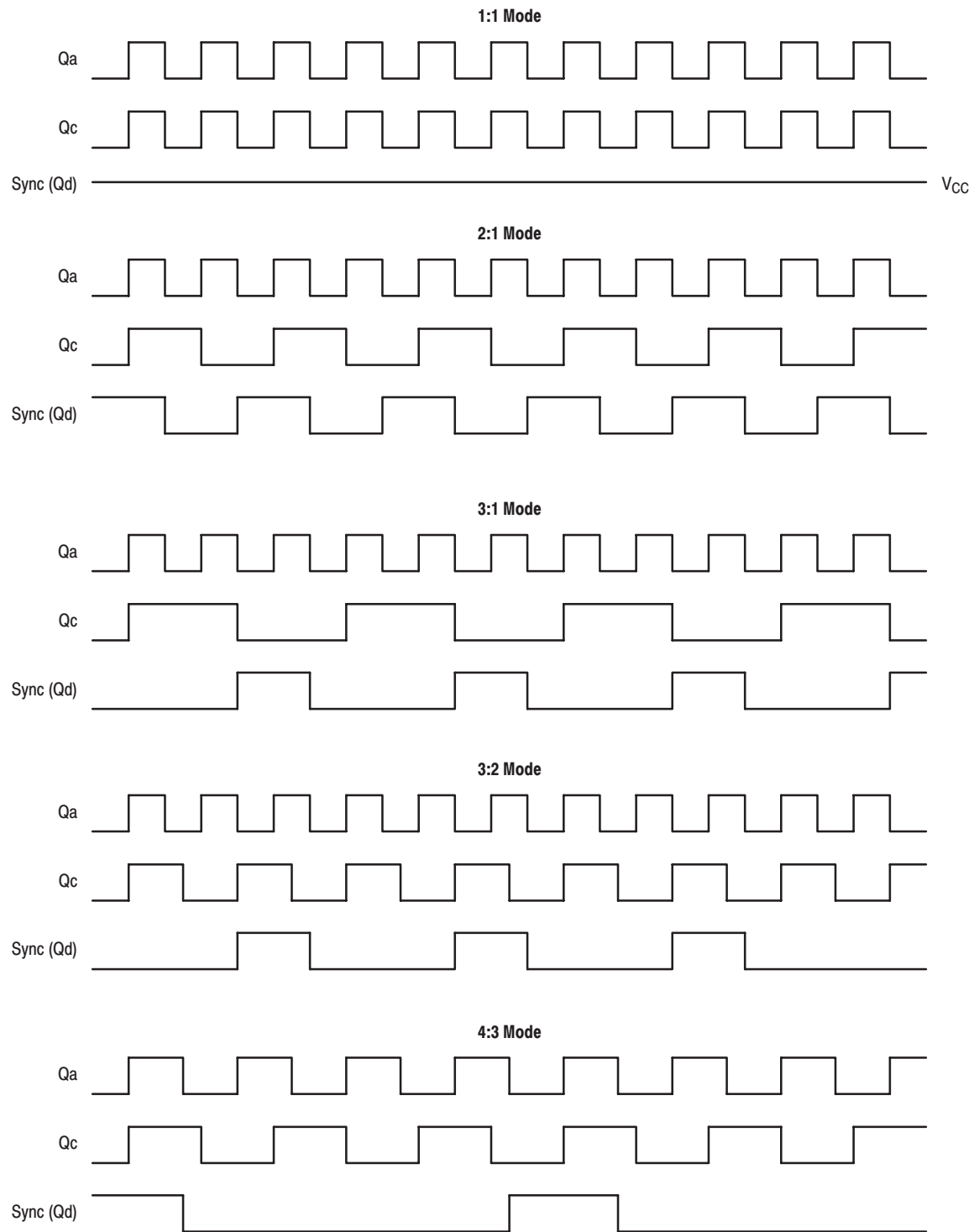
FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
PLL_En	Enable PLL	Bypass PLL
VCO_Sel	fVCO	fVCO/2
Ref_Sel	ECL/PECL	Test_Clk
MR	—	Reset Outputs
SYNC_Sel	SYNC Outputs	Match Qc Outputs



NOTE: ECL\_Clk, Ext\_FB have internal pulldowns, while  $\overline{\text{ECL\_Clk}}$ ,  $\overline{\text{Ext\_FB}}$  have external pullups to ensure stability under open input conditions.

Figure 2. MPC991 Logic Diagram

**Figure 3. Timing Diagrams**

**ECL DC CHARACTERISTICS** ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CCA} = V_{CCI} = V_{CCO} = 0\text{ V}$ ,  $\text{GNDI} = -3.3\text{ V} \pm 5\%$ , Note 1.)

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage	-1.3		-0.7	-1.3	-1.0	-0.7	-1.3		-0.7	V
$V_{OL}$	Output LOW Voltage	-2.0		-1.4	-2.0	-1.7	-1.4	-2.0		-1.4	V
$V_{IH}$	Input HIGH Voltage	-1.1		-0.9	-1.1		-0.9	-1.1		-0.9	V
$V_{IL}$	Input LOW Voltage	-1.8		-1.5	-1.8		-1.5	-1.8		-1.5	V
$V_{PP}$	Minimum Input Swing	500			500			500			mV
$V_{CMR}$	Common Mode Range	$V_{CC}$ -1.3V		$V_{CC}$ -0.5V	$V_{CC}$ -1.3V		$V_{CC}$ -0.5V	$V_{CC}$ -1.3V		$V_{CC}$ -0.5V	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{GNDI}$	Power Supply Current		200	240		200	240		200	240	mA

1. Refer to Motorola Application Note AN1545/D "Thermal Data for MPC Clock Drivers" for thermal management guidelines.

**PECL DC CHARACTERISTICS** ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CCA} = V_{CCI} = V_{CCO} = 3.3\text{ V} \pm 5\%$ ,  $\text{GNDI} = 0\text{ V}$ , Note 2.)

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage (Note 3.)	2.0		2.6	2.0	2.3	2.6	2.3		2.6	V
$V_{OL}$	Output LOW Voltage (Note 3.)	1.3		1.9	1.3	1.6	1.9	1.3		1.9	V
$V_{IH}$	Input HIGH Voltage (Note 3.)	2.2		2.4	2.2		2.4	2.2		2.4	V
$V_{IL}$	Input LOW Voltage (Note 3.)	1.5		1.8	1.5		1.8	1.5		1.8	V
$V_{PP}$	Minimum Input Swing	500			500			500			mV
$V_{CMR}$	Common Mode Range	$V_{CC}$ -1.3V		$V_{CC}$ -0.5V	$V_{CC}$ -1.3V		$V_{CC}$ -0.5V	$V_{CC}$ -1.3V		$V_{CC}$ -0.5V	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{GNDI}$	Power Supply Current		200	240		200	240		200	240	mA

2. Refer to Motorola Application Note AN1545/D "Thermal Data for MPC Clock Drivers" for thermal management guidelines.

3. These values are for  $V_{CC} = 3.3\text{V}$ . Level Specifications will vary 1:1 with  $V_{CC}$ .

**AC CHARACTERISTICS** ( $T_A = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CCA} = V_{CCI} = V_{CCO} = 3.3\text{ V} \pm 5\%$ , Termination of  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ )

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
$t_r, t_f$	Output Rise/Fall Time	0.2		1.0	ns	20% to 80%
$t_{pw}$	Output Duty Cycle	47.5	50	52.5	%	
$t_{os}$	Output-to-Output Skew Same Frequency Different Frequencies		150 250	250 350	ps	
$f_{VCO}$	PLL VCO Lock Range $V_{CO\_Sel} = '0'$ $V_{CO\_Sel} = '1'$	400 200		800 400	MHz	FB +8 to +32 (Note 4.) FB +4 to +32
$t_{pd}$	Ref to Feedback Offset	75	250	425	ps	$f_{ref} = 50\text{MHz}$ (Note 5.)
$f_{max}$	Maximum Output Frequency Qa,Qb,Qc (+2) Qa,Qb,Qc (+4) Qa,Qb,Qc (+6) Qa,Qb,Qc (+8)			400 200 133 100	MHz	
$t_{jitter}$	Cycle-to-Cycle Jitter (Peak-to-Peak)		$\pm 50$		ps	
$t_{lock}$	Maximum PLL Lock Time			10	ms	

4. With  $V_{CO\_Sel} = '0'$ , the PLL will be unstable with a +2, +4 and some +6 feedback configurations. With  $V_{CO\_Sel} = '1'$ , the PLL will be unstable with a +2 feedback ratio.

5.  $t_{pd}$  is specified for 50MHz input reference FB + 8. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The  $t_{pd}$  does not include jitter.

PLL INPUT REFERENCE CHARACTERISTICS (T<sub>A</sub> = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t <sub>r</sub> , t <sub>f</sub>	TCLK Input Rise/Falls		3.0	ns	
f <sub>ref</sub>	Reference Input Frequency VCO_SEL='0'	Feedback divide 6	100	MHz	
		Feedback divide 8	50		
		Feedback divide 16	25		
		Feedback divide 24	16.67		
		Feedback divide 32	12.5		
	VCO_SEL='1'	Feedback divide 4	50		
		Feedback divide 6	33.3		
		Feedback divide 8	25		
		Feedback divide 16	12.5		
		Feedback divide 24	8.33		
		Feedback divide 32	6.25		
f <sub>refDC</sub>	Reference Input Duty Cycle	25	75	%	

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC991 provides a separate power supply for the internal PLL of the device. The purpose of this design technique is to allow the user to filter externally generated system noise from the internal, relatively sensitive analog PLL.

Figure 4 illustrates a suggested power supply filter using an LC filter network. The inductor value should be chosen to maximize the AC filter impedance while maintaining a low DC resistance. An inductor with a maximum DC series resistance of 5 Ω should be used. The parallel capacitor combination on the V<sub>CCA</sub> pin ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

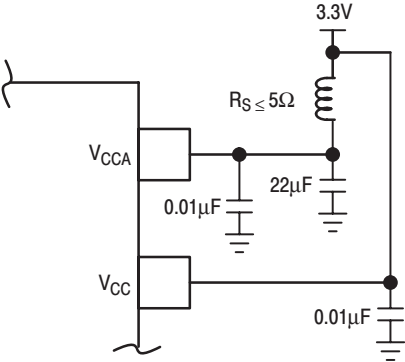


Figure 4. Power Supply Filter