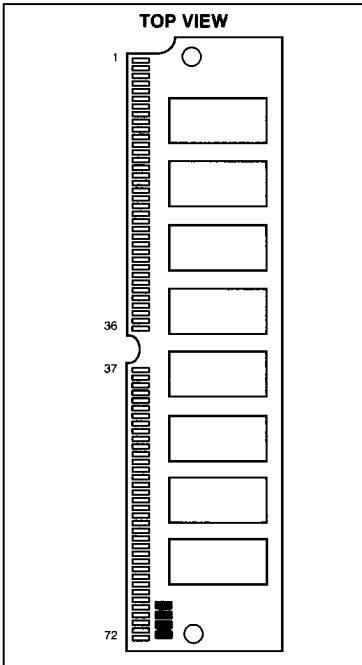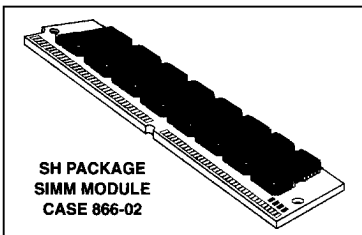# 2M x 32 Bit Dynamic Random Access Memory Module

The MCM32230 is a 64M dynamic random access memory (DRAM) module organized as 2,097,152 x 32 bits. The module is a 72-lead double sided single-in-line memory module (SIMM) consisting of sixteen MCM54400AN DRAMs housed in standard 300 mil SOJ packages mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54400AN is a CMOS high speed, dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM32230 = 16 ms (Max)
  MCM32L230 = 128 ms (Max)
- Consists of Sixteen 1M x 4 DRAMs and Sixteen 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM32230-60 = 60 ns (Max)
  MCM32230-70 = 70 ns (Max)
  MCM32230-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM32230-60 = 5.37 W (Max)
  MCM32230-70 = 4.49 W (Max)
  MCM32230-80 = 3.83 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 130 W (Max)
  CMOS Levels = 88 mW (Max, MCM32230)
  CMOS Levels = 18 mW (Max, MCM32L230)

5

MCM32230
MCM32L230

SH PACKAGE
SIMM MODULE
CASE 866-02

TOP VIEW

PIN NAMES

A0 – A9 . . . . Address Inputs
DQ0 – DQ31 . . . . Data Input/Output
$\overline{CAS0}$ – $\overline{CAS3}$ . . . . . Column Address Strobe
PD1 – PD4 . . . . Presence Detect
$\overline{RAS0}$ – $\overline{RAS3}$ . . . . Row Address Strobe
$\overline{W}$ . . . . Read/Write Input
V_{CC} . . . . Power (+ 5 V)
V_{SS} . . . . Ground
NC . . . . No Connection

All power supply and ground pins must be connected for proper operation of the device.

PIN OUT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ12	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

MOTOD010

PRESENCE DETECT PIN OUT			
Pin Name	60 ns	70 ns	80 ns
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

MOTOD010

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-1 to $+7$	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	-1 to $+7$	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	7.32	W
Operating Temperature Range	T_A	0 to $+70$	°C
Storage Temperature Range	T_{stg}	-55 to $+125$	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPER-ATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	-1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM32230-60, t_{RC} = 110 ns MCM32230-70, t_{RC} = 130 ns MCM32230-80, t_{RC} = 150 ns	I_{CC1}	— — —	976 816 696	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	32	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles MCM32230-60, t_{RC} = 110 ns MCM32230-70, t_{RC} = 130 ns MCM32230-80, t_{RC} = 150 ns	I_{CC3}	— — —	976 816 696	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM32230-60, t_{PC} = 45 ns MCM32230-70, t_{PC} = 45 ns MCM32230-80, t_{PC} = 50 ns	I_{CC4}	— — —	576 576 496	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM32230 MCM32L230	I_{CC5}	— —	16 3.2	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM32230-60, t_{RC} = 110 ns MCM32230-70, t_{RC} = 130 ns MCM32230-80, t_{RC} = 150 ns	I_{CC6}	— — —	976 816 696	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 μs; t_{RAS} = 1 μs; $\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A9 = V_{CC} – 0.2 V or 0.2 V) MCM32L230 only	I_{CC7}	—	2.4	mA	1, 3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	-160	160	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	-20	20	μA	
Output High Voltage ($I_{OH} = -5$ mA)	V_{OH}	2.4	—	V	
Output Low Voltage ($I_{OL} = 4.2$ mA)	V_{OL}	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 μs is only applied to refresh of battery backup. t_{RAS} (max) = 10 μs is applied to functional operating.

MOTOD010

Characteristic	Symbol	Min	Max	Unit	Notes
Input Capacitance (A0 – A9)	C$_{I1}$	—	90	pF	1
Input Capacitance ($\overline{W}$)	C$_{I2}$	—	122	pF	1
Input Capacitance ($\overline{RAS0}$ – $\overline{RAS2}$)	C$_{I3}$	—	38	pF	1
Input Capacitance ($\overline{CAS0}$ – $\overline{CAS3}$)	C$_{I4}$	—	38	pF	1
I/O Capacitance (DQ0 – DQ31)	C$_{DQ}$	—	24	pF	1

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V$_{CC}$ = 5.0 V ± 10%, T$_A$ = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

	Symbol		MCM32230-60 MCM32L230-60		MCM32230-70 MCM32L230-70		MCM32230-80 MCM32L230-80			
Parameter	Std	Alt	Min	Max	Min	Max	Min	Max	Unit	Notes
Random Read or Write Cycle Time	t$_{RELREL}$	t$_{RC}$	110	—	130	—	150	—	ns	5
Fast Page Mode Cycle Time	t$_{CELCEL}$	t$_{PC}$	45	—	45	—	50	—	ns	
Access Time from $\overline{RAS}$	t$_{RELQV}$	t$_{RAC}$	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{CAS}$	t$_{CELQV}$	t$_{CAC}$	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t$_{AVQV}$	t$_{AA}$	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t$_{CEHQV}$	t$_{CPA}$	—	40	—	40	—	45	ns	6
$\overline{CAS}$ to Output in Low-Z	t$_{CELQX}$	t$_{CLZ}$	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t$_{CEHQZ}$	t$_{OFF}$	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t$_T$	t$_T$	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t$_{REHREL}$	t$_{RP}$	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t$_{RELREH}$	t$_{RAS}$	60	10 k	70	10 k	80	10 k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t$_{RELREH}$	t$_{RASP}$	60	100 k	70	100 k	80	100 k	ns	
$\overline{RAS}$ Hold Time	t$_{CELREH}$	t$_{RSH}$	20	—	20	—	20	—	ns	
$\overline{CAS}$ Hold Time	t$_{RELCEH}$	t$_{CSH}$	60	—	70	—	80	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t$_{CEHREH}$	t$_{RHCP}$	40	—	40	—	45	—	ns	
$\overline{CAS}$ Pulse Width	t$_{CELCEH}$	t$_{CAS}$	20	10 k	20	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t$_{RELCEL}$	t$_{RCD}$	20	40	20	50	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	t$_{RELAV}$	t$_{RAD}$	15	30	15	35	15	40	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t$_{CEHREL}$	t$_{CRP}$	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t$_{CEHCEL}$	t$_{CP}$	10	—	10	—	10	—	ns	

(continued)

NOTES:
1. V$_{IH}$ (min) and V$_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between V$_{IH}$ and V$_{IL}$.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V$_{IH}$ and V$_{IL}$ (or between V$_{IL}$ and V$_{IH}$) in a monotonic manner.
4. AC measurements t$_T$ = 5.0 ns.
5. The specification for t$_{RC}$ (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T$_A$ ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V$_{OH}$ = 2.0 V and V$_{OL}$ = 0.8 V.
7. Assumes that t$_{RCD}$ ≤ t$_{RCD}$ (max).
8. Assumes that t$_{RCD}$ ≥ t$_{RCD}$ (max).
9. Assumes that t$_{RAD}$ ≥ t$_{RAD}$ (max).
10. t$_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t$_{RCD}$ (max) limit ensures that t$_{RAC}$ (max) can be met. t$_{RCD}$ (max) is specified as a reference point only; if t$_{RCD}$ is greater than the specified t$_{RCD}$ (max) limit, then access time is controlled exclusively by t$_{CAC}$.
12. Operation within the t$_{RAD}$ (max) limit ensures that t$_{RAC}$ (max) can be met. t$_{RAD}$ (max) is specified as a reference point only; if t$_{RAD}$ is greater than the specified t$_{RAD}$ (max), then access time is controlled exclusively by t$_{AA}$.

MOTOD010

Parameter	Symbol		MCM32230-60 MCM32L230-60		MCM32230-70 MCM32L230-70		MCM32230-80 MCM32L230-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM32230 MCM32L230	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	30	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	

NOTES:
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), th cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.
16. To avoid bus contention and potential damage to the module, $\overline{RAS0}$ and $\overline{RAS1}$ may not be active low simultaneously. Similarly, $\overline{RAS2}$ and $\overline{RAS3}$ may not be simultaneously active low.

MOTOD010

READ CYCLE

EARLY WRITE CYCLE

MOTOD010
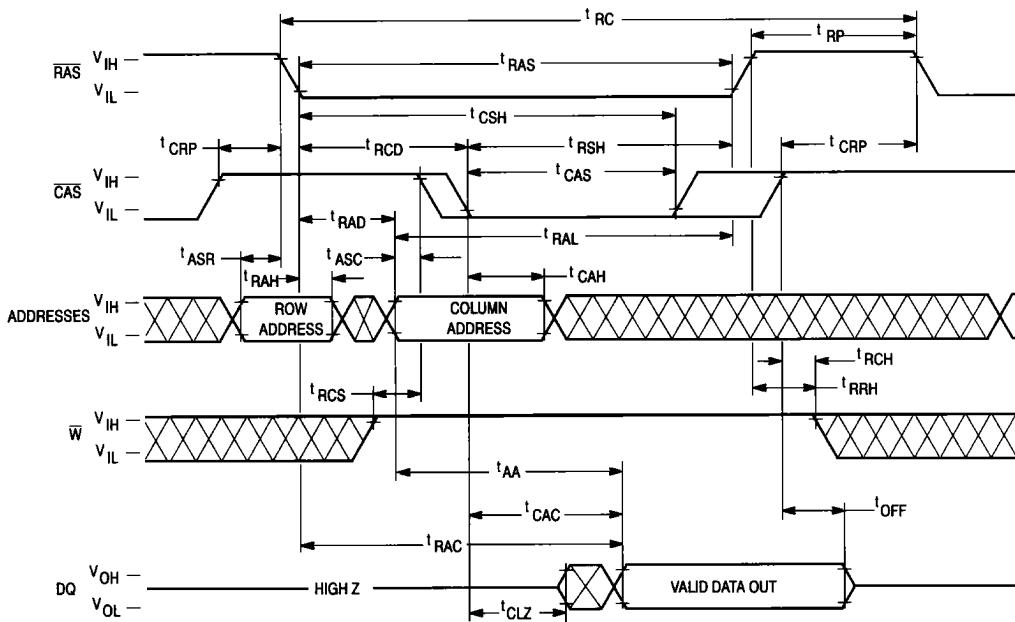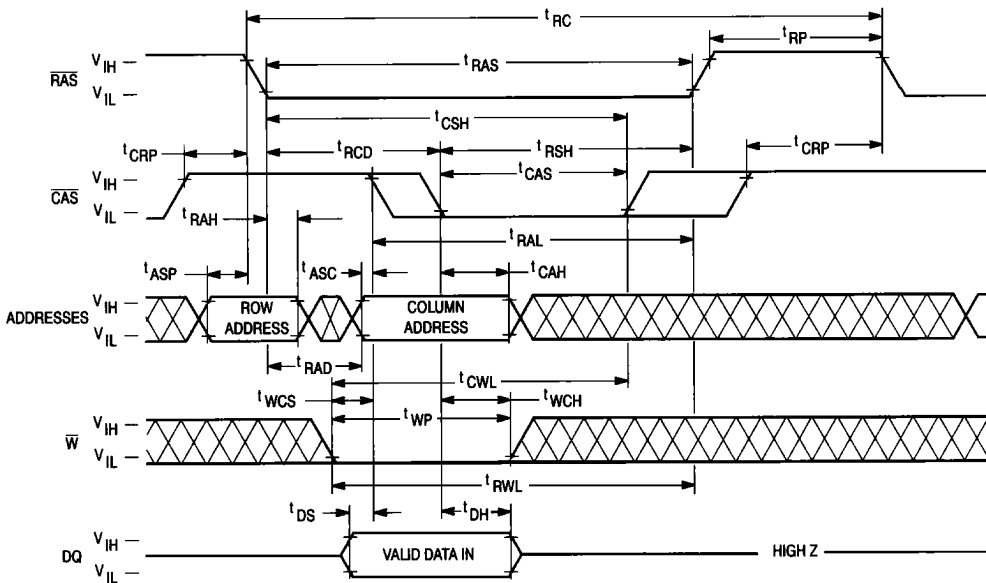
FAST PAGE MODE READ CYCLE
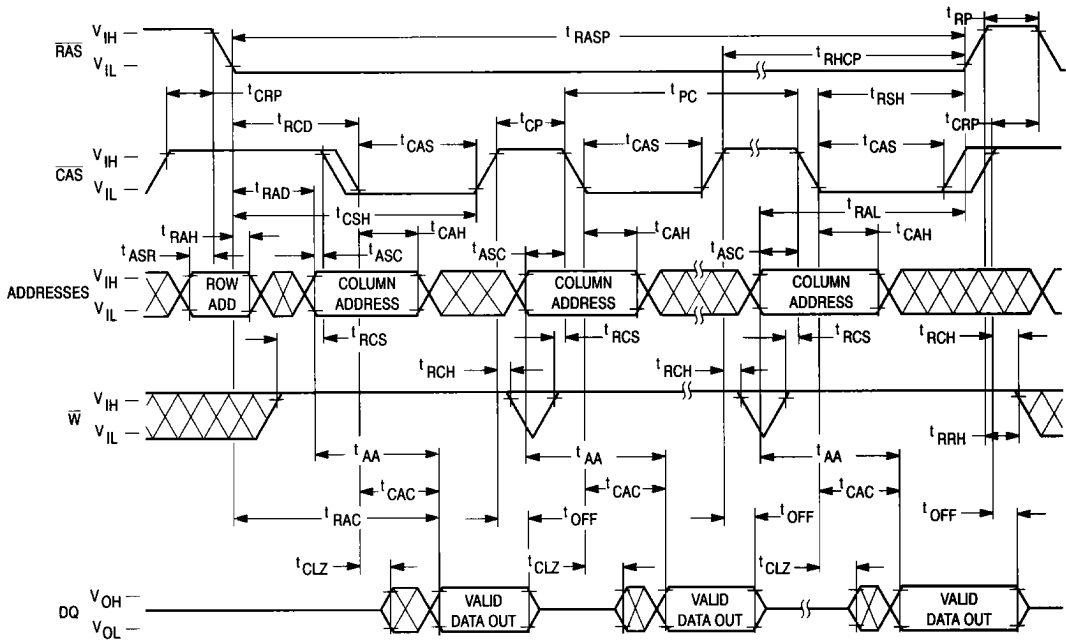
FAST PAGE MODE EARLY WRITE CYCLE

MOTOD010
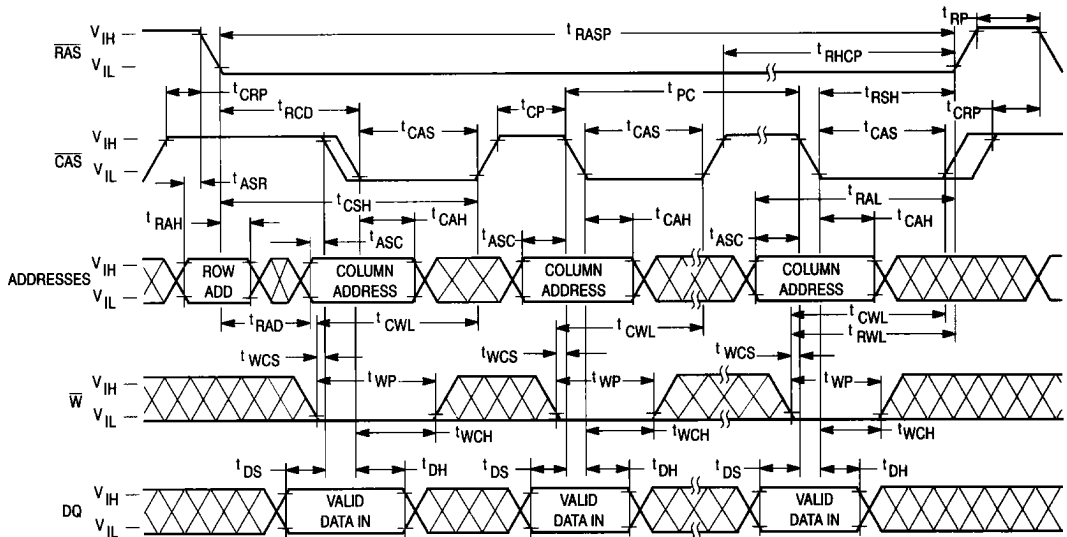
RAS ONLY REFRESH CYCLE
(W̄ Is Don't Care)
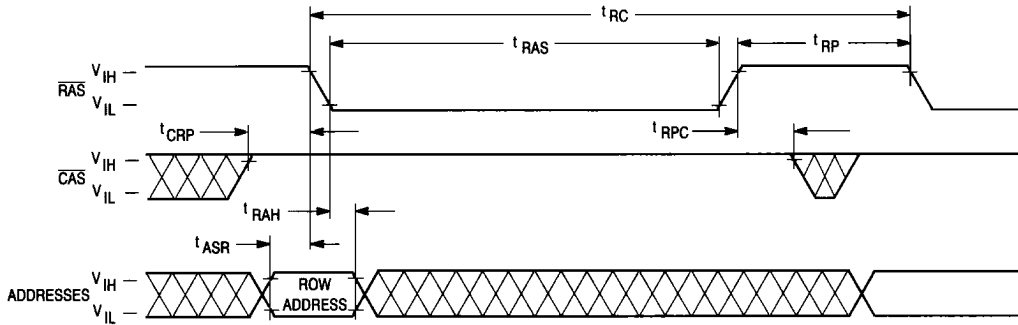
C̄A̅S̅ BEFORE R̄A̅S̅ REFRESH CYCLE
(A0 – A9 are Don't Care)

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MOTOD010
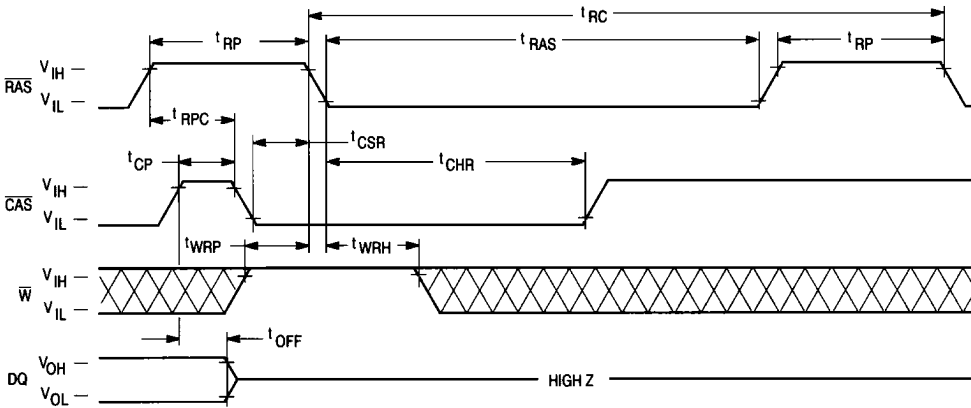
HIDDEN REFRESH CYCLE (READ)
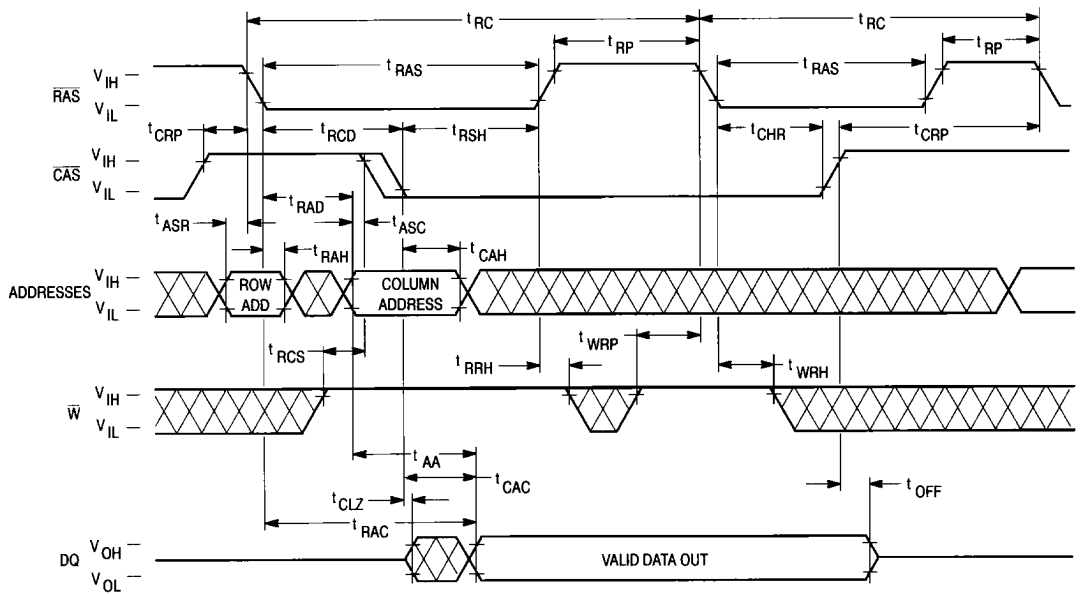
HIDDEN REFRESH CYCLE (EARLY WRITE)

MOTOD010

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MOTOD010
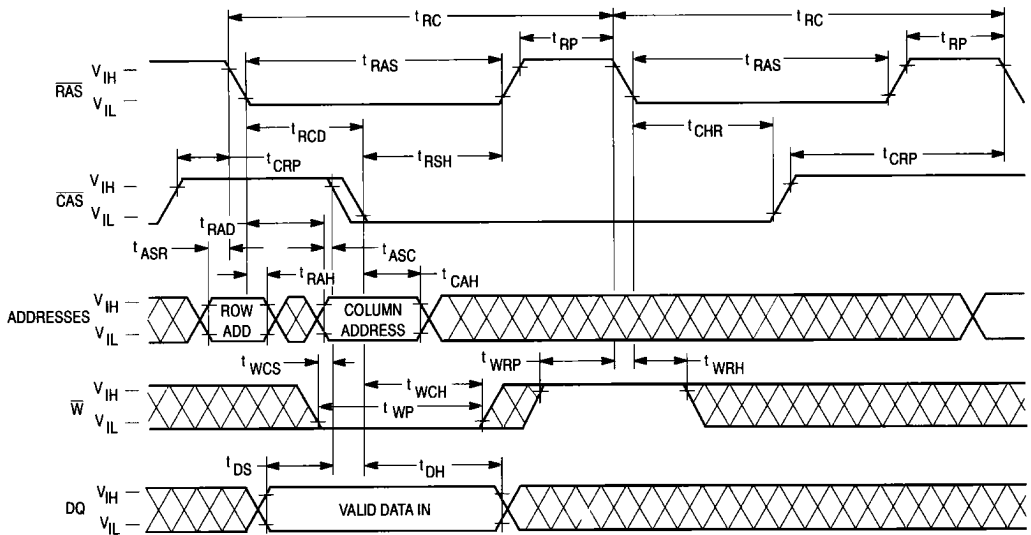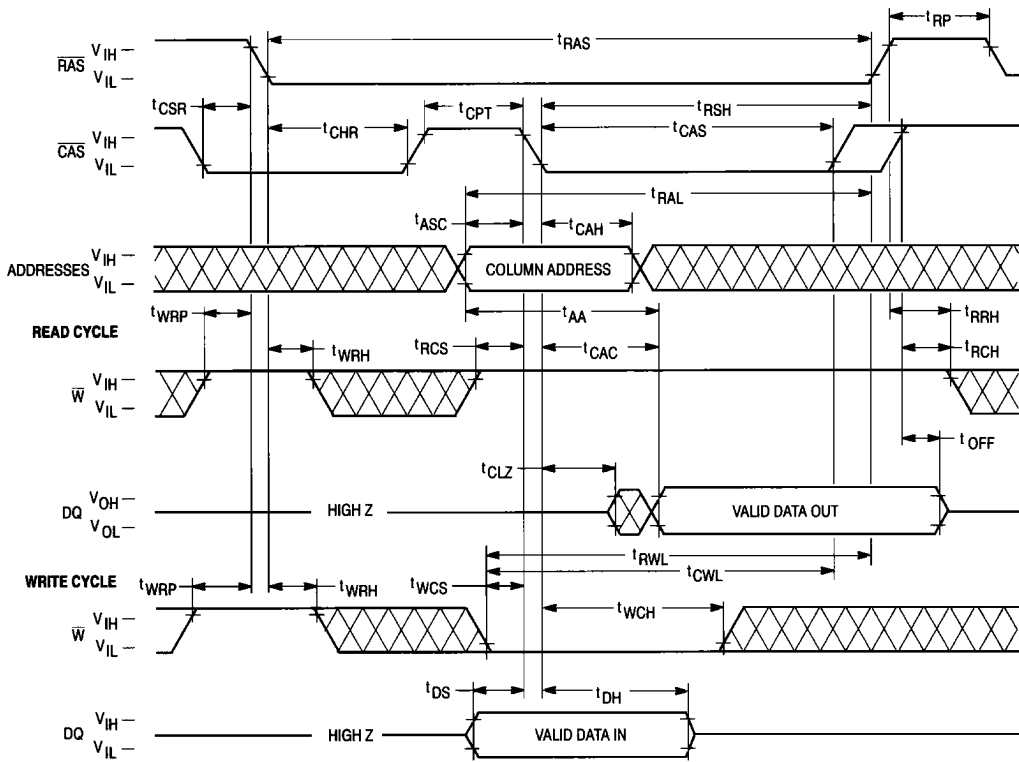
DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the module: **$\overline{RAS}$ only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{CAS}$ controls read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active

cycle. DQ is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with either an early write or a page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (DQ) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM32230 require refresh every 16 milliseconds, while refresh time for the MCM32L230 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM32230, and 124.8 microseconds for the MCM32L230. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM32230 and 128 milliseconds on the MCM32L230.

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A normal read or write operation to the RAM will refresh all the bits associated with the particular row decodes. Three other methods of refresh, **RAS-only refresh**, **CAS before RAS refresh**, and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a CAS before RAS refresh counter test. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See CAS before RAS refresh counter test cycle timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
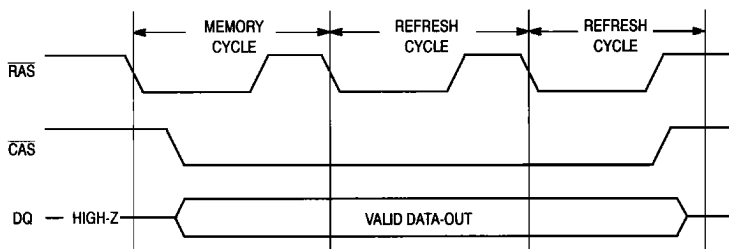5. Repeat steps 1 to 4 using complement data.

Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

Full Part Numbers —	
MCM32230SH60	MCM32230SHG60
MCM32230SH70	MCM32230SHG70
MCM32230SH80	MCM32230SHG80
MCM32L230SH60	MCM32L230SHG60
MCM32L230SH70	MCM32L230SHG70
MCM32L230SH80	MCM32L230SHG80

NOTE: For mechanical data, please see Chapter 10.

MOTOD010