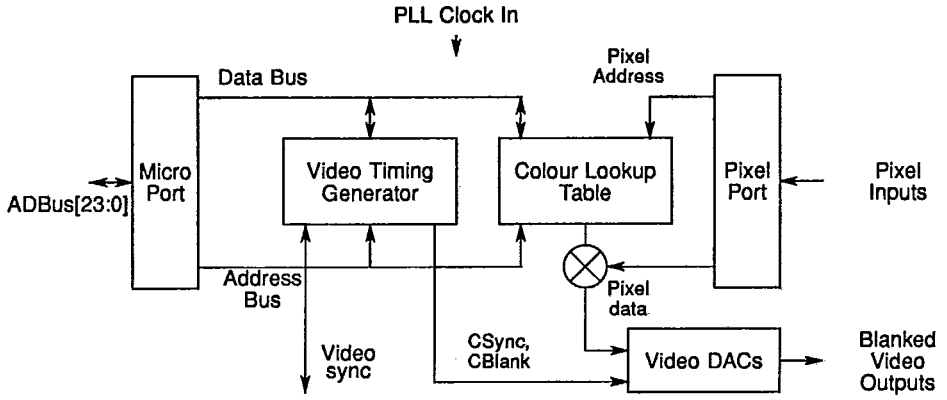
IMS G300
colour video controller

T-52-33-09

Preliminary Data



FEATURES

Video rates up to 120MHz
Software configurable video timing generator
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

4 into 1 multiplexed Pixel input
On chip 256 location x 24 bits colour palette
Triple high speed 8 bit video DACs
RS 170a and EIA 343-A compatible
Indirect 8 planes per pixel mode via palette, or:
24 planes per pixel mode direct to DACs

General purpose Video RAM support
Synchronous VRAM DataTransfer strobing
Video RAM Row address auto-increment
Screen line length independent of VRAM architecture
On-chip phase-locked loop (PLL)
All external signals and clocks at 1/4 video rate

APPLICATIONS

General purpose raster scan control
CRT Screen control
Colour plotters and printers
Plane-based workstations
Portable personal computers

Three dimensional modelling
Real time animation systems
Computer visualisation
Multiple processor systems
Frame swapping systems
Scene insertion into live camera data

Distributed computing environments

6.1 Introduction

The IMS G300 is a dedicated support chip which provides all necessary functions for controlling real time operation of a raster scan video system, using dual ported video DRAMs. The facilities provided are designed to isolate the host processor from the constraints of the real time system without in any way interfering with the ability of the processor to specify and manipulate screen data.

The device consists of a programmable video timing generator with screen refresh and auto line increment capability, a 256 location by 24 bit colour lookup table (LUT), a triple 8 bit video DAC and an on chip phase-locked loop (PLL); see figure 6.1.

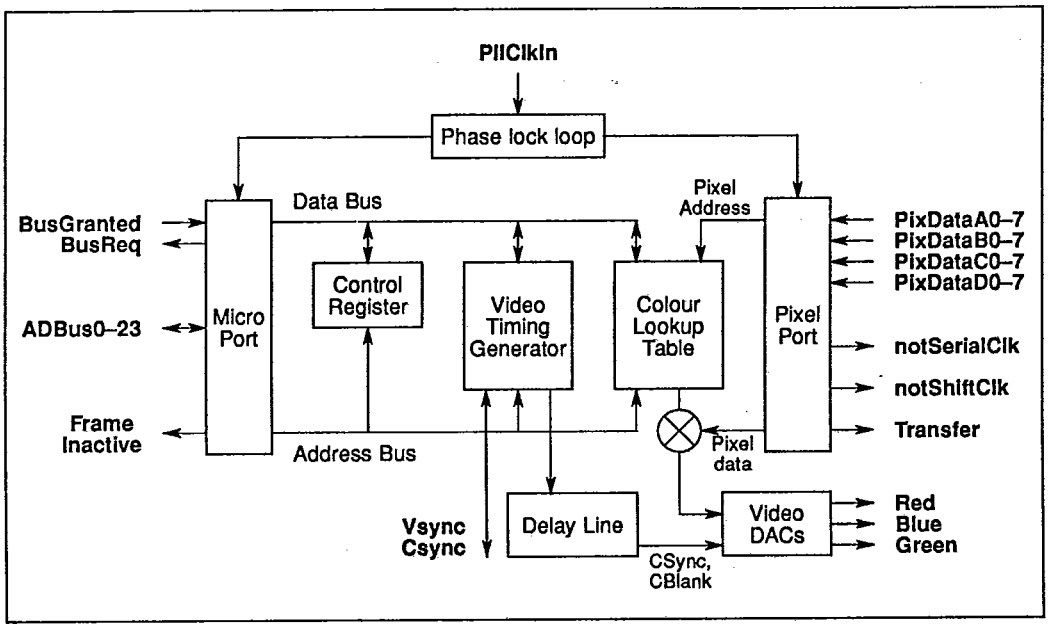


Figure 6.1 IMS G300 Block Diagram

6.1.1 Clocks

Use of the phase-locked loop allows the part to be driven from a low speed clock in the 5MHz to 9MHz range, which is internally multiplied by a user-specified factor to achieve video data rates. The controller can be clocked by a full rate system clock if desired, although at a reduced frequency compared to that achievable with the PLL. This option is selected by making a PCB link.

6.1.2 Video timing

The video timing generator is a programmable finite state machine which is programmed by loading a number of screen description parameters. It can be configured to free run, providing composite or separate sync, or to lock onto an external synchronising source which may be another IMS G300, giving the potential for multiple, synchronous video systems. In either mode, it supplies composite blank to the video DACs and is capable of supplying them with tesselated or plain composite sync when in internal (master) mode. The timing generator runs at one quarter of the video dot rate and the screen parameters are defined in terms of its resolution. Thus the screen is defined in multiples of four pixels.

6.1.3 Screen management

Video RAM support is provided by a screen refresh mechanism which performs a DMA to the video RAM and which allows seamless mid-line update of the screen. The video RAM shift register can be made to behave as though it is infinitely long and the flow of pixels onto the screen is controlled by starting and stopping the pixel shift clock at the appropriate times (a true serial clock output is also provided for system synchronisation). This method of control divorces the screen line length from dependence on the video RAM shift register length, allowing for very long display lines without extra multiplexing and for efficient use of memory irrespective of screen dimensions.

6.1.4 Pixel port

The pixel port is 32 bits wide and has two modes of operation, which are selectable in software.

In mode 1, the port interprets each 32-bit word as four byte-wide pixel addresses and accelerates them to full dot rate before addressing the LUT. The 24 bits of pixel data thus accessed are then sent to the video DACs for display.

In mode 2, the top byte of the input word is ignored and the remaining 24 bits are interpreted as pixel data. No acceleration takes place and the data is sent directly to the DACs.

Mode 2 is usable only when an external dot-rate clock is supplied, mode 1 can also be used with the phase-locked loop.

6.1.5 Video DACs

The triple video DAC has 8 bit resolution at the full video rate and produces blanked video signals. It is possible to select various styles of analogue output to conform with generally approved monitor and broadcast television output levels and timings, including RS170a and EIA-343.

6.1.6 Programming port

The IMS G300 has a memory mapped architecture which enables fast configuration and colour cycling through the use of block move or some other simple memory write cycle. Its micro-port appears as a block of memory (occupying 1/2Kword of address space) with the additional capability of operating in byte-wide or word-wide (24-bit) modes.

6.1.7 System Operation

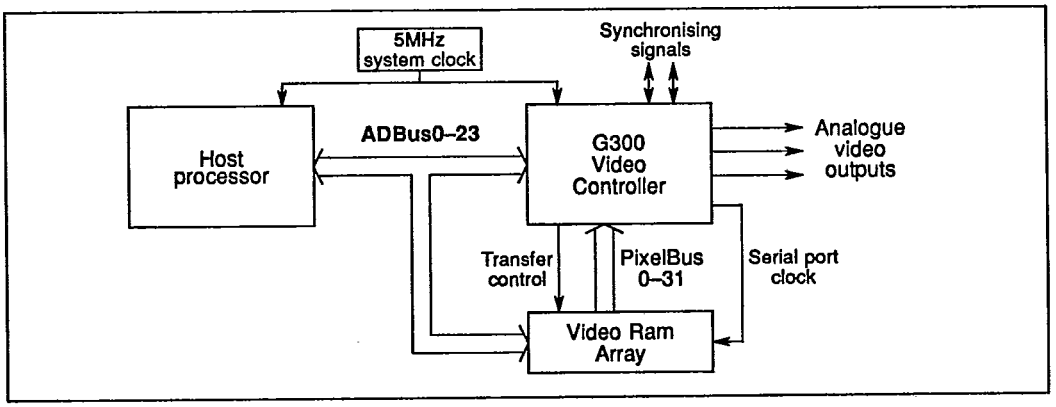


Figure 6.2 IMS G300 operating in a simple graphics system

Figure 6.2 shows how the IMS G300 would fit into a typical single-bitmap display system. The clock is sourced from a 5MHz crystal and the video data is being streamed to the screen at the full video rate of up to 120MHz. The video RAM array is directly accessed by the host and screen management is performed by the G300 on a DMA basis. All external digital signals and clocks are running at one quarter of the video rate.

6.2 Pin function reference guide

6.2.1 Micro port

Pin name	I/O	Page No.	Comments
FrameInactive	O	92	Timing signal which is high whenever the VTG is in Frame Flyback.
BusReq **BusGranted**	O I	88	DMA signals which, along with **Transfer**, supply the timing information to synchronously refresh the video ram shift registers.
ReadnotWrite **notCS**	I I	87	These signals provide all the timing information for accesses as well as defining access type.
ADBus0–23	I/O	87	Multiplexed address and data bus. All 24 bits are used for data; addresses are supplied to **ADBus2-11**. A byte-wide mode is available; the port is also used to drive out the 24-bit VRAM transfer address

6.2.2 Pixel port

Pin name	I/O	Page No.	Comments
notSerialClk **notShiftClk**	O O	93	**notSerialClk** runs at one quarter the video frequency, **notShiftClk** is similar but controls the pixel flow by starting and stopping under the control of the timing generator. Both of these clocks must be buffered.
Transfer	O	88	**Transfer** refreshes the video ram shift register synchronised to **notShiftClk**
PixClkIn	I	95	**PixClkIn** is the Dot-rate clock source when not using the Phase locked loop.
PixDataA0–7 **PixDataB0–7** **PixDataC0–7** **PixDataD0–7**	I I I I	93	The four pixel address bytes are used in the order A, B, C, D. In mode 2 **PixDataD0–7** is not used and RGB maps to ABC.

6.2.3 Miscellaneous

Pin name	I/O	Page No.	Comments
Reset	I	84	Active high, must be held active with clocks running for at least six cycles of **notSerialClk**.

6.2.4 Phase locked loop

Pin name	I/O	Page No.	Comments
CapPlus **CapMinus**	N/A	101	Phase locked loop decoupling pins, also used to select external dot rate clock source by connecting **CapPlus** to **CapMinus**.
PllClkIn	I	101	Low speed clock in the range 5MHz to 9MHz, for multiplication by the Phase locked loop to video dot rate.

6.2.5 Video signals

Pin name	I/O	Page No.	Comments
Red **Green** **Blue**	O O O	95	Blanked video outputs. Drive into doubly terminated 75Ω load.
Iref	I	96	Video DAC reference current.
VSync **CorHSync**	I/O I/O	86	These pins can be used as outputs to supply various software-selectable sync signals or as inputs to lock the device to a system. They are both active high.

6.2.6 Supplies

Pin name	I/O	Page No.	Comments
AVdd	N/A	97	**AVdd** supplies analogue portions of chip
Vdd	N/A	97	**Vdd** supplies digital portions of chip
Ground	N/A	102	

6.3 Register function reference guide

Register	Address	Page No.	Comments
Boot Location	#X1A0	87	Startup location to which must be written the clock multiplication factor in PLL mode. Writing to this location sets the Byte counter to zero.
Top of Screen	#X180	88	Read/write register giving ability to reprogram the top of screen pointer at any time.
Control Register	#X160	79	Read/write control register. Read/write accessible at all times, contains all configuration information. Used to start and stop timing generator. Only ADBus[15:0] valid on read, unassigned bits must be written with zero.
Mask Register	#X140	93	Read/write mask register. Read/write accessible at all times, masks each pixel address byte.
Datapath Registers	#X121 to #X12C	80	Read/write registers containing the screen description parameters. These are accessible only when the timing generator is not running.
Datapath Incrementers	#X12D #X12E #X12F	80	Read only incrementers. These are accessible for test purposes only when the timing generator is not running.
Byte Counter	#X100	87	Incrementing counter used in byte access mode. This may be set by writing the current byte number to it. On startup, it is set to zero by the bootstrap routine.
Colour Palette	#X00 to #XFF	93	256 locations of 24 bit colours read/write accessible at all times, programmed via micro port.

All other addresses in the range are reserved and must not be written to.

6.4 The control register and boot location

The bit pattern written to the control register determines the operating mode of the part. The function of each bit is given in table 6.1.

Bit	Function	Comments
23–16	Reserved	Not valid on read, write zero.
15	Turn off blanking	1 = blanking disabled for test 0 = blanking enabled
14	Turn Off DMA	1 = No video RAM management 0 = DMA VRAM update operational
13	Reserved	Write zero
12	Black level	Selects blanking level 0 = Blank = Black level
11–9	Delay value	Delays internal Sync and Blank by 0 to 7 clock cycles
8	Pixel port mode	0 = mode1, 1 = mode2
7	Micro port mode	0 = word mode, 1 = Byte mode
6	Reserved	Write zero
5	Frame flyback pattern	1 = plain synchronising waveform 0 = tesselated synchronising waveform
4	Digital sync format	0 = mixed sync, 1 = separate sync.
3	Analogue video format	1 = video only 0 = video and sync composite
2	Device operating mode	0 = master mode, 1 = slave mode
1	Screen format	0 = non-interlaced, 1 = interlaced
0	Enable VTG	0 = VTG disabled, 1 = VTG running

Table 6.1 Control Register bit allocations

Boot Address	Bit Allocation
#X1A0	**ADbus5–23** = Don't care **ADBus0–4** = Binary coded PLL multiplication factor (when in external clock mode, load zero)

Table 6.2 Boot location bit allocations

6.5 The video timing generator

6.5.1 Introduction

The Video Timing Generator is a programmable finite state machine. It provides composite sync and blanking to the on-chip video DACs, it controls the timing of **BusReq** and **Transfer** and it starts and stops **notShiftClk** to control the flow of pixels onto the screen. It also provides a **FrameInactive** signal which is asserted whenever the display enters frame flyback, enabling the controlling processor to perform frame flipping or major screen updates invisibly.

The timing generator can be configured to control an interlaced or non interlaced monitor and to generate the synchronising waveforms required by the RS170a studio television standard, among others. These options are selectable in software and are controlled by the contents of the control register.
Also controlled by this register is the operating mode of the device; it can be set to free run in which case it will drive synchronising signals out, or it can be set into slave mode when it will lock onto frame and line sync pulses supplied externally.

Programming of the timing generator is achieved by writing a set of screen description parameters to the timing registers. Its resolution is one quarter that of the individual pixels hence the scan lines must be described in 'screen units' of four pixels each (i.e. a line with 1024 pixels is described as having 256 screen units).

6.5.2 The display screen

In a raster scan display system, the picture is built up of a number of visible lines, which are displayed and a much smaller number of frame flyback lines, which are blanked. Each of the displayed lines has a single, visible, display period and a blanked line flyback period made up of front and back porch and line sync. The total linetime is the sum of the displayed and blanked periods.

The frame timing periods are specified in multiples of half a linetime while the line timings are specified in screen units of four pixels duration each.

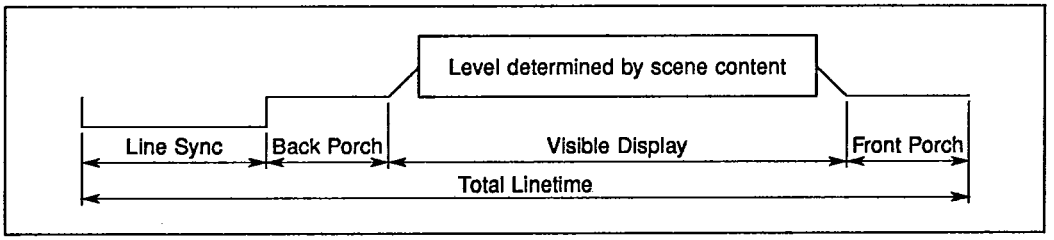


Figure 6.3 Scan line segments

Each displayed scan line of the raster is built up of the sections shown in figure 6.3. The visible portion is contained within the period 'display', so that, if a screen width of 1024 visible pixels is required, this number is reflected in the screen description parameter written to the 'display' register.
At all other times, the display is in line flyback and is therefore blanked.

The total linetime is the sum of all the sections of figure 6.3 and this is the number written to the 'linetime' register.

6.5.3 Line timing parameters

The line segments shown in figure 6.3 are used directly to program the timing generator with two exceptions. First, the line synchronising pulse is split into two states of equal duration which are used in immediate succession — the parameter used for this is 'halfsync'— and second, there is no programmed delay for frontporch, rather the total line time is programmed into a separate register and the machine is reset to line state 'Halfsync1' when this timebase period expires. The resulting flexibility in the duration of frontporch makes the device very easy to program and is essential when it is used as a slave. Any jitter in the global sync is taken up in this front porch period.

Figure 6.4(a) shows the flowchart of a standard displayed or blanked scan line (as distinct from the truncated unscanned lines used in vertical sync and equalisation). The state machine proceeds from one state to the next according to the delay programmed in by the user; on entering a new state the Sync and blanking outputs are modified depending on what part of the cycle is being executed.

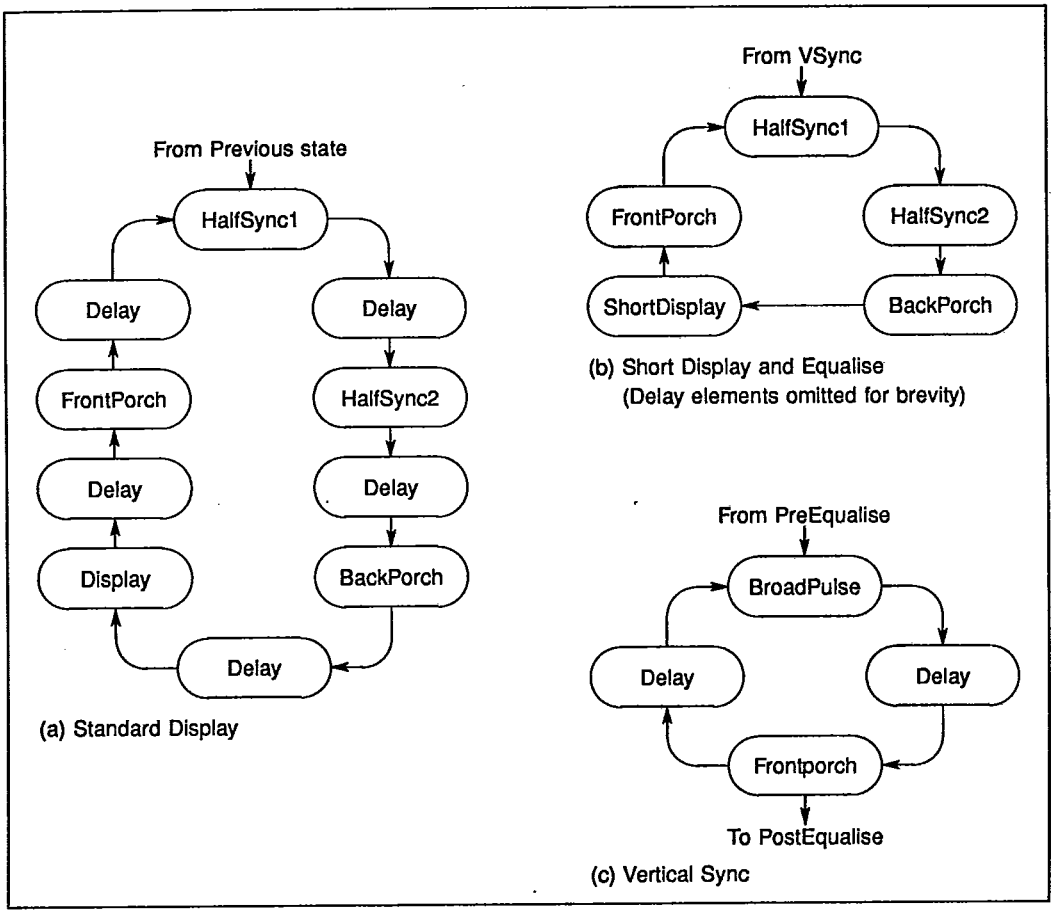


Figure 6.4 Flow diagrams for video timing generator

Figure 6.5a shows the relationship of the screen description parameters to a full scan line. Note that frontporch is undefined and halfsync is used twice in succession to construct the line sync pulse.

6.5.4 Frame timing parameters

The G300 generates synchronising signal timings and levels conforming to both broadcast and closed circuit television standards. This means that, as well as being capable of generating the ordinary frame sync patterns associated with non-interlaced computer graphics systems, it is also able to produce tesselated sync signals for an interlaced television system (see figure 6.6).

A further requirement of the television standards is that each frame may contain an odd number of scan lines. As a result, the frame timing parameters need to be specified in terms of half line times. Thus a non-interlaced screen of 1024 visible lines has the value 2048 written to the VDisplay register. (An interlaced screen of that

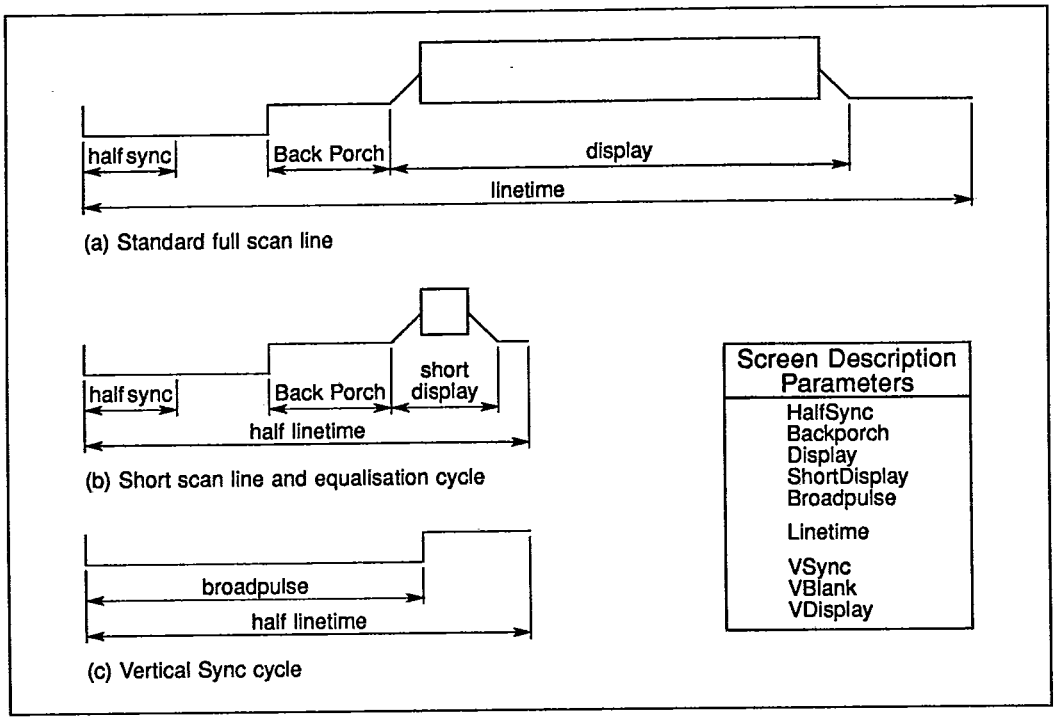


Figure 6.5 Screen description parameter definitions

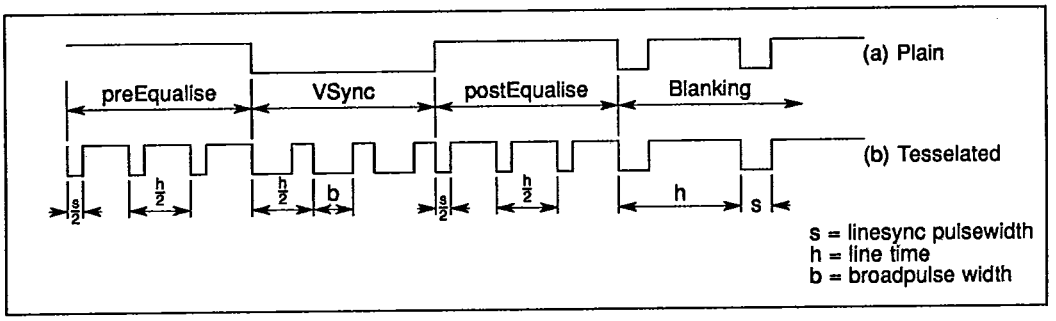


Figure 6.6 Composite Sync Frame Flyback Waveforms

size would have 1024 in that register since in interlace, the VDisplay register decribes the vertical display field rather than the entire frame — see table 6.3).

The duration of preEqualise, postEqualise and VSync are all set by the VSync parameter and are hence always equal, the blanking period is independent and has its own parameter, Vblank.

In order to generate the tesselated equalisation and blanking waveforms shown in figure 6.6(b), some additions to the basic line parameters are needed. The low period during VSync is defined as 'broadpulse' with its duration stored in the 'broadpulse' register. The shorter low period during pre and post equalisation is equal to half the line sync period and hence uses the value stored in the 'halfsync' register.

Screen Type	Lines per Frame	Value in VDisplay Register	Lines per Field
non-Interlace	1024	2048	1024
Interlace	1024	1024	512
non-Interlace	625	1250	625
Interlace	625	625	312.5

Table 6.3 Frame Programming examples

Reference to figure 6.4(b) and (c) shows that, on entering frame flyback, the state machine loop shortens to give a period of half a linetime. In equalisation, this is achieved simply by substituting 'shortdisplay' for 'display' in the sequence, whereas in vsync the sequence is changed to include only 'broadpulse' and 'frontporch'.

6.5.5 Parameter calculation

Calculation of the frame timing parameters is obvious and direct — to produce the flyback waveform in figure 6.6(a) the parameter VSync is set to 3 — and the line parameters are easily derived from the equations in table 6.4.

During a full line cycle (VBlank, VDisplay)		
Halfsync	=	Horizontal Sync/2
BackPorch	=	Backporch
Display	=	Display
FrontPorch	=	Linetime – (2*HalfSync + BackPorch + Display)
During an Equalisation Cycle		
Low period	=	HalfSync
ShortDisplay	=	LineTime/2 – (2*HalfSync + BackPorch + FrontPorch)
High period	=	HalfSync + BackPorch + ShortDisplay + FrontPorch
FrontPorch	=	Linetime/2 – (2*HalfSync + BackPorch + ShortDisplay)
During a VSync cycle		
Low Period	=	BroadPulse
High period	=	FrontPorch
FrontPorch	=	Linetime/2 – BroadPulse

Table 6.4 Screen description parameter equations

The following restrictions on parameter values must be observed:

- All parameters must be non-zero.
- Linetime must be an even multiple of the period of notSerialClk.
- The Halfline point must fall within active display period with at least one notSerialClk period of display on either side of it.
- The total number of displayed lines in each frame must be a whole number. (Note that this means each field of an interlaced frame may have a half line in it)
- The Vertical blanking period must be a whole number of lines.

- Backporch must exceed TransferDelay by at least one notSerialClk period.
- TransferDelay must not exceed ShortDisplay.

(The parameter TransferDelay is described in section 6.8)

6.5.6 The startup sequence

Reading from and writing to the VTG registers, which are memory mapped, is accomplished while the timing generator is disabled.

On startup, after reset, the host processor must write a configuration pattern to the G300 bootstrap location. The effect of this is to set the PLL multiplication factor, if the G300 is to be used in PLL mode, and to set the micro port into a usable state, independent of whether word or byte accesses are to be used. Following this write it must set the micro-port mode by writing to the relevant bits in the control register.

Startup sequence:

1 Assert, then deassert **Reset**.

2 Write configuration pattern to bootstrap location.

3 Write to control register to set microport to desired state.

After this the screen parameters and colour table data can be written to the appropriate locations in any order. The processor must then make another write to the control register to enable the VTG.
It will then either start up immediately at the beginning of frame sync, or wait in Pre-Equalise frontporch for an external sync pulse, depending on the mode to which it has been set. In master mode, it will free run, producing all sync pulses internally, whereas in slave mode, it will lock onto an external sync, resynchronising at the start of each line and at the start of each frame.

Normally the screen parameters are set by the host as part of a powerup sequence and do not change subsequently but there is nothing to prevent the user redefining the screen as often as necessary while the display is being used.

The reprogramming sequence has three steps;

1 Write to the control register, disabling VTG.

2 Write to screen parameter registers chosen for redefinition.

3 Write to the control register, redefining modes if necessary and enabling VTG.

If only the operating mode is to be changed, step 2 only may be omitted, the remainder of the address space is programmed without disabling the VTG. If the clock multiplication factor is to be changed, **Reset** must be asserted first.

6.6 The G300 Address Map

The various register locations of the IMS G300 are memory mapped as shown in the table below. The values given are hexadecimal word addresses driven on to **ADBus2–11** All other locations within the address space occupied by the G300 are reserved and must not be addressed. The datapath incrementers are read only, The boot location is not readable, all other locations are read/write.

Location	Address
Colour Palette	
starts	#X000
ends	#X0FF
Byte Counter	#X100
Mask Register	#X140
Control Register	#X160
Top of Screen	#X180
Boot Location	#X1A0

Location	Address
DataPath Registers	
HalfSync	#X121
BackPorch	#X122
Display	#X123
ShortDisplay	#X124
BroadPulse	#X125
VSync	#X126
VBlank	#X127
VDisplay	#X128
Linetime	#X129
LineStart	#X12A
MemInit	#X12B
TransferDelay	#X12C
Datapath Incrementers	
HIncrementer	#X12D
VIncrementer	#X12E
TBIncrementer	#X12F

Table 6.5 IMS G300 Address Map

6.7 Synchronising signals

6.7.1 Introduction

The video timing generator produces Sync and blank signals to a pattern specified by a combination of the operating mode of the G300 and the screen description parameters. Internally, composite sync and composite blank are supplied to all three video DACs by default. However, both of these functions can be disabled by setting the relevant bits of the control register.

The internal sync and blank signals are supplied with the correct delay to allow for the transfer of data from the video ram array into the G300 and the difference in delay due to the alternate operating modes is automatically catered for.

In order to allow a certain amount of system flexibility, the IMS G300 includes a programmable delay line which can be set (via the Control Register) to insert a further delay of up to seven clock cycles between the outputs of the VTG and the inputs of the DACs.
This enables the system designer to insert pipeline stages between the video ram array and the G300 for the implementation of cursor or text overlay, etc and also allows video data to be buffered along a backplane using TTL parts.

6.7.2 Master mode

When running in master (internal sync) mode, the **VSync** and **CorHSync** pins are outputs and the G300 drives them in the appropriate fashion, active high. Composite or Horizontal sync selection is specified in the Control Register. Untesselated frame sync always appears on the **VSync** pin while the **CorHSync** pin is switchable to supply one of Line sync, untesselated composite sync or tesselated composite sync (see table 6.6).

Control Bits		**Vsync**	**CorHSync**	
			HSync	*CSync*
4	5			
0	0	Plain	–	Tesselated
0	1	Plain	–	Plain
1	0	Plain	Plain	—
1	1	Plain	Plain	—

Table 6.6 Sync Style Selection

6.7.3 Slave mode

In slave mode the **VSync** and **CorHSync** pins are designated as inputs and the G300 will lock onto vertical and horizontal sync pulses supplied to them. The system must provide both horizontal and untesselated vertical sync, active high.

The sampling circuit on the Sync inputs means that the IMS G300 can be locked to a completely asynchronous source without metastability problems. It will tolerate a large amount of instantaneous variation in the synchronising inputs due to the inbuilt flexibility of the timing algorithm. This provides synchronisation guaranteed to within one period of **notSerialClk**, which may not be adequate in a system where the monitor and G300 are synchronised separately from a single external source; because of possible jitter on the sync signal there may be random errors visible on the screen. In this case, it is necessary to observe the timing shown in figure 6.7 in which case, the G300 will give no synchronising errors.

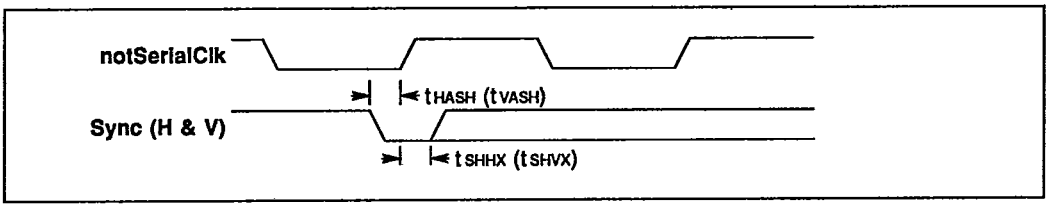


Figure 6.7 External synchronisation

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{VASH}	Vsync setup time	SClk/4		ns
t_{HASH}	Hsync setup time	SClk/4		ns
t_{SHVX}	Vsync hold time	0		ns
t_{SHHX}	Hsync hold time	0		ns
Note: These figures are not characterised and are subject to change				

Table 6.7 External sync waveform timings

6.8 The Micro-port

6.8.1 Introduction

The micro-port is a bidirectional 24 bit interface which can be configured to operate in byte wide or 24 bit wide mode (word mode). It consists of a multiplexed address and data bus with several control signals, described below, and is used for programming both the video timing generator screen description registers and the colour lookup table. The micro port timings are asynchronous with the remainder of the G300.

As well as serving as a programming port the interface is also capable of performing a video RAM shift register transfer operation using a fully handshaken DMA. The timing of this operation is synchronous with the pixel port and is arranged so that seamless update of the video RAM shift register is possible.

6.8.2 Initialisation

The choice of clock source is made by a wiring option. If the phase locked loop is to be used, a suitable crystal oscillator must be connected to the **PllClkIn** pin. If the direct drive option is used, the system must supply a dot rate clock to the **PixClkIn** pin. On Power up, the **Reset** pin must be taken high and PllClkIn or PixClkIn must have been running for at least t_{CVRL} after **Vdd** is valid before the end of **Reset**. After deasserting **Reset**, the first access to the Micro-port must be a preliminary configuration access to the boot location as specified in section 6.5. This sets the micro-port byte counter and the PLL multiplication factor if the clock source is to be the PLL.

Following this, a write should be performed to the control register to set the width of the programming port — byte or word. The option is selected by writing to bit 7 in the control register. (Since this is in the lowest byte of the control word, the value is guaranteed to be set correctly with one write cycle). If byte-wide mode is selected, a further two writes to the control register must be made to complete the cycle.

Once these two write cycles have been performed normal operation of the micro-port may commence using the programmed format whether it be byte-wide or 24-bit word-wide.

6.8.3 Programming operation

For normal read and write cycles the address is latched into the G300 on the falling edge of **notCS**. **ReadNotWrite** is sampled 1/2 a period of **notSerialClk** later to establish the cycle type. In a read cycle, the data lines will be driven a certain time later and will remain valid until **notCS** goes high. In a Write cycle, data will be latched into the G300 on the rising edge of either **ReadNotWrite** or **notCS**, whichever occurs first. When the part is configured to byte-wide mode, three complete read or write cycles must be made to the same address in order to complete the cycle. The data is written to or read from **ADBus0–7** least significant byte first. If a byte wide cycle is aborted before completion, the counter must be reset by writing the number one to the byte counter register. If the aborted cycle happened to be a write, data corruption at the written location will occur.

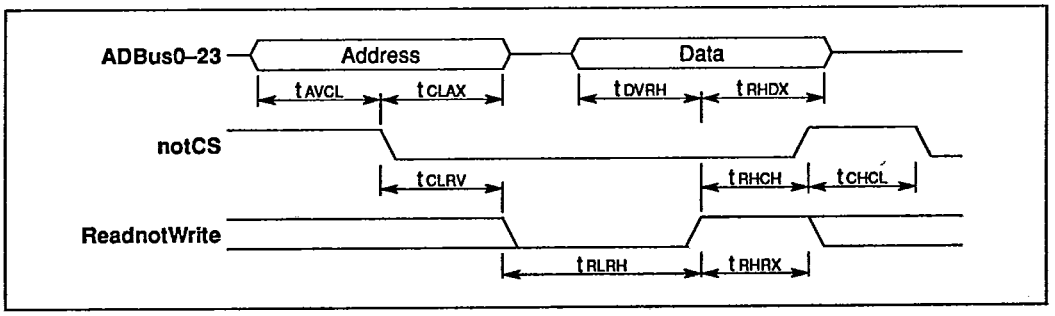


Figure 6.8 Micro-Port Write Cycle

Symbol	Description	Min	Max	Units
t_{AVCL}	address setup time	20		ns
t_{CLAX}	address hold time	10		ns
t_{CLRV}			0.5	periods SClk
t_{CHCL}		1		period SClk
t_{DVRH}	data setup time	0		ns
t_{RHDX}	data hold time	20		ns
t_{RHCH}		0		ns
t_{RLRH}		3		periods SClk
t_{RHRX}		1		period SClk
t_{CLCL}	cycle time	5		periods SClk
where SClk is the period of **notSerialClk**				
Note: These figures are not characterised and are subject to change				

Table 6.8 Write cycle parameters

6.8.4 The screen transfer operation

The G300 provides two software programmable strobes which enable it to perform the necessary screen data-transfer cycles on video RAMs to reload the internal shift registers with new data. These may be synchronous updates which happen part way across a line or updates which occur during flyback.

The user may program these strobes, **busRequest** and **Transfer**, to cause the data transfer cycles to occur at the correct points during the screen display to implement seamless line update, thus decoupling the screen configuration from dependence on the video RAM architecture. These strobes are controlled by values loaded into two special purpose registers, MemInit and TransferDelay. The G300 also outputs a transfer address specifying the new row of pixels to be displayed. It is left to the user to generate RAS, CAS and any other strobes he may need from **busRequest**, **Transfer**, **notSerialClk** and **notShiftClk**.

The G300 is primarily designed to be used with video RAMs, although it can be used with static or standard dynamic rams if desired. In this case the strobes provided can be used to arbitrate bitmap accesses.

6.8.5 The transfer address

The G300 outputs a new 22 bit address on **ADBus2–23** during every transfer cycle it initiates. The first address in each frame is specified in the Top of Screen register, which is programmed on startup but which can be modified at any time.

Unless a new address is supplied by the host, the current row address will be incremented by the G300 and used for the next row transfer until the bottom of screen is reached. The address counter is then reset to Top of screen unless the G300 has been set to interlace mode, in which case the address will carry on being incremented until both fields of the frame have been displayed. The effect of this is to separate out the fields of an interlaced image into two consecutive bitmaps as shown in figure 6.9.

The address will be incremented as one 22-bit number in bits 2–23 and it is left to the user to split this into row and column fields for strobing into the video RAMs. Ordinarily the bottom n-bits of the address would be used as a row value and the top bits for the column value as shown in table 6.9

It is open to the user to modify either or both of these fields at any time (other than during a row transfer operation) so that panning and scrolling can be implemented.

Row Address Field	Col Address Field
ADBus 2 to n–1	ADBus n to 23

Table 6.9 Shift Register Transfer Address Fields

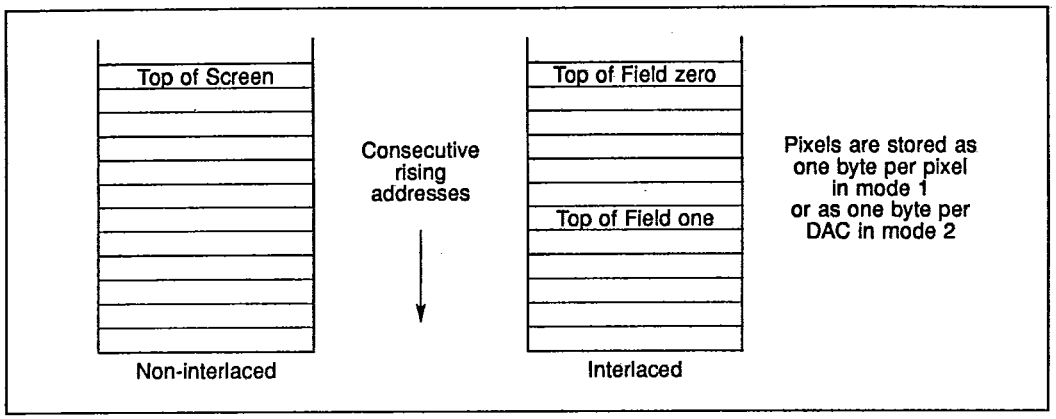


Figure 6.9 Bitmap Formats for interlaced and non Interlaced displays

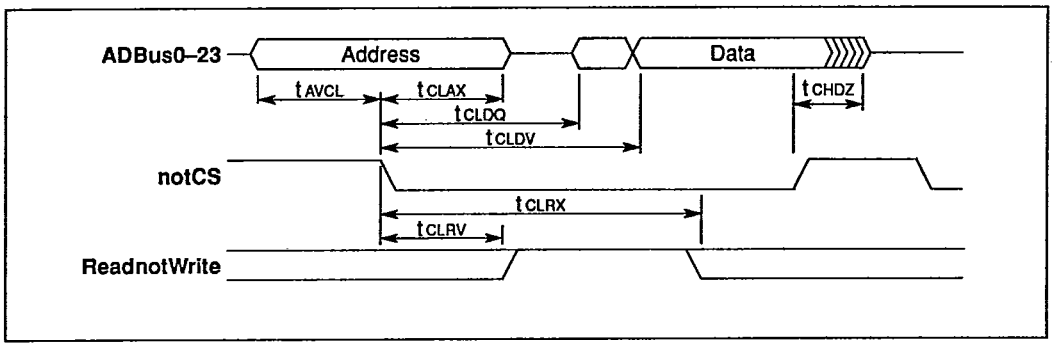


Figure 6.10 Micro-Port Read Cycle

Symbol	Description	Min	Max	Units
tAVCL	address setup time	20		ns
tCLAX	address hold time	10		ns
tCLDQ	time to bus driven	1.5		periods SClk
tCLDV	data access time		4sClk + 20nS	
tCLRV			0.5	periods SClk
tCLRX		1.5		periods SClk
tCHDZ	data turn off delay		20	ns
tCLCL	cycle time	7		periods SClk
where SClk is the period of **notSerialClk**				
Note: These figures are not characterised and are subject to change				

Table 6.10 Read cycle parameters

6.8.6 Transfer cycle timing

Video RAMs reload their shift registers by performing a normal read cycle with a special pin (usually called notDT or notDT/notOE) held low as RAS falls. The address values presented to the VRAM on the falling edges of RAS and CAS define which row is loaded into the shift register and which bit in the shift register is shifted out first, respectively. The instant at which the actual transfer takes place is set by the time at which

notDT is brought high again and this edge alone must be synchronised to the shift clock which clocks data out of the shift registers.

In many systems the reloading of the shift registers takes place at the end of the line during retrace. However, one of the most useful features of using the G300 with VRAMs is the ability to reload the shift registers mid-line. This allows screens with an arbitrary number of pixels per line to be constructed with any length shift register. In order to do this however some look-ahead is required in order to be able to make the transfer at exactly the right point without any discontinuity on the screen. This look-ahead is provided by programming the appropriate values into the MemInit and TransferDelay registers.

At the start of each display frame, the G300 will initiate a transfer cycle at the beginning of the backporch period of the first line and will perform the data transfer with the delay specified in the TransferDelay register.

The G300 has the following requirement:

$$\text{TransferDelay} \leq \text{BackPorch} - 1$$

This ensures that there is data loaded ready for the first line scan to begin.

The G300 will then begin to count **notShiftClk** cycles and will initiate a further transfer cycle after MemInit cycles of **notShiftClk** by asserting **BusReq**. After a further number of cycles of **notShiftClk** equal to TransferDelay, the G300 will take **Transfer** low and the new data will be loaded into the shift registers.

Thus the period of row transfer operations is

$$\text{MemInit} + \text{TransferDelay}$$

and apart from the restriction quoted above, it need bear no relation to the screen line length at all. This permits any display line length with any type of video RAM.

The critical parameter as far as DMA accesses are concerned is TransferDelay which needs to be long enough to allow for the DMA latency of the controlling processor as well as the access time of the video RAMs. The G300 imposes an extra overhead of one notSerialClk period which needs to be added to the Transferdelay parameter but which does not appear as part of the delay between BusReq and notDataTransfer. Thus:

$$\begin{aligned}\text{TransferDelay} = {} & \text{System DMA Latency} \\ + {} & \text{VRAM Access time} \\ + {} & \text{SClk}\end{aligned}$$

If there is a data transfer operation pending when the system enters flyback, (i.e. the G300 would have control of the bus for a considerable length of time) then the transfer cycle is aborted before **BusReq** is made and will be restarted on the next following active display backporch. This ensures that any DRAM is never left unrefreshed during frame flyback and also makes best use of the available memory bandwidth. In order to implement this function, the G300 predicts, after a DMA is internally sheduled but before BusReq is asserted, that the video RAM shift registers are not going to run out of pixels before the end of the current line and hence the Row refresh may be left until the following active backporch. The internal system is pipelined by one delay stage which is the reason for adding one **notSerialClk** cycle extra to the TransferDelay parameter over the actual DMA latency of the system. When **BusReq** is rescheduled the DMA is restarted at the beginning of backporch in the same way as the first line in the frame but the transfer delay parameter is carried over from the previous line (or frame) and is incremented only when the system re-enters active display. This preserves the correct ordering of data onto the screen, while the insertion of the backporch period ensures that the DMA latency is always exceeded.

Figure 6.11 shows the sequence of events during a synchronised VRAM row transfer operation performed by the G300 which takes place part-way along a display line. That is to say an uninterrupted stream of pixels is maintained during a reload of the shift registers.

It should be noted that the G300 signals **notShiftClk**, **notSerialClk** and **Transfer** are all designed to be buffered by inverting buffers outside the G300 and so are the logical inverses of the signals driving the VRAMs.

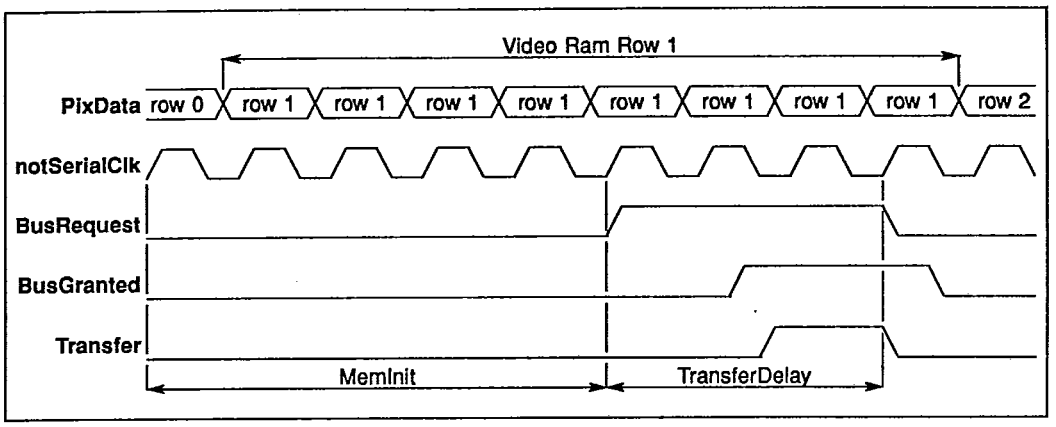


Figure 6.11 Data Transfer Sequence

MemInit defines the number of periods of **notShiftClk** before the G300 asserts **busRequest**. This is the first event which signals the start of a transfer cycle. When the host processor returns **busGranted** the G300 asserts **Transfer** and drives out the new transfer address to be strobed into the VRAMs. Only after a further number of **notShiftClk** cycles equal to TransferDelay, does the G300 remove **Transfer** (synchronously with respect to **notShiftClk**) and so perform the actual transfer. **busRequest** is also taken away at this point to return the **ADBus** back to the host. The user should arrange for TransferDelay to be sufficiently long to allow for the worst case bus request latency plus the time required to strobe RAS and CAS with the address supplied from the G300.

The most memory-efficient way of using the transfer cycle feature is to make Meminit + TransferDelay equal to the length of the video RAM shift registers thus packing the bitmap into the smallest possible space, but it is obviously possible to specify a smaller number and then use the remainder of the bitmap as a larger 'world' which can be panned through by modifying the Top of screen pointer between frames.

The G300 will not respond to a BusGranted signal which it has not itself requested. This feature simplifies connection into a system which includes more than one DMA source.

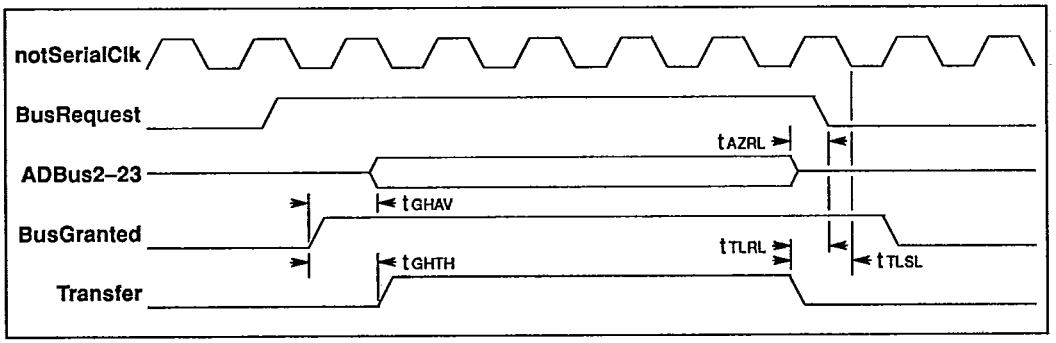


Figure 6.12 Data Transfer Timings

Symbol	Description	Min	Max	Units
t_{GHAV}	**busGranted** high to address valid		3*SClk+30	ns
t_{AZRL}	Address invalid to **busRequest low**	0		ns
t_{GHTH}	**busGranted** high to **Transfer** high		SClk+20	ns
t_{TLRL}	**Transfer** low to **Bus Request low**	−5	5	ns
t_{TLSL}	**Transfer** low to **notSerialClk** low	10	SClk−10	ns
Note: These figures are not characterised and are subject to change				

Table 6.11 Micro port DMA and Transfer timings

6.8.7 FrameInactive

A further timing signal, **FrameInactive**, is provided which can be used to convey frame timing information to the host. This signal may be used in multiboard systems where frame swapping is used to implement animation, for example. **FrameInactive** is asserted whenever the timing generator enters frame flyback and is deasserted on entering active display.

6.9 The pixel ports

6.9.1 Pixel port operation

The pixel port takes in the pixel data from the video RAM and has two modes of operation;

mode 1 — via the lookup table
mode 2 — direct write through to the DACs.

The mode is defined by a single bit in the G300 control register. The clock source is set by a wiring option (See the section on the programming interface). By varying these options it is possible to use the G300 in one of three configurations as shown in table 6.12

Mode	Clock Option	Video Clock Source	Pixel Route
1	**pllClkIn** (nom 5MHz)	output of on-chip PLL	through LUT
1	**pixClkIn** (video rate)	**pixClkIn**	through LUT
2	**pllClkIn** (nom 5MHz)	not available	
2	**pixClkIn** (video rate)	**pixClkIn**	direct to DACs

Table 6.12 Clock and pixel port options

6.9.2 Mode 1 operation

In mode 1 the G300 latches four 8-bit pixels on **PixDataA0–7**, **PixDataB0–7**, **PixDataC0–7** and **PixDataD0–7** on a single falling edge of **notShiftClk**. These four pixels are then serialised to the full pixel rate internally and applied to the colour palette address inputs in turn — A, B, C and D.

The eight bit pixels used in mode 1 allow a choice of 256 simultaneous colours from a palette of 16 million. Changing the palette through the programming interface allows rapid colour selection and modification. The colour palette may be loaded and read back via the programming interface (see the G300 memory map). If the G300 memory interface is being used in word-mode, then a colour word may be loaded in one G300 external memory interface cycle and a complete colour palette may be block moved into or out of the G300 by the processor.

Mode 1 allows the pixel input to be multiplexed 4 into 1, this allows clocking of the video RAMs at 1/4 the pixel clock frequency.
The G300 supplies a signal **notShiftClk** which is designed to be buffered through a single inverting driver outside the G300 directly into the SC (serial clock) of each of the video RAMs. This clock (which runs at 1/4 the pixel clock frequency) pulses once for each new group of 4 pixels required by the display. It is not free running, but stops during line and frame flyback.
A free-running clock **notSerialClk** is also generated by the G300. This provides a continous clock synchronous to the video stream. If this clock is loaded identically to **notShiftClk** then its edges will be coincident to **notShiftClk**, the only difference being that it will not stop during flyback.

By taking 4 pixels into the G300 in one go, the clock rate to the video rams for a nominal 120MHz system can be reduced to 30MHz. It is therefore possible to use standard video RAMs without extra multiplexing on the board. It is also possible to drive the pixel data down a backplane using easily available TTL parts in order to gang up extra boards in a distributed system. It has the further advantage that all external clocks and signals are running at comparatively low frequencies.

A memory mapped mask register is available for masking the incoming pixel address to the LUT in mode 1. The contents of this register (mapped onto **ADBus0–7**) are logically ANDed with the incoming pixel stream. By altering the contents of this register the microprocessor may achieve simple rapid colour changes on the screen.

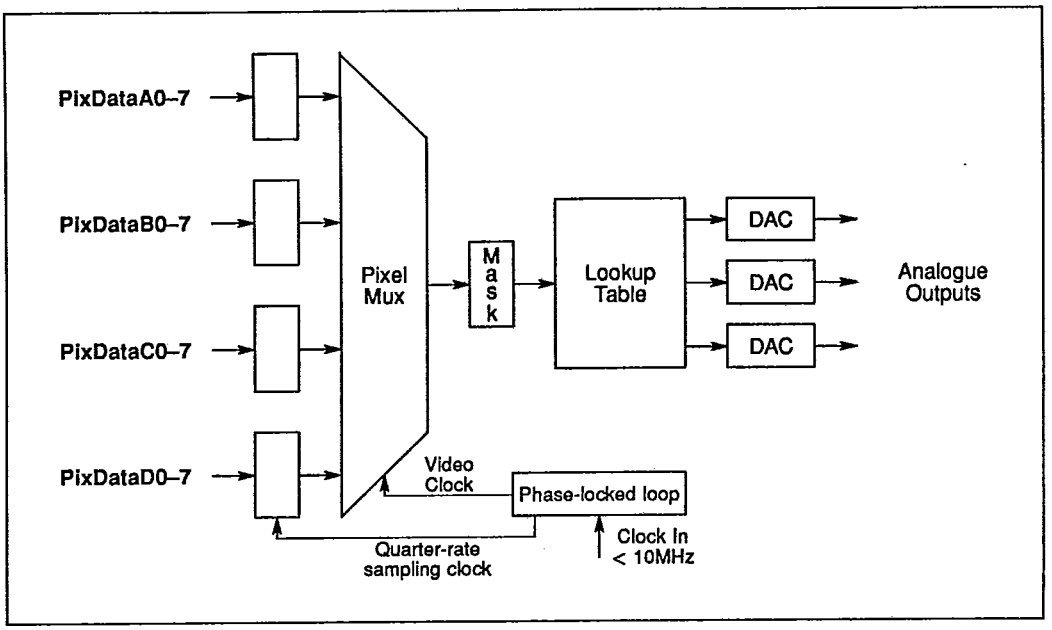


Figure 6.13 Pixel Port in mode 1

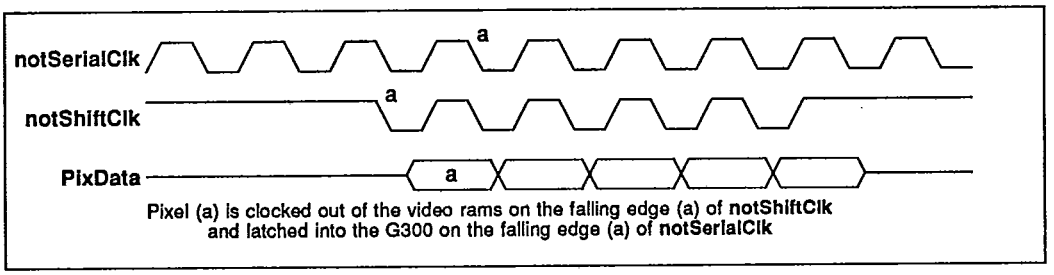


Figure 6.14 Relationship of Serial and Shift Clocks to pixel data

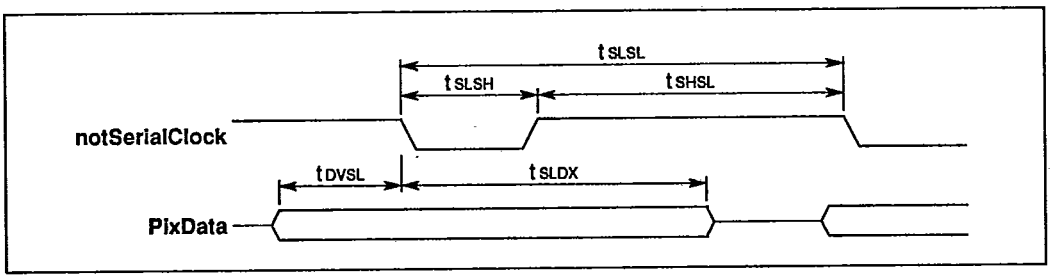


Figure 6.15 Pixel Port signals in mode 1

Symbol	Description	-66 Min	-85 Min	-100 Min	-110 Min	Units
t_{SLSL}	notSerialClk period	61	47	40	36	ns
t_{SLSH}	Clk low time	12	10	10	10	ns
t_{SHSL}	Clk high time	12	10	10	10	ns
t_{DVSL}	data setup time	3	0	0	0	ns
t_{SLDX}	data hold time	25	20	18	15	ns
Note: These figures are not chracterised and are subject to change						

Table 6.13 Pixel port mode 1 timings

6.9.3 Mode 2 operation

In mode 2, direct write, pixel inputs are applied direct to the DACs so bypassing the LUT. This allows the use of the full range of up to 16 million colours simultaneously displayed on the screen but requires pixels to be supplied to the G300 at the full video rate.

One 24-bit wide pixel is latched into the G300 on every *rising* edge of the externally supplied pixel clock — **pixClkIn**. (The PLL is not used in mode 2.)
PixDataA0–7 feeds the red DAC, **PixDataB0–7** feeds the green DAC and **PixDataC0–7** feeds the blue DAC. The DAC outputs will then reflect this pixel data directly on their respective analogue outputs.

Note that in both modes, the specified timings for the pixel setup and hold times must be observed, even during flyback.

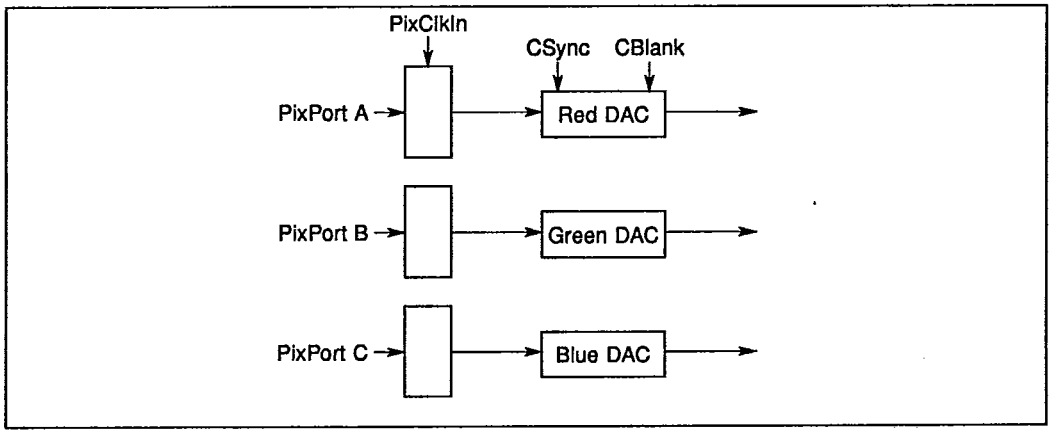


Figure 6.16 Pixel port in mode 2

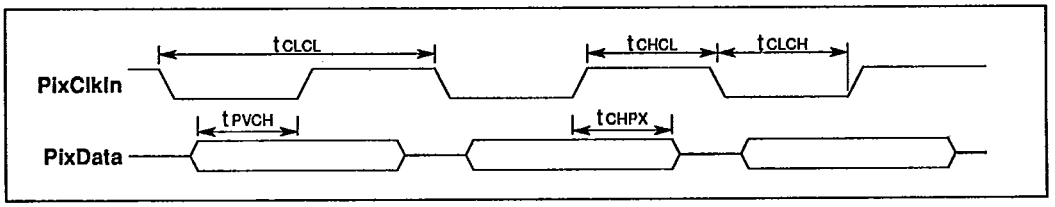


Figure 6.17 Pixel Port signals in Mode 2

Symbol	Description	All Max	-66 Min	-85 Min	-100 Min	-110 Min	Units
t_{CLCL}	pixel period	10000	31	25	20	18	ns
t_{CHCL}	pixClkIn high time	10000	10	8	7	6	ns
t_{CLCH}	pixClkIn low time	10000	10	8	7	6	ns
t_{PVCH}	pixel data setup time		6	5	4	4	ns
t_{CHPX}	pixel data hold time		6	5	4	4	ns
Note: These figures are not chracterised and are subject to change							

Table 6.14 Pixel Port Mode 2 Timings

6.10 The video DACs

6.10.1 General

The video DACs on the G300 have 8-bit resolution at the full video rate. They are designed to drive a doubly terminated 75Ω transmission line and produce analogue video signals compatible with either the RS-170 or RS-343 video standards.

6.10.2 DAC output waveform

The DACs work by sourcing a current proportional to their digital input. The unit current sourced for each digital increment is defined by a reference current drawn from the part using an external current source.

The complete analogue video signal comprises three components as shown in figure 6.20. The current sourced by each component is defined in terms of DACunits. The value of 1 DACunit is set by the reference current drawn from the **Iref** pin :

$$1\ \text{DACunit} = \textbf{Iref}/120$$

The colour information output by each gun ranges from 0 to 255 units under control of the digital input from the colour palette or the pixel port.

A black-level pedestal of 20 DACunits is provided. This extra pedestal distinguishes between a displayed value of intensity 0 during display (ie black) and the 'blacker than black' level present when the electron beam is blanked for flyback. When enabled (by setting the relevant bit in the control register), this extra level is switched on only during the active display time of each line. It is switched off during blanking so as to ensure no visible trace of the beam appears on the screen during this period.

A sync pedestal, again selected using the control register, is provided to allow the superposition of the sync timing signals on the video outputs. When this composite sync option is selected the sync level is added to the output during blanking and active display. Sync pulses are present on all three of the video DACs. The size of the sync pedestal is 108 units.

Table 6.15 defines the value of each of the three components which make up the complete video output current sourced by each DAC.

Both the black-level pedestal and the sync signals may be independently turned on or off by setting bits 12 and 3 in the control register respectively.

(Note that the extra blanking pedestal units, if used, add to the full scale deflection so that the current source must be redefined in order to use this mode).

6.10.3 DAC characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES (1,2)
	Resolution		8		bits	
VO(max)	Output voltage			1.5	V	IO ≤10mA
IO(max)	Output current			−32	mA	VO ≤1V
	Full scale error			±5	%	3
	Sync pedestal error			±10	%	
	Black level pedestal error			±10	%	
	DAC to DAC correlation error			±2.5	%	4
	Integral Linearity error			±1	LSB	5
	Glitch Energy		75		pVSec	6,7
IREF	Reference current	−7		−10	mA	
VREF	Reference voltage	VDD−3V		VDD	Volts	
Note: These figures are not characterised and are subject to change						

Notes

1 All voltages with respect to **Ground** unless specified otherwise.

2 Tested over the operating temperature range and at nominal supply voltage with IREF = −8.88mA.

3 From the value predicted by the design equation, sync and black level pedestals off.

4 About the mid point of the distribution of the 3 DACs measured at full scale deflection.

5 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

6 Load = 37.5Ω + 30 pF with IREF = −8.88mA.

7 This parameter is sampled not 100% tested.

SYMBOL	PARAMETER	−66 MAX	−85 MAX	−100 MAX	−110 MAX	UNITS	NOTES
	DAC Risetime	6	6	4	4	ns	1
	DAC Settling Time	15.3	11.7	10	9.1	ns	1,2,3
Note: These figures are not characterised and are subject to change							

Notes

1 Load = 37.5Ω + 30pF, IREF = −8.88mA.

2 From a 2% change in output voltage until settling to within 2% of the final value.

3 This parameter is sampled not 100% tested.

6.10.4 Power supply and reference current

The DACs in the G300 draw current from a positive supply pin designated **AVdd** (analogue VDD). This pin is separate from the rest of the positive supply pins to the G300 which power the digital circuitry. It is recommended that a high frequency decoupling capacitor (preferably a chip-capacitor) in parallel with a larger tantalum capacitor (22μF to 47μF) be placed between **AVdd** and **Ground** to provide the best possible supply to the analogue circuitry of the DACs.

In cases where the positive supply local to the G300 is unavoidably noisy, an inductor may be placed in series with the entire positive supply to improve the local supply to the G300. If this approach is taken however, care should be taken to ensure that there is no significant DC voltage drop across the inductor during operation.

The G300 requires a simple current source to provide a reference current for the DAC outputs. This current

is drawn from the positive rail. The principle considerations when choosing a current source for a video DAC are accuracy, stability and a fast AC response.

Figure 6.18 shows a recommended current source based around the LM334 precision current reference. The device is used in its temperature compensated mode. This device can supply reference currents up to 10mA. the resistor RSET sets the basic current drawn, with the second resistor R1 and the silicon diode (IN4148) providing temperature compensation.

The component values shown in the figure are chosen to set the reference current at 8.88mA; this is the normal reference current for the G300 used with doubly terminated DAC outputs.

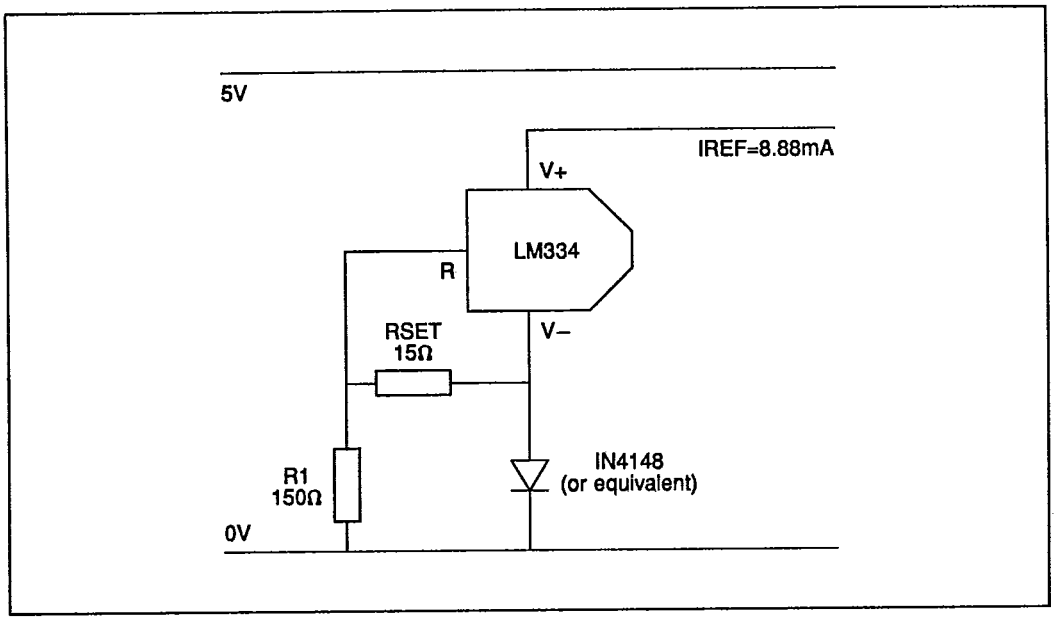


Figure 6.18 Current reference based on the LM334

6.10.5 Analogue output — line driving

The G300 is designed to drive a doubly terminated 75Ω line. This arrangement is illustrated in figure 6.19. The effective load seen by the G300 video outputs with this circuit is 37.5Ω.

The connection beteween the DAC outputs on the G300 and the input to the colour monitor should be regarded as a transmission line. Impedance changes along this line will result in reflection of part of the video signal back along the line. These reflections can result in a degradation of the picture displayed by the monitor. To ensure good fidelity RF techniques should be used; in particular the PCB trace from the G300 video output pins to the video sockets on the graphics board should be kept short (less than 3 inches is ideal). If this is done then any reflections due to a mismatched impedance at the video connectors will occur within the risetime of the DAC waveform and not cause a degradation of the image quality.

6.10.6 Analogue output — protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G300 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G300 are made available at connectors outside the graphic system they are still exposed

to static damage and other hazardous voltages. Protection diodes to the power rails are recommended at this exposed interface.

	Colour Data (Full Scale)	Black Level Pedestal	Sync
units	255	20	108

Table 6.15 DAC output level components

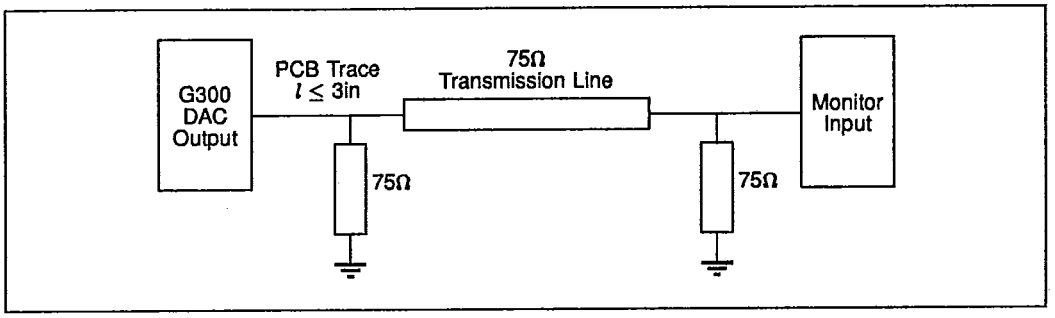


Figure 6.19 Dac Output Loading

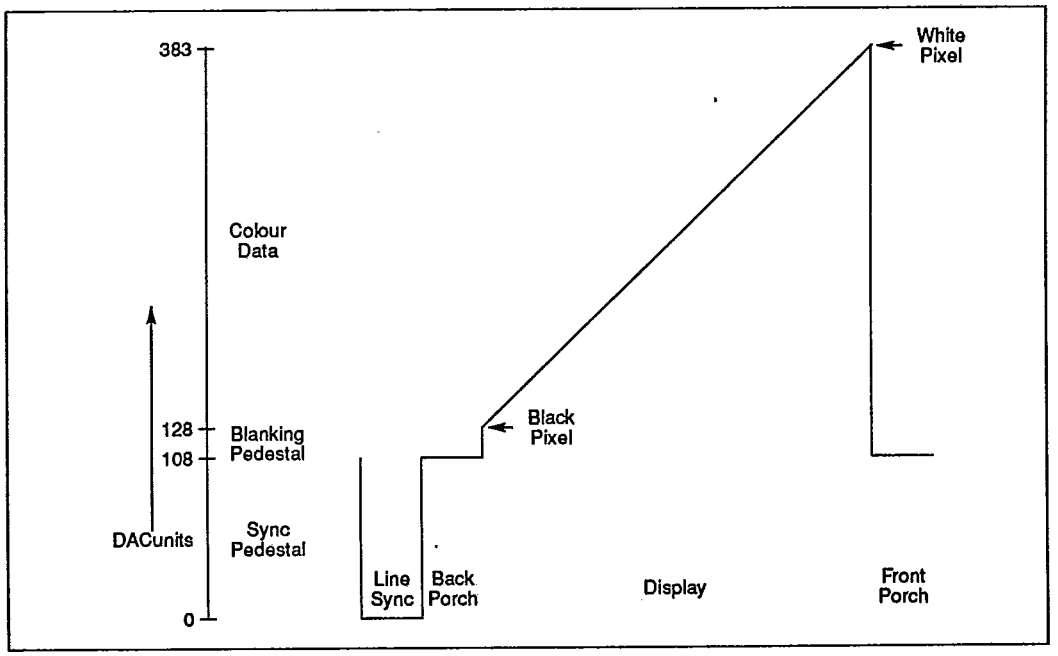


Figure 6.20 Dac Output Levels

6.11 Clock generation and phase locked loop

6.11.1 Introduction

The IMS G300 has two alternate clocking schemes which between them provide a high degree of system flexibility. The primary clocking system uses a phase locked loop on the chip to multiply the low frequency (<10MHz) input clock up to the required video data rate. This scheme is used only when the part is in mode 1 and contributes to its overall ease of design. A full dot-rate clock is supplied to the **PixClkIn** pad for the alternate scheme, which must be used when the IMS G300 is in mode 2 and when mode 1 is to be driven in 'times one' configuration.

6.11.2 PllClkIn

A clock must be supplied to this pad whenever the phase locked loop is to be used. **PllClkIn** must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. **PllClkIn** must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits. Phase locked loop mode is selected by placing a capacitor between **CapPlus** and **CapMinus**.

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TDCLDCH	ClockIn pulse width low	20			ns	
TDCHDCL	ClockIn pulse width high	20			ns	
TDCLDCL	ClockIn period	110		200	ns	1
TDCerror	ClockIn timing error			±1.5	ns	2
TDCr	ClockIn rise time			10	ns	3
TDCf	ClockIn fall time			8	ns	3
Note: These figures are not characterised and are subject to change						

Table 6.16 **PllClkIn** timings

Notes

1 Measured between corresponding points on consecutive falling edges.

2 Variation of individual falling edges from their normal times.

3 Clock transitions must be monotonic within the range **VIH** to **VIL**.

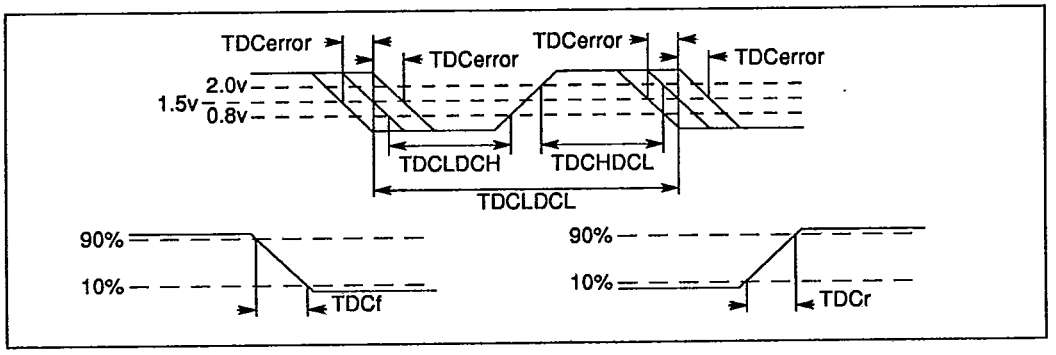


Figure 6.21 ClockIn timing

6.11.3 CapPlus, CapMinus

The internally derived power supply for internal clocks requires an external low leakage, low inductance 1uF capacitor to be connected between **CapPlus** and **CapMinus**. A ceramic capacitor is preferred, with an impedance of less than 3Ω between 100kHz and 10MHz. If a polarised capacitor is used the negative terminal must be connected to **CapMinus**. Total PCB track length should be less than 50mm. The connections must not touch power supplies or other noise sources.

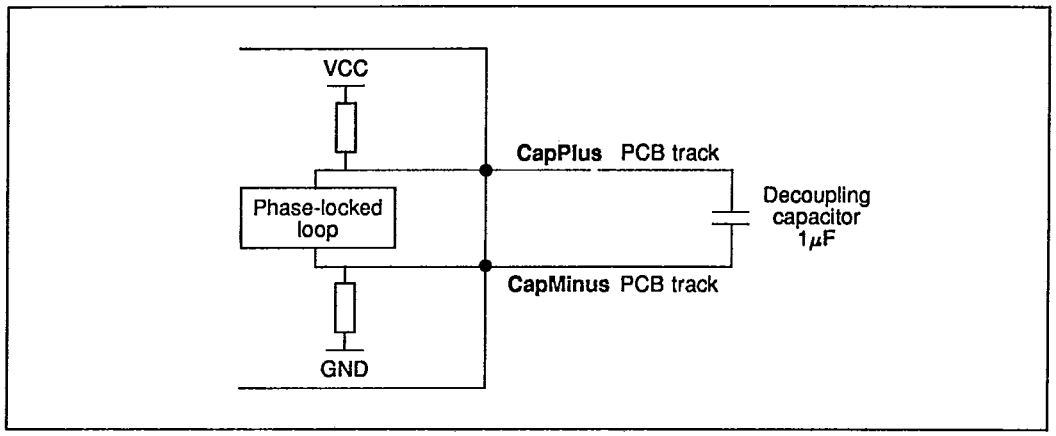


Figure 6.22 Recommended PLL decoupling

6.11.4 Speed selection

The multiplication factor of the phase locked loop is set by writing a binary value to the IMS G300 boot location. This location is enabled for writing by performing a reset cycle. Once it has been written to, another reset must be performed before reprogramming is possible. Only **ADBus**[4:0] are valid as data during these write cycles, in all other respects they conform to the diagrams given in section 6.8 . Although all possible multiplication factors will work with all permissible input frequencies up to the speed rating of the part, the quoted figures are guaranteed only if the recommended combinations are adhered to. The multiplication factor selected is the binary number written to the boot location.

6.11.5 Recommended input clock and multiplication factors

Video data rate (MHz)	PllClkIn (MHz)	Clock Multiplication
30	6	5
40	6.66	6
50	7.142	7
60	7.5	8
70	7.777	9
80	8	10
90	8.181	11
100	8.333	12
110	8.461	13
120	8.571	14

Intermediate video data frequencies can be produced by choosing the multiplication factor for the quoted frequency closest to that desired and varying the input clock frequency to achieve the correct value. Clock multiplication factors less than 5 are not allowed.

6.11.6 PixClkIn

This clock input must be used whenever mode 2 is selected or if mode 1 is to be used without the phase locked loop. Times one mode is selected by shorting **CapPlus** to **CapMinus** using a wire link or a switch.

6.12 General parametric conditions and characteristics

6.12.1 Operating conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts	
GND	Ground		0		Volts	
VIH	Input Logic '1' Voltage	2.0		VDD+0.5	Volts	
VIL	Input Logic '0' Voltage	−0.5		0.8	Volts	
TCPGA	Maximum Case Temperature			**tbd**	deg C	1
TCQC	Maximum Case Temperature			**tbd**	deg C	1
Note: These figures are not characterised and are subject to change						

Notes

1 Measured on the lid of the package at maximum power dissipation.

6.12.2 Operating characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
IDD	Power Supply Current		300	400	mAmps	
IIN	Digital Input Current			± 10	uAmps	
IOZ	Off State Dig Output Current			± 50	uAmps	
VOH	Output Logic '1' Voltage	2.4			Volts	
IOH	Output Logic '1' Current	−5			mAmps	
VOL	Output Logic '0' Voltage			0.4	Volts	
IOH	Output Logic '0' Current	5			mAmps	
Note: These figures are not characterised and are subject to change						

6.12.3 Output drive capability

PIN	MIN	TYP	MAX	UNITS
notShiftClk			25	pF
notSerialClk			25	pF
Transfer			25	pF
ADBus [23:0]			25	pF

6.13 Package specifications

6.13.1 84 pin grid array package

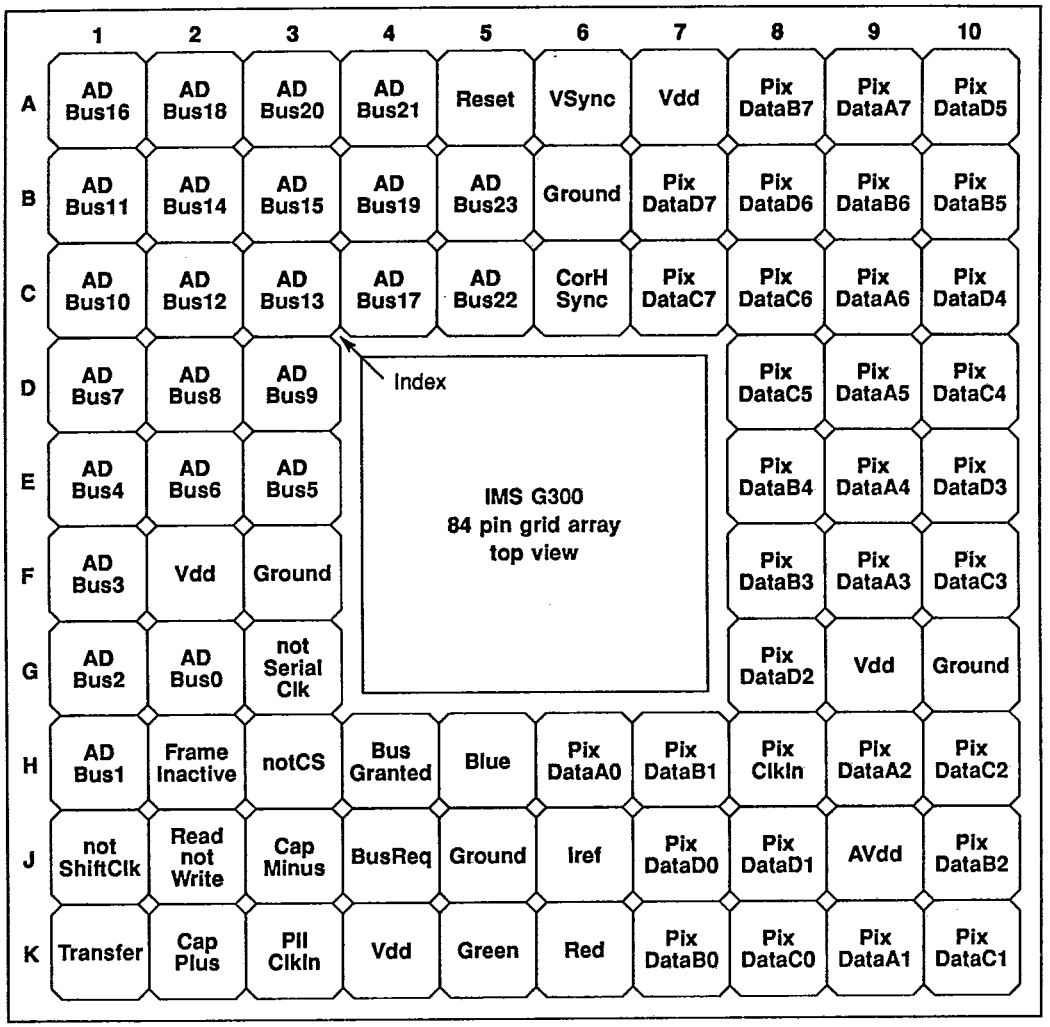


Figure 6.23 IMS G300 pin configuration

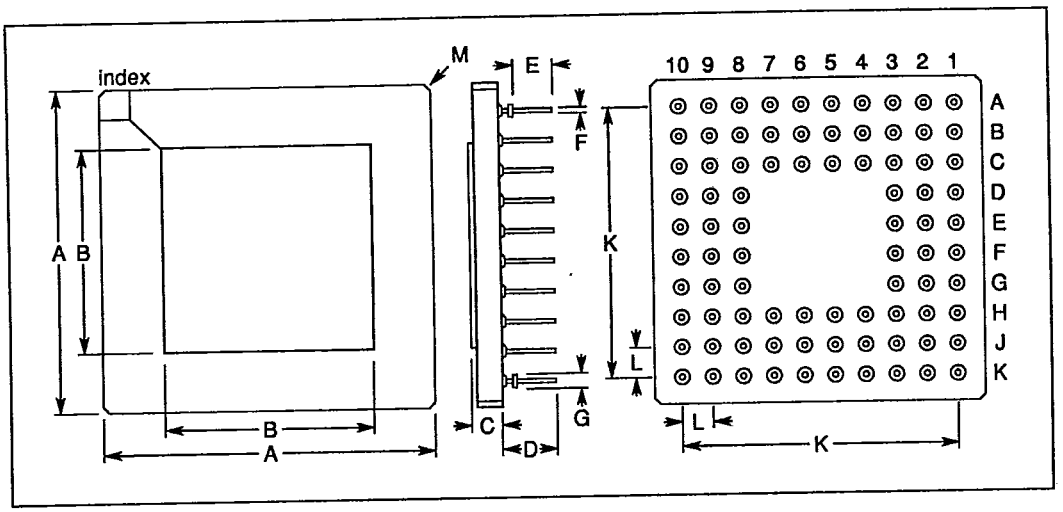


Figure 6.24 84 pin grid array package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	26.924	±0.254	1.060	±0.010	
B	17.019	±0.127	0.670	±0.005	
C	2.456	±0.278	0.097	±0.011	
D	4.572	±0.127	0.180	±0.005	
E	3.302	±0.127	0.130	±0.005	
F	0.457	±0.025	0.018	±0.001	Pin diameter
G	1.143	±0.127	0.045	±0.005	Flange diameter
K	22.860	±0.127	0.900	±0.005	
L	2.540	±0.127	0.100	±0.005	
M	0.508		0.020		Chamfer
Package weight is approximately 7.2 grams					

Table 6.17 84 pin grid array package dimensions

6.13.2 84 lead quad cerpack package

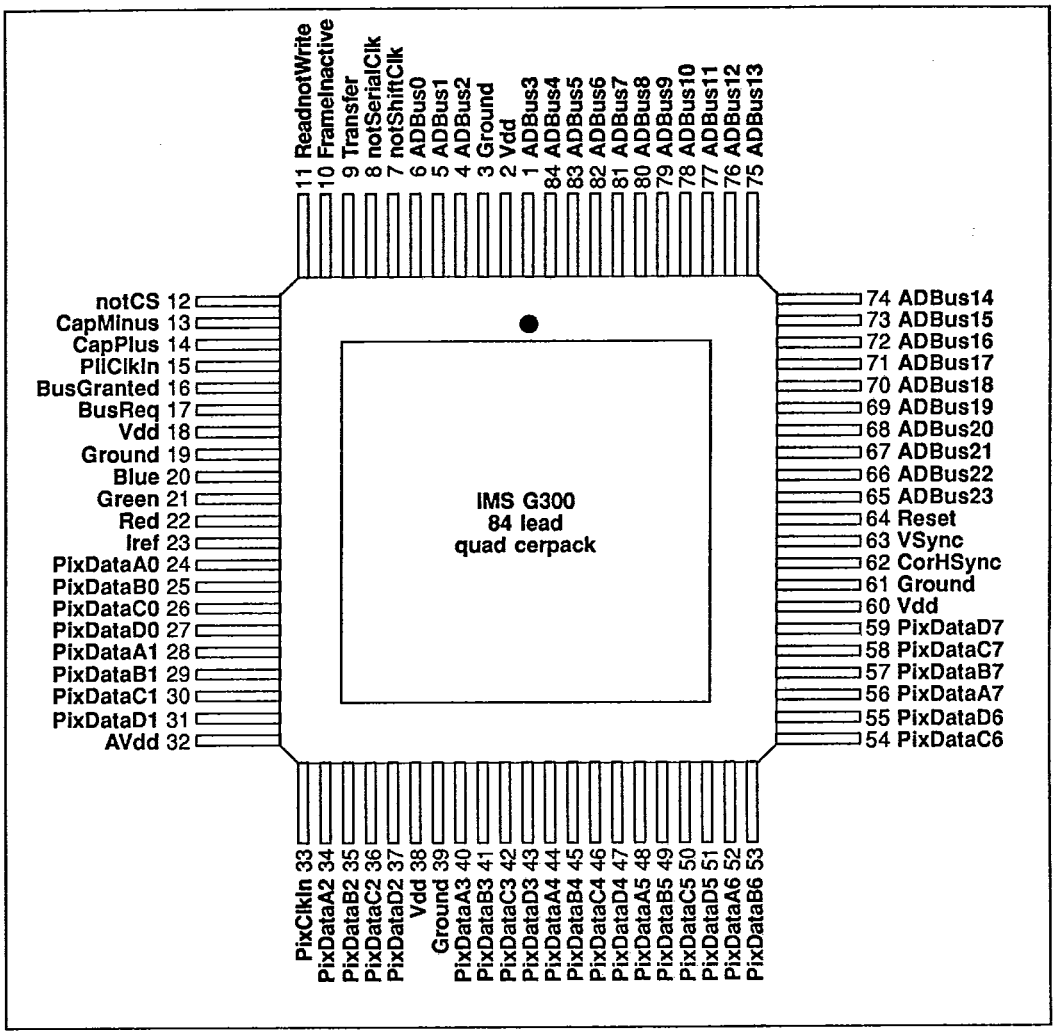


Figure 6.25 IMS G300 pin configuration

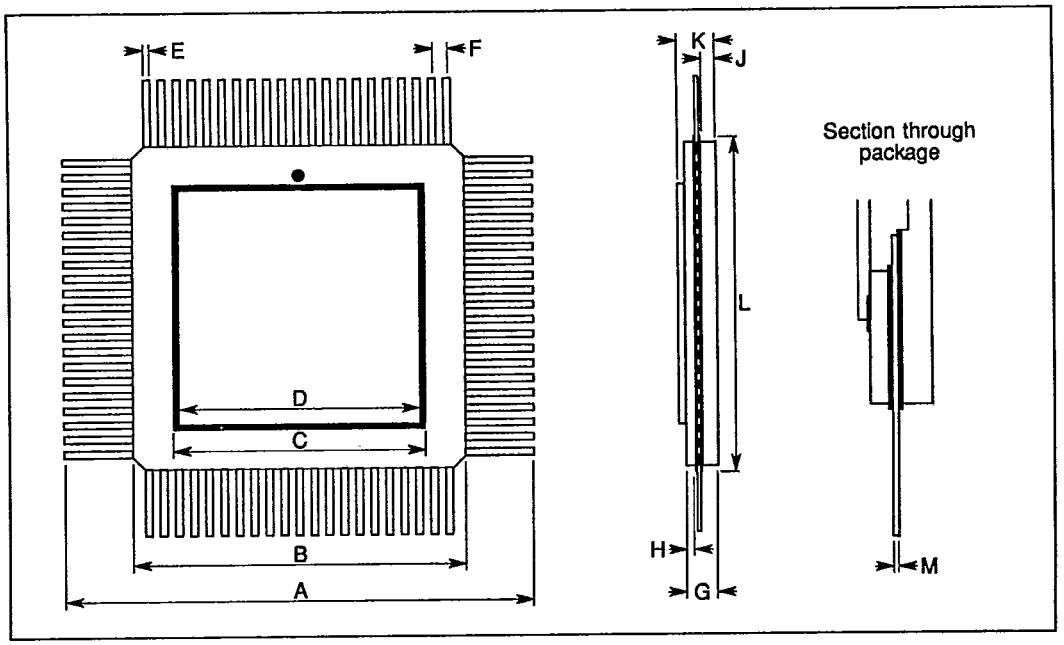


Figure 6.26 84 lead quad cerpack package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	38.100	±0.508	1.500	±0.020	
B	26.924	±0.305	1.060	±0.012	
C	20.574	±0.203	0.810	±0.008	
D	19.558	±0.254	0.770	±0.010	
E	0.508		0.020		
F	1.270	±0.051	0.050	±0.002	
G	2.489	±0.305	0.098	±0.012	
H	0.635	±0.076	0.025	±0.003	
J	1.143	±0.102	0.045	±0.004	
K	3.099		0.122		Max.
L	27.940		1.100		Max.
M	0.178	±0.025	0.007	±0.001	

Table 6.18 84 lead quad cerpack package dimensions

6.13.3 Ordering information

Device	Clock rate	Package	Part number
IMS G300	66 MHz	84 pin PGA	IMS G300G-66
IMS G300	85 MHz	84 pin PGA	IMS G300G-85
IMS G300	100 MHz	84 pin PGA	IMS G300G-10
IMS G300	110 MHz	84 pin PGA	IMS G300G-11
* IMS G300	120 MHz	84 pin PGA	IMS G300G-12
IMS G300	66 MHz	84 pin QUAD CERPAC	IMS G300Q-66
IMS G300	85 MHz	84 pin QUAD CERPAC	IMS G300Q-85
IMS G300	100 MHz	84 pin QUAD CERPAC	IMS G300Q-10
IMS G300	110 MHz	84 pin QUAD CERPAC	IMS G300Q-11
* IMS G300	120 MHz	84 pin QUAD CERPAC	IMS G300Q-12

* Available 2nd half 1989

6.14 Programming example for Hitachi HM-4219/4119 monitor

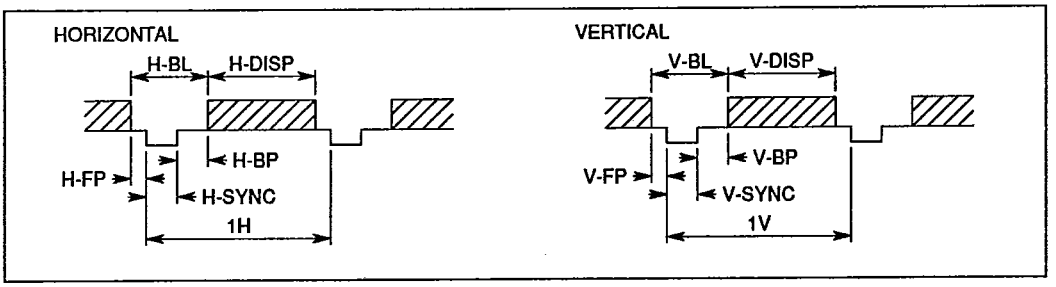


Figure 6.27 Hitachi HM-4219/4119 timing

	Item	Equation	Rating (64KHz Version)	Unit
a	Resolution H		1280	Pixel
b	Resolution V		1024	Pixel
c	Pixel rate		9.296	ns
d	Pixel frequency	1/c	107.573	MHz
e	H-DISP	a × c	11.899	μs
f	H-BL	g + h + i	3.800	μs
g	H-FP		0.200	μs
h	H-SYNC		1.600	μs
i	H-BP		2.000	μs
j	1H		15.699	μs
k	H frequency	1/j	63.7	KHz
l	V-DISP	b × j	(1024H)	ms
m	V-BL	n + o + p	(37H)	ms
n	V-FP		(0H)	ms
o	V-SYNC		(3H)	ms
p	V-BP		(34H)	ms
q	1V	l + m	(1061H)	ms
r	V frequency	1/q	60.0	Hz

Table 6.19 Recommended timings for monitor (64Khz version)

6.14.1 Calculation of parameters

At the recommended pixel rate of 9.296ns,

1 screen unit = 4 × 9.296ns = 37.184ns

All line timing parameters are calculated as multiples of this figure.

Line Scan period

Linetime = 15.699μs / 37.184ns = 422.19

so set Linetime = 422

This obeys the rule associated with the Linetime parameter; that it should be an even number of screen units.

If it is absolutely necessary to meet the recommended linescan frequency then it is best to specify the input clock frequency as the variable but, in practice, all monitors will synchronise to a close approximation.

Line sync pulse

The G300 constructs this from two halfsync periods so:

$$\text{Halfsync} = 1.6\mu s / (2 \times 37.184ns) = 21.5$$

so set Halfsync = 21 screen units

Backporch

$$\text{Backporch} = 2\mu s / 37.184ns = 53.7$$

so set Backporch = 54 screen units

Display

This parameter is set in terms of the number of pixels you wish to display so in this case:

$$\text{Display} = 1280 / 4 = 320 \text{ screen units.}$$

Frontporch

There is no explicit frontporch parameter; this period being implied as the difference between the sum of the other parameters and the linetime period.

$$\begin{aligned}\text{Frontporch} &= \text{Linetime} - ((\text{Halfsync} \times 2) + \text{Backporch} + \text{Display}) \\ &= 422 - (21 \times 2 + 54 + 320) \\ &= 6 \text{ screen units} \\ &= 6 \times 37.184 \text{ ns} = 0.223\ \mu s\end{aligned}$$

Which compares with the monitor requirement of 0.2 μs.

The 'halfline point' rule is obeyed by these timings since:

$$(\text{HalfSync} \times 2) + \text{Backporch} + \text{Display} < \text{Linetime} / 2 > (\text{HalfSync} \times 2) + \text{Backporch}$$

In a non interlaced system such as this the remaining two line parameters are actually used only during frame flyback in order to count in multiples of half a line time. In an interlaced system, the parameter Shortdisplay is used to construct the short displayed lines at top and bottom of the screen if the total number of displayed lines is odd. BroadPulse is used to produce the low pulses in a tesselated frame sync period. Both of these parameters must always be programmed whether or not your system explicitly uses them.

ShortDisplay

$$\begin{aligned}\text{Shortdisplay} &= (\text{Linetime} / 2) - (\text{HalfSync} \times 2) + \text{Backporch} + \text{FrontPorch} \\ &= 211 - (42 + 54 + 6) \\ &= 109 \text{ screen units}\end{aligned}$$

$$\begin{aligned}\text{BroadPulse} &= (\text{Linetime} / 2) - \text{Frontporch} \\ &= 211 - 6 \\ &= 205 \text{ screen units}\end{aligned}$$

Frame timing parameters

All frame timings are specified in terms of half line times.

Number of Displayed lines is 1024

$$\text{VDisplay} = 1024 \times 2 = 2048$$

Which complies with the requirement that each frame must contain an even number of half lines.

The G300 produces frame flyback waveforms in accordance with the broadcast standards which means that:

$$VSync = PreEqualisation = PostEqualisation$$

$$VSync = 6$$

Total Blanked period is 37H so :

$$VBlank = 74 - (6 \times 3) = 56$$

Which is a whole number of lines.

Thus the complete list of screen parameters is:

HalfSync	=	21
BackPorch	=	54
Display	=	320
LineTime	=	422
ShortDisplay	=	109
BroadPulse	=	205
VSync	=	6
VBlank	=	56
VDisplay	=	2048

The remaining three parameters are concerned with management of the video ram bitmap. Assuming that 256K video rams are being used, the shift register length will be 256 bits. The sum of the parameters MemInit and TransferDelay must not exceed this figure unless some external form of multiplexing is used which generates an effective register length greater than this. It is possible to use parameters which total less than 256 in order to implement a hardware pan function, but for the purpose of this example, we will assume that all of the bitmap is to be displayed. Thus:

$$MemInit + TransferDelay = 256$$

Transfer delay is

System DMA latency + VRAM access time + 1 Screen unit

Assume DMA latency to be around 500ns and the VRAM access time to be 100ns then:

$$\begin{aligned} TransferDelay &= 600ns / 37.184ns + 1 = 17.13 \\ &= 18 \text{ screen units} \end{aligned}$$

Which obeys the conditions for TransferDelay that:

$$TransferDelay < Backporch$$
$$TransferDelay < ShortDisplay$$

(These are the only screen related limitations on the value of the VRAM management parameters)

$$MemInit = 256 - 18 = 238 \text{ screen units.}$$

LineStart is the top of screen pointer and it can be programmed to any value but with the following restrictions.

If the bitmap is to appear byte-linear to the processor, the SAM start address must be zero.

The SAM start address must never become greater than (256 – TransferDelay)