HMC

HM 6116L, HM 6116LK, HM 6116LM
2K X 8 CMOS STATIC RAM

General Description

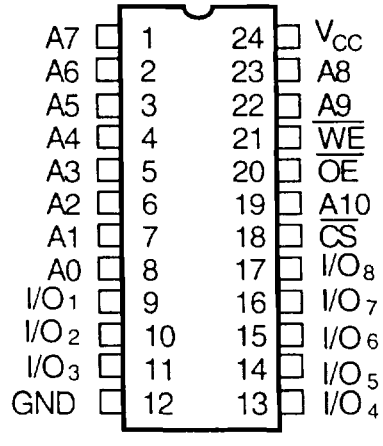
The HM 6116L is a 16,384-bit static random access memory organized as 2,048 words by 8 bits and operates from a single 5 volt supply. It is built with high performance twin tub CMOS process. Six-transistor full CMOS memory cell provides low stand by current and high-reliability. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Features

* High speed - 70/90/120 ns(MAX.).
* Low Power consumption.
  250mW(Typ.) Operating. 5 μW(Typ.) Standby.
* Single 5V power supply.
* Fully static operation.
* All inputs and outputs directly TTL compatible.
* Three-state outputs.
* Data retention supply voltage: 2.0-5.5V.
* Package : HM 6116L - 24 pin 600 mil plastic DIP.
  HM 6116LK - 24 pin 300 mil plastic Skinny DIP.
  HM 6116KM - 24 pin 300 mil plastic SOP.

Pin Assignment

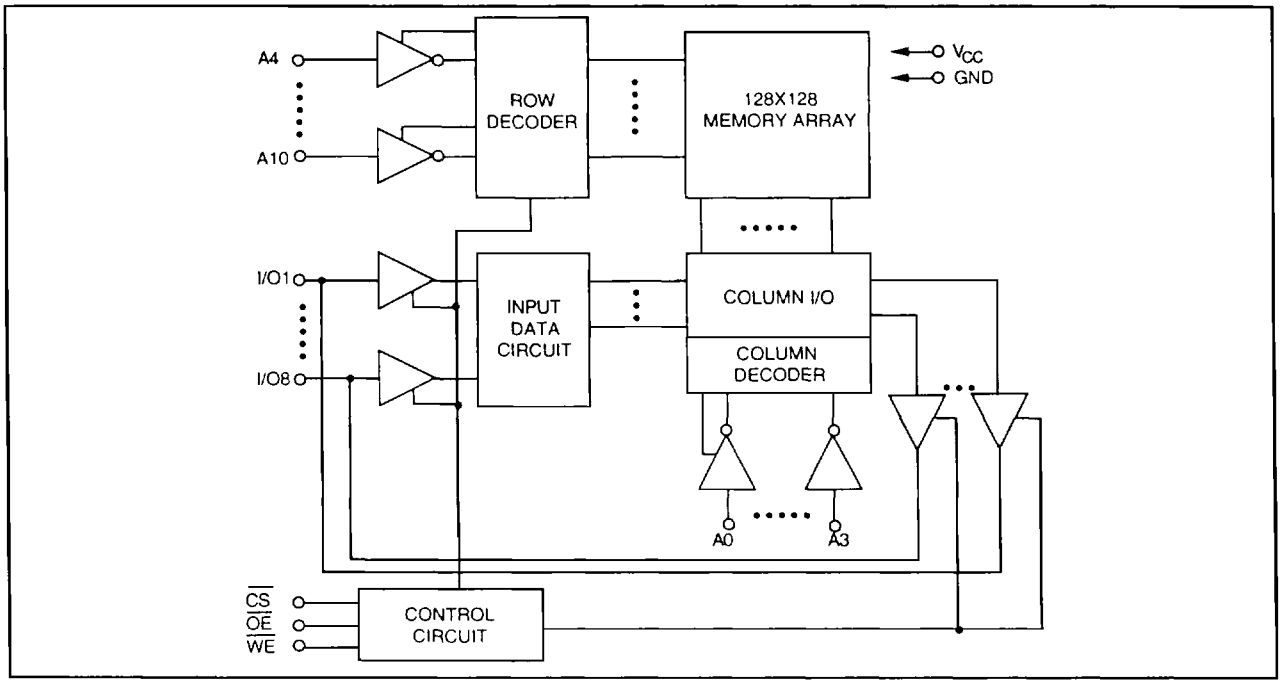
HM 6116L, HM 6116LK, HM 6116LM



Pin Description

A_0-A_{10}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1-I/O_8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER	$\overline{CS}$	CHIP SELECT
GND	GND GROUND		

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	RATING	Units
Supply Voltage		V_{CC} GND	- 0.3 to 7	V
Input Voltage		V_{IN}	- 0.3 to 7	V
Input/Output Voltage Applied		$V_{I/O}$	- 0.3 to V_{CC} + 0.3	V
Temp under Bias	Plastic	T_{BIAS}	- 10 to 85	°C
Storage Temperature	Plastic	T_{STG}	- 40 to + 125	°C
Power Dissipation		P_T	1.0	W
D.C. Output Current		I_{OUT}	50	mA

* Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operation Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V±10%

Recommended DC Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	3.5	5.8	V
Input Low Voltage	V_{IL}	-0.3	-	+0.8	V
Output Load	C_L	-	-	100	pF
Output Load	TTL	-	-	1	-

D.C. Electrical Characteristics

over the operating range (V_{CC}=5V, T_A=25°C)

Parameter	Sym.	6116L-70 Min	Typ	Max	6116L-90 Min	Typ	Max	6116L-120 Min	Typ	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	-	-	10	-	-	10	µA	V_{CC}=5.5V, V_{IN}=GND to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	-	-	10	-	-	10	µA	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=GND to V_{CC}
Operating Power Supply Current	I_{CC}	-	50	80	-	50	80	-	50	80	mA	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA
	I_{CC1}	-	45	-	-	45	-	-	45	-	mA	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0 mA
Dynamic Operating Current	I_{CC2}	-	-	80	-	-	80	-	-	80	mA	Min. Duty Cycle=100%
Standby Supply Power Current	I_{SB}	-	5	10	-	5	10	-	5	15	mA	$\overline{CS}$=V_{IH}
	I_{SB1}	-	1	3	-	1	3	-	1	3	µA	$\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥ V_{CC}-0.2V or V_{IN}≤ 0.2V
Output Low Voltage	V_{OL}	-	-	0.4	-	-	0.4	-	-	0.4	V	I_{OL}=4mA
Output High Voltage	V_{OH}	2.4	-	-	2.4	-	-	2.4	-	-	V	I_{OH}=-1.0mA

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{out}
Output Disable	L	H	H	High Z
Write	L	X	L	D_{in}

Capacitance*

(T_A=25°C , f=1.0MHz)

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	8	pF	V_{IN}=0V
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{I/O}$=0V

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output	1.5V
Timing Reference Levels	1 TTL Gate
Output Load	and C_L=100pF (including scope and jig.)

* This parameter is periodically sampled and not 100% tested.

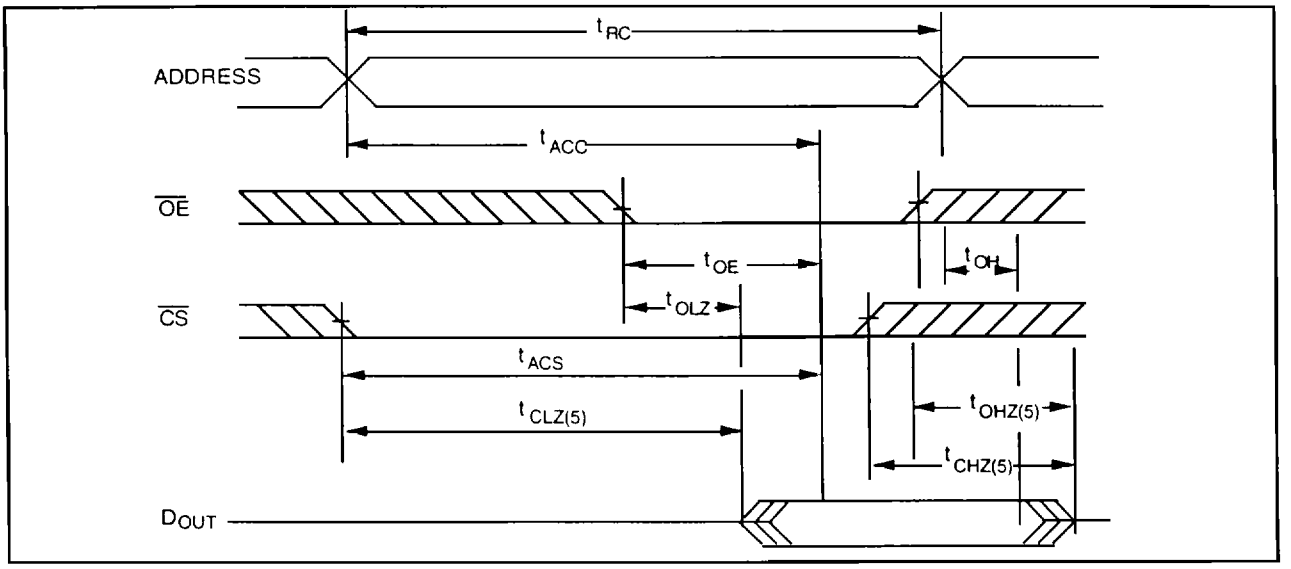
AC Electrical Characteristics

over the operating range

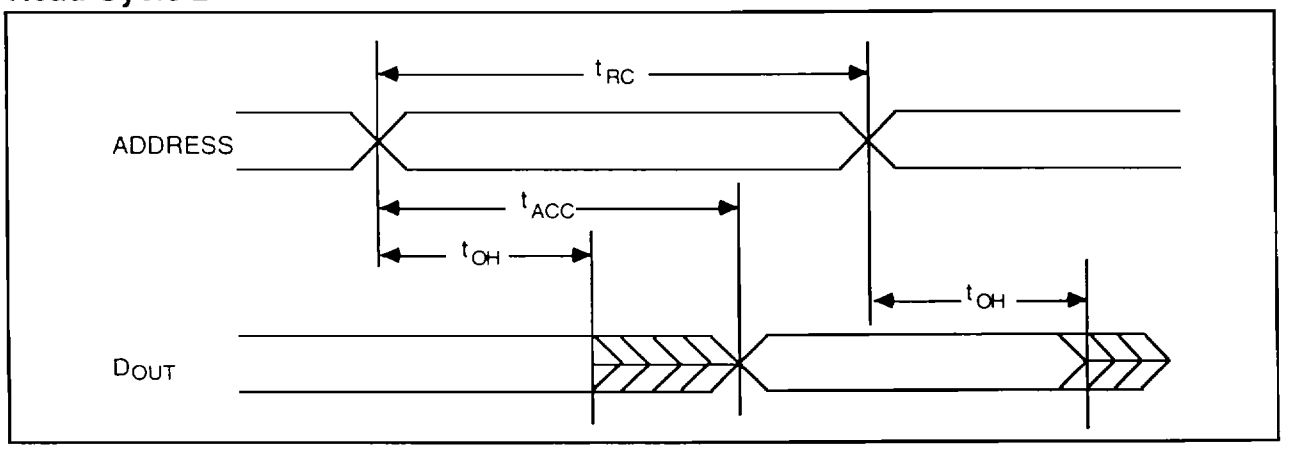
Parameter	Symbol	6116L-70		6116L-90		6116L-120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
Read Cycle Time	t_{RC}	70	-	90	-	120	-	ns
Address Access Time	t_{Acc}	-	70	-	90	-	120	ns
Chip Select Access Time	t_{ACS}	-	70	-	90	-	120	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	5	-	ns
Output Enable to Output Valid	t_{OE}	-	30	-	65	-	80	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	ns
Chip Deselection to Output In High Z	t_{CHZ}	0	35	0	40	0	40	ns
Output Disable to Output In High Z	t_{OHZ}	0	35	0	40	0	40	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
Write Cycle								
Write Cycle Time	t_{WC}	70	-	90	-	120	-	ns
Chip Selection to End of Write	t_{CW}	45	-	55	-	75	-	ns
Address Valid to End of Write	t_{AW}	65	-	80	-	105	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	20	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	5	-	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	40	ns
Write to Output in High Z	t_{WHZ}	0	40	0	50	0	50	ns
Data to Write Time Overlap	t_{DW}	30	-	30	-	30	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	0	-	0	-	0	-	ns

Timing Waveforms of Read Cycle No.1

Note (1).

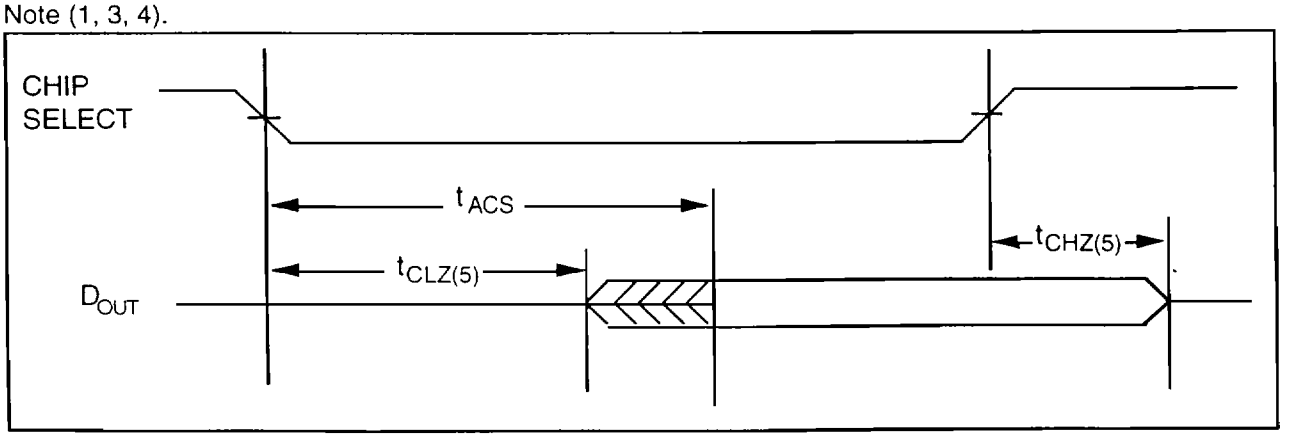


Read Cycle 2



Read Cycle 3

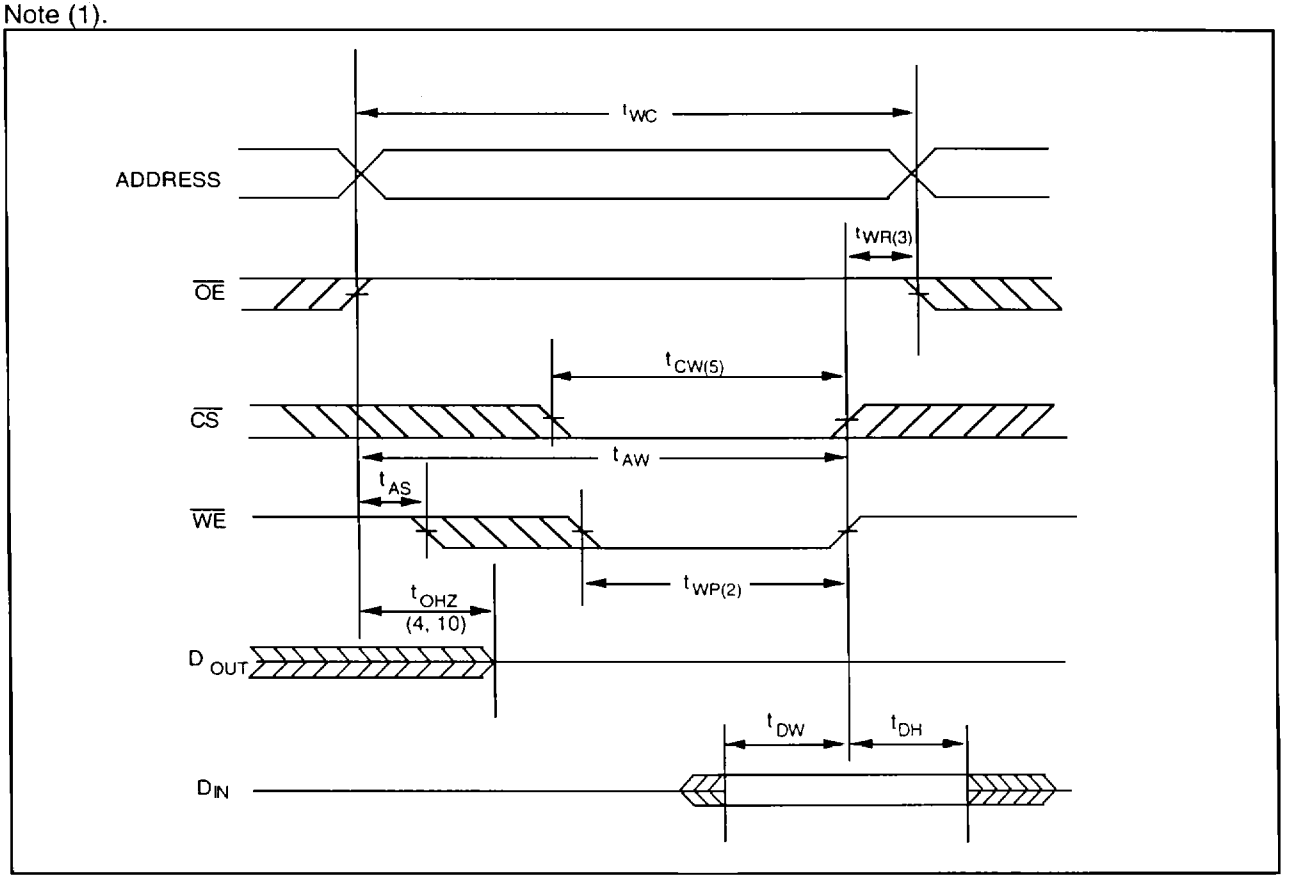
Note (1, 3, 4).



Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}=V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}=V_{IL}$.
5. Transition is measured ±500 mV from steady state. This parameter is sampled and not 100% tested.

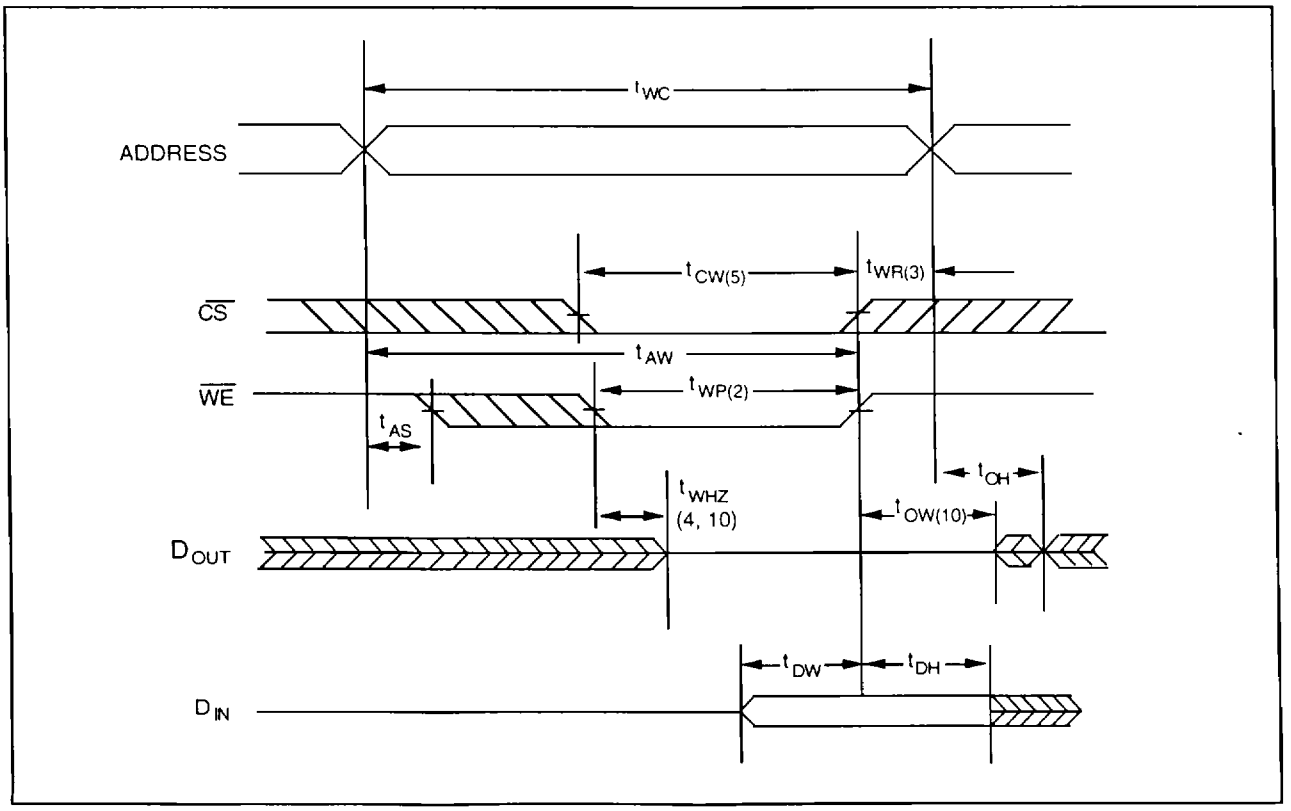
Timing Waveforms Of Write Cycle 1

Note (1).



Write Cycle 2

(1, 6)



Notes: 1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP})of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$=V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500 mV from steady state. This parameter is sampled and not 100% tested.

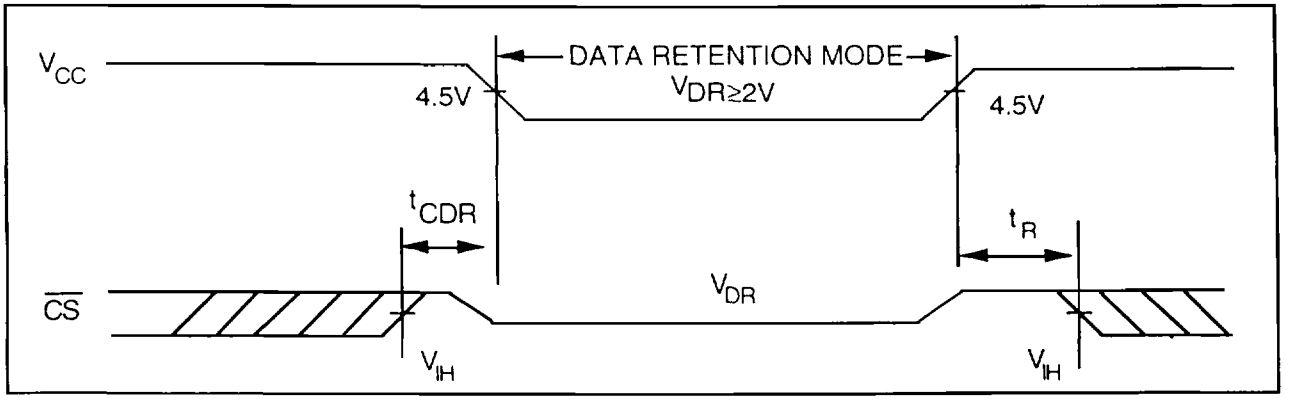
Data Retention Characteristics

over the operating temperature range

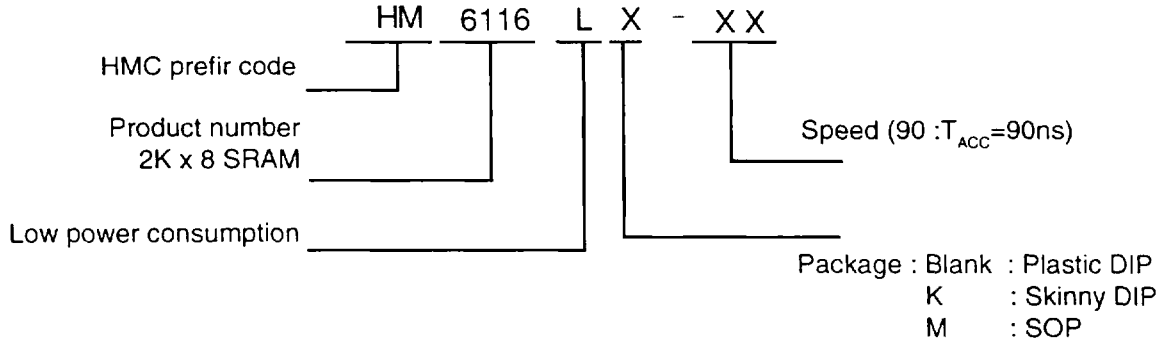
Parameter	Symbol	Min.	Typ.(1)	Max.	Unit	Conditions
V_{CC} for Retention Data	V_{DR}	20	-	-	V	$\overline{CS}$= V_{CC}
Data retention Current	I_{CCDR}	-	2	3	µA	V_{IN}=0V or V_{CC}
Chip Deselect to Data Retention Time	t_{CDR}	0	-	-	ns	V_{CC}=2.0V, CS=V_{CC}
Operation Recovery Time	t_R	t_{RC}(2)	-	-	ns	V_{IN}=0V or V_{CC}

1. V_{CC}=2V, T_A=+25°C .
2. t_{RC}=Read Cycle Time.

Low V_{CC} DATA Retention Waveform

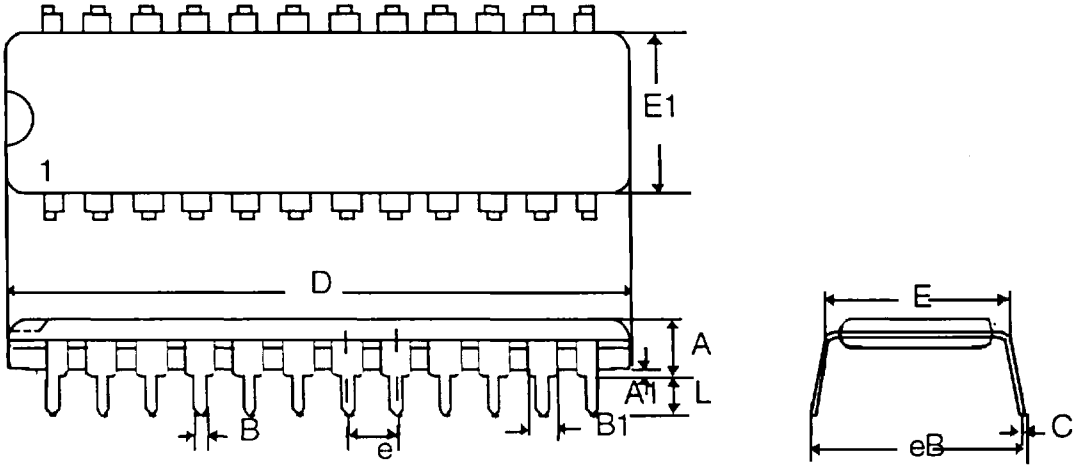


Ordering Information



Order Number	Access Time (ns)	Operation Current (mA)	Standby Current (μA)	Package Type
HM 6116L- 70	70	100	10	
HM 6116L- 90	90	100	10	24L DIP
HM 6116L-120	120	100	10	
HM 6116L-150	150	100	10	
HM 6116LK- 70	70	100	10	
HM 6116LK- 90	90	100	10	24L
HM 6116LK-120	120	100	10	Skinny DIP
HM 6116LK-150	150	100	10	
HM 6116LM- 70	70	100	10	
HM 6116LM- 90	90	100	10	24LSOP
HM 6116LM-120	120	100	10	(300 mil)
HM 6116LM-150	150	100	10	

24 Lead Plastic Skinny DIP

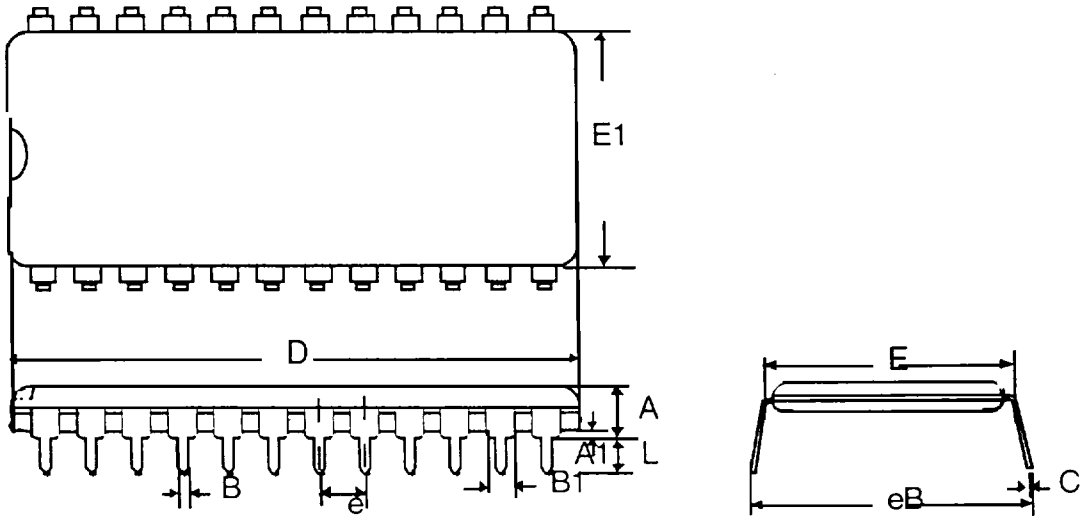


Notes :
1. DIM D & E1 do not include mold flash or protrusions.
2. DIM eB measured at the lead tips with the leads unconstrained.

DIM	MILIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	----	5.334	----	.210
A1	0.381	----	.015	----
B	0.356	0.558	.014	.022
B1	1.150	1.778	.045	.070
C	0.204	0.381	.008	.015
D	28.96	32.26	1.140	1.270
E	7.62	8.255	.300	.325
E1	6.096	7.112	.240	.280
e	2.286	2.794	.090	.110
eB	----	10.92	----	.430
L	2.921	4.064	.115	.160

Package Information

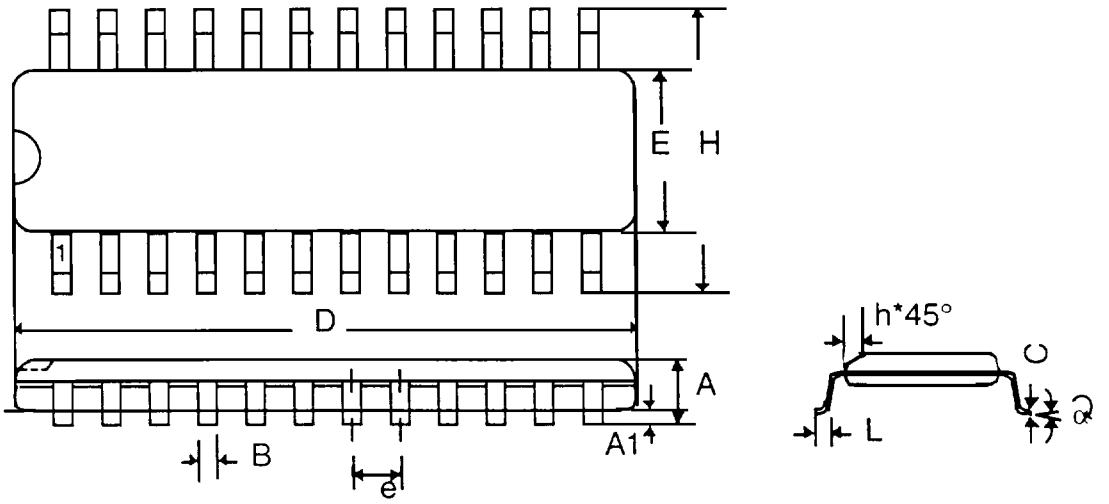
24 Lead Plastic Dual - Inline Package



Notes :
1. DIM D & E1 do not include mold flash or protrusions.
2. DIM eB measured at the lead tip with the leads unconstrained.

DIM	MILIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	----	6.350	----	.250
A1	0.381	----	.015	----
B	0.356	0.558	.014	.022
B1	1.016	1.778	.040	.070
C	0.204	0.381	.008	.015
D	30.48	32.77	1.200	1.290
E	15.24	15.88	.600	.625
E1	13.21	14.73	.520	.580
e	2.286	2.794	.090	.110
eB	----	17.78	----	.700
L	2.921	5.080	.115	.200

24Lead Plastic Small Outline Package



Notes :
1. DIM D & E do not include mold flash or protrusions protrusions shall not exceed 0.15mm/.006in.
2. Controlling dimension : millimeter.

DIM	MILIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	.0926	.1043
A1	0.10	0.30	.0040	.0118
B	0.35	0.49	.0138	.0192
C	0.23	0.32	.0060	.0125
D	15.20	15.60	.5985	.6141
E	7.40	7.60	.2914	.2992
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	.25	0.75	.010	.029
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°