m i c r o e l e c t r o n i c s group

Lucent Technologies
Bell Labs Innovations

ORCA® ORT4622 Field-Programmable System Chip (FPSC) Four-Channel x 622 Mbits/s Backplane Transceiver

Introduction

Lucent Technologies Microelectronics Group has developed a solution for designers who need the many advantages of FPGA-based design implementation, coupled with high-speed serial backplane data transfer. The 622 Mbits/s backplane transceiver offers a clockless, high-speed interface for interdevice communication on a board or across a backplane. The built-in clock recovery of the ORT4622 allows for higher system performance, easier-to-design clock domains in a multiboard system, and fewer signals on the backplane. Network designers will benefit from the backplane transceiver as a network termination device. The backplane transceiver offers SONET scrambling/descrambling of data and streamlined SONET framing, pointer moving and transport overhead handling, plus the programmable logic to terminate the network into proprietary systems.

Embedded Core Features

- Implemented in an *ORCA* Series 3 FPGA array.
- Allows wide range of applications for SONET network termination application as well as generic data moving for high-speed backplane data transfer.
- High-speed interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- HSI function uses Lucent Technologies Microelec-

tronics Group's proven 622 Mbits/s serial interface core.

- Four-channel HSI function provides 622 Mbits/s serial interface per channel for a total chip bandwidth of 2.5 Gbits/s (full duplex).
- LVDS I/Os for HSI compliant with *EIA**-644.
- 8:1 data multiplexing/demultiplexing for 77.76 MHz byte-wide data processing in FPGA logic.
- On-chip phase-lock loop (PLL) clock meets B jitter tolerance specification of ITU-T Recommendation G.958.
- Powerdown option of HSI receiver on a per-channel basis.
- Pseudo-SONET protocol including A1/A2 framing.
- SONET scrambling and descrambling for required ones density (optional).
- Selected transport overhead (TOH) bytes insertion and extraction for interdevice communication via the TOH serial link.
- Streamlined pointer processor (pointer mover) for 8 kHz frame alignment.
- FIFOs align incoming data across all four channels for STS-48 operation (in quad STS-12 format).
- Independent data stream enables in pseudo-SONET processor.
- Supports STS-12/STS-48 redundancy by either software or hardware control for protection switching applications.

* *EIA* is a registered trademark of Electronic Industries Association.

Table 1. *ORCA* ORT4622—Available FPGA Logic

Device	Usable Gates[†]	Number of LUTs	Number of Registers	Max User RAM	Max User I/Os	Array Size	Number of PFUs
ORT4622	60K—120K	4032	5304	64K	259	18 x 28	504

† The embedded core and interface are not included in the above gate counts. The usable gate count range from a logic-only gate count to a gate count assuming 30% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates per PFU/SLIC), including 12 gates pre-LUT/FF pair (eight per PFU), and 12 gates per SLC/FF pair (one per PFU). Each of the four PIOs per PIC is counted as 16 gates (two FFs, fast-capture latch, output logic, CLK drivers, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU.

Table of Contents

Table of Contents (continued)

FPSC Highlights

- Implemented as an embedded core in the *ORCA* Series 3+ FPSC architecture.

- Allows the user to integrate the core with up to 120K gates of programmable logic (all in one device) and provides up to 242 user I/Os in addition to the embedded core I/O pins.

- FPGA portion retains all of the features of the *ORCA* Series 3 FPGA architecture:
  — High-performance, cost-effective, 0.25 μm, 5-level metal technology.
  — Twin-quad programmable function unit (PFU) architecture with eight 16-bit look-up tables (LUTs) per PFU, organized in two nibbles for use in nibble- or byte-wide functions. Allows for mixed arithmetic and logic functions in a single PFU.
  — Softwired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU.
  — Supplemental logic and interconnect cell (SLIC) provides 3-statable buffers, up to 10-bit decoder, and *PAL**-like AND-OR-INVERT (AOI) in each programmable logic cell (PLC).
  — Up to three ExpressCLK inputs allow extremely fast clocking of signals on- and off-chip plus access to internal general clock routing.
  — Dual-use microprocessor interface (MPI) can be used for configuration, as well as for a general-purpose interface to the FPGA. Glueless interface to *i960*[†] and *PowerPC*[‡] processors with user-configurable address space provided.
  — Programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 5 MHz to 120 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops, frequency counters, and frequency synthesizers or clock doublers. Two PCMs are provided per device.
  — True internal 3-state, bidirectional buses with simple control provided by the SLIC.
  — 32 x 4 RAM per PFU, configurable as single or dual port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  — Built-in boundary scan (*IEEE*[§] 1149.1 JTAG) and TS_ALL testability function to 3-state all I/O pins.

- High-speed on-chip interface provided between FPGA logic and embedded core to reduce bottlenecks typically found when interfacing off-chip.

Software Support

- Supported by *ORCA* Foundry software and third-party CAE tools for implementing *ORCA* Series 3+ devices and simulation/timing analysis with the embedded core functions.

- Embedded core configuration options and simulation netlists generated by FPSC Configuration Manager utility.

---

* *PAL* is a trademark of Advanced Micro Devices, Inc.
† *i960* is a registered trademark of Intel Corporation.
‡ *PowerPC* is a registered trademark of International Business Machines Corporation.
§ *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Description

What Is an FPSC?

FPSCs, or field-programmable system chips, are devices that combine field-programmable logic with ASIC or mask-programmed logic on a single device. FPSCs provide the time to market and flexibility of FPGAs, the design effort savings of using soft intellectual property (IP) cores, and the speed, design density, and economy of ASICs.

FPSC Overview

Lucent's Series 3+ FPSCs are created from Series 3 *ORCA* FPGAs. To create a Series 3+ FPSC, several rows of programmable logic cells (see FPGA Logic Overview section for FPGA logic details) are removed from a Series 3 *ORCA* FPGA, and the area is replaced with an embedded logic core. Other than replacing some FPGA gates with ASIC gates, at greater than 10:1 efficiency, none of the FPGA functionality is changed—all of the Series 3 FPGA capability is retained: MPI, PCMs, boundary scan, etc. The rows of programmable logic are replaced at the bottom of the device, allowing pins on the bottom and sides of the replaced rows to be used as I/O pins for the embedded core. The remainder of the device pins retain their FPGA functionality as do special function FPGA pins within the embedded core area.

The embedded cores can take many forms and generally come from Lucent Technologies ASIC libraries. Future offerings will allow customers to supply their own core functions for the creation of custom FPSCs.

FPSC Gate Counting

The total gate count for an FPSC is the sum of its embedded core (standard cell/ASIC gates) and its FPGA gates. Because FPGA gates are generally expressed as a usable range with a nominal value, the total FPSC gate count is sometimes expressed in the same manner. Standard-cell/ASIC gates are, however, 10 to 25 times more silicon area efficient than FPGA gates. Therefore, an FPSC with an embedded function is gate equivalent to an FPGA with a much larger gate count.

FPGA/Embedded Core Interface

The interface between the FPGA logic and the embedded core is designed to look like FPGA I/Os from the FPGA side, simplifying interface signal routing and providing a unified approach with general FPGA design. Effectively, the FPGA is designed as if signals were going off of the device to the embedded core, but the on-chip interface is much faster than going off-chip and requires less power. All of the delays for the interface are precharacterized and accounted for in the *ORCA* Foundry Development System.

Clock spines also can pass across the FPGA/embedded core boundary. This allows for fast, low-skew clocking between the FPGA and the embedded core. Many of the special signals from the FPGA, such as DONE and global set/reset, are also available to the embedded core, making it possible to fully integrate the embedded core with the FPGA as a system.

For even greater system flexibility, FPGA configuration RAMs are available for use by the embedded core. This allows for user-programmable options in the embedded core, in turn allowing for greater flexibility. Multiple embedded core configurations may be designed into a single device with user-programmable control over which configurations are implemented, as well as the capability to change core functionality simply by reconfiguring the device.

ORCA Foundry Development System

The *ORCA* Foundry Development System is used to process a design from a netlist to a configured FPSC. This system is used to map a design onto the *ORCA* architecture and then place and route it using *ORCA* Foundry's timing-driven tools. The development system also includes interfaces to, and libraries for, other popular CAE tools for design entry, synthesis, simulation, and timing analysis.

The *ORCA* Foundry Development System interfaces to front-end design entry tools and provides the tools to produce a configured FPSC. In the design flow, the user defines the functionality of the FPGA portion of the FPSC and embedded core settings at two points in the design flow: at design entry and at the bit stream generation stage. Following design entry, the development system's map, place, and route tools translate the netlist into a routed FPSC. A static timing analysis tool is provided to determine device speed and a back-annotated netlist can be created to allow simulation.

Description (continued)

Timing and simulation output files from *ORCA* Foundry are also compatible with many third-party analysis tools. Its bit stream generator is then used to generate the configuration data which is loaded into the FPSC's internal configuration RAM.

When using the bit stream generator, the user selects options that affect the functionality of the FPSC. Combined with the front-end tools, *ORCA* Foundry produces configuration data that implements the various logic and routing options discussed in this data sheet.

FPSC Design Kit

Development is facilitated by an FPSC Design Kit which, together with *ORCA* Foundry and third-party synthesis and simulation engines, provides all software and documentation required to design and verify an FPSC implementation. Included in the kit are the FPSC Configuration Manager, HDL gate-level structural netlists, all necessary synthesis libraries, and complete online documentation. The kit's software couples with *ORCA* Foundry, providing a seamless FPSC design environment. More information can be obtained by visiting the *ORCA* website or contacting a local sales office, both listed on the last page of this document.

FPGA Logic Overview

ORCA Series 3 FPGA logic is a new generation of SRAM-based FPGA logic built on the successful Series 2 FPGA line from Lucent Technologies Microelectronics Group, with enhancements and innovations geared toward today's high-speed designs on a single chip. Designed from the start to be synthesis friendly and to reduce place and route times while maintaining the complete routability of the *ORCA* Series 2 devices, the Series 3 more than doubles the logic available in each logic block and incorporates system-level features that can further reduce logic requirements and increase system speed. *ORCA* Series 3 devices contain many new patented enhancements and are offered in a variety of packages, speed grades, and temperature ranges.

ORCA Series 3 FPGA logic consists of three basic elements: programmable logic cells (PLCs), programmable input/output cells (PICs), and system-level features. An array of PLCs is surrounded by PICs. Each PLC contains a programmable function unit (PFU), a supplemental logic and interconnect cell (SLIC), local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC. The PICs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, and other functions on two output signals. Some of the system-level functions include the new microprocessor interface (MPI) and the programmable clock manager (PCM).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) look-up tables (LUTs), eight latches/flip-flops (FFs), and one additional flip-flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion: two sets of four LUTs and FFs that can be controlled independently. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

The SLIC is connected to PLC routing resources and to the outputs of the PFU. It contains 3-state, bidirectional buffers and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT (AOI) to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections to the PFU outputs make fast, true 3-state buses possible within the FPGA logic, reducing required routing and allowing for real-world system performance.

Description (continued)

PIC Logic

The Series 3 PIC addresses the demand for ever-increasing system clock speeds. Each PIC contains four programmable inputs/outputs (PIOs) and routing resources. On the input side, each PIO contains a fast-capture latch that is clocked by an ExpressCLK. This latch is followed by a latch/FF that is clocked by a system clock from the internal general clock routing. The combination provides for very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer. Two input signals are available to the PLC array from each PIO, and the *ORCA* Series 2 capability to use any input pin as a clock or other global input is maintained.

On the output side of each PIO, two outputs from the PLC array can be routed to each output flip-flop, and logic can be associated with each I/O pad. The output logic associated with each pad allows for multiplexing of output signals and other functions of two output signals.

The output FF, in combination with output signal multiplexing, is particularly useful for registering address signals to be multiplexed with data, allowing a full clock cycle for the data to propagate to the output. The I/O buffer associated with each pad is the same as the *ORCA* Series 3 buffer.

System Features

The Series 3 also provides system-level functionality by means of its dual-use microprocessor interface (MPI) and its innovative programmable clock manager (PCM). These functional blocks allow for easy glueless system interfacing and the capability to adjust to varying conditions in today's high-speed systems. Since these and all other Series 3 features are available in every Series 3+ FPSC, they can also interface to the embedded core providing for easier system integration.

Routing

The abundant routing resources of *ORCA* Series 3 FPGA logic are organized to route signals individually or as buses with related control signals. Clocks are routed on a low-skew, high-speed distribution network and may be sourced from PLC logic, externally from any I/O pad, or from the very fast ExpressCLK pins. ExpressCLKs may be glitchlessly and independently enabled and disabled with a programmable control signal using the StopCLK feature. The improved PIC routing resources are now similar to the patented intra-PLC routing resources and provide great flexibility in moving signals to and from the PIOs. This flexibility translates into an improved capability to route designs at the required speeds when the I/O signals have been locked to specific pins.

Configuration

The FPGA logic's functionality is determined by internal configuration RAM. The FPGA logic's internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The RAM is loaded by using one of several configuration modes, including serial EEPROM, the microprocessor interface, or the embedded function core.

More Series 3 Information

For more information on Series 3 FPGAs, please refer to the Series 3 FPGA data sheet, available on the *ORCA* worldwide website or by contacting Lucent Technologies as directed on the back of this data sheet.

ORT4622 Overview

Device Layout

The ORT4622 FPSC provides a high-speed backplane transceiver combined with FPGA logic. The device is based on a 2.5 V/3.3 V OR3L125B FPGA. The OR3L125B has a 28 x 28 array of programmable logic cells (PLCs). For the ORT4622, the bottom ten rows of PLCs in the array were replaced with the embedded backplane transceiver core. The ORT4622 embedded core comprises the HSI macrocell, the synchronous transport module (STM) macrocell, a CPU interface, and LVDS I/Os. The four full-duplex channels perform data transfer, scrambling/descrambling and framing at the rate of 622 Mbits/s. Figure 1 shows the ORT4622 block diagram.

Figure 2 shows a schematic view of the ORT4622. The upper portion of the device is an 18 x 28 array of PLCs surrounded on the left, top, and right by programmable input/output cells (PICs). At the bottom of the PLC array are the core interface cells (CICs) connecting to the embedded core region. The embedded core region contains the backplane transceiver functionality of the device. It is surrounded on the left, bottom, and right by backplane transceiver dedicated I/Os as well as power and special function FPGA pins. Also shown are the interquad routing blocks (hIQ, vIQ) present in the Series 3 FPGA devices. System-level functions (located in the corners of the PLC array), routing resources, and configuration RAM are not shown in Figure 2.

Backplane Transceiver Interface

The advantage of the ORT4622 FPSC is to bring specific networking functions to an early market presence with programmable logic in FPGA system.

The 622 Mbits/s backplane transceiver core allows the ORT4622 to communicate across a backplane or on a given board at an aggregate speed of 2.5 Gbits/s, providing a physical medium for high-speed asynchronous serial data transfer between system devices. This device is intended for, but not limited to, connecting terminal equipment in SONET/SDH and ATM systems.

For networking applications, the ORT4622 offers a SONET framer and scrambler/descrambler interface capable of frame synchronization and insertion/extraction of selectable transport overhead bytes and SONET scrambling and descrambling for four STS-12 (622 Mbits/s) channels. The channels are synchronized to each other by a user provided 8 kHz frame pulse. The ORT4622 also provides STS-48 (2.5 Gbits/s) operation across all four channels as long as each channel is in STS-12 format. Figure 3 shows the architecture of the ORT4622 backplane transceiver core.
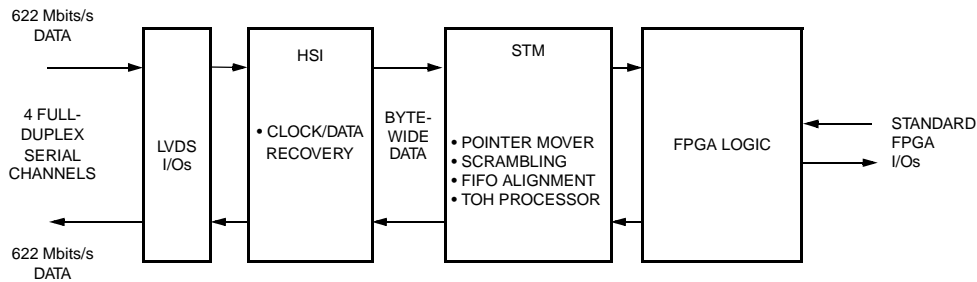
5-8113(F)

Figure 1. _ORCA_ ORT4622 Block Diagram

ORT4622 Overview (continued)
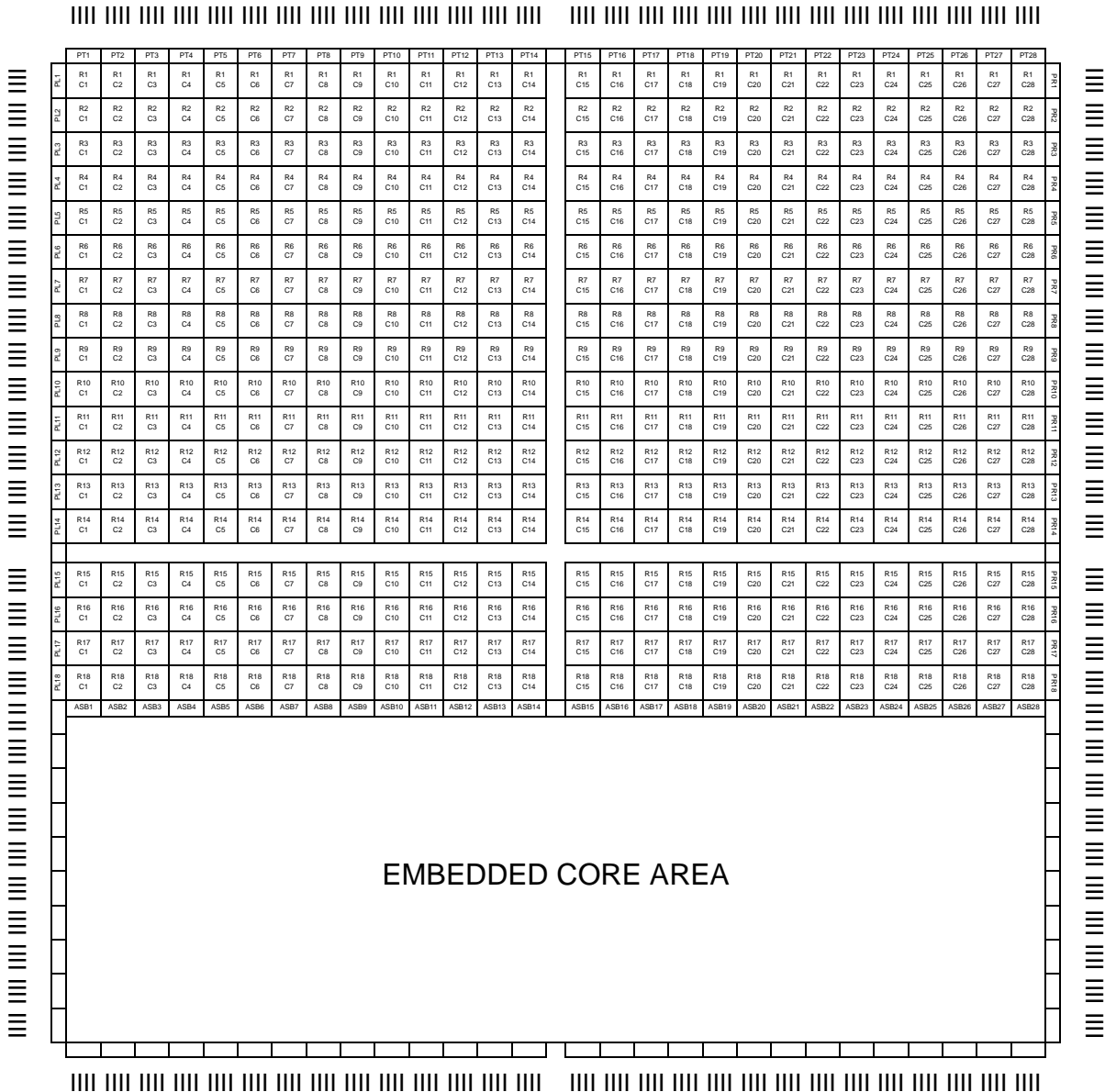
Figure 2. ORT4622 Array

ORT4622 Overview (continued)

HSI Interface

The high-speed interconnect (HSI) macrocell is used for clock/data recovery and MUX/deMUX between 77.76 MHz byte-wide internal data buses and 622 Mbits/s external serial links.

The HSI interface receives four 622 Mbits/s serial input data streams from the LVDS inputs and provides four independent 77.76 MHz byte-wide data streams and recovered clock to the STM macro. There is no requirement for bit alignment since SONET type framing will take place inside the ORT4622 core. For transmit, the HSI converts four byte-wide 77.76 MHz data streams to serial streams at 622 Mbits/s at the LVDS outputs.

STM Macrocell

The STM portion of the embedded core consists of transmitter (Tx) and receiver (Rx) sections. The STM receives four byte-wide data streams at 77.76 MHz and the associated clock from the HSI. The incoming streams are SONET framed and descrambled before they are written into a FIFO which absorbs phase and delay variations and allows the shift to the system clock. The TOH is then extracted and sent out on the four serial ports. The pointer interpreter will then put the synchronous transport signal (STS) synchronous payload envelopes (SPE) into a small elastic store from which the pointer generator will produce four byte-wide STS-12 streams of data that are aligned to the system timing pulse. Transmitted data for each channel is received through a parallel bus and a serial port from the FPGA circuit. TOH bytes are received from the serial input port and can be optionally inserted from programmable registers or serial inputs to the STS-12 frame via the TOH processor. Each of the four parallel input buses is synchronized to a free-running system clock. Then the SPE and TOH data is transferred to the HSI.

The STM macrocell also has a scrambler/descrambler disable feature, allowing the user to disable the scrambler of the transmitter and the descrambler of the receiver.

CPU Interface

The embedded core has a dedicated, asynchronous, MPC860 compatible, CPU interface that is used for device setup, control, and monitoring. Dual sets of I/O pins of this CPU interface with a bit stream configurable scheme provide designers a convenient and flexible option for configuration. One set of CPU I/O pins goes off chip allowing direct connection with an onboard CPU. Another set of CPU I/O pins are available to the FPGA logic allowing for a stand-alone system free of an external CPU interface.

The CPU interface is composed of an 8-bit data bus, a 7-bit address bus, a chip select signal, a read/write signal, and an interrupt signal.

FPGA Interface

The FPGA logic will receive/transmit frame aligned streams of 77.76 MHz data (maximum of four streams in each direction) from/to the backplane transceiver embedded core. All frames transmitted to the FPGA will be aligned to the FPGA frame pulse which will be provided by the FPGA user's logic to the STM macro. All frames received from the FPGA logic will be aligned to the system frame pulse that will be supplied to the STM macro from the FPGA user's logic.

FPSC Configuration

Configuration of the ORT4622 occurs in two stages, FPGA bit stream configuration and embedded core setup.

FPGA Configuration

The FPGA logic is configured by standard FPGA bit stream configuration means as discussed in the Series 3 FPGA data sheet. Additionally, for the ORT4622, the location of the CPU interface to the embedded core, either on the device pins or at the FPGA/embedded core boundary, is configured via FPGA configuration and is defined via the ORT4622 design kit.

Embedded Core Setup

The embedded core operation is set up via the embedded core CPU of the interface. All options for the operation of the core are configured according to the device register map presented in the detailed description section of this data sheet.

ORT4622 Overview (continued)
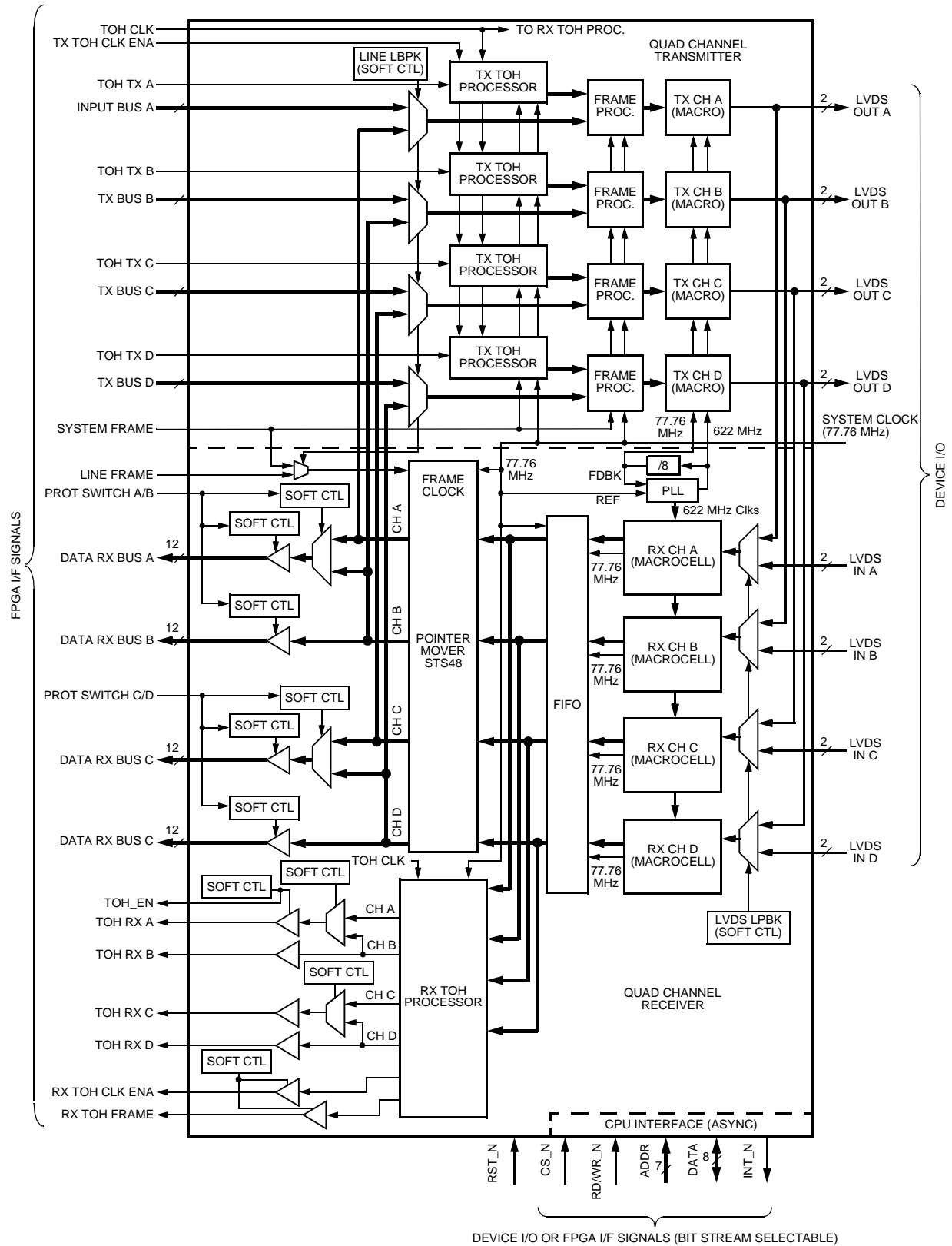
5-8576 (F)

Figure 3. Architecture of ORT4622 Backplane Transceiver

Backplane Transceiver Core Detailed Description

HSI Macro

The high-speed interface (HSI) provides a physical medium for high-speed asynchronous serial data transfer between the ORT4622 and other devices. The devices can be mounted on the same board or mounted on different boards and connected through the shelf backplane. The 622 Mbits/s CDR macro is a four-channel clock phase select (CPS) and data retime function with serial to parallel demultiplexing for the incoming data stream and parallel to serial multiplexing for outgoing data. The HSI macro consists of three functionally independent blocks: receiver, transmitter, and PLL synthesizer as shown in Figure 4.

The PLL synthesizer block receives a 77.76 MHz reference clock at its input, and provides a phase-locked 622.08 MHz clock to the transmitter block and phase control signal to the receiver block. The PLL synthesizer block is a common asset shared by four receive and transmit channels.

The HSI receiver receives four channels of differential 622.08 Mbits/s serial data without clock at its LVDS receive inputs. The received data must be scrambled, conforming to SONET STS-12 and SDH STM-4 data formats using either a PN7 or PN9 sequence. The PN7 characteristic polynomial is $1 + x^6 + x^7$ and PN9 characteristic polynomial is $1 + x^4 + x^9$. The clock phase select and data retime (CPS/DR) module performs a clock recovery and data retiming function by using phase control information. The resultant 622.08 Mbits/s data and clock are then passed to the deserializer module, which performs serial to parallel conversion and provides a 77.76 Mbits/s parallel data and clock at its output.

The HSI transmitter receives four channels of 77.76 Mbits/s parallel data that is synchronous to the reference clock at its inputs. The serializer performs a parallel to serial conversion using a 622.08 MHz clock provided by the PLL/synthesizer block. The 622 Mbits/s serial data streams are then transmitted through the LVDS drivers.

Backplane Transceiver Core Detailed Description (continued)
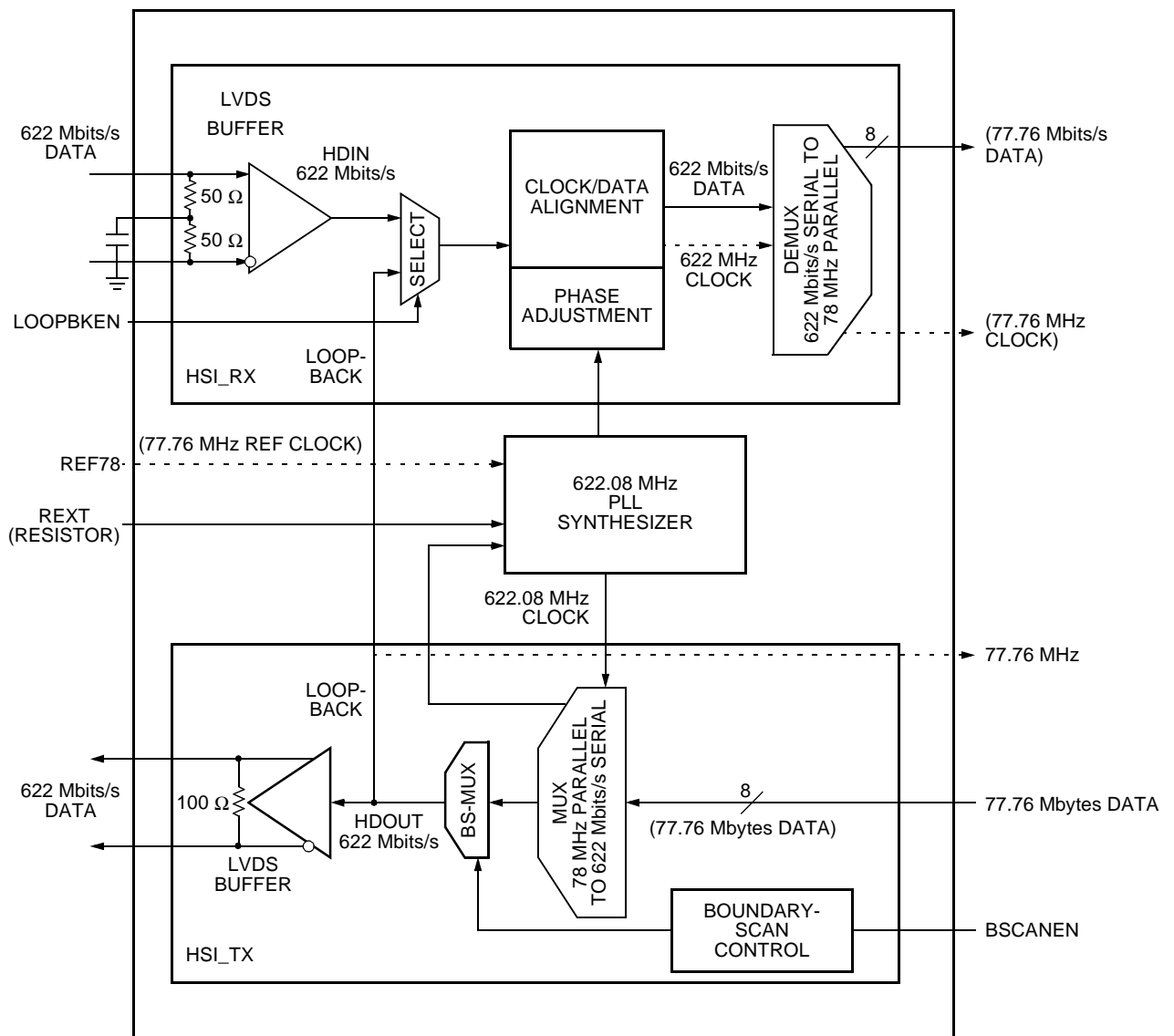
5-8592 (F)

Figure 4. HSI Functional Block Diagram

Backplane Transceiver Core Detailed Description (continued)

STM Transmitter (FPGA -> Backplane)

The STM has four STS-12 transmit channels which can be treated as a single STS-48 channel. In general, the transmitter circuit receives four byte-wide 77.76 MHz data from the FPGA which nominally represents four STS-12 streams (A, B, C, and D). This data is synchronized to the system (reference) clock and an 8 kHz system frame pulse from the FPGA logic. Transport overhead bytes are then optionally inserted into these streams and the streams are forwarded to the HSI. All byte timing pulses required to isolate individual overhead bytes (e.g., A1, A2, B1, D1—D3, etc.) are generated internally based on the system frame pulse (SYS_FP) received from the FPGA logic. All streams operate byte-wide at 77.76 MHz in all modes. The TOH processor operates from 25 MHz to 77.76 MHz and supports the following TOH signals: A1 and A2 insertion and optional corruption; H1, H2, and H3 pass transparently; BIP-8 parity calculation (after scrambling) and B1 byte insertion and optional corruption

(before scrambling); optional K1 and K2 insert; optional S1/M0 insert; optional E1/F1/E2 insert; optional section and line data communication channel (DCC, D1—D3) insertion (for intercard communications channel); scrambling of outgoing data stream with optional scrambler disabling; optional stream disabling.

When the ORT4622 is used in nonnetworking applications as a generic high-speed backplane data mover, the TOH serial ports are unused or can be used for slow-speed off-channel communication between devices. Data received on the parallel bus is optionally scrambled and transferred to LVDS outputs.

Byte Ordering Information

The core supports quad STS-12 mode of operation on the input/output ports. STS-48 is also supported when received in quad STS-12 format. When operating in quad STS-12 mode, each of the independent byte streams carries an entire STS-12 within it. Figure 5 reveals the byte ordering of the individual STS-12 streams and for STS-48 operation.

12	9	6	3	11	8	5	2	10	7	4	1	→ STS-12 #1
24	21	18	15	23	20	17	14	22	19	16	13	→ STS-12 #2
36	33	30	27	35	32	29	26	34	31	28	25	→ STS-12 #3
48	45	42	39	47	44	41	38	46	43	40	37	→ STS-12 #4

STS-48 IN QUAD STS-12 FORMAT

1, 12	1, 9	1, 6	1, 3	1, 11	1, 8	1, 5	1, 2	1, 10	1, 7	1, 4	1, 1	→ STS-12 #1
2, 12	2, 9	2, 6	2, 3	2, 11	2, 8	2, 5	2, 2	2, 10	2, 7	2, 4	2, 1	→ STS-12 #2
3, 12	3, 9	3, 6	3, 3	3, 11	3, 8	3, 5	3, 2	3, 10	3, 7	3, 4	3, 1	→ STS-12 #3
4, 12	4, 9	4, 6	4, 3	4, 11	4, 8	4, 5	4, 2	4, 10	4, 7	4, 4	4, 1	→ STS-12 #4

QUAD STS-12

5-8574 (F)

Figure 5. Byte Ordering of Input/Output Interface in STS-12 Mode

Backplane Transceiver Core Detailed Description (continued)

Transport Overhead Insertion (Serial Link)

The TOH serial links are used to insert TOH bytes into the transmit data. The transmit TOH data and TOH_CLK_EN get retimed by TOH_CLK in order to meet setup and hold specifications of the device.

The retimed TOH data is shifted into a 288-bit (32-bit by 9-bit) shift register and then multiplexed as an 8-bit bus to be inserted into the byte-wide data stream. Insertion or passthrough of TOH is under software control.

A1/A2 Frame Insert and Testing

All 12 A1 bytes of each STS-12 are set to 0xF6 and all 12 A2 bytes of the STS-12 are set to 0x28 when not overridden with a user-specified value for testing.

A1/A2 testing (corruption) is controlled per stream by the A1/A2 error insert register. When A1/A2 corruption detection is set for a particular stream, the A1/A2 values in the corrupted A1/A2 value registers are sent for the number of frames defined in the corrupted A1/A2 frame count register. When the corrupted A1/A2 frame count register is set to zero, A1/A2 corruption will continue until the A1/A2 error insert register is cleared.

On a per-device basis, the A1 and A2 byte values are set, as well as the number of frames of corruption. Then, to insert the specified A1/A2 values, each channel has an enable register. When the enable register is set, the A1/A2 values are corrupted for the number specified in the number of frames to corrupt. To insert errors again, the per-channel fault insert register must be cleared, and set again. Only the last A1 and the first A2 are corrupted.

B1 Calculation and Insertion

The B1 calculation block computes a BIP-8 code, using even parity over all bits of the previous STS-12 frame after scrambling and is inserted in the B1 byte of the current STS-12 frame before scrambling. Per-bit B1 corruption is controlled by the force BIP-8 corruption register (register address 0F). For any bit set in this register, the corresponding bit in the calculated BIP-8 is inverted before insertion into the B1 byte position. Each stream has an independent fault insert register that enables the inversion of the B1 bytes. B1 bytes in all other STS-1s in the stream are filled with zeros.

Stream Disable

When disabled via the appropriate bit in the stream enable register, the prescrambled data for a stream is set to all ones, feeding the HSI. The HSI macro is powered down on a per-stream basis, as are its LVDS outputs.

Scrambler

The data stream is scrambled using a frame synchronous scrambler of sequence length 127. The scrambling function can be disabled by software. The generating polynomial for the scrambler is $1 + x^6 + x^7$. This polynomial conforms to the standard SONET STS-12 data format. The scrambler is reset to 1111111 on the first byte of the SPE (byte following the Z0 byte in the twelfth STS-1). That byte and all subsequent bytes to be scrambled are exclusive ORed, with the output from the byte-wise scrambler. The scrambler runs continuously from that byte on throughout the remainder of the frame. A1, A2, J0, and Z0 bytes are not scrambled.

STM Receiver (Backplane -> FPGA)

The ORT4622 has four receiving channels that can be treated as one STS-48 stream, or treated as independent channels. Incoming data is received through LVDS serial ports at the data rate of 622 Mbits/s. The receiver can handle the data streams with frame offsets of up to ±12 bytes. The received data streams are processed in the HSI and the STM, then passed through the CIC boundary to the FPGA logic.

Backplane Transceiver Core Detailed Description (continued)

Framer Block

The framer block, in Figure 6, takes byte-wide data from the HSI, and outputs a byte-aligned, byte-wide data stream and 8 kHz sync pulse. The framer algorithm determines the out-of-frame/in-frame status of the incoming data and will cause interrupts on both an errored frame and an out-of-frame (OOF) state. The framer detects the A1/A2 framing pattern and generates the 8 kHz frame pulse. When the framer detects OOF, it will generate an interrupt. Also, the framer detects an errored frame and increments an A1/A2 frame error counter. The counter can be monitored by a processor to compile performance status on the quality of the backplane.

Because the ORT4622 is intended for use between another ORT4622 or other devices via a backplane, there is only one errored frame state. Thus after two transitions are missed, the state machine goes into the OOF state and there is no severely errored frame (SEF) or loss-of-frame (LOF) indication.
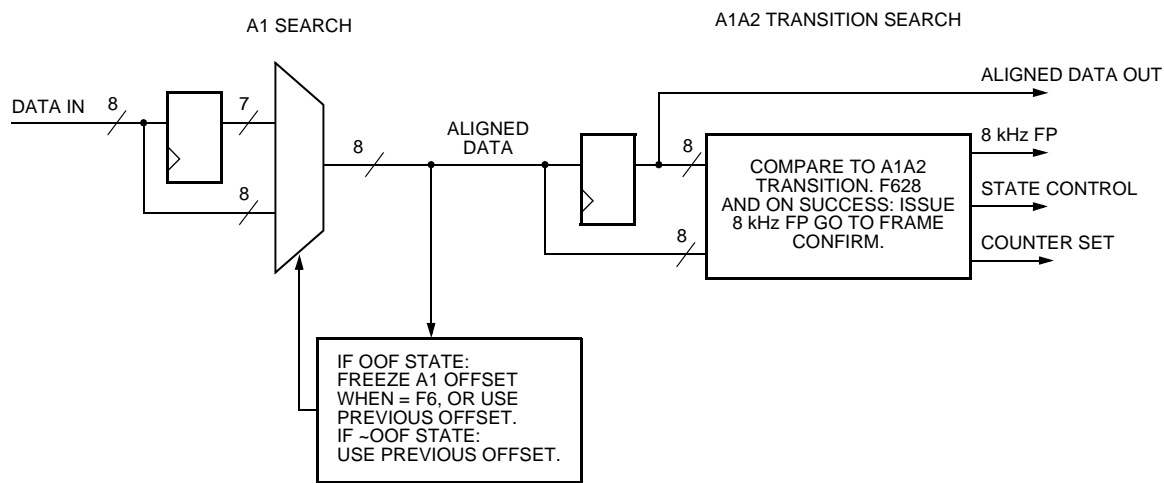
5-8582 (F)

Figure 6. Framer Circuit

B1 Calculate and Descramble (Backplane -> FPGA)

Each Rx block receives byte-wide scrambled 77.76 MHz data and a frame sync from the framer. Since each HSI is independently clocked, the Rx block operates on individual streams. Timing signals required to locate overhead bytes to be extracted are generated internally based on the frame sync. The Rx block produces byte-wide (optionally) descrambled data and an output frame sync for the alignment FIFO block.

The B1 calculation block computes a BIP-8 code, using even parity over all bits of the previous STS-12 frame before descrambling and this value is checked against the B1 byte of the current frame after descrambling. A per-stream B1 error counter is incremented for each bit that is in error. The error counter may be read via the CPU interface.

Descrambling. The streams are descrambled using a frame synchronous descrambler of sequence length 127 with a generating polynomial of $1 + x^6 + x^7$. The section trace byte (J0) and the growth bytes (Z0) are not descrambled. The descrambling function can be disabled by software.

AIS-L Insertion. If enabled in the AIS_L force register, AIS-L is inserted into the received frame by writing all ones for all bytes of the descrambled stream.

Lucent Technologies Inc.

Backplane Transceiver Core Detailed Description (continued)

AIS-L Insertion on Out-of-Frame. If enabled via the register AIS-L is inserted into the received frame by writing all ones for all bytes of the descrambled stream when the framer indicates that an out-of-frame condition exists.

Internal Parity Generation

Even parity is generated on all data bytes and is routed in parallel with the data to be checked before the protection switch MUX at the parallel output.

FIFO Alignment (Backplane -> FPGA)

The alignment FIFO allows the transfer of all data to the system clock. The FIFO sync block (Figure 7) allows the system to be configured to allow the frame alignment of multiple slightly varying data streams. This optional alignment ensures that matching STS-12 streams will arrive at the FPGA end in perfect data sync. The frame alignment is configurable to allow for the possibility of fully independent (i.e., total frame misalignment) STS-12s.
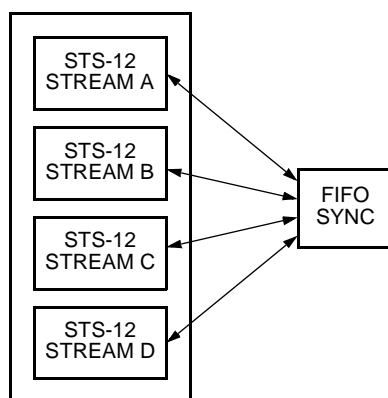
5-8577 (F)

Figure 7. Interconnect of Streams for FIFO Alignment

The incoming data from the clock and data recovery can be separated into four STS-12 channels (A, B, C, and D). These streams can be frame aligned in the patterns shown in Figure 8.
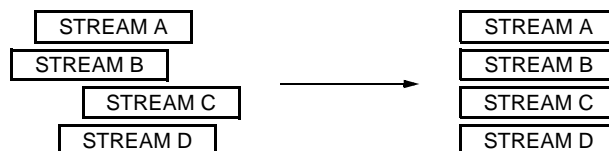
5-8575 (F)

Figure 8. Alignment of Four STS-12 Streams

There is also a provision to allow certain streams to be disabled (i.e., not producing interrupts or affecting synchronization). These streams can be enabled at a later time without disrupting other streams.

The FIFO block consists of a 24 by 10-bit FIFO per link. This FIFO is used to align up to ±154.3 ns of interlink skew and to transfer to the system clock. The FIFO sync circuit takes metastable hardened frame pulses from the write control blocks and produces sync signals which indicate when the read control blocks should begin reading from the first FIFO location. On top of the sync signals this block produces an error indicator which indicates that the signals to be aligned are too far apart for alignment (i.e., greater than 18 clocks apart). Sync and error signals are sent to read control block for alignment. The read control block is synched only once on start-up, any further synchronization is S/W controlled. The action of resynching a read control block will always cause a data hit. A S/W register allows the read control block to be resynched.

17

Lucent Technologies Inc.

Backplane Transceiver Core Detailed Description (continued)

Link Alignment. The general operation of the link alignment algorithm is to wait 12 clocks (i.e., half the FIFO) from the arriving frame pulse and then signal the read control block to begin reading. For perfectly aligned frame pulses across the links, it is simply a matter of counting down 12 and then signaling the read control block.

The algorithm down counts by one until all of the frame pulses have arrived and then by two when they are all present. For example (Figure 9), if all pulses arrive together then alignment algorithm would count 24 (12 clocks); if, however, the arriving pulses are spread out over four clocks, then it would count one for the first four pulses and then two per clock afterward which gives a total of 14 clocks between first frame pulse and the first read. This puts the center of arriving frame pulses at the halfway point in the buffer. This is the extent of the algorithm and it has no facility for actively correcting problems once they occur.

The write control block receives byte-wide data at 77.76 MHz and a frame pulse two clocks before the first A1 byte of the STS-12 frame. It generates the write address for the FIFO block. The first A1 in every STS-12 stream is written in the same location (address 0) in the FIFO. Also, a frame bit is passed through the FIFO along with the first byte before the first A1 of the STS-12. The read control block synchronizes the reading of the FIFO for streams that are to be aligned. Reading begins when the FIFO sync signals that all of the applicable A1s and the appropriate margin have been written to the FIFO. All of the read blocks to be synchronized begin reading at the same time and same location in memory (address 0).

The alignment algorithm takes the difference between read address and write address to indicate the relative clock alignments between STS-12 streams. If this depth indication exceeds certain limits (12 clocks), then an interrupt is given to the microprocessor (alignment overflow). Each STS-12 stream can be realigned by software if it gets too far out of line (this would cause a data hit).

PERFECTLY ALIGNED FRAMES   4-byte SPREAD IN ARRIVING FRAMES

5-8584 (F)
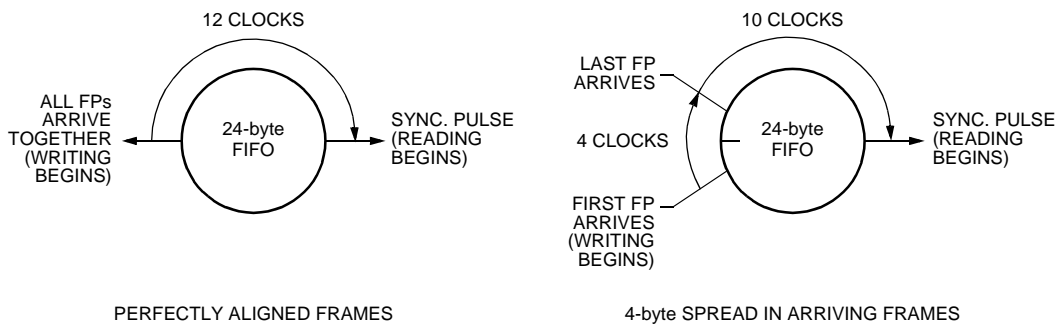
Figure 9. Examples of Link Alignment

Pointer Mover Block (Backplane -> FPGA)

The pointer mover maps incoming frames to the line framing that is supplied by the FPGA logic. The K1/K2 bytes and H1-SS bits are also passed through to the pointer generator so that the FPGA can receive them. The pointer mover handles both concatenations inside the STS-12, and to other STS-12s inside the core.

Backplane Transceiver Core Detailed Description (continued)

The pointer mover block can correctly process any length of concatenation of STS frames (multiple of three) as long as it begins on an STS-3 boundary (i.e., STS-1 number one, four, seven, 10, etc.) and is contained within the smaller of STS-3, 12, or 48. See details in Table 2.

Table 2. Valid Starting Positions for an STS-MC

STS-1 Number	STS-3cSPE	STS-6cSPE	STS-9cSPE	STS-12cSPE	STS-15cSPE	STS-18c to STS-48c SPEs
1	YES	YES	YES	YES	YES	YES
4	YES	YES	YES	NO	YES	—
7	YES	YES	NO	NO	YES	—
10	YES	NO	NO	NO	YES	—
13	YES	YES	YES	YES	YES	—
16	YES	YES	YES	NO	YES	—
19	YES	YES	NO	NO	YES	—
22	YES	NO	NO	NO	YES	—
25	YES	YES	YES	YES	YES	—
28	YES	YES	YES	NO	YES	—
31	YES	YES	NO	NO	YES	—
34	YES	NO	NO	NO	YES	NO
37	YES	YES	YES	YES	NO	NO
40	YES	YES	YES	NO	NO	NO
43	YES	YES	NO	NO	NO	NO
46	YES	NO	NO	NO	NO	NO

Note: YES = STS-Mc SPE can start in that STS-1.

    NO = STS-Mc SPE cannot start in that STS-1.

    — = YES or NO, depending on the particular value of M.

Pointer Interpreter State Machine. The pointer interpreter's highest priority is to maintain accurate dataflow (i.e., valid SPE only) into the elastic store. This will ensure that any errors in the pointer value will be corrected by a standard, fully SONET compliant, pointer interpreter without any data hits. This means that error checking for increment, decrement, and new data flag (NDF) (i.e., eight of 10) are maintained in order to ensure accurate dataflow. A single valid pointer (i.e., 0—782) that differs from the current pointer will be ignored. Two consecutive incoming valid pointers that differ from the current pointer will cause a reset of the J1 location to the latest pointer value (the generator will then produce an NDF). This block is designed to handle single bit errors without affecting dataflow or changing state.

The pointer interpreter has only three states (NORM, AIS, and CONC). NORM state will begin whenever two consecutive NORM pointers are received. If two consecutive NORM pointers are received that both differ from the current offset, then the current offset will be reset to the last received NORM pointer. When the pointer interpreter changes its offset it causes the pointer generator to receive a J1 value in a new position. When the pointer generator gets an unexpected J1 it resets its offset value to the new location and declares an NDF. The interpreter is only looking for two consecutive pointers that are different from the current value. These two consecutive NORM pointers do not have to have the same value. For example, if the current pointer is ten and a NORM pointer with offset of 15 and a second NORM pointer with offset of 25 are received, then the interpreter will change the current pointer to 25. The receipt of two consecutive CONC pointers causes CONC state to be entered. Once in this state offset values from the head of the concatenation chain are used to determine the location of the STS SPE for each STS in the chain. Two consecutive AIS pointers cause the AIS state to occur. Any two consecutive normal or concatenation pointers will end this AIS state. This state will cause the data leaving the pointer generator to be overwritten with 0xFF.

Backplane Transceiver Core Detailed Description (continued)
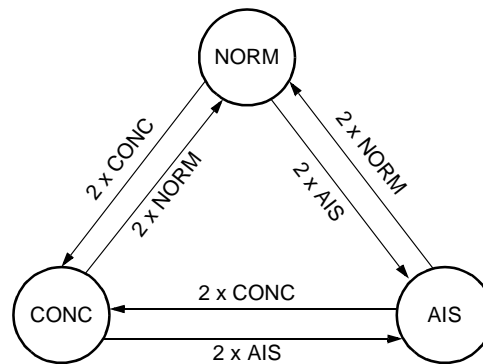
5-8589 (F)

Figure 10. Pointer Mover State Machine

Pointer Generator. The pointer generator maps the corresponding bytes into their appropriate location in the outgoing byte stream. The generator also creates offset pointers based on the location of the J1 byte as indicated by the pointer interpreter. The generator will signal NDFs when the interpreter signals that it is coming out of AIS state. The pointer generator resets the pointer value and generates NDF every time a byte marked J1 is read from the elastic store that doesn't match the previous offset.

Increment and decrement signals from the pointer interpreter are latched once per frame on either the F1 or E2 byte times (depending on collisions), this ensures constant values during the H1 through H3 times. The choice of on which byte time to do the latching is made once when the relative frame phases (i.e., received and system) are determined. This latch point is then stable unless the relative framing changes and the received H byte times collide with the system F1 or E2 times in which case the latch point would be switched to the collision free byte time.

There is no restriction on how many or how often increments and decrements are processed. Any received increment or decrement is immediately passed to the generator for implementation regardless of when the last pointer adjustment was made. The responsibility for meeting the SONET criteria for max frequency of pointer adjustments is left to an upstream pointer processor.

When the interpreter signals an AIS state, the generator will immediately begin sending out 0xFF in place of data and H1, H2, H3. This will continue until the interpreter returns to NORM or CONC (pointer mover state machine) states and a J1 byte is received.

Transport Overhead Extraction

Transport overhead is extracted from the receive data stream by the TOH extract block. The incoming data gets loaded into a 36-byte shift register on the system clock domain. This in turn is clocked onto the TOH clock domain at the start of the SPE time, where it can be clocked out.

During the SPE time, the receiver TOH frame pulse is generated, RX_TOH_FP, which indicates the start of the row of 36 TOH bytes. This pulse, along with the receive TOH clock enable, RX_TOH_CK_EN, as well as the TOH data, are all launched on the rising edge of the TOH clock TOH_CLK.

Special TOH Byte Functions

K1 and K2 Handling. K1 and K2 bytes can be optionally passed through the pointer mover under software control, or can set to zero with the other TOH bytes.

A1 and A2 Handling. A1 and A2 bytes are always regenerated and set to hexadecimal F6 and 28, respectively.

Backplane Transceiver Core Detailed Description (continued)

SPE and C1J1 Outputs. These two signals for each channel are passed to the FPGA logic to allow a pointer processor or other function to extract payload without interpreting the pointers. For the ORT4622, each frame has 12 STS-1s. In the SPE region, there are 12 J1 pulses for each STS-1s. There is one C1(J0) pulse in the TOH area for one frame since all 12 STS-1s share the same row of TOH. Thus, there is a total of 12 J1 pulses and one C1(J0) pulse per frame. C1(J0) pulse is coincident with the J0 of STS1 #1. In each frame, the SPE flag is active when the data stream is in SPE area. SPE behavior is dependent on pointer movement and concatenation. Note that in the TOH area, H3 can also carry valid data. When valid SPE data is carried in this H3 slot, SPE is high in this particular TOH time slot. In the SPE region, if there is no valid data during any SPE column, the SPE signal will be set to low. SPE allow a pointer processor to extract payload without interpreting the pointers. The SPE and C1J1 functionality are described in Table 3.

Table 3. SPE and C1J1 Functionality

SPE	C1J1	Description
0	0	TOH information excluding C1(J0) of STS1 #1
0	1	Position of C1(J0) of STS1 #1
1	0	SPE information excluding the 12 J1 bytes
1	1	Position of the 12 J1 bytes

Note: The following rules must be observed for generating SPE and C1J1 signals: on occurrence of AIS-P on any of the STS-1, there must be no corresponding J1 pulse. In case of concatenated payloads (up to STS48c), only the head STS-1 of the group must have an associated J1 pulse. C1J1 signal must track any pointer movements. During a negative justification event, SPE must be set high during the H3 byte to indicate that payload data is available. During a positive justification event, SPE must be set low during the positive stuff opportunity byte to indicate that payload data is not available.

Powerdown Mode

Powerdown mode will be entered when the corresponding channel is disabled. Channels can be independently enabled or disabled under software control.

Parallel data bus output enable and TOH serial data output enable signals are made available to the FPGA logic. The outputs can be 3-stated when the corresponding channel is disabled. The HSI macrocell's corresponding channel is also powered down. The device will power up with all four channels in powerdown mode.

In addition, an LVDS_EN pin has been added to control the LVDS pins during boundary scan. During functional operation, enabling/disabling LVDS buffers is controlled by software registers. When in boundary scan mode, LVDS_EN controls the enabling/disabling of LVDS buffers instead of software registers. This LVDS_EN pin should be pulled high on the board for functional operation, and pulled low during boundary scan.

Redundancy and Protection Switching

The ORT4622 supports STS-12/STS-48 redundancy by either software or hardware control for protection switching applications. For the transmitter mode, no additional functionality is required for redundant operation. For receiving data, STS-12 data redundancy can be implemented within the same device; while STS-48 data stream requires multiple devices to support redundancy.

In STS-12 mode, the channel A receive data bus port is used for both channel A and channel B. Similarly, the channel C receive data bus port is used for both channel C and channel D. Channel B and channel D become the redundant channels. The channel B and channel D receive data bus ports are unused. Soft registers provide independent control to the protection switching MUXes for both parallel data ports and serial TOH data ports. When direct hardware control for protection switching is needed, external protection switch pins are available for channels A and B, and also channels C and D. The hardware redundancy only supports parallel SPE/TOH data protection switching, but not the serial TOH data.

In STS-48 mode, both parallel and serial port output pins on the FPGA side should be 3-stated if two or more devices are tied to the appropriate data bus. The existing local bus enable signals at the CIC can be used as 3-state controls if needed, which can be easily accessed by software control. Users can also create their own protection switch 3-state enable signals either in FPGA logic or, external to the device, depending on the specific application.

Lucent Technologies Inc.

Memory Map

Definition of Register Types

There are six structural register elements: sreg, creg, preg, iareg, isreg, and iereg. There are no mixed registers in the chip. This means that all bits of a particular register (particular address) are structurally the same.

Table 4. Structural Register Elements

Element	Register	Description
sreg	Status Register	A status register is read only, and, as the name implies, is used to convey the status information of a particular element or function of the ORT4622 core. The reset value of an sreg is really the reset value of the particular element or function that is being read. In some cases, an sreg is really a fixed value. An example of which is the fixed ID and revision registers.
creg	Control Register	A control register is read and writable memory element inside core control. The value of a creg will always be the value written to it. Events inside the ORT4622 core cannot effect creg value. The only exception is a soft reset, in which case the creg will return to its default value. The control register have default values as defined in the default value column of Table 5, memory map.
preg	Pulse Register	Each element, or bit, of a pulse register is a control or event signal that is asserted and then deasserted when a value of one is written to it. This means that each bit is always of value 0 until it is written to, upon which it is pulsed to the value of one and then returned to a value of 0. A pulse register will always have a read value of 0.
iareg	Interrupt Alarm Register	Each bit of an interrupt alarm register is an event latch. When a particular event is produced in the ORT4622 core, its occurrence is latched by its associated iareg bit. To clear a particular iareg bit, a value of one must be written to it. In the ORT4622 core, all iareg reset values are 0.
isreg	Interrupt Status Register	Each bit of an interrupt status register is physically the logical OR function. It is a consolidation of lower level interrupt alarms and/or isreg bits from other registers. A direct result of the fact that each bit of the isreg is a logical OR function means that it will have a read value of one if any of the consolidation signals are of value one, and will be of value 0 if and only if all consolidation signals are of value 0. In the ORT4622 core, all iareg default values are 0.
ereg	Interrupt Enable Register	Each bit of a status register or alarm register has an associated enable bit. If this bit is set to value one, then the event is allowed to propagate to the next higher level of consolidation. If this bit is set to zero, then the associated iareg or isreg bit can still be asserted but an alarm will not propagate to the next higher level. An interrupt enable bit is an interrupt mask bit when it is set to value 0.

Registers Access and General Description

The memory map comprises three address blocks:

- Generic register block: ID, revision, scratch pad, lock, FIFO alignment, and reset registers.
- Device register block: control and status bits, common to the four channels.
- Channel register blocks: each of the four channels have an address block. The four address blocks have the exact same structure with a constant address offset between channel register blocks.

All registers are write-protected by the lock register, except for the scratch pad register. The lock register is a 16-bit read/write register. Write access is given to registers only when the key value 0xA001 is present in the lock register. An error flag will be set upon detecting a write access when write permission is denied. The default value is 0x0000.

After powerup reset or soft reset, unused register bits will be read as zeros. Unused address locations are also read as zeros. Write only register bits will be read as zeros. The detailed information on register access and function are described on the tables, memory map, and memory map bit description.

Lucent Technologies Inc.

Memory Map (continued)

Memory Map Overview

Table 5. Memory Map

ADDR [6:0]	Reg. Type	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Default Value (hex)	Notes
Generic Register Block											
00	sreg	fixed ID MSB [7:0]								A0	1
01	sreg	fixed ID LSB [7:0]								01	
02	sreg	fixed rev [7:0]								01	
03	creg	scratch pad [7:0]								00	
04	creg	lockreg MSB [7:0]								00	
05	creg	lockreg LSB [7:0]								00	
06	preg	—	—	—	—	—	—	FIFO alignment command	global reset command	NA	
Device Register Block											
08	creg	—	—	—	Rx TOH frame and Rx TOH clock enable hi-z control	ext prot sw en	ext prot sw function	STS-48 STS-12 sel	LVDS lpbk control	00	2
09	creg	—	—	—	—	parallel port output MUX select for ch C	parallel port output MUX select for ch A	serial port output MUX select for ch C	serial port output MUX select for ch A	0F	
0a	creg	—	—	—	FIFO aligner threshold value (min) [4:0]					02	
0b	creg	—	—	—	FIFO aligner threshold value (max) [4:0]					15	
0c	creg	—	scrambler/ descrambler control	input/ output parallel bus parity control	line lpbk control	number of consecutive A1/A2 errors to generate [3:0]				60	3
0d	creg	A1 error insert value [7:0]								00	
0e	creg	A2 error insert value [7:0]								00	
0f	creg	transmitter B1 error insert mask [7:0]								00	

Notes:
1. Generic register block.

2. Device register block-Rx.

3. Device register block-Tx.

Memory Map (continued)

Table 5. Memory Map (continued)

ADDR [6:0]	Reg. Type	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Default Value (hex)	Notes
Device Register Block (continued)											
10	isreg	—	—	—	per device int	ch D interrupt	ch C interrupt	ch B interrupt	ch A interrupt	00	4
11	iereg	—	—	—	enable/mask register [4:0]					00	
12	iareg	—	—	—	—	—	—	write to locked register error flag	frame offset error flag	00	
13	iereg	—	—	—	—	—	—	enable/mask register [1:0]		00	
Channel Register Block											
20, 38, 50, 68 *	creg	hi-z control of TOH data output	hi-z control of parallel output bus	channel enable/ disable control	parallel output bus parity err ins cmd	Rx K1/K2 source select	TOH serial output port par err ins cmd	force ais-l control	Rx behavior in LOF	01	5
21, 39, 51, 69	creg	Tx mode of opera- tion	Tx E1 F1 E2 source select	Tx S1 M0 source select	Tx K1/K2 source select	Tx D12 source select	Tx D11 source select	Tx D10 source select	Tx D9 source select	00	6
22, 3a, 52, 6a	creg	Tx D8 source select	Tx D7 source select	Tx D6 source select	Tx D5 source select	Tx D4 source select	Tx D3 source select	Tx D2 source select	Tx D1 source select	00	
23, 3b, 53, 6b	creg	—	—	—	—	—	—	B1 error insert command	A1/A2 error ins command	00	
24, 3c, 54, 6c	sreg	—	—	—	—	Concat indication 12	Concat indication 9	Concat indication 6	Concat indication 3	NA	7
25, 3d, 55, 6d	sreg	Concat indication 11	Concat indication 8	Concat indication 5	Concat indication 2	Concat indication 10	Concat indication 7	Concat indication 4	Concat indication 1	NA	

Notes:

1. Generic register block.

2. Device register block-Rx.

3. Device register block-Tx.

4. Top level interrupts.

5. Rx control.

6. Tx control signals.

7. Per STS#1 cos flag.

* ADDR values delimited by a comma indicate the address for each of 4 channels, from channel A to D. For example, the register to Tx control sig-nals has addresses of 20, 38, 50, and 68. This indicates that channel A Tx control signals are at address 20, channel B Tx control signals are at address 38, channel C Tx control signals are at address 50, and channel D Tx control signals are at address 68.

Memory Map (continued)

Table 5. Memory Map (continued)

ADDR [6:0]	Reg. Type	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Default Value (hex)	Notes
Channel Register Block (continued)											
26, 3e, 56, 6e	isreg	—	—	—	—	—	elastic store overflow flag	ais-p flag	per STS-12 alarm flag	00	8
27, 3f, 57, 6f	iereg	—	—	—	—	—	enable/mask register [2:0]			00	
28, 40, 58, 70	iareg	—	—	TOH serial input port parity error flag	input parallel bus parity error flag	LVDS link B1 parity error flag	LOF flag	Receiver internal path parity error flag	FIFO aligner threshold error flag	00	9
29, 41, 59, 71	iereg	—	—	enable/mask register [5:0]						00	
2a, 42, 5a, 72	iareg	—	—	—	—	AIS interrupt flags 12	AIS interrupt flag 9	AIS interrupt flag 6	AIS interrupt flags 3	00	10
2b, 43, 5b, 73	iareg	AIS interrupt flag 11	AIS interrupt flag 8	AIS interrupt flag 5	AIS interrupt flag 2	AIS interrupt flag 10	AIS interrupt flag 7	AIS interrupt flag 4	AIS interrupt flag 1	00	
2c, 44, 5c, 74	iereg	—	—	—	—	enable/ mask AIS interrupt flag 12	enable/ mask AIS interrupt flag 9	enable/ mask AIS interrupt flag 6	enable/ mask AIS interrupt flag 3	00	
2d, 45, 5d, 75	iereg	enable/ mask AIS interrupt flag 11	enable/ mask AIS interrupt flag 8	enable/ mask AIS interrupt flag 5	enable/ mask AIS interrupt flag 2	enable/ mask AIS interrupt flag 10	enable/ mask AIS interrupt flag 7	enable/ mask AIS interrupt flag 4	enable/ mask AIS interrupt flag 1	00	
2e, 46, 5e, 76	iareg	—	—	—	—	ES overflow flag 12	ES overflow flag 9	ES overflow flag 6	ES overflow flag 3	00	

Notes:

1. Generic register block.

2. Device register block-Rx.

3. Device register block-Tx.

4. Top level interrupts.

5. Rx control.

6. Tx control signals.

7. Per STS#1 cos flag.

8. Per channel interrupt.

9. Per STS–12 interrupt flags.

10. Per STS–1 interrupt flags.

Memory Map (continued)

Table 5. Memory Map (continued)

ADDR [6:0]	Reg. Type	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Default Value (hex)	Notes
Channel Register Block (continued)											
2f, 47, 5f, 77	iareg	ES overflow flag 11	ES overflow flag 8	ES overflow flag 5	ES overflow flag 2	ES overflow flag 10	ES overflow flag 7	ES overflow flag 4	ES overflow flag 1	00	10
30, 48, 60, 78	iereg	—	—	—	—	enable/ mask ES overflow flags 12	enable/ mask ES overflow flag 9	enable/ mask ES overflow flags 6	enable/ mask ES overflow flags 3	00	
31, 49, 61, 79	iereg	enable/ mask ES overflow flag 11	enable/ mask ES overflow flag 8	enable/ mask ES overflow flag 5	enable/ mask ES overflow flag 2	enable/ mask ES overflow flag 10	enable/ mask ES overflow flag 7	enable/ mask ES overflow flag 4	enable/ mask ES overflow flag 1	00	
32, 4a, 62, 7a	counter	overflow	LVDS link B1 parity error counter							00	11
33, 4b, 63, 7b	counter	overflow	LOF counter							00	
34, 4c, 64, 7c	counter	overflow	A1/A2 frame error counter							00	

Notes:

1. Generic register block.

2. Device register block-Rx.

3. Device register block-Tx.

4. Top level interrupts.

5. Rx control.

6. Tx control signals.

7. Per STS#1 cos flag.

8. Per channel interrupt.

9. Per STS–12 interrupt flags.

10. Per STS–1 interrupt flags.

11. Binning.

Memory Map (continued)

Memory Map Bit Descriptions

Table 6. Memory Map Bit Descriptions

Bit/Register Name(s)	Bit/Register Location (hex)	Register Type	Default Value (hex)	Description		
Generic Register Block						
fixed ID MSB [7:0] fixed ID LSB [7:0] fixed rev [7:0]	00 [7:0] 01 [7:0] 02 [7:0]	sreg	A0 01 01	—		
scratch pad [7:0]	03 [7:0]	creg	00	The scratch pad has no function and is not used anywhere in the ORT4622 core. However, this register can be written to and read from.		
lockreg MSB [7:0] lockreg LSB [7:0]	04 [7:0] 05 [7:0]	creg	00 00	In order to write to registers in memory locations 06 to 7F, lockreg MSB and lockreg LSB must be respectively set to the values of A0 and 01. If the MSB and LSB lockreg values are not set to {A0, 01}, then any values written to the registers in memory locations 06 to 7F will be ignored. After reset (both hard and soft) the ORT4622 core is in a write locked mode. The ORT4622 core needs to be unlocked before it can be written to. Also note that the scratch pad register (03) can always be written to as it is unaffected by write lock mode.		
FIFO alignment command global reset command	06 [0] 06 [1]	preg	NA	The FIFO alignment and global reset commands are both accessed via the pulse register in memory address 06. The FIFO alignment command is used to frame align the outputs of the four receive stm stream FIFOs. The global reset command is a soft (software initiated) reset. Nevertheless, the global reset command will have the exact reset effect as a hard (RST_N pin) reset.		
Device Register Block						
LVDS lpbk control	08 [0]	creg	0	0	No loopback.	
				1	LVDS loopback, transmit to receive on.	
STS48 STS12 sel	08 [1]	creg	0	This control signal is untracked in the ORT4622 core. It is a scratch bit, and it's value has no effect on the ORT4622 core.		
ext prot sw en ext prot sw func	08 [3:2]	creg	0	ext prot sw en	ext prot sw func	Switching Control Master.
				0	—	MUX is controlled by software (one control bit per MUX). Output buffers are controlled by software (one control bit per channel).
				1	0	MUX on parallel output bus of channel A is controlled by Prot_Switch A/B pin (0-> channel A, 1-> channel B). MUX on parallel output bus of channel C is controlled by Prot_Switch C/D pin (0 -> channel C, 1-> channel D). Output buffers are controlled by software (one control bit per channel).
				1	1	MUX is controlled by software (one control bit per MUX). Output buffers on parallel output bus of channels A and B are controlled by Prot_Switch A/B pin (0-> buffers active, 1-> hi-z). Output buffers on parallel output bus of channels C and D are controlled by Prot_Switch C/D pin (0 -> buffers active, 1-> hi-z).

Lucent Technologies Inc.

Memory Map (continued)

Table 6. Memory Map Bit Descriptions (continued)

Bit/Register Name(s)	Bit/ Register Location (hex)	Register Type	Default Value (hex)	Description	
Device Register Block (continued)					
Rx TOH frame and Rx TOH clock enable hi-z control	08 [4]	creg	0	0	hi-z.
				1	Enable receive TOH CLK and FP outputs.
serial port output MUX select for channel A serial port output MUX select for channel C parallel port output MUX select for channel A parallel port output MUX select for channel C	09 [0] 09 [1] 09 [2] 09 [3]	creg	1 1 1 1	**Serial Port Output MUX Select for Channel 1**	
				0	TOH output one is multiplexed to channel B.
				1	TOH output one is multiplexed to channel A.
				Serial Port Output MUX Select for Channel 3	
				0	TOH output three is multiplexed to channel D.
				1	TOH output three is multiplexed to channel C.
				Parallel Port Output MUX Select for Channel 1	
				0	Parallel output data bus one is multiplexed to channel B.
				1	Parallel output data bus one is multiplexed to channel A.
				Parallel Port Output MUX Select for Channel 3	
				0	Parallel output data bus three is multiplexed to channel D.
				1	Parallel output data bus three is multiplexed to channel C.
FIFO aligner threshold value (min) [4:0] FIFO aligner threshold value (max) [4:0]	0A [4:0] 0B [4:0]	creg	02 15	These are the minimum and maximum thresholds values for the per channel receive direction alignment FIFOs. If and when the minimum or maximum threshold value is violated by a particular channel, then the interrupt event FIFO aligner threshold error will be generated for that channel and latched as a FIFO aligner threshold error flag in the respective per STS-12 interrupt alarm register. The allowable range for minimum threshold values is 0 to 23. The allowable range for maximum threshold values is 0 to 22. Note that the minimal and maximum FIFO aligner threshold values apply to all four channels.	
number of consecutive A1/A2 errors to generate [3:0] A1 error insert value [7:0] A2 error insert value [7:0]	0C [7:0] 0D [7:0] 0E [7:0]	creg	00 00 00	These three per device control signals are used in conjunction with the per channel A1/A2 error insert command control bits to force A1/A2 errors in the transmit direction. If a particular channel's A1/A2 error insert command control bit is set to the value one then the A1 and A2 error insert values will be inserted into that channels respective A1 and A2 bytes. The number of consecutive frames to be corrupted is determined by the number of consecutive A1, A2 errors to generate[3:0] control bits. The error insertion is based on a rising edge detector. As such, the control must be set to value 0 before trying to initiate a second A1/A2 corruption.	
line lpbk control	0C [4]	creg	0	0	No loopback.
				1	Receive to transmit loopback on FPGA side.
input/output parallel bus parity control	0C [5]	creg	0	0	Even parity.
				1	Odd parity.

Memory Map (continued)

Table 6. Memory Map Bit Descriptions (continued)

Bit/Register Name(s)	Bit/Register Location (hex)	Register Type	Default Value (hex)	Description	
Device Register Block (continued)					
scrambler/ descrambler control	0C [6]	creg	1	0	No receive direction descramble/transmit direction scramble.
				1	In receive direction descramble channel after SONET frame recovery. In transmit direction scramble data just before parallel to serial conversion.
transmit B1 error insert mask [7:0]	0F [7:0]	creg	00	0	No error insertion.
				1	Invert corresponding bit in B1 byte.
channel A int channel B int channel C int channel D int per device int enable/mask register [4:0]	10 [0] 10 [1] 10 [2] 10 [3] 10 [4] 11 [4:0]	creg creg creg creg creg iereg	0 0 0 0 0 0	**Consolidation Interrupts**	
				0	No interrupt.
				1	Interrupt.
frame offset error flag write to locked register error flag enable/mask register [1:0]	12 [0] 12 [1] 13 [1:0]	iareg iareg iereg	0 0 0	If in the receive direction the phase offset between any two channels exceeds 17 bytes, then a frame offset error event will be issued. This condition is continuously monitored. If the ORT4622 core memory map has not been unlocked (by writing A1 00 to the lock registers), and any address other than the lockreg registers or scratch pad register is written to, then a write to locked register event will be generated.	
Channel Register Block					
Rx behavior in LOF force AIS-L control	20 38 50 68 [0] 20 38 50 68 [1]	—	1 0	**Receive Behavior in Log**	
				0	When receive direction OOF occurs, do not insert AIS-L.
				1	When receive direction OOF occurs, insert AIS-L.
				Force AIS-1 Control	
				0	Do not force AIS-L.
				1	Force AIS-L.
TOH serial output port par err ins cmd	20 38 50 68 [2]	—	0	0	Do not insert a parity error.
				1	Insert parity error in parity bit of receive TOH serial output for as long as this bit is set.
Rx K1/K2 source select	20 38 50 68 [3]	—	0	0	Set receive direction K1/K2 bytes to 0.
				1	Pass receive direction K1/K2 though pointer mover.
parallel output bus parity err ins cmd	20 38 50 68 [4]	—	0	0	Do not insert parity error.
				1	Insert parity error in the parity bit of receive direction parallel output bus for as long as this bit is set.

Memory Map (continued)

Table 6. Memory Map Bit Descriptions (continued)

Bit/Register Name(s)	Bit/ Register Location (hex)	Register Type	Default Value (hex)	Description	
Channel Register Block (continued)					
channel enable/ disable control hi-z control of parallel output bus hi-z control of TOH data output	20, 38, 50, 68 [5] 20, 38, 50, 68 [6] 20, 38, 50, 68 [7]	creg creg creg	0 0 0	**Channel Enable/Disable Control**	
				0	Powerdown channel and 3-state output buses.
				1	Functional mode.
				hi-z Control of Parallel Output Bus	
				0	3-state output bus.
				1	Functional mode.
				hi-z Control of TOH Data Output	
				0	3-state output lines.
				1	Functional mode.
Tx mode of operation Tx E1 F2 E2 source select Tx S1 M0 source select Tx K1 K2 source select Tx D12—D9 source select Tx D8—D1 source select	21, 39, 51, 69 [7] 21, 39, 51, 69 [6] 21, 39, 51, 69 [5] 21, 39, 51, 69 [4] 21, 39, 51, 69 [3:0] 22, 40, 52, 70 [7:0]	creg creg creg creg creg creg	0 0 0 0 4'h0 8'h00	**Transmit Mode of Operation**	
				0	Insert TOH from serial ports.
				1	Pass through all TOH.
				Other Registers	
				0	Insert TOH from serial ports.
				1	Pass through that particular TOH byte.
A1/A2 error insert command B1 error insert command	23, 3b, 53, 6b [0] 23, 3b, 53, 6b [1]	creg creg	0 0	0	Do not insert error[*].
				1	Insert error for number of frames in register hex 0C[*].
				0	Do not insert error[†].
				1	Insert error for one frame in B1 bits defined by register hex 0F[†].
concat indication 12, 9, 6, 3 concat indication 11, 8, 5, 2, 10, 7, 4, 1	24, 3c, 54, 6c [3:0] 25, 3d, 55, 6d [7:0]	sreg sreg	0 0	The value one in any bit location indicates that STS# is in CONCAT mode. A 0 indicates that the STS in not in CONCAT mode, or is the head of a concat group.	
per STS–12 alarm flag AIS-P flag elastic store overflow flag enable/mask register [2:0]	26, 3e, 56, 6e [0] 26, 3e, 56, 6e [1] 26, 3e, 56, 6e [2] 27, 3f, 57, 6f [3]	isreg isreg isreg iereg	0 0 0 3'b000	These flag register bits per STS-12 alarm flag, AIS-P flag, and elastic store overflow flag are the per-channel interrupt status (consolidation) register.	

* The error insertion is based on a rising edge detector. As such, the control must be set to value 0 before trying to initiate a second A1/A2 corruption.
† The error insertion is based on a rising edge detector. As such, the control must be set to value 0 before trying to initiate a second B1 corruption.

Memory Map (continued)

Table 6. Memory Map Bit Descriptions (continued)

Bit/Register Name(s)	Bit/Register Location (hex)	Register Type	Default Value (hex)	Description
Channel Register Block (continued)				
FIFO aligner threshold error flag receiver internal path parity error flag LOF flag LVDS link B1 parity error flag input parallel bus parity error flag TOH serial input port parity error flag enable/mask register [5:0]	28, 40, 58, 70 [0] 28, 40, 58, 70 [1] 28, 40, 58, 70 [2] 28, 40, 58, 70 [3] 28, 40, 58, 70 [4] 28, 40, 58, 70 [5] 28, 40, 58, 70 [6]	iareg iareg iareg iareg iareg iareg iareg	0 0 0 0 0 0 6'h00	These are per the STS-12 alarm flags.
AIS interrupt flags 12, 9, 6, 3 AIS interrupt flags 11, 8, 5, 2, 10, 7, 4, 1 enable/mask register 12, 9, 6, 3 enable/mask register 11, 8, 5, 2, 10, 7, 4, 1	29, 41, 59, 71[3:0] 2a, 42, 5a, 72 [7:0] 2b, 43, 5b, 73[3:0] 2c, 44, 5c, 74 [7:0]	iareg iareg iereg iereg	4'h0 8'h00 4'h0 8'h00	These are the AIS-P alarm flags.
ES overflow flags 12, 9, 6, 3 ES overflow flags 11, 8, 5, 2, 10, 7, 4, 1 enable/mask register 12, 9, 6, 3 enable/mask register 11, 8, 5, 2, 10, 7, 4, 1	2d, 45, 5d, 75 [3:0] 2e, 46, 5e, 76 [7:0] 2f, 47, 5f, 77 [3:0] 30, 48, 60, 78 [7:0]	—	4'h0 8'h00 4'h0 8'h00	These are the elastic store overflow alarm flags.
LVDS link B1 parity error counter	31, 49, 61, 79 [7:0]	counter	8'h00	7-bit count + overflow-reset on read.
LOF counter	32, 4a, 62, 7a [7:0]	counter	8'h00	7-bit count + overflow-reset on read.
A1/A2 frame error counter	33, 4b, 63, 7b [7:0]	counter	8'h00	7-bit count + overflow-reset on read.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The *ORCA* Series 3+ FPSCs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Table 7. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{stg}	Storage Temperature	65	150	°C
V_{DD}	Supply Voltage with Respect to Ground	0.5	7.0	V
—	Input Signal with Respect to Ground	0.5	V_{DD} + 0.3	V
—	Signal Applied to High-impedance Output	0.5	V_{DD} + 0.3	V
—	Maximum Package Body Temperature	—	220	°C

Recommend Operating Conditions

Table 8. Recommend Operating Conditions

ORT4622			
Temperature Range (Ambient)	Temperature Range (Junction)	I/O Supply Voltage (V_{DD})	Internal Supply Voltage (V_{DD2})
–40 °C to +85 °C	–40 °C to +125 °C	3.135 V to 3.465 V	2.3 V to 2.7 V

Electrical Characteristics

Table 9. Electrical Characteristics for FPGA I/O

ORT4622 Industrial: V_{DD} = 3.0 V to 3.6 V, $V_{DD}2$ = 2.3 V to 2.7 V, –40 °C < T_A < +85 °C.

Symbol	Parameter	Test Conditions	ORT4622		Unit
			Min	**Max**	
V_{IH} V_{IL}	Input Voltage: High Low	Input configured as CMOS (clamped to V_{DD})	50% V_{DD} GND – 0.5	V_{DD} + 0.3 30% V_{DD}	V V
V_{IH} V_{IL}	Input Voltage: High Low	Input configured as 5 V tolerant	50% V_{DD} GND – 0.5	5.8 30% V_{DD}	V V
V_{OH} V_{OL}	Output Voltage: High Low	V_{DD} = min, I_{OH} = 6 mA or 3 mA V_{DD} = min, I_{OL} = 12 mA or 6 mA	2.4 —	— 0.4	V V
I_L	Input Leakage Current	V_{DD} = max, V_{IN} = V_{SS} or V_{DD}	–10	10	µA
I_{DDSB}	Standby Current	(T_A = 25 °C, V_{DD} = 3.3 V, $V_{DD}2$ = 2.5 V) internal oscillator running, no output loads, inputs at V_{DD} or GND (after configuration)	—	5.3	mA
I_{DDSB}	Standby Current	(T_A = 25 °C, V_{DD} = 3.3 V, $V_{DD}2$ = 2.5 V) internal oscillator stopped, no output loads, inputs at V_{DD} or GND (after configuration)	—	1.4	mA
V_{DR}	Data Retention Voltage	T_A = 25 °C	2.3	—	V
I_{PP}	Powerup Current	Power supply current at approximately 1 V, within a recommended power supply ramp rate of 1 ms—200 ms	2.7	—	mA
C_{IN}	Input Capacitance	(T_A = 25 °C, V_{DD} = 3.3 V, $V_{DD}2$ = 2.5 V) test frequency = 1 MHz	—	8	pF
C_{OUT}	Output Capacitance	(T_A = 25 °C, V_{DD} = 3.3 V, $V_{DD}2$ = 2.5 V) test frequency = 1 MHz	—	9	pF
R_{DONE}	DONE Pull-up Resistor*	—	100	—	kΩ
R_M	M[3:0] Pull-up Resistors*	—	100	—	kΩ
I_{PU}	I/O Pad Static Pull-up Current*	(V_{DD} = 3.6 V, V_{IN} = V_{SS}, T_A = 0 °C)	14.4	50.9	µA
I_{PD}	I/O Pad Static Pull-down Current	(V_{DD} = 3.6 V, V_{IN} = V_{SS}, T_A = 0 °C)	26	103	µA
R_{PU}	I/O Pad Pull-up Resistor*	V_{DD} = all, V_{IN} = V_{SS}, T_A = 0 °C	100	—	kΩ
R_{PD}	I/O Pad Pull-down Resistor	V_{DD} = all, V_{IN} = V_{DD}, T_A = 0 °C	50	—	kΩ

* On the Series 3 devices, the pull-up resistor will externally pull the pin to a level 1.0 V below V_{DD}.

Electrical Characteristics (continued)

Table 10. Electrical Characteristics for Embedded Core I/O Other than LVDS I/O

Symbol	Parameter	Min	Max	Unit
V$_{IH}$	Input High Voltage (TTL input)	2.0	5.5	V
V$_{IL}$	Input Low Voltages (TTL input)	—	0.8	V
V$_{OH}$	Output High Voltage (TTL output)	2.4	—	V
V$_{OH}$	Output Low Voltage (TTL output)	—	0.4	V

Note: All outputs are driving 35 pF, except CPU data bus pins which drive 100 pF. It is assumed that the TTL buffers from the standard-cell library can handle the 100 pF load.

HSI Circuit Specifications

Input Data

The 622 Mbits/s scrambled input data stream must conform to SONET STS-12 and SDH STM-4 data format using either a PN7 or PN9 sequence. The PN7 characteristic is $1 + x^6 + x^7$ and the PN9 characteristic is $1 + x^4 + x^9$. The longest allowable stream of nontransitional 622 Mbits/s input data is 60 bits. This sequence should not occur more often than once per minute. An input signal phase change of no more than 100 ps is allowed over 200 ns time interval, which translates to a frequency change of 500 ppm. The signal eye opening must be greater than 0.4 UIp-p and the unit interval for 622 Mbits/s is 1.6075 ns.

Jitter Tolerance

The input jitter tolerance of the ORT4622 is shown in Table 11.

Table 11. Jitter Tolerance

Frequency	UIp-p
250 kHz	0.6
25 kHz	6.0
2 kHz	60

Generated Output Jitter

The generated output jitter is a maximum of 0.2 UIp-p from 250 kHz to 5 MHz.

PLL

PLL requires an external 10 kΩ pull-down resistor.

Table 12. PLL

Parameter	Min	Max	Unit
Loop Bandwidth	—	6	MHz
Jitter Peaking	—	2	dB
Powerup Reset Duration	10	—	µs
Lock Acquisition	—	1	ms

Input Reference Clock

Table 13. Input Reference Clock

Parameter	Min	Max
Frequency Deviation	—	± 20 ppm
Frequency Change	—	500 ppm
Phase Change in 200 ns	—	100 ps

LVDS I/O

Table 14. LVDS Driver dc Data*

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Driver Output Voltage High, V_{OA} or V_{OB}	R_{LOAD} = 100 Ω ± 1%	—	—	1.475*	V
V_{OL}	Driver Output Voltage Low, V_{OA} or V_{OB}	R_{LOAD} = 100 Ω ± 1%	0.925*	—	—	V
V_{OD}	Driver Output Differential Voltage V_{OD} = (V_{OA} – V_{OB}) (with External Reference Resistor)	R_{LOAD} = 100 Ω ± 1%	0.25	—	0.45*	V
V_{OS}	Driver Output Offset Voltage V_{OS} = (V_{OA} + V_{OB})/2	R_{LOAD} = 100 Ω ± 1%	1.125*	—	1.275*	V
R_O	Output Impedance, Single Ended	V_{CM} = 1.0 V and 1.4 V	40	50	60	Ω
delta R_O	R_O Mismatch Between A and B	V_{CM} = 1.0 V and 1.4 V	—	—	10	%
—	Change in $\|V_{OD}\|$ Between 0 and 1	R_{LOAD} = 100 Ω ± 1%	—	—	25	mV
—	Change in $\|V_{OS}\|$ Between 0 and 1	R_{LOAD} = 100 Ω ± 1%	—	—	25	mV
I_{SA}, I_{SB}	Output Current	Driver shorted to ground	—	—	24	mA
I_{SAB}	Output Current	Drivers shorted together	—	—	12	mA
$\|xa\|$, $\|xb\|$	Power-off Output Leakage	V_{DD} = 0 V V_{PAD}, V_{PADN} = 0 – 3 V	—	—	30	µA

* External reference, REF10 = 1.0 V ± 3%, REF14 = 1.4 V ± 3%

Table 15. LVDS Driver ac Data

Symbol	Parameter	Test Conditions	Min	Max	Unit
T_{FALL}	V_{OD} Fall Time, 80% to 20%	Z_{LOAD} = 100 Ω ± 1% C_{PAD} = 3.0 pF, C_{PAD} = 3.0 pF	100	200	ps
T_{RISE}	V_{OD} Rise Time, 20% to 80%	Z_{LOAD} = 100 Ω ± 1% C_{PAD} = 3.0 pF, C_{PAD} = 3.0 pF	100	200	ps
T_{SKEW1}	Differential Skew $\|tpHLA–tpLHB\|$ or $\|tpHLB–tpLHA\|$	Any differential pair on package at 50% point of the transition	—	50	ps
T_{SKEW2}	Channel-to-channel Skew $\|tpDIFFm–tpDIFFn\|$,	Any two signals on package at 0 V differential	—	—	ps
T_{PLH} T_{PHL}	Propagation Delay Time	Z_{LOAD} = 100 W ± 1% C_{PAD} = 3.0 pF, C_{PADN} = 3.0 pF	0.50 0.55	0.90 1.03	ps

LVDS I/O (continued)

LVDS Receiver Buffer Requirements

Table 16. LVDS Receiver dc Data

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_I	Receiver Input Voltage Range, V_{IA} or V_{IB}	$|V_{GPD}|$ < 925 mVdc 1 MHz	0	1.2	2.4	V
$|V_{IDTH}|$	Receiver Input Differential Threshold	$|V_{GPD}|$ < 925 mV 400 MHz	−100	—	100	mV
V_{HYST}	Receiver Input Differential Hysteresis	$V_{IDTHH} − V_{IDTHL}$	—	—	—*	mV
R_{IN}	Receiver Differential Input Impedance	With built-in termination, center-tapped	80	100	120	Ω

* Buffer will not produce output transition when input is open-circuited.

Note: V_{DD} = 3.1V—3.5 V, 0 °C—125 °C, slow-fast process.

Table 17. LVDS Receiver ac Data

Symbol	Parameter	Test Conditions	Min	Max	Unit
T_{PWD}	Receiver Output Pulse-width Distortion	$|V_{IDTH}|$ = 100 mV 311 MHz	—	TBD	ps
T_{PLH}, T_{PHL}	Propagation Delay Time	C_L = 1.5 pF	0.75 0.74	1.65 1.82	ns
—	With Common-mode Variation, (0 V to 2.4 V)	C_L = 1.5 pF	—	50	ps
T_{RISE}	Receiver Output Signal Rise Time, V_{OD} 20% to 80%	C_L = 1.5 pF	150	350	ps
T_{FALL}	Receiver Output Signal Fall Time, V_{OD} 80% to 20%	C_L = 1.5 pF	150	350	ps

Table 18. LVDS Receiver Power Consumption

Symbol	Parameter	Test Conditions	Min	Max	Unit
PR_{dc}	Receiver dc Power	dc	—	34.8	mW
PR_{ac}	Receiver ac Power	ac, C_L = 1.5 pF	—	0.026	mW/MHz

Table 19. LVDS Operating Parameters

Parameter	Test Conditions	Min	Normal	Max	Unit
Transmit Termination Resistor	—	—	100	—	Ω
Receiver Termination Resistor	—	—	50	—	Ω
Temperature Range	—	−40	—	125	°C
Power Supply V_{DD}	—	3.1	—	3.5	V
Power Supply V_{SS}	—	—	0	—	V

Note: Under worst-case operating condition, the LVDS driver will withstand a disabled or unpowered receiver for an unlimited period of time without being damaged. Similarly, when outputs are short-circuited to each other or to ground, the LVDS will not suffer permanent damage.

Lucent Technologies Inc.

Timing Characteristics
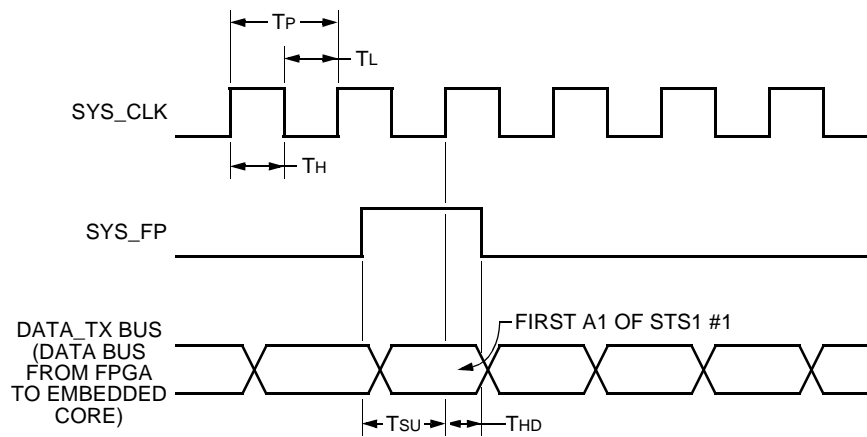
5-8605 (F)

Figure 11. Transmit Parallel Port Timing (Backplane -> FPGA)

Table 20. Timing Requirements (Transmit Parallel Port Timing)

Symbol	Parameter	Min	Max	Unit
T_P	Clock Period	12.86	—	ns
T_L	Clock Low Time	5.1	7.7	ns
T_H	Clock High Time	5.1	7.7	ns
T_{SU}	Data Setup Time	3	—	ns
T_{HD}	Data Hold Time	0	—	ns

Timing Characteristics (continued)
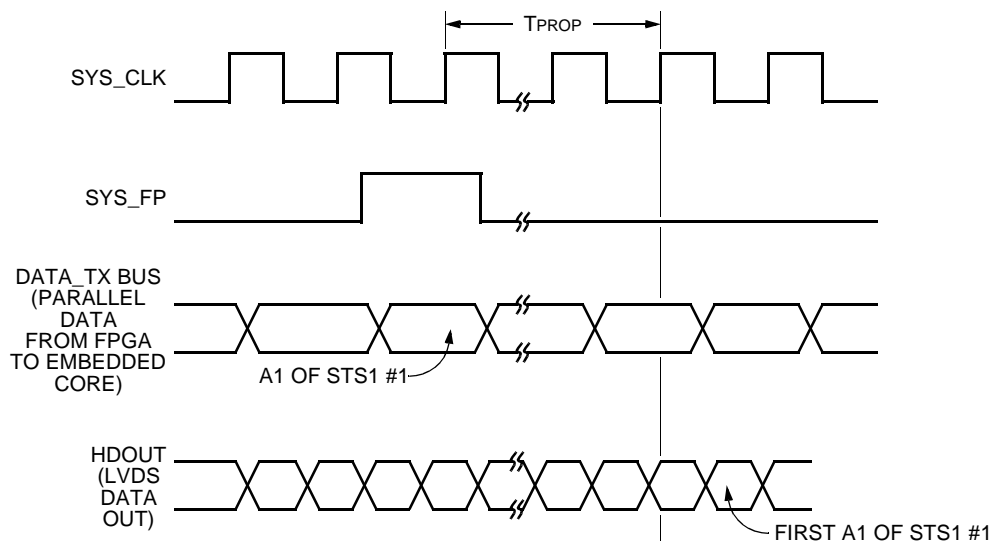
5-8606

Figure 12. Transmit Transport Delay (FPGA -> Backplane)

Table 21. Timing Requirements (Transmit Transport Delay)

Symbol	Parameter	Min	Nom	Max	Unit
T$_{PROP}$	Number of Clocks of Delay from Parallel Bus Input to LVDS Output	4	7	8	SYS_CLK

Timing Characteristics (continued)
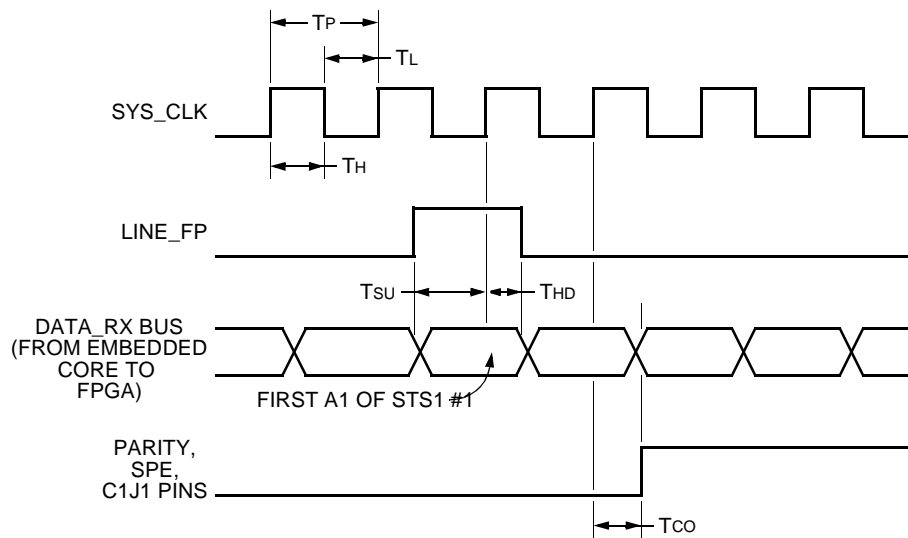
5-8607 (F)

Figure 13. Receive Parallel Port Timing (Backplane -> FPGA)

Table 22. **Timing Requirements (Receive Parallel Port Timing)**

Symbol	Parameter	Min	Nom	Max	Unit
T_P	Clock Period	12.86	—	—	ns
T_L	Clock Low Time	5.1	6.43	7.7	ns
T_H	Clock High Time	5.1	6.43	7.7	ns
T_{SU}	Data Setup Time	3	—	—	ns
T_{HD}	Data Hold Time	0	—	—	ns
T_{CO}	Clock to Output Time of Data, Parity, SPE, and C1J1 Pins	1.3	—	7	ns

Lucent Technologies Inc.

Timing Characteristics (continued)
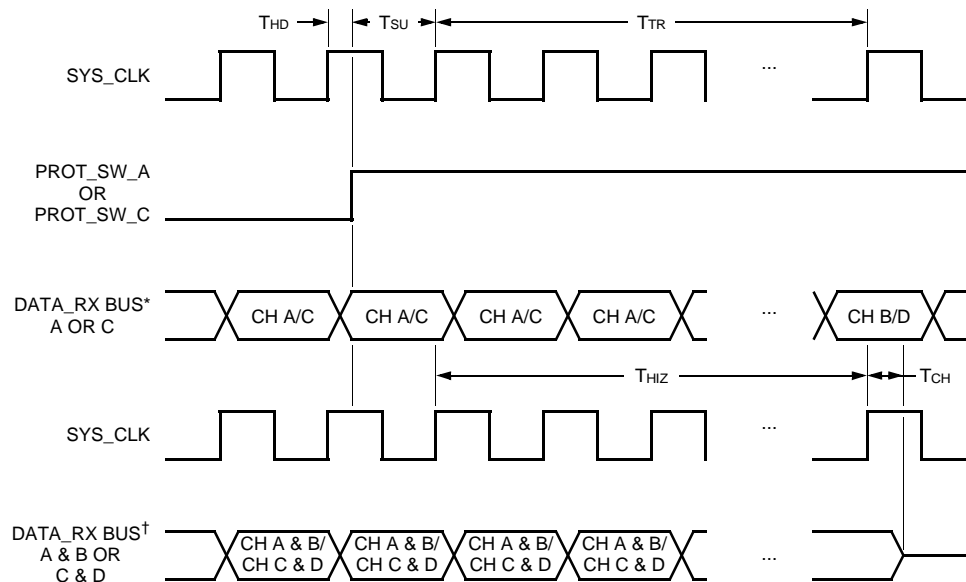
5-8608 (F)

* Data bus refers to 8 bits data, 1 bit parity, 1 bit SPE, and 1 bit C1J1.
† Channel A or C refers to whether the PROT_SW_A or PROT_SW_C pins that are activated. For example, if the PROT_SW_A pin is activated, the timing diagram for output bus A or C refers to output bus A.

Figure 14. Protection Switch Timing

Table 23. Timing Requirements (Protection Switch Timing)

Symbol	Parameter	Min	Nom	Max	Unit
T_{TR}	Transport Delay from Latching of PROT_SW_A/C to Actual Data Switch	7	8	9	Leading edge SYS_CLKs
T_{HIZ}	Transport Delay from Latching of PROT_SW_A/C to Actual Hi-z	4	5	6	Leading edge SYS_CLKs
T_{CH}	Propagation Delay from SYS_CLK to HI-Z of Output Bus	—	—	25	Leading edge SYS_CLKs
T_{SU}	Setup Time Required from Change in PROT_SW_A/C to Rising SYS_CLK	3	—	—	ns
T_{HD}	Hold Time Required from Rising SYS_CLK to Change in PROT_SW_A/C	0	—	—	ns

Timing Characteristics (continued)
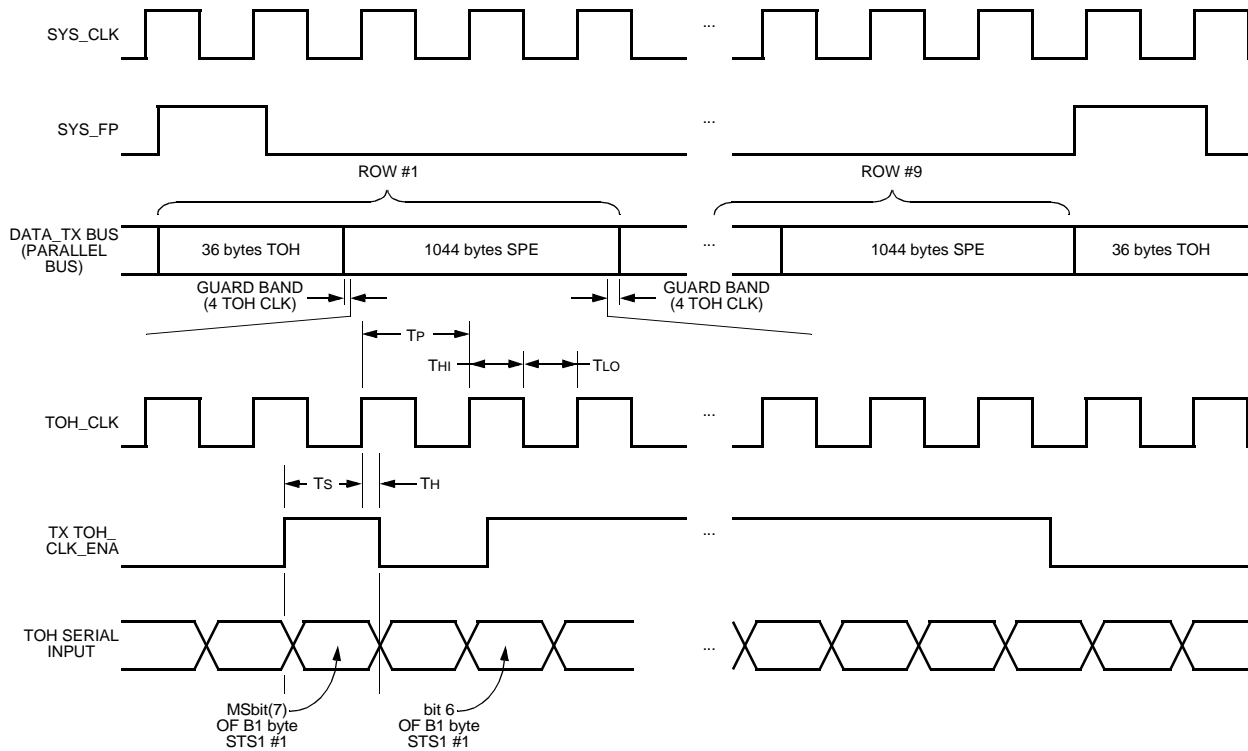
5-8609 (F)

Figure 15. TOH Input Serial Port Timing (FPGA -> Backplane)

Table 24. Timing Requirements (TOH Input Serial Port Timing)

Symbol	Parameter	Min	Nom	Max	Unit
T_P	Clock Period	12.86	—	40	ns
T_{HI}	Clock High Time	5.1	6.43	7.7	ns
T_{LO}	Clock Low Time	5.1	6.43	7.7	ns
T_S	Data Setup Time	3	—	—	ns
T_H	Data Hold Time	0	—	—	ns

Timing Characteristics (continued)
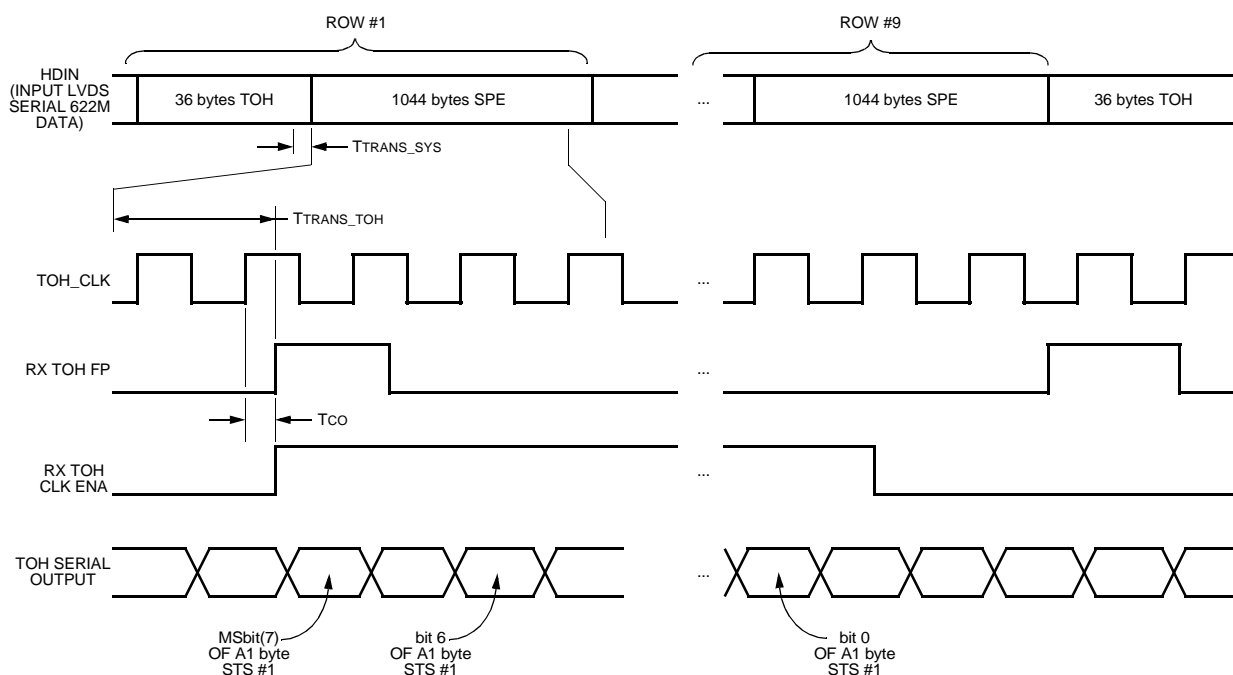
5-8610 (F)

Note: The total delay from A1 STS1 #1 arriving at LVDS input to RX_TOH_FP is 56 SYS_CLKs and 6 TOH_CLKs. This will vary by ±14 SYS_CLKs, 12 each way for the FIFO alignment, and ±2 SYS_CLKs due to the variability in the clock recovery of the HSI macro.

Figure 16. TOH Output Serial Port Timing (Backplane -> FPGA)

Table 25. Timing Requirements (TOH Output Serial Port Timing)

Symbol	Parameter	Min	Nom	Max	Unit
T_{CO}	Data Clock to Out	2	—	8	ns
T_{TRANS_SYS}	Delay from First A1 LVDS Serial Input to Transfer to TOH_CLK	44	56	68	SYS_CLKs
T_{TRANS_TOH}	Delay from Transfer to TOH_CLK to RX_TOH_FP	—	6	—	TOH_CLKs

Timing Characteristics (continued)
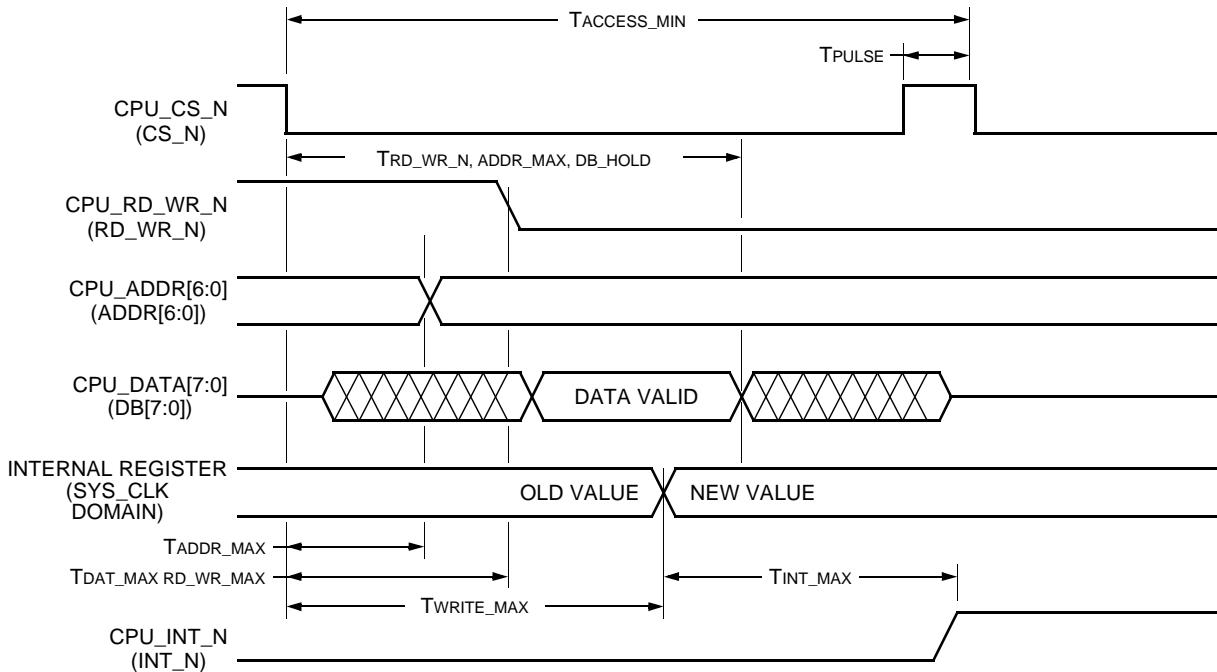
5-8611 (F)

Note: The CPU interface can be bit stream selected either from device I/O or FPGA interface. The timing diagram applies to both interfaces.

Figure 17. CPU Write Transaction

Table 26. Timing Requirements (CPU Write Transaction)

Symbol	Parameter	Min	Max	Unit
T_{PULSE}	Minimum Pulse Width for CS_N	5	—	ns
T_{ADDR_MAX}	Maximum Time from Negative Edge of CS_N to ADDR Valid	—	18	ns
T_{DAT_MAX}	Maximum Time from Negative Edge of CS_N to Data Valid	—	25	ns
$T_{RD\_WR\_MAX}$	Maximum Time from Negative Edge of CS_N to Negative Edge of RD_WR_N	—	26	ns
T_{WRITE_MAX}	Maximum Time from Negative Edge of CS_N to Contents of Internal Register Latching DB[7:0]	—	60	ns
T_{ACCESS_MIN}	Minimum Time Between a Write Cycle (Falling Edge of CS_N) and Any Other Transaction (Read or Write at Falling Edge of CS_N)	60	—	ns
T_{INT_MAX}	Maximum Time from Register FF to Pad	—	20	ns
$T_{RW\_WR\_N,}$ ADDR, DB_HOLD	Minimum Hold Time that RD_WR_N, ADDR and DB Must be Held Valid from the Negative Edge of CS_N	57	—	ns

Timing Characteristics (continued)
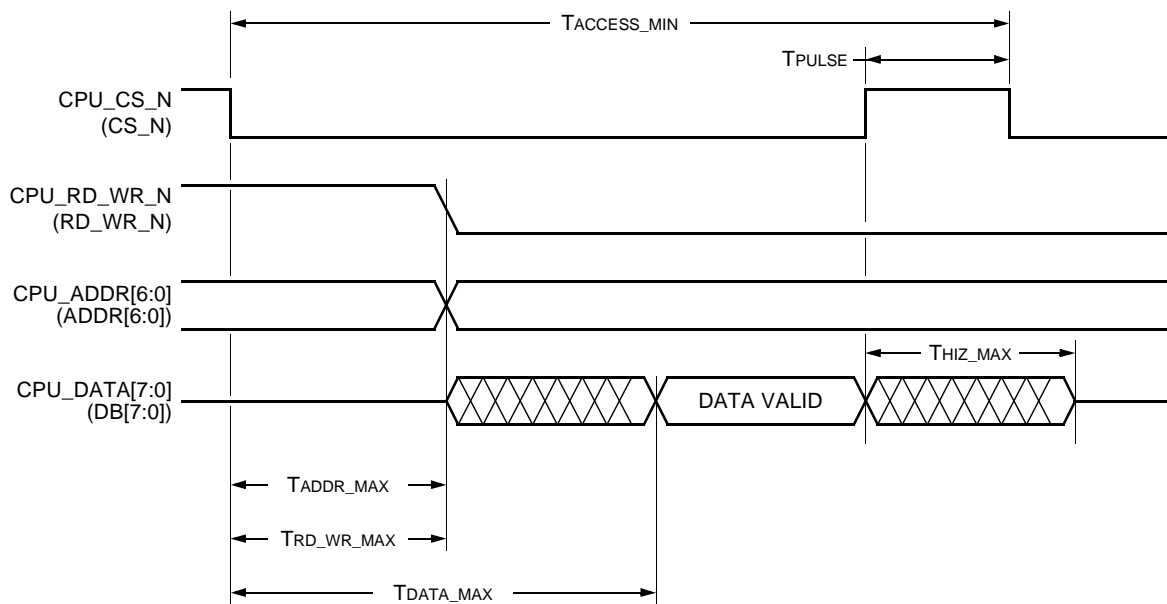
5-8612 (F)

Notes:

The CPU interface can be bit stream selected either from device I/O or FPGA interface. The timing diagram applies to both interfaces.

The time delay between the advanced SYS_CLK and the distributed SYS_CLK used to sample CS_N is of no consequence. However, the path delay of CS_N from pad to where is it sampled by SYS_CLK must be minimized.

The calculated delays assume a 100 pF loading on the DB pins.

Figure 18. CPU Read Transaction

Table 27. Timing Requirements (CPU Read Transaction)

Symbol	Parameter	Min	Max	Unit
T_{PULSE}	Minimum Pulse Width for CS_N	5	—	ns
T_{ADDR_MAX}	Maximum Time from Negative Edge of CS_N to ADDR Valid	—	5	ns
$T_{RD\_WR\_MAX}$	Maximum Time from Negative Edge of CS_N to RD_WR_N Falling	—	5	ns
T_{DATA_MAX}	Maximum Time from Negative Edge of CS_N to Data Valid on DB Port	—	56	ns
T_{HIZ_MAX}	Maximum Time from Rising Edge of CS_N to DB Port Going HI-Z	—	12	ns
T_{ACCESS_MIN}	Minimum Time Between a Read Cycle (Falling Edge of CS_N) and Any Other Transaction (Read or Write at Falling Edge of CS_N)	60	—	ns

Input/Output Buffer Measurement Conditions
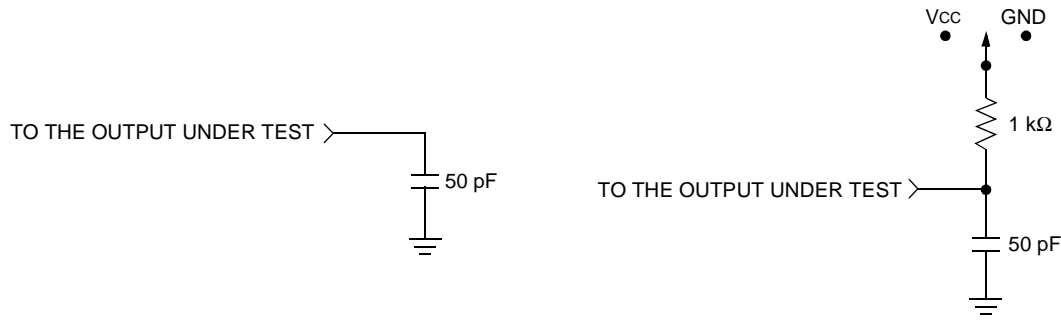
A. Load Used to Measure Propagation Delay

B. Load Used to Measure Rising/Falling Edges

5-3234(F)

Note: Switch to VDD for TPLZ/TPZL; switch to GND for TPHZ/TPZH.

Figure 19. ac Test Loads
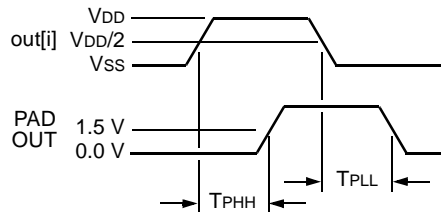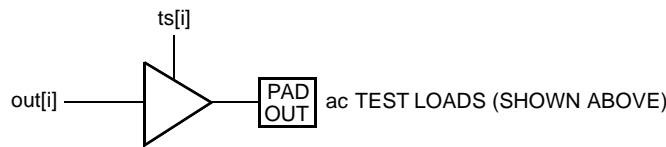
5-3233.a(F)

Figure 20. Output Buffer Delays
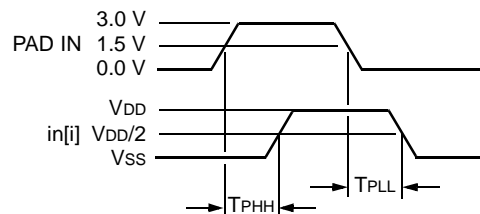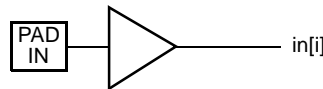
5-3235(F)

Figure 21. Input Buffer Delays

Lucent Technologies Inc.

FPGA Output Buffer Characteristics

5-6865(F)
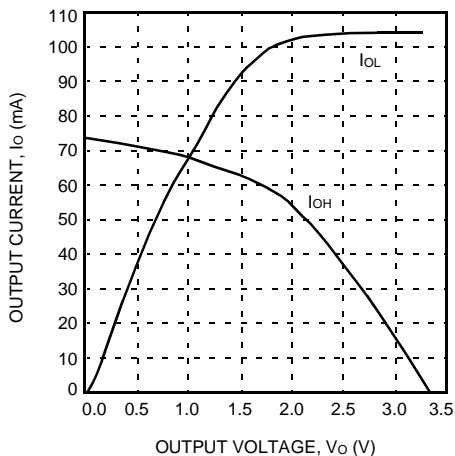
Figure 22. Sinklim (TJ = 25 °C, VDD = 3.3 V)

5-6867(F)
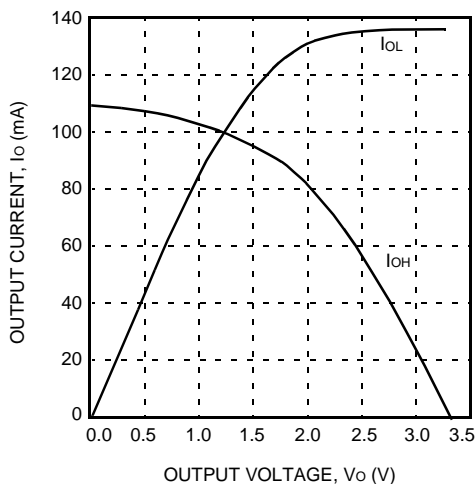
Figure 23. Slewlim (TJ = 25 °C, VDD = 3.3 V)

5-6867(F)
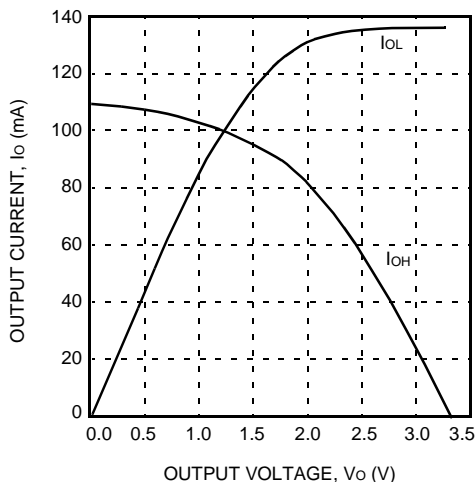
Figure 24. Fast (TJ = 25 °C, VDD = 3.3 V)
Lucent Technologies Inc.

5-6866(F)
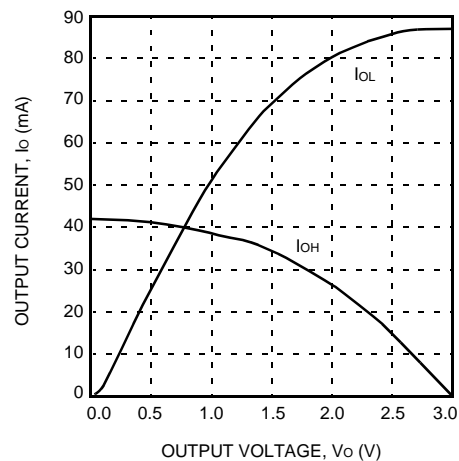
Figure 25. Sinklim (TJ = 125 °C, VDD = 3.0 V)

5-6868(F)
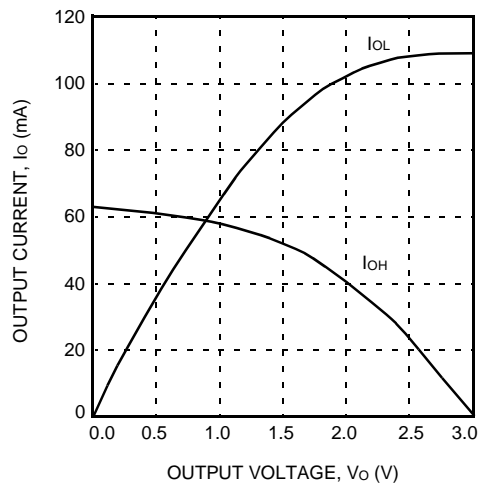
Figure 26. Slewlim (TJ = 125 °C, VDD = 3.0 V)

5-6868(F)
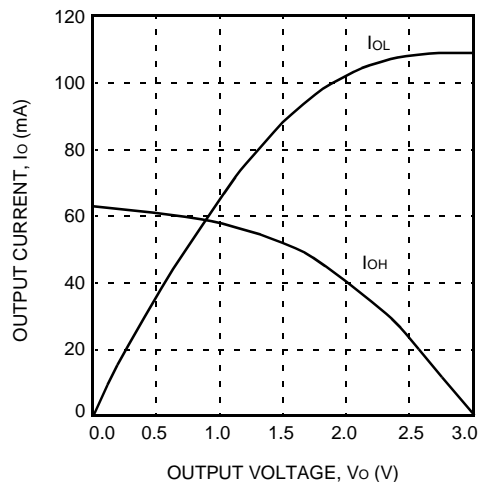
Figure 27. Fast (TJ = 125 °C, VDD = 3.0 V)

47

Estimating Power Dissipation

This section will be included in a future release of this data sheet.

General FPGA power estimation parameters can be found in the *ORCA* Series 3 data sheet.

Pin Information

Table 28. **FPGA Common-Function Pin Description**

Symbol	I/O	Description
Dedicated Pins		
V$_{DD}$	—	3.3 V power supply.
V$_{DD}$2	—	2.5 V power supply
GND	—	Ground supply.
$\overline{RESET}$	I	During configuration, $\overline{RESET}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{RESET}$ can be used as an FPGA logic direct input, which causes all PLC latches/FFs to be asynchronously set/reset.
CCLK	I	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in. In the slave or synchronous peripheral mode, CCLK is input synchronous with the data on DIN or D[7:0]. In microprocessor mode, CCLK is used internally and output for daisy-chain operation.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.*
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has a permanent pull-up resistor.
$\overline{PRGM}$	I	$\overline{PRGM}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
$\overline{RD\_CFG}$	I	This pin must be held high during device initialization until the $\overline{INIT}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{RD\_CFG}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{RD\_CFG}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{RD\_CFG}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary scan, TDO is test data out.
Special-Purpose Pins		
M0, M1, M2	I	During powerup and initialization, M0, M1, and M2 are used to select the configuration mode with their values latched on the rising edge off $\overline{INIT}$. During configuration, a pull-up is enabled. After configuration, these pins cannot be user-programmable I/Os.
M3	I	During powerup and initialization, M3 is used to select the speed of the internal oscillator during configuration with their values latched on the rising edge of $\overline{INIT}$. When M3 is low, the oscillator frequency is 10 MHz. When M3 is high, the oscillator is 1.25 MHz. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.*

* The *ORCA* Series 3 FPGA data sheet contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

Table 28. FPGA Common-Function Pin Description (continued)

Symbol	I/O	Description
Special-Purpose Pins (continued)		
TDI, TCK, TMS	I	If boundary scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary scan is not used, either TCK or TMS must be held at logic one during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O.*
RDY/RCLK/ MPI_ALE	O	During configuration in peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode.
	O	During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I	In *i960* microprocessor mode, this pin acts as the address latch enable (ALE) input.
	I/O	After configuration, if the MPI is not used, this pin is a user-programmable I/O pin.*
HDC	O	High during configuration (HDC) is output high until configuration is complete. It is used as a control output indicating that configuration is not complete.
$\overline{LDC}$	O	Low during configuration ($\overline{LDC}$) is output low until configuration is complete. It is used as a control output indicating that configuration is not complete.
$\overline{INIT}$	I/O	$\overline{INIT}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{INIT}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{INIT}$ holds the FPGA in the wait-state before the start of configuration.
$\overline{CS0}$, CS1	I	$\overline{CS0}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{CS0}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O pins.*
$\overline{RD}$/MPI_STRB	I	$\overline{RD}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{RD}$ changes D7 into a status output. As a status indication, a high indicates ready, and a low indicates busy. $\overline{WR}$ and $\overline{RD}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the microprocessor interface (MPI) data transfer strobe. For *PowerPC*, it is the transfer start ($\overline{TS}$). For *i960*, it is the address/data strobe ($\overline{ADS}$).
	I/O	After configuration, if the MPI is not used, this pin is a user-programmable I/O pin.*
$\overline{WR}$	I	$\overline{WR}$ is used in the asynchronous peripheral configuration mode. When the FPGA is selected, a low on the write strobe, $\overline{WR}$, loads the data on D[7:0] inputs into an internal data buffer. $\overline{WR}$ and $\overline{RD}$ should not be used simultaneously. If they are, the write strobe overrides.
	I/O	After configuration, this pin is a user-programmable I/O pin.*

* The *ORCA* Series 3 FPGA data sheet contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

Table 28. FPGA Common-Function Pin Description (continued)

Symbol	I/O	Description
Special-Purpose Pins (continued)		
$\overline{\text{MPI\_IRQ}}$	O	MPI active-low interrupt request output.
$\overline{\text{MPI\_BI}}$	O	*PowerPC* mode MPI burst inhibit output.
	I/O	If the MPI is not in use, this is a user-programmable I/O.
$\overline{\text{MPI\_ACK}}$	O	In *PowerPC* mode MPI operation, this is the active-high transfer acknowledge ($\overline{\text{TA}}$) output. For *i960* MPI operation, it is the active-low ready/record ($\overline{\text{RDYRCV}}$) output. If the MPI is not in use, this is a user-programmable I/O.
MPI_RW	I	In *PowerPC* mode MPI operation, this is the active-low write/active-high read control signals. For *i960* operation, it is the active-high write/active-low read control signal.
	I/O	If the MPI is not in use, this is a user-programmable I/O.
MPI_CLK	I	This is the clock used for the synchronous MPI interface. For *PowerPC*, it is the CLK-OUT signal. For *i960*, it is the system clock that is chosen for the *i960* external bus interface.
	I/O	If the MPI is not in use, this is a user-programmable I/O.
A[4:0]	I	For *PowerPC* operation, these are the *PowerPC* address inputs. The address bit mapping (in *PowerPC*/FPGA notation) is A[31]/A[0], A[30]/A[1], A[29]/A[2], A[28]/A[3], A[27]/A[4]. Note that A[27]/A[4] is the MSB of the address. The A[4:2] inputs are not used in *i960* MPI mode.
	I/O	If the MPI is not in use, this is a user-programmable I/O.
A[1:0]/$\overline{\text{MPI\_BE[1:0]}}$	I	For *i960* operation, $\overline{\text{MPI\_BE[1:0]}}$ provide the *i960* byte enable signals, $\overline{\text{BE[1:0]}}$, that are used as address bits A[1:0] in *i960* byte-wide operation.
D[7:0]	I	During peripheral, and slave parallel configuration modes, D[7:0] receive configuration data, and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input. D[7:0] are also the data pins for *PowerPC* microprocessor mode and the address/data pins for *i960* microprocessor mode.
	I/O	After configuration, the pins are user-programmable I/O pins.*
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave LCA devices. Data out on DOUT changes on the falling edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.*

* The *ORCA* Series 3 FPGA data sheet contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

This section describes device I/O signals to/from the embedded core excluding the signals at the CIC boundary.

Table 29. FPSC Function Pin Description

Symbol	I/O	Description
HSI LVDS Pins		
STS_INA	I	LVDS input receiver A.
STS_INAN	I	LVDS input receiver A.
STS_INB	I	LVDS input receiver B.
STS_INBN	I	LVDS input receiver B.
STS_INC	I	LVDS input receiver C.
STS_INCN	I	LVDS input receiver C.
STS_IND	I	LVDS input receiver D.
STS_INDN	I	LVDS input receiver D.
STS_OUTA	O	LVDS output receiver A.
STS_OUTAN	O	LVDS output receiver A.
STS_OUTB	O	LVDS output receiver B.
STS_OUTBN	O	LVDS output receiver B.
STS_OUTC	O	LVDS output receiver C.
STS_OUTCN	O	LVDS output receiver C.
STS_OUTD	O	LVDS output receiver D.
STS_OUTDN	O	LVDS output receiver D.
CTAP_REFA	—	LVDS input center tap (RX A) (use 0.01 µF to GND).
CTAP_REFB	—	LVDS input center tap (RX B) (use 0.01 µF to GND).
CTAP_REFC	—	LVDS input center tap (RX C) (use 0.01 µF to GND).
CTAP_REFD	—	LVDS input center tap (RX D) (use 0.01 µF to GND).
REF10	I	LVDS reference voltage: 1.0 V ± 3%.
REF14	I	LVDS reference voltage: 1.4 V ± 3%.
RESHI	—	Resistor input (use 100 Ω ± 1% to RESLO input).
RESLO	—	Resistor input.
REXT	—	Reference resistor for PLL (10 kΩ to ground).
PLL_V_{DD}A	—	PLL analog V_{DD} (3.3 V ± 5%).
PLL_V_{SS}A	—	PLL analog V_{SS} (GND).
HSI Test Signals		
TSTMODE	I	Enables CDR test mode
BYPASS	I	Enables bypassing of the 622 MHz clock synthesis with TSTCLK.
TSTCLK	I	Test clock for emulation of 622 MHz clock during PLL bypass.
MRESET	I	Test mode reset.
RESETRN	I	Resets receiver clock division counter.
RESETTN	I	Resets transmitter clock division counter.

Pin Information (continued)

Table 29. FPSC Function Pin Description (continued)

Symbol	I/O	Description
HSI Test Signals (continued)		
TSTSHFTLD	I	Enables the test mode control register for shifting in selected tests by a serial port.
ECSEL	I	Enables external test control of 622 MHz clock phase selecion.
EXDNUP	I	Direction of phase change.
ETOGGLE	I	Moves 622.08 MHz clock selection on phase per positive pulse.
LOOPBKEN	I	Enables 622 Mbits/s loopback mode.
TSTPHASE	I	Controls bypass of 16 PLL-generated phases with 16 low-speed phases.
TSTMUX[8:0]S	O	Test mode output port.
CPU Interface Pins		
DB<7:0>	I/O	CPU interface data bus.
ADDR<6:0>	I	CPU interface address bus.
RD_WR_N	I	CPU interface read/write.
CS_N	I	Chip select.
INT_N	O	Interrupt output.
MISC System Signals		
RST_N	I	Global reset. External pull-down allows chip to stay in reset state when external driver loses power.
SYS_CLK	I	System clock (77.76 MHz), 50% duty cycle, also the reference clock of PLL.
DXP	—	Temperature sensing diode (anode +).
DXN	—	Temperature sensing diode (cathode –).
SCAN and BSCAN Pins*		
SCAN_TSTMD	I	Scan test mode input.
SCANEN	I	Scan mode enable input.
LVDS_EN	I	LVDS enable used during BSCAN. During normal operation, LVDS_EN needs to be pulled high. LVDS_EN needs to be pulled low for boundary scan.
Universal BIST Controller Pins		
SYS_DOBIST	I	SYS_DOBIST is asserted high to start the BIST, should be kept high during the entire BIST operation.
SYS_RSSIGO	O	This 32-bit serial out RSB signature consists of the 4-bit FSM state and the BIST flag flip-flop states from each SBRIC_RS element.
BC	O	This flag is asserted to one when BIST is complete, is used for polling the end of BIST.

* BSCAN pins-TDI, TDO, TCK, TMS are on FPGA side.

Pin Information (continued)

In Table 30, an input refers to a signal flowing into the FGPA logic (out of the embedded core) and an output refers to a signal flowing out of the FPGA logic (into the embedded core).

Table 30. Embedded Core/FPGA Interface Signal Description

Pin Name	I/O	Description
DATA_TXA<7:0>	O	Parallel bus of transmitter A. MSB is bit 7.
DATA_TXA_PAR	O	Parity for transmitter A.
DATA_TXB<7:0>	O	Parallel bus of transmitter B. MSB is bit 7.
DATA_TXB_PAR	O	Parity for transmitter B.
DATA_TXC<7:0>	O	Parallel bus of transmitter C. MSB is bit 7.
DATA_TXC_PAR	O	Parity for transmitter C.
DATA_TXD<7:0>	O	Parallel bus of transmitter D. MSB is bit 7.
DATA_TXD_PAR	O	Parity for transmitter D.
DATA_RXA<7:0>	I	Parallel bus of receiver A. MSB is bit 7.
DATA_RXA_PAR	I	Parity for parallel bus of receiver A.
DATA_RXA_SPE	I	SPE signal for parallel bus of receiver A.
DATA_RXA_C1J1	I	C1J1 signal for parallel bus of receiver A.
DATA_RXA_EN	I	Enable for parallel bus of receiver A.
DATA_RXB<7:0>	I	Parallel bus of receiver B. MSB is bit 7.
DATA_RXB_PAR	I	Parity for parallel bus of receiver B.
DATA_RXB_SPE	I	SPE signal for parallel bus of receiver B.
DATA_RXB_C1J1	I	C1J1 signal for parallel bus of receiver B.
DATA_RXB_EN	I	Enable for parallel bus of receiver B.
DATA_RXC<7:0>	I	Parallel bus of receiver C. MSB is bit 7.
DATA_RXC_PAR	I	Parity for parallel bus of receiver C.
DATA_RXC_SPE	I	SPE signal for parallel bus of receiver C.
DATA_RXC_C1J1	I	C1J1 signal for parallel bus of receiver C.
DATA_RXC_EN	I	Enable for parallel bus of receiver C.
DATA_RXD<7:0>	I	Parallel bus of receiver D. MSB is bit 7.
DATA_RXD_PAR	I	Parity for parallel bus of receiver D.
DATA_RXD_SPE	I	SPE signal for parallel bus of receiver D.
DATA_RXD_C1J1	I	C1J1 signal for parallel bus of receiver D.
DATA_RXD_EN	I	Enable for parallel bus of receiver D.
TOH_CLK	O	TX and RX TOH serial links clock (25 MHz to 77.76 MHz).
TOH_TXA	O	TOH serial link for transmitter A.
TOH_TXB	O	TOH serial link for transmitter B.
TOH_TXC	O	TOH serial link for transmitter C.
TOH_TXD	O	TOH serial link for transmitter D.
TX_TOH_CK_EN	O	TX TOH serial link clock enable.
TOH_RXA	I	TOH serial link for receiver A.
TOH_RXB	I	TOH serial link for receiver B.
TOH_RXC	I	TOH serial link for receiver C.

Pin Information (continued)

Table 30. Embedded Core/FPGA Interface Signal Description (continued)

Pin Name	I/O	Description
TOH_RXD	I	TOH serial link for receiver D.
RX_TOH_CK_EN	I	RX TOH serial link clock enable.
RX_TOH_FP	I	RX TOH serial link frame pulse.
TOH_CK_FP_EN	I	TX TOH clock and frame pulse enable.
TOH_EN_A	I	TX TOH enable, soft register control. Can be used for channel A, B, C, or D.
CPU_DATA_TX<7:0>	O	CPU interface data bus.
CPU_DATA_RX<7:0>	I	CPU interface data bus.
CPU_ADDR<6:0>	O	CPU interface address bus.
CPU_RD_WR_N	O	CPU interface read/write.
CPU_CS_N	O	Chip select.
CPU_INT_N	I	Interrupt.
SYS_FP	O	System frame pulse for transmitter section.
LINE_FP	O	Line frame pulse for receiver section.
FPGA_SYSCLK	O	System clock (77.76 MHz).
PROT_SW_A	O	Protection switching control signal.
PROT_SW_C	O	Protection switching control signal.
CORE_READY	I	Flag indicates that the embedded core is out of its reset state.
FIFOSYNC_FP	I	The alignment FIFO synchronizes and locates the data frames and outputs an optimal frame pulse for the four arriving data streams.
CDR_CLK_A	I	77.76 MHz recovered clock for channel A.
CDR_CLK_B	I	77.76 MHz recovered clock for channel B.
CDR_CLK_C	I	77.76 MHz recovered clock for channel C.
CDR_CLK_D	I	77.76 MHz recovered clock for channel D.
RB_MP_SEL	I	Bit stream selection for microprocessor interface selection. A 0 indicates the microprocessor interface on the core side is selected. A 1 selects the CPU interface from the FPGA side.

Pin Information (continued)

Table 31 lists the physical locations of all signals on the embedded core/FPGA interface.

Table 31. Embedded Core/FPGA Interface Signal Locations

Embedded Core/FPGA Interface Site	FPGA Input Signal	FPGA Output Signal	Embedded Core/FPGA Interface Site	FPGA Input Signal	FPGA Output Signal
ASB1A	TOH_RXA	TOH_TXA	ASB10C	DATA_RXC1	—
ASB1B	TOH_RXB	TOH_TXB	ASB10D	DATA_RXC0	—
ASB1C	TOH_RXC	TOH_TXC	ASB11A	DATA_RXC_PAR	PROT_SW_C
ASB1D	TOH_RXD	TOH_TXD	ASB11B	DATA_RXC_SPE	—
CKTOASB1	—	TOH_CLK	ASB11C	DATA_RXC_C1J1	—
ASB2A	RX_TOH_CK_EN	—	ASB11D	DATA_RXC_EN	
ASB2B	RX_TOH_FP	—	ASB12A	DATA_RXD7	—
ASB2C	TOH_CK_FP_EN	TX_TOH_CK_EN	ASB12B	DATA_RXD6	—
ASB2D	TOH_EN_A	—	ASB12C	DATA_RXD5	—
ASB3A	DATA_RXA7	—	ASB12D	DATA_RXD4	—
ASB3B	DATA_RXA6	—	ASB13A	DATA_RXD3	—
ASB3C	DATA_RXA5	—	ASB13B	DATA_RXD2	—
ASB3D	DATA_RXA4	—	ASB13C	DATA_RXD1	—
ASB4A	DATA_RXA3	—	ASB13D	DATA_RXD0	—
ASB4B	DATA_RXA2	—	ASB14A	DATA_RXD_PAR	LINE_FP
ASB4C	DATA_RXA1	—	ASB14B	DATA_RXD_SPE	SYS_FP
ASB4D	DATA_RXA0	—	ASB14C	DATA_RXD_C1J1	—
ASB5A	DATA_RXA_PAR	PROT_SW_A	ASB14D	DATA_RXD_EN	—
ASB5B	DATA_RXA_SPE	—	CKFRASB14	—	—
ASB5C	DATA_RXA_C1J1	—	ASB15A	FIFOSYNC_FP	DATA_TXA7
ASB5D	DATA_RXA_EN	—	ASB15B	—	DATA_TXA6
ASB6A	DATA_RXTB7	—	ASB15C	—	DATA_TXA5
ASB6B	DATA_RXB6	—	ASB15D	—	DATA_TXA4
ASB6C	DATA_RXB5	—	ASB16A	—	DATA_TXA3
ASB6D	DATA_RXB4	—	ASB16B	—	DATA_TXA2
ASB7A	DATA_RXB3	—	ASB16C	—	DATA_TXA1
ASB7B	DATA_RXB2	—	ASB16D	—	DATA_TXA0
ASB7C	DATA_RXB1	—	ASB17A	—	DATA_TXB7
ASB7D	DATA_RXB0	—	ASB17B	—	DATA_TXB6
ASB8A	DATA_RXB_PAR	—	ASB17C	—	DATA_TXB5
ASB8B	DATA_RXB_SPE	—	ASB17D	—	DATA_TXB4
ASB8C	DATA_RXB_C1J1	—	ASB18A	—	DATA_TXB3
ASB8D	DATA_RXB_EN	—	ASB18B	—	DATA_TXB2
ASB9A	DATA_RXC7	—	ASB18C	—	DATA_TXB1
ASB9B	DATA_RXC6	—	ASB18D	—	DATA_TXB0
ASB9C	DATA_RXC5	—	ASB19A	—	DATA_TXA_PAR
ASB9D	DATA_RXC4	—	ASB19B	—	DATA_TXB_PAR
ASB10A	DATA_RXC3	—	ASB19C	—	DATA_TXC_PAR
ASB10B	DATA_RXC2	—	ASB19D	—	DATA_TXD_PAR

Pin Information (continued)

Table 31. Embedded Core/FPGA Interface Signal Locations (continued)

Embedded Core/FPGA Interface Site	FPGA Input Signal	FPGA Output Signal	Embedded Core/FPGA Interface Site	FPGA Input Signal	FPGA Output Signal
ASB20A	—	DATA_TXC7	ASB24D	CPU_DATA_RX4	CPU_DATA_TX4
ASB20B	—	DATA_TXC6	ASB25A	CPU_DATA_RX3	CPU_DATA_TX3
ASB20C	—	DATA_TXC5	ASB25B	CPU_DATA_RX2	CPU_DATA_TX2
ASB20D	—	DATA_TXC4	ASB25C	CPU_DATA_RX1	CPU_DATA_TX1
ASB21A	—	DATA_TXC3	ASB25D	CPU_DATA_RX0	CPU_DATA_TX0
ASB21B	—	DATA_TXC2	ASB26A	CPU_INT_N	CPU_ADDR6
ASB21C	—	DATA_TXC1	ASB26B	—	CPU_ADDR5
ASB21D	—	DATA_TXC0	ASB26C	—	CPU_ADDR4
ASB22A	—	DATA_TXD7	ASB26D	CORE_READY	CPU_ADDR3
ASB22B	—	DATA_TXD6	ASB27A	—	CPU_ADDR2
ASB22C	—	DATA_TXD5	ASB27B	—	CPU_ADDR1
ASB22D	—	DATA_TXD4	ASB27C	—	CPU_ADDR0
ASB23A	—	DATA_TXD3	ASB27D	—	CPU_RD_WR_N
ASB23B	—	DATA_TXD2	ASB28A	CDR_CLK_A	CPU_CS_N
ASB23C	—	DATA_TXD1	ASB28B	CDR_CLK_B	—
ASB23D	—	DATA_TXD0	ASB28C	CDR_CLK_C	—
ASB24A	CPU_DATA_RX7	CPU_DATA_TX7	ASB28D	CDR_CLK_D	—
ASB24B	CPU_DATA_RX6	CPU_DATA_TX6	BMLKCNTL	FPGA_SYSCLK	—
ASB24C	CPU_DATA_RX5	CPU_DATA_TX5			

Pin Information (continued)

The ORT4622 is pin compatible with a Series 3 OR3L125B device in the same package in terms of V_{DD}, V_{SS}, configuration, and special function pins. The uses and characteristics of the FPGA user I/O pins in the embedded core area of the device have changed to support the ORT4622 functionality. Additionally, the lower-left programmable clock manager (PCM) clock input pin (SECKLL) has been relocated.

Table 32. 432-Pin EBGA Pinout

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
E4	PRD_CFGN	$\overline{RD\_CFG}$	P1	$V_{DD}2$	$V_{DD}2$
D3	PR1D	I/O	R3	PR14D	I/O
D2	PR1C	I/O	R2	PR14C	I/O
D1	PR1B	I/O	R1	PR14B	I/O
F4	PR1A	I/O	T2	PECKR	I/O-ECKR
E3	PR2D	I/O	T4	PR15D	I/O
E2	PR2C	I/O	T3	PR15C	I/O
E1	PR2B	I/O	U1	PR15B	I/O
F3	PR2A	I/O	U2	PR15A	I/O
F2	PR3D	I/O	U3	PR16D	I/O
F1	PR3C	I/O	V1	PR16B	I/O
H4	PR3B	I/O	V2	PR16A	I/O
G3	PR3A	I/O-$\overline{WR}$	V3	PR17D	I/O
G2	PR4D	I/O	W1	PR17A	I/O-M3
G1	PR4C	I/O	V4	PR18D	I/O
J4	PR4B	I/O	W2	PR18B	I/O
H3	$V_{DD}2$	$V_{DD}2$	W3	PR18A	I/O
H2	PR5A	I/O	Y2	PR19D	—
J3	PR6C	I/O	W4	PR19A	M2
K4	PR6A	I/O	Y3	PR20D	—
J2	PR7A	I/O-$\overline{RD}$/MPI_STRB	AA1	PR20C	—
J1	PR8D	I/O	AA2	PR20B	—
K3	PR8C	I/O	Y4	PR20A	—
K2	PR8B	I/O	AA3	$V_{DD}2$	$V_{DD}2$
K1	PR8A	I/O	AB1	PR21C	—
L3	PR9D	I/O	AB2	PR21B	—
M4	PR9C	I/O	AB3	PR21A	—
L2	PR9B	I/O	AC1	PR22D	M1
L1	PR9A	I/O-$\overline{CS0}$	AC2	PR23D	—
M3	PR10D	I/O	AB4	PR23B	—
N4	PR10A	I/O	AC3	PR23A	—
M2	PR11D	I/O	AD2	PR24A	—
N3	PR11A	I/O-CS1	AD3	PR25C	—
N2	PR12D	I/O	AC4	PR25B	—
P4	PR12C	I/O	AE1	PR25A	DB3 (core)
N1	PR12A	I/O	AE2	PR26D	DB2 (core)
P3	PR13D	I/O	AE3	PR26C	DB1 (core)
P2	PR13C	I/O	AD4	PR26B	DB0 (core)

Pin Information (continued)

Table 32. 432-Pin EBGA Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
AF1	PR26A	DB7 (core)	AL11	PB20A	$\overline{\text{LDC}}$
AF2	PR27D	DB6 (core)	AJ12	PB19D	TSTSHFTLD (core)
AF3	PR27C	DB5 (core)	AH13	PB19B	RESETRN (core)
AG1	PR27B	DB4 (core)	AK12	PB19A	TSTCLK (core)
AG2	VDD2	VDD2	AJ13	PB18D	BYPASS (core)
AG3	PR28D	INT_N (core)	AK13	PB18B	TSTMODE (core)
AF4	PR28C	—	AH14	PB18A	HDC
AH1	PR28B	RST_N	AL13	PB17D	—
AH2	PR28A	M0	AJ14	PB17B	—
AH3	PPRGMN	$\overline{\text{PRGM}}$	AK14	PB17A	SYS_CLK (core)
AG4	PRESETN	$\overline{\text{RESET}}$	AL14	PB16D	—
AH5	PDONE	DONE	AJ15	VDD2	VDD2
AJ4	PB28D	RD_WR_N (core)	AK15	PB15D	STS_OUTD (core)
AK4	PB28C	CS_N (core)	AL15	PB15C	STS_OUTDN (core)
AL4	PB28B	ADDR0 (core)	AK16	PB15B	—
AH6	PB28A	ADDR1 (core)	AH16	PECKB	STS_OUTC (core)
AJ5	PB27D	ADDR2 (core)	AJ16	PB14D	STS_OUTCN (core)
AK5	PB27C	ADDR3 (core)	AL17	PB14C	RESLO (core)
AL5	PB27B	ADDR4 (core)	AK17	PB14B	RESHI (core)
AJ6	PB27A	ADDR5 (core)	AJ17	PB14A	—
AK6	PB26D	ADDR6 (core)	AL18	PB13D	REF14 (core)
AL6	PB26C	TSTMUX0S (core)	AK18	PB13B	REF10 (core)
AH8	PB26B	TSTMUX1S (core)	AJ18	PB13A	REXT
AJ7	PB26A	TSTMUX2S (core)	AL19	PB12D	PLL_VssA
AK7	PB25D	TSTMUX4S (core)	AH18	PB12A	PLL_VDDA
AL7	PB25C	TSTMUX7S (core)	AK19	PB11D	STS_OUTB (core)
AH9	PB25B	TSTMUX3S (core)	AJ19	PB11B	STS_OUTBN (core)
AJ8	VDD2	VDD2	AK20	PB11A	—
AK8	PB24D	TSTMUX6S (core)	AH19	PB10D	STS_OUTA (core)
AJ9	PB24C	TSTMUX5S (core)	AJ20	PB10B	STS_OUTAN (core)
AH10	PB24B	TSTMUX8S (core)	AL21	VDD2	VDD2
AK9	PB24A	$\overline{\text{INIT}}$	AK21	PB9D	CTAP_REFD (core)
AL9	PB23D	TSTPHASE (core)	AH20	PB9A	STS_IND (core)
AJ10	PB23C	LOOPBKEN (core)	AJ21	PB8D	STS_INDN (core)
AK10	PB23A	EXDNUP (core)	AL22	PB8A	STS_INC (core)
AL10	PB22A	ECSEL (core)	AK22	PB7D	STS_INCN (core)
AJ11	PB21D	ETOGGLE (core)	AJ22	PB7A	CTAP_REFC (core)
AH12	PB21A	RESETTN (core)	AL23	PB6D	STS_INB (core)
AK11	PB20D	MRESET (core)	AK23	PB6A	STS_INBN (core)

Pin Information (continued)

Table 32. 432-Pin EBGA Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
AH22	PB5D	CTAP_REFB (core)	AC30	PL22D	—
AJ23	PB5C	STS_INA (core)	AC31	PL21A	—
AK24	PB5B	STS_INAN (core)	AB29	PL21B	—
AJ24	PB5A	CTAP_REFA (core)	AB30	PL21C	—
AH23	PB4D	—	AB31	PL21D	—
AL25	PB4C	—	AA29	PL20A	—
AK25	PB4B	—	Y28	PL20B	—
AJ25	PB4A	LVDS_EN (core)	AA30	PL20C	—
AH24	PB3D	SCAN_TSTMD (core)	AA31	PL20D	—
AL26	PB3C	SCANEN (core)	Y29	PL19A	MPI_IRQ
AK26	PB3B	DXP (core)	W28	PL19D	—
AJ26	PB3A	DXN (core)	Y30	PL18A	I/O-SECKLL
AL27	V$_{DD}$2	V$_{DD}$2	W29	PL18C	I/O
AK27	PB2C	SYS_DOBIST (core)	W30	PL18D	I/O
AJ27	PB2B	SYS_RSSIGO (core)	V28	PL17A	I/O-$\overline{\text{MPI\_BI}}$
AH26	PB2A	BC (core)	W31	PL17C	I/O
AL28	PB1D	—	V29	PL17D	I/O
AK28	PB1C	—	V30	PL16A	I/O
AJ28	PB1B	—	V31	PL16C	I/O
AH27	PB1A	—	U29	PL16D	I/O
AG28	PCCLK	CCLK	U30	PL15A	I/O-MPI_RW
AH29	PL28A	—	U31	PL15B	I/O
AH30	PL28B	—	T30	V$_{DD}$2	V$_{DD}$2
AH31	PL28C	—	T28	PL15D	I/O
AF28	PL28D	—	T29	PL14A	I/O-MPI_CLK
AG29	PL27A	—	R31	PL14B	I/O
AG30	PL27B	—	R30	PL14C	I/O
AG31	PL27C	—	R29	PECKL	I/O-ECKL
AF29	PL27D	—	P31	PL13A	I/O
AF30	PL26A	—	P30	PL13D	I/O
AF31	PL26B	—	P29	PL12A	I/O
AD28	PL26C	—	N31	PL12C	I/O
AE29	V$_{DD}$2	V$_{DD}$2	P28	PL12D	I/O
AE30	PL25A	—	N30	PL11A	I/O-A4
AE31	PL25B	—	N29	PL11C	I/O
AC28	PL25C	—	M30	PL11D	I/O
AD29	PL24A	—	N28	PL10A	I/O
AD30	PL24D	—	M29	PL10C	I/O
AC29	PL23D	—	L31	V$_{DD}$2	V$_{DD}$2
AB28	PL22C	—	L30	PL9A	I/O-A3

Pin Information (continued)

Table 32. 432-Pin EBGA Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
M28	PL9B	I/O	C25	PT3D	I/O
L29	PL9C	I/O	B25	PT4A	I/O-TMS
K31	PL9D	I/O	A25	PT4B	I/O
K30	PL8A	I/O-A2	D23	PT4C	I/O
K29	PL8B	I/O	C24	PT4D	I/O
J31	PL8C	I/O	B24	V$_{DD}$2	V$_{DD}$2
J30	PL8D	I/O	C23	PT5B	I/O
K28	PL7D	I/O-A1/$\overline{\text{MPI\_BE1}}$	D22	PT5C	I/O
J29	PL6B	I/O	B23	PT5D	I/O
H30	PL6C	I/O	A23	PT6A	I/O-TDI
H29	PL6D	I/O	C22	PT6D	I/O
J28	PL5D	I/O	B22	PT7A	I/O
G31	PL4B	I/O	A22	PT7D	I/O
G30	PL4C	I/O	C21	PT8A	I/O
G29	V$_{DD}$2	V$_{DD}$2	D20	PT8D	I/O
H28	PL3A	I/O	B21	PT9A	I/O
F31	PL3B	I/O	A21	PT9D	I/O
F30	PL3C	I/O	C20	PT10A	I/O-DOUT
F29	PL3D	I/O	D19	PT10D	I/O
E31	PL2A	I/O	B20	PT11A	I/O
E30	PL2B	I/O	C19	PT11C	I/O
E29	PL2C	I/O	B19	PT11D	I/O
F28	PL2D	I/O-A0/$\overline{\text{MPI\_BE0}}$	D18	PT12A	I/O-D0/DIN
D31	PL1A	I/O	A19	PT12C	I/O
D30	PL1B	I/O	C18	PT12D	I/O
D29	PL1C	I/O	B18	PT13A	I/O
E28	PL1D	I/O	A18	PT13C	I/O
D27	PRD_DATA	RD_DATA/TDO	C17	PT13D	I/O-D1
C28	PT1A	I/O-TCK	B17	PT14A	I/O-D2
B28	PT1B	I/O	A17	V$_{DD}$2	V$_{DD}$2
A28	PT1C	I/O	B16	PT14C	I/O
D26	PT1D	I/O	D16	PT14D	I/O
C27	PT2A	I/O	C16	PT15A	I/O-D3
B27	PT2B	I/O	A15	PT15B	I/O
A27	PT2C	I/O	B15	PT15C	I/O
C26	PT2D	I/O	C15	PECKT	I/O-ECKT
B26	PT3A	I/O	A14	PT16A	I/O-D4
A26	PT3B	I/O	B14	PT16B	I/O
D24	PT3C	I/O	C14	PT16D	I/O

Pin Information (continued)

Table 32. 432-Pin EBGA Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
A13	PT17A	I/O	A3	V_{SS}	V_{SS}
D14	PT17B	I/O	A30	V_{SS}	V_{SS}
B13	PT17D	I/O	A8	V_{SS}	V_{SS}
C13	PT18A	I/O-D5	AD1	V_{SS}	V_{SS}
B12	PT18B	I/O	AD31	V_{SS}	V_{SS}
D13	V_{DD2}	V_{DD2}	AJ1	V_{SS}	V_{SS}
C12	PT19A	I/O	AJ2	V_{SS}	V_{SS}
A11	PT19D	I/O	AJ30	V_{SS}	V_{SS}
B11	PT20A	I/O	AJ31	V_{SS}	V_{SS}
D12	PT20D	I/O-D6	AK1	V_{SS}	V_{SS}
C11	PT21A	I/O	AK29	V_{SS}	V_{SS}
A10	PT21D	I/O	AK3	V_{SS}	V_{SS}
B10	PT22D	I/O	AK31	V_{SS}	V_{SS}
C10	PT23B	I/O	AL12	V_{SS}	V_{SS}
A9	PT23C	I/O	AL16	V_{SS}	V_{SS}
B9	V_{DD2}	V_{DD2}	AL2	V_{SS}	V_{SS}
D10	PT24A	I/O	AL20	V_{SS}	V_{SS}
C9	PT24B	I/O	AL24	V_{SS}	V_{SS}
B8	PT24C	I/O	AL29	V_{SS}	V_{SS}
C8	PT24D	I/O-D7	AL3	V_{SS}	V_{SS}
D9	PT25A	I/O	AL30	V_{SS}	V_{SS}
A7	PT25B	I/O	AL8	V_{SS}	V_{SS}
B7	PT25C	I/O	B1	V_{SS}	V_{SS}
C7	PT25D	I/O	B29	V_{SS}	V_{SS}
D8	PT26A	I/O	B3	V_{SS}	V_{SS}
A6	PT26B	I/O	B31	V_{SS}	V_{SS}
B6	PT26C	I/O	C1	V_{SS}	V_{SS}
C6	PT26D	I/O	C2	V_{SS}	V_{SS}
A5	PT27A	I/O-RDY/RCLK	C30	V_{SS}	V_{SS}
B5	PT27B	I/O	C31	V_{SS}	V_{SS}
C5	PT27C	I/O	H1	V_{SS}	V_{SS}
D6	PT27D	I/O	H31	V_{SS}	V_{SS}
A4	PT28A	I/O	M1	V_{SS}	V_{SS}
B4	PT28B	I/O	M31	V_{SS}	V_{SS}
C4	PT28C	I/O	T1	V_{SS}	V_{SS}
D5	PT28D	I/O-SECKUR	T31	V_{SS}	V_{SS}
A12	V_{SS}	V_{SS}	Y1	V_{SS}	V_{SS}
A16	V_{SS}	V_{SS}	Y31	V_{SS}	V_{SS}
A2	V_{SS}	V_{SS}	A1	V_{DD}	V_{DD}
A20	V_{SS}	V_{SS}	A31	V_{DD}	V_{DD}
A24	V_{SS}	V_{SS}	AA28	V_{DD}	V_{DD}
A29	V_{SS}	V_{SS}	AA4	V_{DD}	V_{DD}

Pin Information (continued)

Table 32. 432-Pin EBGA Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
AE28	V_{DD}	V_{DD}	C29	V_{DD}	V_{DD}
AE4	V_{DD}	V_{DD}	C3	V_{DD}	V_{DD}
AH11	V_{DD}	V_{DD}	D11	V_{DD}	V_{DD}
AH15	V_{DD}	V_{DD}	D15	V_{DD}	V_{DD}
AH17	V_{DD}	V_{DD}	D17	V_{DD}	V_{DD}
AH21	V_{DD}	V_{DD}	D21	V_{DD}	V_{DD}
AH25	V_{DD}	V_{DD}	D25	V_{DD}	V_{DD}
AH28	V_{DD}	V_{DD}	D28	V_{DD}	V_{DD}
AH4	V_{DD}	V_{DD}	D4	V_{DD}	V_{DD}
AH7	V_{DD}	V_{DD}	D7	V_{DD}	V_{DD}
AJ29	V_{DD}	V_{DD}	G28	V_{DD}	V_{DD}
AJ3	V_{DD}	V_{DD}	G4	V_{DD}	V_{DD}
AK2	V_{DD}	V_{DD}	L28	V_{DD}	V_{DD}
AK30	V_{DD}	V_{DD}	L4	V_{DD}	V_{DD}
AL1	V_{DD}	V_{DD}	R28	V_{DD}	V_{DD}
AL31	V_{DD}	V_{DD}	R4	V_{DD}	V_{DD}
B2	V_{DD}	V_{DD}	U28	V_{DD}	V_{DD}
B30	V_{DD}	V_{DD}	U4	V_{DD}	V_{DD}

Pin Information (continued)

Table 33. 680-Pin PBGAM Pinout

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
D1	PL1D	I/O	P3	PL11D	I/O
E2	—	—	P2	PL11C	I/O
E1	—	—	P1	PL11B	I/O
F4	PL1C	I/O	R5	PL11A	I/O-A4
F3	PL1B	I/O	R4	PL12D	I/O-A5
F2	PL1A	I/O	R2	PL12C	I/O
F1	PL2D	I/O-A0	R1	PL12B	I/O
G5	PL2C	I/O	T5	PL13D	I/O
G4	PL2B	I/O	T4	PL13C	I/O
G2	PL2A	I/O	T2	PL13B	I/O
G1	PL3D	I/O	T1	PL13A	I/O
H5	PL3C	I/O	U5	PECKL	I/O-ECKL
H4	PL3B	I/O	U4	—	—
H2	PL3A	I/O	U3	PL14C	I/O
H1	PL4C	I/O	U2	PL14B	I/O
J5	PL4B	I/O	U1	PL14A	I/O
J4	PL4A	I/O	V1	PL15D	I/O
J3	PL5D	I/O	V2	PL15B	I/O
J2	PL5C	I/O	V3	PL15A	I/O
J1	PL5B	I/O	V4	PL16D	I/O
K5	PL5A	I/O	V5	PL16C	I/O
K4	PL6D	I/O	W1	PL16B	I/O
K3	PL6C	I/O	W2	PL16A	I/O
K2	PL6B	I/O	W4	PL17D	I/O
K1	PL6A	I/O	W5	PL17C	I/O
L5	PL7D	I/O-A1	Y1	PL17B	I/O
L4	PL7C	I/O	Y2	PL17A	I/O
L2	PL7B	I/O	Y4	PL18D	I/O
L1	PL7A	I/O	Y5	PL18C	I/O
M5	PL8D	I/O	AA1	PL18B	I/O
M4	PL8C	I/O	AA2	PL18A	I/O-SECKLL
M2	PL8B	I/O	AA3	PL19D	—
M1	PL8A	I/O-A2	AA4	PL19C	—
N5	PL9D	I/O	AA5	PL19B	—
N4	PL9C	I/O	AB1	PL19A	MPI_IRQ
N3	PL9B	I/O	AB2	PL20D	—
N2	PL9A	I/O-A3	AB3	PL20C	—
N1	PL10C	I/O	AB4	PL20A	—
P5	PL10B	I/O	AB5	PL21D	—
P4	PL10A	I/O	AC1	PL21C	—

Pin Information (continued)

Table 33. 680-Pin PBGAM Pinout (continued)

Pin	ORT4622 Pad	Function
AC2	PL21B	—
AC4	PL21A	—
AC5	PL22D	—
AD1	PL22C	—
AD2	PL22B	—
AD4	PL22A	—
AD5	PL23D	—
AE1	PL23C	—
AE2	PL23B	—
AE3	PL23A	—
AE4	PL24D	—
AE5	PL24C	—
AF1	PL24B	—
AF2	PL24A	—
AF3	PL25D	—
AF4	PL25C	—
AF5	PL25B	—
AG1	PL25A	—
AG2	PL26C	—
AG4	PL26B	—
AG5	PL26A	—
AH1	PL27D	—
AH2	PL27C	—
AH4	PL27B	—
AH5	PL27A	—
AJ1	—	—
AJ2	—	—
AJ3	PL28D	—
AJ4	PL28C	—
AK1	PL28B	—
AK2	PL28A	—
AL1	PCCLK	CCLK
AP4	PB1A	—
AN5	PB1B	—
AP5	—	—
AL6	—	—
AM6	PB1C	—
AN6	PB1D	—
AP6	PB2A	BC
AK7	PB2B	SYS_RSSIGO

Pin	ORT4622 Pad	Function
AL7	PB2C	SYS_DOBIST
Pin	ORT4622 Pad	Function
AN7	PB3A	DXN (core)
AP7	PB3B	DXP (core)
AK8	PB3C	SCANEN (core)
AL8	PB3D	SCAN_TSTMD (core)
AN8	PB4A	LVDS_EN (core)
AP8	PB4B	—
AK9	PB4C	—
AL9	PB4D	—
AM9	PB5A	CTAP_REFA (core)
AN9	PB5B	STS_INAN (core)
AP9	PB5C	STS_INA (core)
AK10	PB5D	CTAP_REFB (core)
AL10	PB6A	STS_INBN (core)
AM10	PB6B	STS_INB (core)
AN10	PB6C	—
AP10	PB6D	—
AK11	PB7A	CTAP_REFC (core)
AL11	PB7B	—
AN11	PB7C	—
AP11	PB7D	—
AK12	PB8A	STS_INCN (core)
AL12	PB8B	STS_INC (core)
AN12	PB8C	STS_INDN (core)
AP12	PB8D	STS_IND (core)
AK13	PB9A	—
AL13	PB9B	—
AM13	PB9C	—
AN13	PB9D	CTAP_REFD (core)
AP13	PB10B	—
AK14	PB10C	STS_OUTAN (core)
AL14	PB10D	STS_OUTA (core)
AM14	PB11A	—
AN14	PB11B	STS_OUTBN (core)
AP14	PB11C	STS_OUTB (core)
AK15	PB11D	—
AL15	PB12A	PLL_VDDA (core)
AN15	PB12B	—
AP15	PB12C	—
AK16	PB12D	PLL_VSSA (core)

Pin Information (continued)

Table 33. 680-Pin PBGAM Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
AL16	PB13A	REXT (core)	AK24	PB22D	—
AN16	PB13B	REF10 (core)	AP25	PB23A	EXDNUP (core)
AP16	PB13C	—	AN25	PB23B	—
AK17	PB13D	REF14 (core)	AM25	PB23C	LOOPBKEN (core)
AL17	—	—	AL25	PB23D	TSTPHASE (core)
AM17	PB14B	RESHI (core)	AK25	PB24A	INIT
AN17	—	—	AP26	PB24B	TSTMUX8S (core)
AP17	PB14C	RESLO (core)	AN26	PB24C	TSTMUX5S (core)
AP18	PB14D	STS_OUTCN (core)	AM26	PB24D	TSTMUX6S (core)
AN18	PECKB	STS_OUTC (core)	AL26	PB25B	TSTMUX3S (core)
AM18	PB15B	—	AK26	PB25C	TSTMUX7S (core)
AL18	PB15C	STS_OUTDN (core)	AP27	PB25D	TSTMUX4S (core)
AK18	PB15D	STS_OUTD (core)	AN27	PB26A	TSTMUX2S (core)
AP19	PB16B	—	AL27	PB26B	TSTMUX1S (core)
AN19	PB16C	—	AK27	PB26C	TSTMUX0S (core)
AL19	PB16D	—	AP28	PB26D	ADDR6 (core)
AK19	PB17A	SYS_CLK	AN28	PB27A	ADDR5 (core)
AP20	PB17B	—	AL28	PB27B	ADDR4 (core)
AN20	PB17C	—	AK28	PB27C	ADDR3 (core)
AL20	PB17D	—	AP29	PB27D	ADDR2 (core)
AK20	PB18A	HDC	AN29	PB28A	ADDR1 (core)
AP21	PB18B	TSTMODE	AM29	PB28B	ADDR0 (core)
AN21	PB18C	—	AL29	—	—
AM21	PB18D	BYPASS	AP30	PB28C	CS_N (core)
AL21	PB19A	TSTCLK	AN30	PB28D	RD_WR_N (core)
AK21	PB19B	RESETRN	AP31	PDONE	DONE
AP22	PB19C	TSTSHFTLD	AL34	PRESETN	RESET
AN22	PB20A	LDC	AK33	PPRGMN	PRGM
AM22	PB20B	—	AK34	PR28A	M0
AL22	PB20C	—	AJ31	PR28B	RST_N
AK22	PB20D	MRESET (core)	AJ32	PR28C	—
AP23	PB21A	RESETTN (core)	AJ33	PR28D	INT_N
AN23	PB21B	—	AJ34	PR27B	DB4 (core)
AL23	PB21C	—	AH30	PR27C	DB5 (core)
AK23	PB21D	ETOGGLE (core)	AH31	PR27D	DB6 (core)
AP24	PB22A	ECSEL (core)	AH33	PR26A	DB7 (core)
AN24	PB22B	—	AH34	PR26B	DB0 (core)
AL24	PB22C	—	AG30	PR26C	DB1 (core)

Pin Information (continued)

Table 33. 680-Pin PBGAM Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
AG31	PR26D	DB2 (core)	V33	PR15C	I/O
AG33	PR25A	DB3 (core)	V34	PR15D	I/O
AG34	PR25B	—	U34	PECKR	I/O-ECKR
AF30	PR25C	—	U33	PR14B	I/O
AF31	PR25D	—	U32	PR14C	I/O
AF32	PR24A	—	U31	PR14D	I/O
AF33	PR24B	—	U30	PR13B	I/O
AF34	PR24C	—	T34	PR13C	I/O
AE30	PR24D	—	T33	PR13D	I/O
AE31	PR23A	—	T31	PR12A	I/O
AE32	PR23B	—	T30	PR12B	I/O
AE33	PR23C	—	R34	PR12C	I/O
AE34	PR23D	—	R33	PR12D	I/O
AD30	PR22A	—	R31	PR11A	I/O-CS1
AD31	PR22B	—	R30	PR11B	I/O
AD33	PR22C	—	P34	PR11C	I/O
AD34	PR22D	M1	P33	PR11D	I/O
AC30	PR21A	—	P32	PR10A	I/O
AC31	PR21B	—	P31	PR10B	I/O
AC33	PR21C	—	P30	PR10C	I/O
AC34	PR20A	—	N34	PR9A	I/O-CS0
AB30	PR20B	—	N33	PR9B	I/O
AB31	PR20C	—	N32	PR9C	I/O
AB32	PR20D	—	N31	PR9D	I/O
AB33	PR19A	M2	N30	PR8A	I/O
AB34	PR19B	—	M34	PR8B	I/O
AA30	PR19C	—	M33	PR8C	I/O
AA31	PR19D	—	M31	PR8D	I/O
AA32	PR18A	I/O	M30	PR7A	I/O-RD
AA33	PR18B	I/O	L34	PR7B	I/O
AA34	PR18C	I/O	L33	PR7C	I/O
Y30	PR18D	I/O	L31	PR7D	I/O
Y31	PR17A	I/O-M3	L30	PR6A	I/O
Y33	PR17B	I/O	K34	PR6B	I/O
Y34	PR17C	I/O	K33	PR6C	I/O
W30	PR17D	I/O	K32	PR6D	I/O
W31	PR16A	I/O	K31	PR5A	I/O
W33	PR16B	I/O	K30	PR5B	I/O
W34	PR16C	I/O	J34	PR5C	I/O
V30	PR15A	I/O	J33	PR5D	I/O
V31	—	—	J32	PR4B	I/O
V32	PR15B	I/O	J31	PR4C	I/O

Pin Information (continued)

Table 33. 680-Pin PBGAM Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
J30	PR4D	I/O	D24	PT22C	I/O
H34	PR3A	I/O-$\overline{\text{WR}}$	B24	PT22B	I/O
H33	PR3B	I/O	A24	PT22A	I/O
H31	PR3C	I/O	E23	PT21D	I/O
H30	PR3D	I/O	D23	PT21C	I/O
G34	PR2A	I/O	B23	PT21B	I/O
G33	PR2B	I/O	A23	PT21A	I/O
G31	PR2C	I/O	E22	PT20D	I/O-D6
G30	PR2D	I/O	D22	PT20C	I/O
F34	PR1A	I/O	C22	PT20B	I/O
F33	—	—	B22	PT20A	I/O
F32	PR1B	I/O	A22	PT19D	I/O
F31	PR1C	I/O	E21	PT19C	I/O
E34	—	—	D21	PT19B	I/O
E33	PR1D	I/O	C21	PT19A	I/O
D34	PRD_CFGN	$\overline{\text{RD\_CFG}}$	B21	PT18C	I/O
A31	PT28D	I/O-SECKUR	A21	PT18B	I/O
B30	—	—	E20	PT18A	I/O-D5
A30	PT28C	I/O	D20	PT17D	I/O
D29	—	—	B20	PT17C	I/O
C29	PT28B	I/O	A20	PT17B	I/O
B29	PT28A	I/O	E19	PT17A	I/O
A29	PT27D	I/O	D19	PT16D	I/O
E28	PT27C	I/O	B19	PT16C	I/O
D28	PT27B	I/O	A19	PT16B	I/O
B28	PT27A	I/O-RDY/RCLK	E18	PT16A	I/O-D4
A28	PT26D	I/O	D18	PECKT	I/O-ECKT
E27	PT26C	I/O	C18	PT15B	I/O
D27	PT26B	I/O	B18	—	—
B27	PT26A	I/O	A18	PT15A	I/O-D3
A27	PT25D	I/O	A17	PT14D	I/O
E26	PT25C	I/O	B17	PT14C	I/O
D26	PT25B	I/O	C17	PT14A	I/O-D2
C26	PT25A	I/O	D17	PT13D	I/O-D1
B26	PT24D	I/O-D7	E17	PT13C	I/O
A26	PT24C	I/O	A16	PT13B	I/O
E25	PT24B	I/O	B16	PT13A	I/O
D25	PT24A	I/O	D16	PT12D	I/O
C25	PT23C	I/O	E16	PT12C	I/O
B25	PT23B	I/O	A15	PT12B	I/O
A25	PT23A	I/O	B15	PT12A	I/O-D0/DIN
E24	PT22D	I/O	D15	PT11D	I/O

Pin Information (continued)

Table 33. 680-Pin PBGAM Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
E15	PT11C	I/O	A4	PRD_DATA	RD_DATA/TDO
A14	PT11B	I/O	A1	Vss	Vss
B14	PT11A	I/O	A2	Vss	Vss
C14	PT10D	I/O	A33	Vss	Vss
D14	PT10C	I/O	A34	Vss	Vss
E14	PT10B	I/O	B1	Vss	Vss
A13	PT10A	I/O-DOUT	B2	Vss	Vss
B13	PT9C	I/O	B33	Vss	Vss
C13	PT9B	I/O	B34	Vss	Vss
D13	PT9A	I/O	C3	Vss	Vss
E13	PT8D	I/O	C8	Vss	Vss
A12	PT8C	I/O	C12	Vss	Vss
B12	PT8B	I/O	C16	Vss	Vss
D12	PT8A	I/O	C19	Vss	Vss
E12	PT7D	I/O	C23	Vss	Vss
A11	PT7C	I/O	C27	Vss	Vss
B11	PT7B	I/O	C32	Vss	Vss
D11	PT7A	I/O	D4	Vss	Vss
E11	PT6D	I/O	D31	Vss	Vss
A10	PT6C	I/O	H3	Vss	Vss
B10	PT6B	I/O	H32	Vss	Vss
C10	PT6A	I/O-TDI	M3	Vss	Vss
D10	PT5D	I/O	M32	Vss	Vss
E10	PT5C	I/O	N13	Vss	Vss
A9	PT5B	I/O	N14	Vss	Vss
B9	PT4D	I/O	N15	Vss	Vss
C9	PT4C	I/O	N20	Vss	Vss
D9	PT4B	I/O	N21	Vss	Vss
E9	PT4A	I/O-TMS	N22	Vss	Vss
A8	PT3D	I/O	P13	Vss	Vss
B8	PT3C	I/O	P14	Vss	Vss
D8	PT3B	I/O	P15	Vss	Vss
E8	PT3A	I/O	P20	Vss	Vss
A7	PT2D	I/O	P21	Vss	Vss
B7	PT2C	I/O	P22	Vss	Vss
D7	PT2B	I/O	R13	Vss	Vss
E7	PT2A	I/O	R14	Vss	Vss
A6	PT1D	I/O	R15	Vss	Vss
B6	—	—	R20	Vss	Vss
C6	PT1C	I/O	R21	Vss	Vss
D6	PT1B	I/O	R22	Vss	Vss
A5	—	—	T3	Vss	Vss
B5	PT1A	I/O-TCK	T16	Vss	Vss

Pin Information (continued)

Table 33. 680-Pin PBGAM Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
T17	Vss	Vss	AM3	Vss	Vss
T18	Vss	Vss	AM8	Vss	Vss
T19	Vss	Vss	AM12	Vss	Vss
T32	Vss	Vss	AM16	Vss	Vss
U16	Vss	Vss	AM19	Vss	Vss
U17	Vss	Vss	AM23	Vss	Vss
U18	Vss	Vss	AM27	Vss	Vss
U19	Vss	Vss	AM32	Vss	Vss
V16	Vss	Vss	AN1	Vss	Vss
V17	Vss	Vss	AN2	Vss	Vss
V18	Vss	Vss	AN33	Vss	Vss
V19	Vss	Vss	AN34	Vss	Vss
W3	Vss	Vss	AP1	Vss	Vss
W16	Vss	Vss	AP2	Vss	Vss
W17	Vss	Vss	AP33	Vss	Vss
W18	Vss	Vss	AP34	Vss	Vss
W19	Vss	Vss	C5	VDD2	VDD2
W32	Vss	Vss	C30	VDD2	VDD2
Y13	Vss	Vss	D5	VDD2	VDD2
Y14	Vss	Vss	D30	VDD2	VDD2
Y15	Vss	Vss	E3	VDD2	VDD2
Y20	Vss	Vss	E4	VDD2	VDD2
Y21	Vss	Vss	E5	VDD2	VDD2
Y22	Vss	Vss	E6	VDD2	VDD2
AA13	Vss	Vss	E29	VDD2	VDD2
AA14	Vss	Vss	E30	VDD2	VDD2
AA15	Vss	Vss	E31	VDD2	VDD2
AA20	Vss	Vss	E32	VDD2	VDD2
AA21	Vss	Vss	F5	VDD2	VDD2
AA22	Vss	Vss	F30	VDD2	VDD2
AB13	Vss	Vss	N16	VDD2	VDD2
AB14	Vss	Vss	N17	VDD2	VDD2
AB15	Vss	Vss	N18	VDD2	VDD2
AB20	Vss	Vss	N19	VDD2	VDD2
AB21	Vss	Vss	P16	VDD2	VDD2
AB22	Vss	Vss	P17	VDD2	VDD2
AC3	Vss	Vss	P18	VDD2	VDD2
AC32	Vss	Vss	P19	VDD2	VDD2
AG3	Vss	Vss	R16	VDD2	VDD2
AG32	Vss	Vss	R17	VDD2	VDD2
AL4	Vss	Vss	R18	VDD2	VDD2
AL31	Vss	Vss	R19	VDD2	VDD2

Pin Information (continued)

Table 33. 680-Pin PBGAM Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
T13	V$_{DD2}$	V$_{DD2}$	AK6	V$_{DD2}$	V$_{DD2}$
T14	V$_{DD2}$	V$_{DD2}$	AK29	V$_{DD2}$	V$_{DD2}$
T15	V$_{DD2}$	V$_{DD2}$	AK30	V$_{DD2}$	V$_{DD2}$
T20	V$_{DD2}$	V$_{DD2}$	AK31	V$_{DD2}$	V$_{DD2}$
T21	V$_{DD2}$	V$_{DD2}$	AK32	V$_{DD2}$	V$_{DD2}$
T22	V$_{DD2}$	V$_{DD2}$	AL5	V$_{DD2}$	V$_{DD2}$
U13	V$_{DD2}$	V$_{DD2}$	AL30	V$_{DD2}$	V$_{DD2}$
U14	V$_{DD2}$	V$_{DD2}$	AM5	V$_{DD2}$	V$_{DD2}$
U15	V$_{DD2}$	V$_{DD2}$	AM30	V$_{DD2}$	V$_{DD2}$
U20	V$_{DD2}$	V$_{DD2}$	A3	V$_{DD}$	V$_{DD}$
U21	V$_{DD2}$	V$_{DD2}$	A32	V$_{DD}$	V$_{DD}$
U22	V$_{DD2}$	V$_{DD2}$	B3	V$_{DD}$	V$_{DD}$
V13	V$_{DD2}$	V$_{DD2}$	B4	V$_{DD}$	V$_{DD}$
V14	V$_{DD2}$	V$_{DD2}$	B31	V$_{DD}$	V$_{DD}$
V15	V$_{DD2}$	V$_{DD2}$	B32	V$_{DD}$	V$_{DD}$
V20	V$_{DD2}$	V$_{DD2}$	C1	V$_{DD}$	V$_{DD}$
V21	V$_{DD2}$	V$_{DD2}$	C2	V$_{DD}$	V$_{DD}$
V22	V$_{DD2}$	V$_{DD2}$	C4	V$_{DD}$	V$_{DD}$
W13	V$_{DD2}$	V$_{DD2}$	C7	V$_{DD}$	V$_{DD}$
W14	V$_{DD2}$	V$_{DD2}$	C11	V$_{DD}$	V$_{DD}$
W15	V$_{DD2}$	V$_{DD2}$	C15	V$_{DD}$	V$_{DD}$
W20	V$_{DD2}$	V$_{DD2}$	C20	V$_{DD}$	V$_{DD}$
W21	V$_{DD2}$	V$_{DD2}$	C24	V$_{DD}$	V$_{DD}$
W22	V$_{DD2}$	V$_{DD2}$	C28	V$_{DD}$	V$_{DD}$
Y16	V$_{DD2}$	V$_{DD2}$	C31	V$_{DD}$	V$_{DD}$
Y17	V$_{DD2}$	V$_{DD2}$	C33	V$_{DD}$	V$_{DD}$
Y18	V$_{DD2}$	V$_{DD2}$	C34	V$_{DD}$	V$_{DD}$
Y19	V$_{DD2}$	V$_{DD2}$	D2	V$_{DD}$	V$_{DD}$
AA16	V$_{DD2}$	V$_{DD2}$	D3	V$_{DD}$	V$_{DD}$
AA17	V$_{DD2}$	V$_{DD2}$	D32	V$_{DD}$	V$_{DD}$
AA18	V$_{DD2}$	V$_{DD2}$	D33	V$_{DD}$	V$_{DD}$
AA19	V$_{DD2}$	V$_{DD2}$	G3	V$_{DD}$	V$_{DD}$
AB16	V$_{DD2}$	V$_{DD2}$	G32	V$_{DD}$	V$_{DD}$
AB17	V$_{DD2}$	V$_{DD2}$	L3	V$_{DD}$	V$_{DD}$
AB18	V$_{DD2}$	V$_{DD2}$	L32	V$_{DD}$	V$_{DD}$
AB19	V$_{DD2}$	V$_{DD2}$	R3	V$_{DD}$	V$_{DD}$
AJ5	V$_{DD2}$	V$_{DD2}$	R32	V$_{DD}$	V$_{DD}$
AJ30	V$_{DD2}$	V$_{DD2}$	Y3	V$_{DD}$	V$_{DD}$
AK3	V$_{DD2}$	V$_{DD2}$	Y32	V$_{DD}$	V$_{DD}$
AK4	V$_{DD2}$	V$_{DD2}$	AD3	V$_{DD}$	V$_{DD}$
AK5	V$_{DD2}$	V$_{DD2}$	AD32	V$_{DD}$	V$_{DD}$

Lucent Technologies Inc.

Pin Information (continued)

Table 33. 680-Pin PBGAM Pinout (continued)

Pin	ORT4622 Pad	Function	Pin	ORT4622 Pad	Function
AH3	V$_{DD}$	V$_{DD}$	AM20	V$_{DD}$	V$_{DD}$
AH32	V$_{DD}$	V$_{DD}$	AM24	V$_{DD}$	V$_{DD}$
AL2	V$_{DD}$	V$_{DD}$	AM28	V$_{DD}$	V$_{DD}$
AL3	V$_{DD}$	V$_{DD}$	AM31	V$_{DD}$	V$_{DD}$
AL32	V$_{DD}$	V$_{DD}$	AM33	V$_{DD}$	V$_{DD}$
AL33	V$_{DD}$	V$_{DD}$	AM34	V$_{DD}$	V$_{DD}$
AM1	V$_{DD}$	V$_{DD}$	AN3	V$_{DD}$	V$_{DD}$
AM2	V$_{DD}$	V$_{DD}$	AN4	V$_{DD}$	V$_{DD}$
AM4	V$_{DD}$	V$_{DD}$	AN31	V$_{DD}$	V$_{DD}$
AM7	V$_{DD}$	V$_{DD}$	AN32	V$_{DD}$	V$_{DD}$
AM11	V$_{DD}$	V$_{DD}$	AP3	V$_{DD}$	V$_{DD}$
AM15	V$_{DD}$	V$_{DD}$	AP32	V$_{DD}$	V$_{DD}$

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: Θ_{JA}, ψ_{JC}, and Θ_{JC}. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

Θ_{JA}

This is the thermal resistance from junction to ambient (a.k.a. theta-JA, R-theta, etc.).

$$\Theta_{JA} = \frac{T_J - T_A}{Q}$$

where T_J is the junction temperature, T_A is the ambient air temperature, and Q is the chip power.

Experimentally, Θ_{JA} is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that Θ_{JA} is expressed in units of °C/watt.

ψ_{JC}

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance, and it is defined by:

$$\psi_{JC} = \frac{T_J - T_C}{Q}$$

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the Θ_{JA} measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψ_{JC} is also expressed in units of °C/watt.

Θ_{JC}

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\Theta_{JC} = \frac{T_J - T_C}{Q}$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates Θ_{JC} from ψ_{JC}. Θ_{JC} is a true thermal resistance and is expressed in units of °C/watt.

Θ_{JB}

This is the thermal resistance from junction to board (a.k.a. Θ_{JL}). It is defined by:

$$\Theta_{JB} = \frac{T_J - T_B}{Q}$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board to draw most of the heat out of the leads. Note that Θ_{JB} is expressed in units of °C/watt, and that this parameter and the way it is measured are still in JEDEC committee.

FPGA Maximum Junction Temperature

Once the power dissipated by the FPGA has been determined (see the Estimating Power Dissipation section), the maximum junction temperature of the FPGA can be found. This is needed to determine if speed derating of the device from the 85 °C junction temperature used in all of the delay tables is needed. Using the maximum ambient temperature, T_{Amax}, and the power dissipated by the device, Q (expressed in °C), the maximum junction temperature is approximated by:

$$T_{Jmax} = T_{Amax} + (Q \bullet \Theta_{JA})$$

Table 34 lists the thermal characteristics for all packages used with the *ORCA* ORT4622 Series of FPGAs.

Package Thermal Characteristics

Table 34. *ORCA* ORT4622 Plastic Package Thermal Guidelines

Package	Θ_{JA} (°C/W)			T_{AMB} = 70 °C Max T_J = 125 °C Max 0 fpm (W)
	0 fpm	200 fpm	500 fpm	
432-Pin EBGA	11	8.5	5	5
680-Pin PBGAM	14.5	TBD	TBD	3.8

Package Coplanarity

The coplanarity limits of the *ORCA* Series 3/3+ packages are as follows:

■ EBGA: 8.0 mils

■ PBGAM: 8.0 mils

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 35 lists eight parasitics associated with the *ORCA* packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in $m\Omega$.

The parasitic values in Table 35 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.

Package Parasitics (continued)

Table 35. *ORCA* ORT4622 Package Parasitics

Package Type	L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
432-Pin EBGA	4	1.5	500	1.0	1.0	0.3	3—5.5	0.5—1
680-Pin PBGAM	3.8	1.3	250	1.0	1.0	0.3	2.8—5	0.5—1
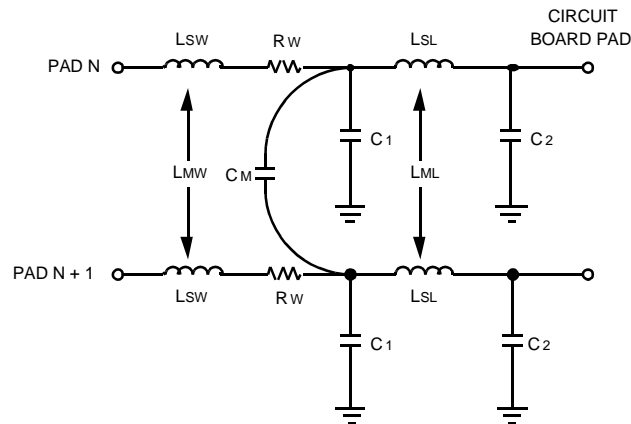
5-3862(C)r2

**Figure 28. Package Parasitics**

Package Outline Diagrams

Terms and Definitions

Basic Size (BSC):   The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

Typical (TYP):   When specified after a dimension, this indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

Reference (REF):   The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or
Maximum (MAX):   Indicates the minimum or maximum allowable size of a dimension.

Package Outline Diagrams (continued)
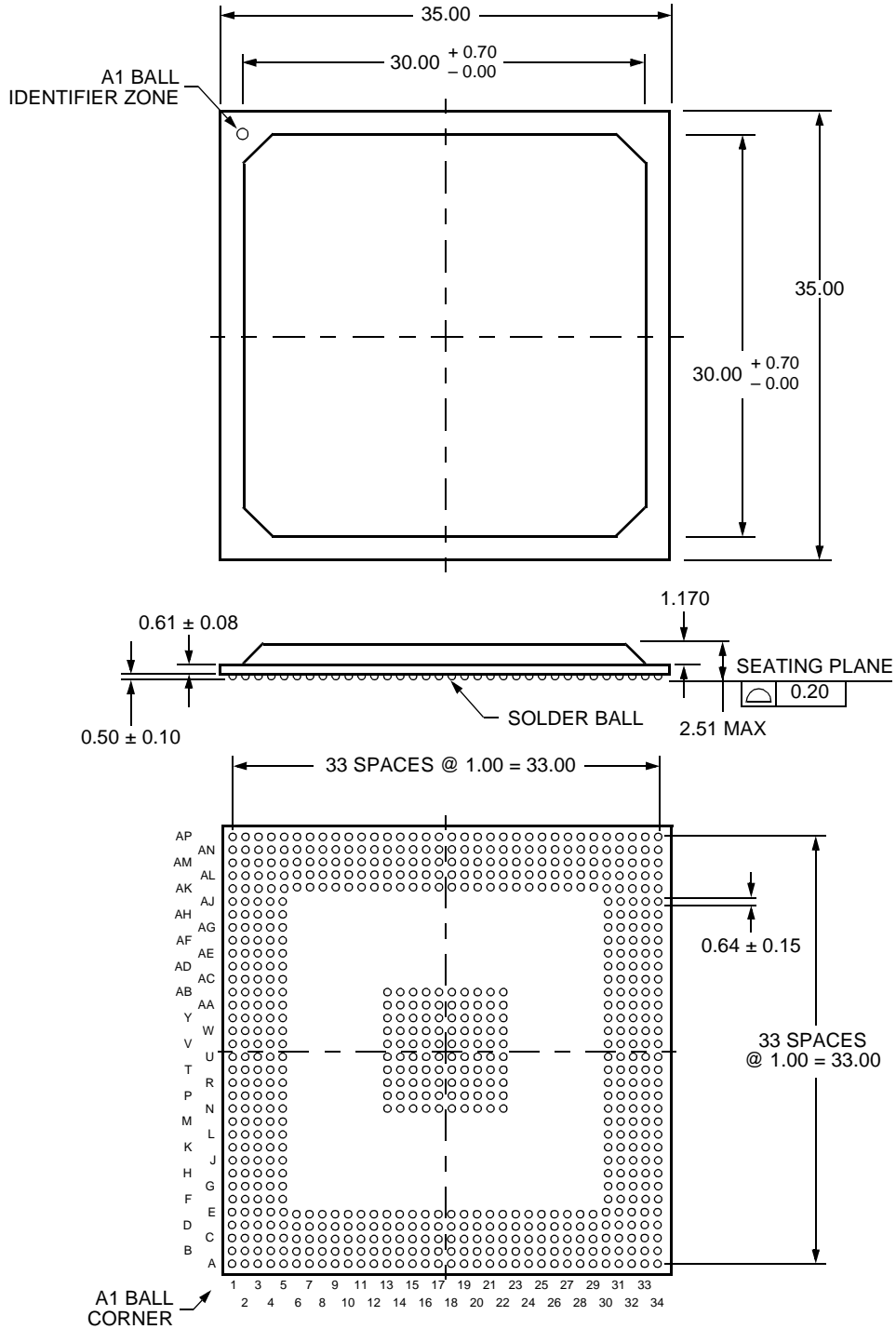
432-Pin EBGA

Dimensions are in millimeters.
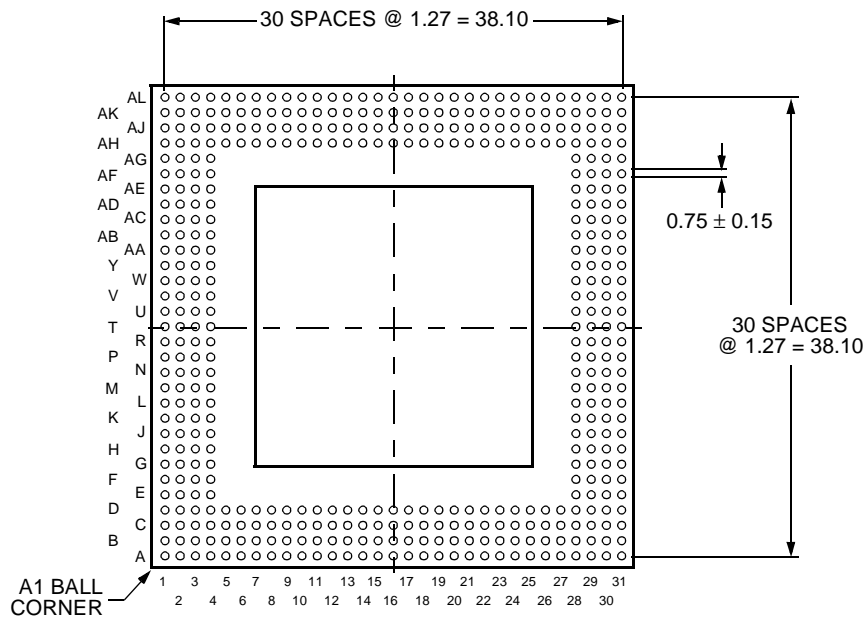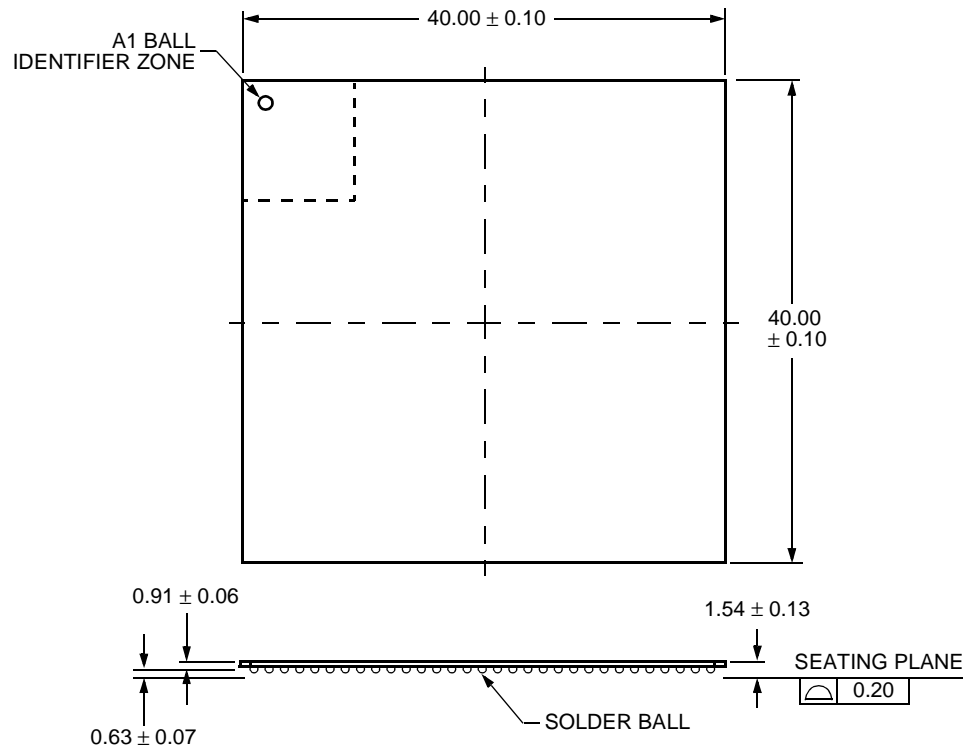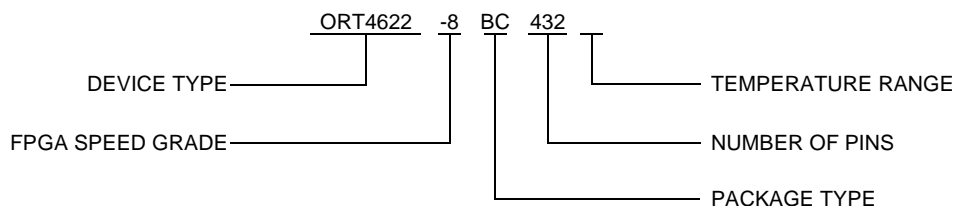
Package Outline Diagrams (continued)

680-Pin PBGAM

Dimensions are in millimeters.

5-4406(F)

Ordering Information

```
                            ORT4622   -8   BC   432

        DEVICE TYPE                                         TEMPERATURE RANGE

        FPGA SPEED GRADE                                    NUMBER OF PINS

                                                            PACKAGE TYPE
```

5-6435 (F).i

Table 36. Voltage Options

Device	Voltage
ORT4622	2.5 V/3.3 V

Table 37. Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	−40 °C to +85 °C

Table 38. Package Type Options

Symbol	Description
BC	Enhanced Ball Grid Array (EBGA)
BM	Plastic Ball Grid Array, Multilayer

Table 39. *ORCA* Series 3+ Package Matrix

Device	Package	
	432-Pin EBGA	680-Pin PBGAM
	BC432	BM680
ORT4622	CI	CI

Key: C = commercial, I = industrial.

For additional information, contact your Microelectronics Group Account Manager or the following:
INTERNET: **http://www.lucent.com/micro**, or for FPGA information, **http://www.lucent.com/orca**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
                1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
                Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Microelectronics Group, Lucent Technologies (China) Co., Ltd., A-F2, 23/F, Zao Fong Universe Building, 1800 Zhong Shan Xi Road,
                Shanghai 200233 P. R. China   **Tel. (86) 21 6440 0468**, **ext. 316**, FAX (86) 21 6440 0652
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
                Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE: **Tel. (44) 7000 582 368**, FAX (44) 1189 328 148
                Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
                    FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 4354 2800** (Helsinki),
                    ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

m i c r o e l e c t r o n i c s   g r o u p

Lucent Technologies
Bell Labs Innovations