ECL 16,384-BIT BIPOLAR RANDOM ACCESS MEMORY

M10480

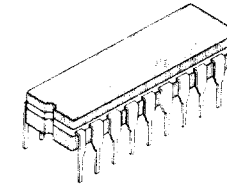
PRELIMINARY

Note: This is not a final specification.
Some parametric limits are subject to change.

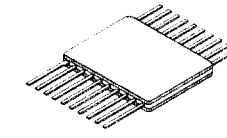
DESCRIPTION

The Fujitsu MBM10480 is a fully decoded 16,384-bit ECL read/write random access memory designed for main frame memory, control and buffer storage applications. This device is organized as 16,384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

Operation for the MBM10480 is specified over a temperature range of 0°C to 75°C (T_A for DIP, T_C for flat package). It features cerdip 20-pin dual in-line and flat packaging, and is fully compatible with industry-standard 10K-series ECL families.



CERDIP PACKAGE
DIP-20C-C03

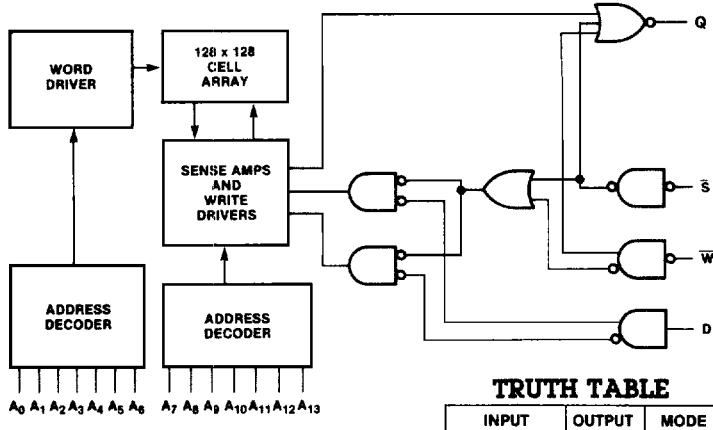


FLATPACK
FPT-20C-C01

FEATURES

- **Organized as 16,384 x 1**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address Access Time: 25 ns max.**
- **Chip select access time: 15 ns max.**
- **Open emitter output for easy memory expansion**
- **Low power dissipation of 0.05 mW/bit**
- **DOPOS processing (Doped Polysilicon)**
- **Pin compatible with the F10480**

MBM10480 BLOCK DIAGRAM

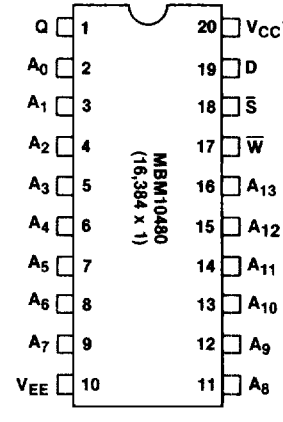


TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't care

PIN ASSIGNMENT



*V_{CC} grounded

ABSOLUTE MAXIMUM RATINGS (See Note)

Parameter		Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})		V_{EE}	+0.5 to −7.0	V
Input Voltage		V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)		I_{OUT}	−30	mA
Temperature Under Bias	DIP	T_A	−55 to +125	°C
	Flat	T_C		
Storage Temperature		T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

GUARANTEED OPERATING CONDITIONS (Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Temperature*
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

* Ambient Temperature for DIP, case temperature for flat package

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	5	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω and 30 pF to −2.0V, T_A = 0°C to 75°C for DIP, T_C = 0°C to 75°C for Flat package and Airflow ≥ 2.5 m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OH}	−1000 − 960 − 900	—	− 840 − 810 − 720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OHC}	−1020 − 980 − 920	—	—	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	− 840 − 810 − 720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\,max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current (V_{IN} = $V_{IL\,min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{S}$ Input Low Current (V_{IN} = $V_{IL\,min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA	0° to 75°C

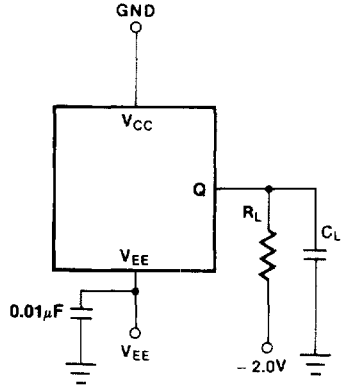
FUNCTIONAL DESCRIPTION

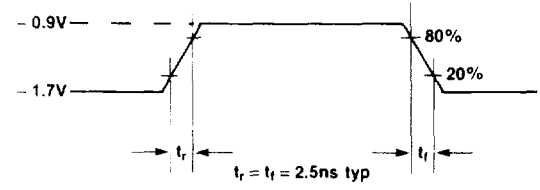
The Fujitsu MBM10480 is a fully decoded 16,384-bit read/write random access memory organized as 16,384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated $A_0 \sim A_{13}$. The active low Chip Select $\overline{S}$ input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{W}$ input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

AC CHARACTERISTICS

(V_{CC} = 0V, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, T_C = 0°C to 75°C for flat package, and Airflow = ≥ 25 m/s, unless otherwise noted.)

AC TEST CONDITIONS





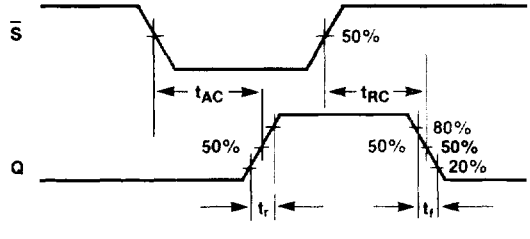
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

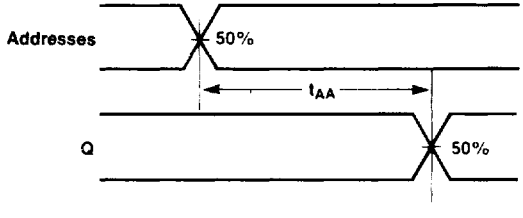
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	—	25	ns
Chip Select Access Time	t_{AC}	—	—	15	ns
Chip Select Recovery Time	t_{RC}	—	—	15	ns

READ CYCLE TIMING DIAGRAMS

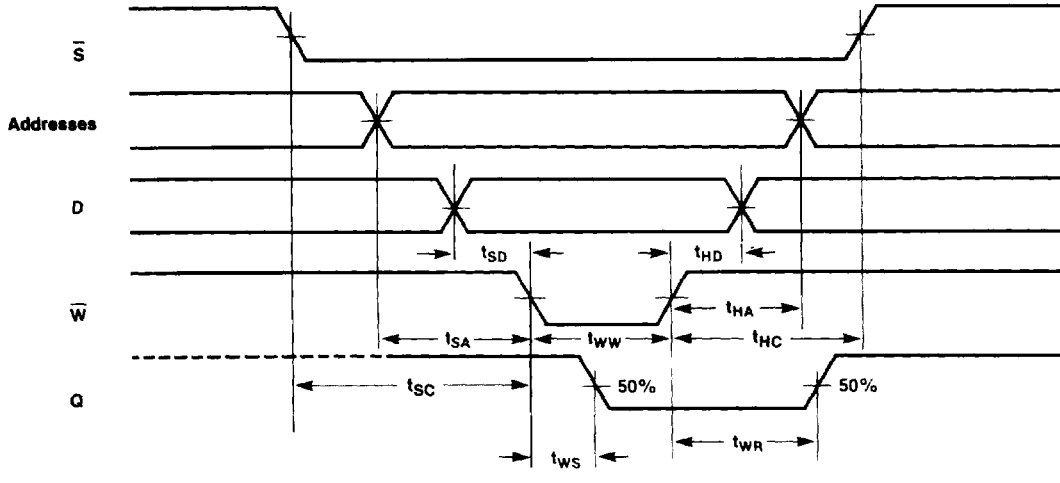




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	25	—	—	ns
Write Disable Time	t_{WS}	—	—	15	ns
Write Recovery Time	t_{WR}	—	—	20	ns
Address Set Up Time	t_{SA}	5	—	—	ns
Chip Select Set Up Time	t_{SC}	5	—	—	ns
Data Set Up Time	t_{SD}	5	—	—	ns
Address Hold Time	t_{HA}	5	—	—	ns
Chip Select Hold Time	t_{HC}	5	—	—	ns
Data Hold Time	t_{HD}	5	—	—	ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME AND FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	3	—	ns
Output Fall Time	t_f	—	3	—	ns